ENERGY AUTONOMOUS CMOS IMAGE SENSORS

A Dissertation

Presented in Partial Fulfillment of the Requirements for the

Degree of Doctor of Philosophy

with a

Major in Electrical Engineering

in the

College of Graduate Studies

University of Idaho

by

Ismail Cevik

April 2014

Major Professor: Suat U. Ay, Ph.D.,P.E.

AUTHORIZATION TO SUBMIT DISSERTATION

This dissertation of Ismail Cevik, submitted for the degree of Doctor of Philosophy with a major in Electrical Engineering and titled "Energy Autonomous CMOS Image Sensors," has been reviewed in final form. Permission, as indicated by signatures and dates given below, is now granted to submit final copies to the College of Graduate Studies for approval.

Major Professor: _____ Date _____

Suat U. Ay, Ph.D., P.E.

Committee Members: _____ Date _____

Aicha Elshabini, Ph.D., P.E.

_____ Date _____

Fred Barlow, III, Ph.D.

_____ Date _____

Ahmed Abdel-Rahim, Ph.D., P.E.

Department Administrator: _____ Date _____

Fred Barlow, III, Ph.D.

Dean of College Of Engineering: _____ Date _____

Larry Stauffer, Ph.D. P.E.

Final Approval and Acceptance

Dean of the College Of Graduate Studies: _____ Date _____

Jie Chen, Ph.D.

ABSTRACT

Harvesting energy from ambient sources is vital for extending the operational lifetime of electronic systems deployed in inaccessible environments where battery replacement is difficult, if not impossible. Ambient sources can power an electronic system as long as the ambient energy source persists and is harvested efficiently, potentially leading to an infinite operational lifetime.

Both image sensors and solar cells require sufficient illumination for proper operation. Ultra-low power complementary metal oxide silicon (CMOS) active pixel sensor (APS) imagers can be powered through harvesting the solar energy incident on the focal plane of the image sensor.

The focus of this study is developing techniques for designing ultra-low power CMOS APS imagers and maximizing the energy harvested on their focal planes with the ultimate goal of achieving continuous self-powered operation. Fundamental problems associated with designing ultra-low power CMOS APS imager systems and on-chip energy harvesting and power management systems are addressed in this research.

The technical inquiry is divided into four research objectives. The first objective is the investigation of fundamental operating principles of photovoltaic energy harvesters and the problems associated with their design. The second objective is to develop pixel structures, which can harvest energy and capture images continuously, as opposed to the current EHI pixels which can harvest energy and capture images sequentially. The third objective is developing micro power management systems for utilizing the harvested energy as a usable power source and integrating these systems with the image sensor. The fourth

objective is designing an ultra-low power CMOS APS imager which could be powered by the harvested energy.

The intellectual merits include: (1) providing a foundation for a new area of research on energy autonomous CMOS APS image sensors, (2) understanding the challenges in the design of ultra-low power image sensors, (3) understanding the challenges in the design of high efficiency solar energy harvesting structures, (4) developing high efficiency micro power management systems.

Two EHI type CMOS APS imagers that achieved all the set goals of the research are reported in this work. A new EHI pixel technology was developed for the first sensor (3rd generation EHI) for increasing the harvested energy fifteen times (15x) compared to the earlier EHI pixel technology. The pixel used in the 4th generation EHI sensor was designed for capturing images and harvesting energy simultaneously. Power generation capacity of the 4th generation EHI sensor was reduced by 33% compared to the 3rd generation EHI sensor. The 4th generation EHI imager achieved the world's lowest power consumption (270nW) while producing low-noise images at 0.7 frames per second, with a 96x96 resolution paving the way for an autonomous CMOS APS imager sensor.

ACKNOWLEDGMENTS

I would like to thank my major professor Dr. Suat Utku Ay for giving me the opportunity to conduct research on CMOS image sensors, for his valuable guidance and support in solving difficult problems throughout my doctoral studies and research, for coping with critical situations, and for his patience and encouragement throughout my doctoral research. His guidance helped me throughout my doctoral studies and research.

I would like to thank my committee members Dr. Fred Barlow, Dr. Aicha Elshabini, and Dr. Ahmed Abdel-Rahim for their valued comments that helped focusing my research direction.

I would also like to thank my colleagues in VLSI Sensors Research Group (VSRG) at University of Idaho for their support and help throughout my research.

DEDICATION

This dissertation is lovingly dedicated to my late mother, Rukiye Cevik.

Her support, encouragement, and constant love have been the main motivation throughout my life.

TABLE OF CONTENTS

LIST OF FIGURES

LIST OF TABLES

CHAPTER 1 - INTRODUCTION

Complementary metal-oxide-semiconductor (CMOS) image sensors has received a growing interest and become the dominant image sensor technology within the last two decades. This progress was due to low power consumption, high integration capability, and low manufacturing cost of CMOS image sensors.

Unlike the Charge Coupled Device (CCD) imagers, CMOS image sensors do not require dedicated manufacturing processes. They are built in the same mainstream CMOS electronic manufacturing processes used for manufacturing analog, digital, and mixed signal integrated circuits (ICs), such as digital logic ICs, microprocessors, memory, and application specific integrated circuits (ASICs). Therefore, CMOS image sensors can be integrated with peripheral digital and analog electronics. Complete camera systems can be integrated on chip, thus reducing the component, packaging, and system costs, [1].

CMOS IC manufacturing technology has grown faster than any other technology in history. Transistors became smaller, faster, and cheaper with continuous technology scaling in every process generation. Thus, more transistors were integrated on microchips, enabling denser and faster ICs that provide extended performance.

The main concern in CMOS IC and electronics design had been to achieve better performance at any cost. However, as the focus of electronic design shifts towards mobile applications, traditional optimization techniques targeting speed and performance are replaced with optimizations for energy efficiency. This is driven by the demand for agile portable multimedia systems that have been dominating the electronics market for the past decade. These systems should be designed to minimize power consumption while maintaining the

high performance demanded by customers. Thus, new design and integration techniques are required to overcome tradeoffs between energy consumption and performance.

A considerable portion of the image sensors manufactured today is used in battery-powered portable devices. Low cost image sensors consuming low power with highly integrated functionality are needed for these portable applications. Thus, one of the main design criteria for image sensors for portable applications is to minimize power consumption while maintaining the imager performance at a satisfactory level.

Portable devices put a limit on physical size and weight of the power source. Therefore, limited battery capacity mandates low-power designs, not only image sensor level but also on system level. A charge coupled device (CCD) image sensor dissipating 3 watts (W) of power will run less than an hour on a 1.2 V battery with 2000 mAh capacity, while a low-power CMOS image sensor consuming 3 μW will run 91 years on the same battery.

Increased heat generation due to increasing circuit density is a serious problem even for non-portable electronics systems. Therefore, power consumption has to be well controlled. Reduced thermal management and packaging costs result in cheaper electronic products with better reliability. Thus, it can be argued that the overall system cost can be reduced by utilizing low power design techniques.

Also, environmental concerns increase the demand for low-power designs and design techniques. Handling dead batteries had become a serious issue, mainly because, today's advanced battery technologies contain heavy metals and toxins. . Low power electronics design maximizes the useful lifetime of these energy source, while meeting performance requirements of the application and reducing the number of the batteries used over a certain time frame.

The power consumption of a system is set by the performance metrics of the application. Consumer electronics such as digital still cameras (DSCs), camcorders, portable multimedia devices, mobile phones, and tablets are all equipped with one or more high resolution image sensors. While power consumption of these image sensors puts a significant constraint on the battery life of the device, the high performance (resolution, frame rate, etc.) demanded by consumers limits the energy savings. Yet, there are applications which do not require high resolution images taken at high frame rates. Many modern wireless sensor applications require sensors to operate in isolated, dangerous, or off-limit remote areas for extended periods of time. In most cases, it is very hard to access these sensor systems to recharge or replace those power sources. Thus, it is required that the devices operate in an extremely energy efficient manner, while providing the demanded performance, making battery lifetime the top design priority.

Even the operation lifetime of a very low power, low-leakage, and energy-efficient system is limited by the finite energy stored and/or left on the power source or battery. Therefore, it is desirable for the sensors and/or systems to harvest ambient energy in the environment to assist the power source or completely eliminate the need for one. Designing electronic systems with energy harvesting capability is a promising field of study resulting in devices that could operate in isolated remote locations over extended periods of time.

The photovoltaic (PV) energy converter is a viable choice, among energy harvesters, due to its high conversion efficiency and compatibility with standard CMOS processes, [2]–[5]. Fortunately, the level of illumination required for operating an image sensor to capture images is sufficient enough for powering the imaging system if the light energy is harvested efficiently. Furthermore, the same PN-junction structures that are used for capturing scene

images in modern semiconductor image sensors could be reconfigured for harvesting required energy, thus eliminating the need for dedicated solar energy harvesting structures. Integrating energy harvesting capability into image sensors enables a reduction in the system cost and volume, [6]–[10]. The design of energy autonomous electronic systems are only possible by combining highly efficient on-chip energy harvesting structures and ultra-low power circuits and systems, [11].

1.1 Motivation and Goals

The focus of this research is to develop an energy autonomous, extremely low-power CMOS active pixel sensor (APS) imager. An energy autonomous CMOS imager can harvest the energy on its focal plane from the focused image and use the harvested solar energy to maintain its operation throughout its operating lifetime with no need to replace or recharge the power source. Research efforts are focused on two aspects to realize this energy autonomous image sensor: (1) reducing the power consumption of image sensor electronics by investigating and developing new circuit design techniques; (2) improving the energy harvesting efficiency of the micro solar cell structures embedded in CMOS APS pixels.

The world's first low-power image sensor with meaningful energy harvesting capacity was developed and presented in 2011 [10]. The Energy Harvesting and Imaging (EHI) sensor technology consumed impressively low power with good image quality and reasonable speed. The power consumption of the image sensor with 54x50 pixel resolution operating at 7.4 frames per second (FPS) was only 13.5 μW. However, the harvested energy was limited. Fundamentally, energy autonomous operation of the EHI imager was not possible with maximum harvested power of 3.5μW by the micro solar cell structures in the pixels. The second issue with this first EHI image sensor and its micro solar cell structure was the

sequential operation which did not allow the EHI imager to capture images and harvest energy at the same time.

Thus, ***the motivation*** of this research is to improve the existing EHI technology and achieve energy autonomous operation in next generation EHI imagers. To achieve these, the research is divided into ***four research goals***. ***The first*** goal is to investigate the fundamental principles, limits, and issues associated with photovoltaic energy harvesters in order to develop new energy harvesting pixel structures that can harvest more power than that of the current state-of-the-art 1st generation EHI imager. ***The second*** goal is the investigation and development of continuous mode micro energy harvesting and imaging structures as opposed to the current state-of-the-art structures that harvest energy and capture images sequentially. ***The third*** goal is to develop and integrate micro power management circuits, systems, and techniques that can condition the harvested energy. ***The fourth*** goal is to design and build an ultralow-power CMOS imager system which can be powered by harvested energy on the focal plane.

1.2 Applications

The primary commercial markets for an energy autonomous image sensor are wireless sensor applications deployed in the human body, such as visual implants, in highly toxic environments, and in remote hard to access areas. There are also military applications that require sensors to operate in enemy territory that might be hard or impossible to access for maintenance. Therefore, replacing or recharging the power sources or batteries is not an option for these sensor applications requiring energy autonomous operation.

1.3 Contributions

This research resulted in several advancements in the field of CMOS image sensors with low-power consumption and energy harvesting capabilities.

The initial phase of this research work explored new energy harvesting micro solar cell structures to overcome aforementioned short comings of the 1st generation EHI imager that motivated the first two goals of this research. This part of the research resulted in developing new energy harvesting micro solar cell structures that roughly produce an order of magnitude (10x) higher energy than that of the existing 1st generation EHI pixels.

The second (2nd) generation CMOS EHI image sensor using the same basic pixel and readout circuits and architecture was developed in 0.18μm CMOS process and published in 2012 [11]. The pixels in the 1st and 2nd generation EHI sensors were built by using different layers of the CMOS process. By comparing the energy harvesting capacity of the 1st and 2nd generation EHI devices, it was demonstrated that the manufacturing layers used in building the energy harvesting photodiode played an important role in energy harvesting capacity, [12]. These findings were used for building new energy harvesting micro solar cells with roughly ten times (10x) greater energy conversion efficiency for the third (3rd) and forth (4th) generation EHI sensors that have optimized sensor architectures and circuit design techniques.

The second contribution of this study is achieving continuous energy harvesting an imaging on the same focal plane. A unique pixel structure that can harvest energy with high conversion efficiency and capture images simultaneously was developed and integrated into the fourth (4th) generation EHI sensor.

The third contribution of this study is developing on chip power management systems that can condition harvested solar energy and generate usable power supply voltage

efficiently. Power management systems that can convert negative harvested voltage to a higher positive voltage are integrated on chip in the proposed 3rd and 4th generation EHI imagers.

The fourth contribution of the research is designing extremely low power image sensor electronics. Imager electronics and architecture were optimized for operating with low supply voltage while achieving the required image sensor performance. Unique readout architecture was developed to minimize the number of blocks that consume static power. The analog blocks that consume static power are biased with extremely low currents. All these unique solutions and approaches were integrated in the 4th generation EHI imager. Design details and measurement results are presented in subsequent chapters.

The overall outcome of this research is the design and implementation of the world's first energy autonomous CMOS image sensor that combines continuous mode highly efficient energy harvesting micro solar cell structures with ultra-low power CMOS electronics.

1.4 Organization of the Thesis

Chapter 1 introduces the research motivation, goals, and applications. It also summarizes the research contributions and the organization of this thesis.

Chapter 2 gives general background on CMOS active pixel sensor (APS) imagers. First, general information on CMOS image sensors are provided. Second, a brief historical background on CMOS image sensors is presented followed by a comparison of CMOS APS and CCD technologies and technical trends. Third, CMOS image sensor architectures, their functional sub-blocks and design requirements are discussed.

Chapter 3 discusses low-power CMOS image sensor design techniques. First, the low-power design methodology in CMOS image sensors at different levels of abstraction is presented.

Chapter 4 discusses the energy harvesting and imaging (EHI) sensor concept. First, details of solar energy harvesting are presented. Second, energy harvesting image sensors reported earlier are presented. Third, details of the 1st and 2nd generation EHI sensors developed in the VLSI Sensor Research Group (VSRG) of the University of Idaho are presented.

The remaining chapters discuss the primary contributions and measurement result of this work including: 1) new circuit and architecture level ultra-low power CMOS image sensor design methodologies, 2) two new energy harvesting and imaging (EHI) sensor designs, 3) details of the 3rd generation energy harvesting and imaging APS imager designed for 1 V operation with 3.3 μW core chip power consumption at 8 FPS and 46 μW power harvesting capacity, 4) 4th generation energy harvesting and imaging active pixel sensor designed for 0.8 V operation with less than 1 μW core chip power consumption and 31 μW power generation capacity.

Architectural and circuit details of the 3rd and 4th generation energy harvesting and imaging sensors are presented in Chapter 5 and Chapter 6. The ultra-low power image sensors are designed for 1.2V and lower supply voltage operation dissipating one-to-two orders of magnitude less power than that of the current state of the art CMOS APS imager. First, the image sensor architecture and details of analog and digital building blocks in these ultra-low power EHI type CMOS APS imagers are presented. Second, the energy harvesting mode of operation and power management blocks are presented.

Chapter 7 reports measurement results of the 3rd and 4th generation EHI sensors. First, electro-optical and imaging performance characteristics of the 3rd and 4th generation EHI sensor are measured and reported. Second, the power generation capabilities of the two sensors are characterized. Third, the performance and efficiency of the power management blocks are characterized. Fourth, 3rd and 4th generation sensors are compared to each other and other similar image sensor technologies in the literature.

Chapter 8 summarizes major accomplishments achieved in this research and presents ideas for future research.

CHAPTER 2 - CMOS IMAGE SENSORS

Solid state image sensor is a semiconductor device that converts photon energy incident on the photo sensitive element (i.e. pixel) into electrical signal (current or voltage). Photons absorbed by the photosensitive materials or structures energize electrons in the valence band into conduction band generating ideally one electron-hole pair per absorbed photon. Image sensor effectively separates these photo-generated electrons from holes, converts them into an electrical signal, processes this signal, and regenerates the scene image dropped on the pixel array.

The most commonly used material in mass production of electronic devices today is silicon. Silicon has a bandgap which makes it a suitable material for absorbing visible light spectrum. Therefore, silicon is commonly used for manufacturing image sensors, [13].

A brief technological and historical background on complementary metal oxide semiconductor (CMOS) image sensors with emphasis on active pixel sensor (APS) is presented in this chapter. First, basics of solid state image sensors are presented. Second, a brief historical background on image sensors together with a comparison of CMOS APS and CCD technologies and technical trends for CMOS APS is presented. Third, image sensor applications are presented. Forth, a generic CMOS image sensor architecture and its functional blocks are introduced. Finally a summary of the chapter is presented.

2.1 Brief Historical Background on Image Sensors

First solid state image sensors before charge coupled device (CCD) and CMOS active pixel sensors (APS) were the metal oxide semiconductor (MOS) image sensors. In the 1960's several groups around the world achieved varying degrees of success in building solid-state

image sensors. In 1967, Weckler proposed using PN-junctions as pixels operating in photon flux integrating mode, [14]. The generated photo current discharges the initial charge stored on the parasitic capacitance of the PN-junction. The change in the stored charge will be proportional to time integral of the photocurrent. He proposed addressing the pixels using a PMOS switch and converting the current pulse into a voltage pulse using a series of resistors. An image sensor with 100x100 array of photodiodes operating in a photon flux integration mode was reported in 1968, [15]. Noble described several configurations of self-scanned 2D silicon image detector arrays in 1968, [16]. Buried photodiodes were also discussed to reduce dark current as well as regular photodiodes. Noble also discussed a charge integration amplifier for readout, and the first use of a MOS source-follower transistor in the pixel for readout buffering. Chamberlain reported an improved model of the sensor in 1969, [17]. The main issue with these early MOS image sensors was the fixed-pattern noise (FPN) due to pixel-to-pixel variations. FPN was explored in 1970 by Fry, Noble, and Rycroft, [18].

The CCD image sensor array was first reported in 1970, [19]. Low FPN was one of the main reasons for its adoption. Another reason for adoption of CCDs was the smaller pixel size due to simplicity of the CCD pixel.

After the CCD's introduction, the main focus of research and development has been CCD sensor performance for decades. Criteria such as quantum efficiency, pixel fill factor (fraction of photo sensitive area to total pixel area), dark current, charge transfer efficiency, smear, readout rate, lag, readout noise, full well, and dynamic range favored CCDs over other solid state imagers. Number of pixels integrated in image sensors has been increasing steadily due to the resolution demand of new TV formats (i.e. HDTV) and scientific applications. In parallel, pixel size has been reduced to increase circuit density on sensor and to reduce cost.

Because of their low image quality due to immature manufacturing technology, MOS image sensors had received little or no attention and research effort in 1970s and 1980s unlike CCDs.

Two independently motivated efforts have led to the rebirth of MOS and CMOS image sensors in early 1990s. The first effort was to create low cost, reasonable performance, highly functional single-chip imaging systems by researchers at the University of Edinburgh in Scotland and Linkoping University in Sweden. The second was the effort by researchers at U.S. Jet Propulsion Laboratory (JPL) to design highly miniaturized, low-power, instrument imaging systems for next-generation deep space exploration spacecraft needed by U.S. National Aeronautical and Space Agency (NASA). The technology developed at JPL was subsequently transferred to AT&T Bell Labs, Kodak, National Semiconductor and several other major US companies, including Photobit (later Aptina). These efforts have led to significant advances in CMOS image sensors and the development of the CMOS APS imagers. The CMOS APS imager performance had become competitive with CCDs in terms of read noise, dynamic range and responsivity as of early 2000s. A noteworthy one is the CMOS APS imager developed by A. Krymski *et al*. from Photobit Corp. that was featured as 500 frames per second frame rate, 1024 x 1024 array size, 8-bit digital output with 450mW power consumption in 1999, [20]. In 2000, Foveon announced a CMOS image sensor with a resolution of 4,096 x 4,096, which is about twice the resolution of 35mm film by some measures. By 2009, market share of CMOS image sensors suppressed CCDs in practically every application market.

2.2 Comparison of CMOS APS and CCD Technologies

Charge-coupled devices (CCDs) and CMOS image sensors are both implemented in silicon substrates. The optical properties of the substrate dictate image sensor response to light. Therefore, CCDs and CMOS image sensors have similar responses to light known as quantum efficiency. The two technologies differ mostly in readout and process steps used during manufacturing.

The CCD is basically an analog shift register that shifts electrons collected in pixels to an output amplifier. The efficient shifting of electrons through thousands of stages requires dedicated CCD fabrication processes providing perfect charge transfer that deviate from main stream CMOS manufacturing processes. The charge transfer operation requires multiple high voltage supplies, which is incompatible with low-power/low-voltage CMOS processes. CCD fabrication processes are also optimized for minimizing the pixel dark current and improving the quantum efficiency. The CMOS APS on the other hand operates from a single supply.

CCD performance has been perfected with tremendous research effort since their introduction. They achieve low readout noise, high dynamic range, and excellent photo responsivity. However, dedicated CCD fabrication process precludes cost-efficient integration of on-chip supplementary circuits. Timing generators, clock drivers, signal processors, and analog to digital converters (ADCs) are commonly off-chip increasing power consumption and volume of CCD based camera systems. CCDs are capacitive devices in nature and significant supply currents are needed by the circuits driving horizontal and vertical CCD shift register circuits. On the other hand, CMOS APS needs address only one or two rows for readout and/or reset and uses much less power compared to the CCDs, [1][21].

The most important advantage of CMOS APS image sensors over CCDs is their ability to *integrat*e many functional blocks (i.e analog and digital signal processors, drivers, ADCs, DAC, etc.) on-chip same die as the pixel array. Integration of electronics enables miniaturization of imaging systems and reduces amount of interfaces. The CMOS APS, which is fabricated in common CMOS process technologies, offers low-power consumption, low-supply voltage operation, good imaging performance, low noise, no lag, no smear, good blooming control, simple clocks and monolithic integration. Additionally, random pixel or window access is possible since the pixel outputs are not shifted out sequentially, [1].

CCD has analog output(s) running at high frequency with a large voltage swing. Driving analog data off-chip requires very large bias current to charge output pad capacitors at the serial data rate because the analog output must settle quickly to preserve dynamic range. In contrast, the CMOS APS imager with on-chip ADC(s) has digital output. Driving digital output pad requires less current since digital output is much more robust and settling is not an issue. The overall power consumption of pixel readout circuits in CMOS APS imagers such as pixel source followers and charge amplifiers are significantly lower compared to CCD output amplifiers, [22].

Despite aforementioned advantages, image quality of CMOS APS imagers have been lacking behind the CCDs for many years. Early CMOS image sensors suffered from large FPN caused by wide dark current variations. However, this issue is improved over the past two decades and modern CMOS APS imagers have similar or in some cases better FPN performance than the CCDs.

2.3 CMOS Image Sensors

When a flux of photons is incident on a semiconductor material, the photons that have energy exceeding the semiconductor's bandgap energy generate electron hole pairs. Photon energy is given by (2.1).

$$E = h\nu = \frac{hc}{\lambda} \tag{2.1}$$

Silicon bandgap energy of 1.11 eV corresponds to a wavelength of 1100nm which means silicon material absorbs photons with wavelengths shorter than 1100nm. Photons absorbed in semiconductor image sensors goes through several steps before a scene image is generated as shown on Figure 2-1.

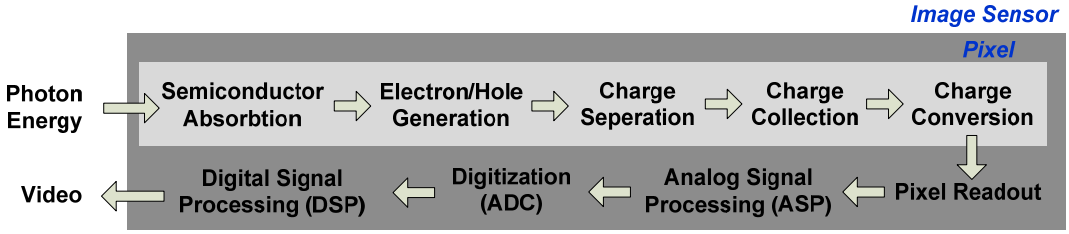


Figure 2-1. Journey of impinging photons in an image sensor.

Electron hole pairs generated in semiconductor material recombine unless they are separated. Positive (holes) and negatively (electrons) charged carriers can be separated by applying an electric field. The separated charges could either be quantified as a current or stored on a capacitor and converted to a voltage. Two structures are commonly used for

applying electric field and storing photo generated charges; a reverse biased PN-junction diode (photodiode) or a Metal Oxide Semiconductor (MOS) capacitor (photogate), [23].

Conversion of photons to electrical charge is followed by reading out the collected charge. The collected charge is converted into measurable voltage or current quantities. The analog voltage or current is buffered, processed and converted to digital data. These operations can be done at different levels. In CCDs charge transfer and buffering are on chip and signal processing and digital conversion are off chip. In all CMOS APS imagers buffering is done in pixel. Readout, signal processing and digital conversion may be global, column level, or pixel level.

CMOS image sensor system in general consists of a pixel array, row and column addressing circuits, column read out circuits, analog signal processors (ASPs) and analog to digital converters as shown in Figure 2-2. The pixels are typically selected one row at a time by row addressing circuit built as either a shift register or a decoder. The pixels are read out through vertical column busses connected to column readout circuitry. Column readout is followed by analog signal processors (ASPs). The ASP(s) perform functions such as charge integration, gain, sample and hold, correlated-double-sampling and FPN suppression. Analog output from ASP(s) is converted into digital video by the ADC block. ADC block might consist of a single or multiple ADCs. Column parallel image sensors have an ASP and an ADC on each column of pixels. In this structure a shift register or a multiplexer is required for reading out the ADC outputs. Column Series image sensors have global ADC(s) processing analog outputs from all columns. In this architecture, analog outputs of the ASPs delivered to the ADC are selected by column addressing logic that can be either a shift register or decoder.

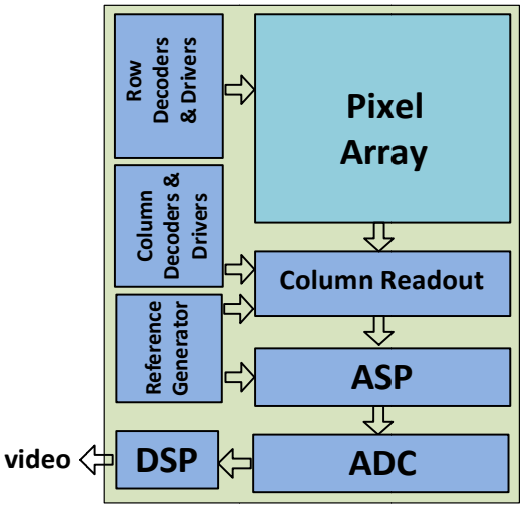


Figure 2-2. Functional blocks in a CMOS image sensor.

Single chip CMOS imager systems have voltage and current references, timing generator, logic controls, and digital signal processing (DSP) circuits integrated on the same die as the pixel array. The digital blocks are defined at a high level and implemented on-chip using automated synthesis and place-and-route tools, [1].

2.3.1 **CMOS Pixels**

There are three fundamental approaches to build pixels in CMOS APS imagers: photodiode-type passive pixel, photodiode-type active pixel, and photogate-type active pixel, [1]. Active pixels have an amplifier in the each pixel for non-destructively buffering the photo generated charge and driving the output buses, while photodiode is directly connected to the output bus in a passive pixel.

2.3.1.1 *Passive CMOS Pixels*

The photodiode-type passive pixel approach was first suggested by Weckler in 1967, [14], [15]. Figure 2-3 shows the basic structure of a passive pixel and the column charge

amplifier. Passive pixel consists of a photodiode and an access switch. When the access switch is turned on, the photodiode is connected to a column bus. A column charge amplifier connected to the column bus keeps the voltage on the column bus constant and reduces thermal noise, [16]. When the photodiode is accessed, the voltage on the photodiode is reset to the column bus voltage. The charge transferred to the photodiode, is converted to an output voltage by the column amplifier. The photodiode passive pixel has a very high pixel fill factor (ratio of photosensitive area or photodiode to total pixel area) due to the fact that only on access transistor is integrated in each pixel along with the photodiode. Thus, the pixel size can be very small. A second selection transistor could also be added to achieve X-Y addressing. Quantum efficiency of the passive pixel (ratio of collected electrons to incident photons) can be quite high as a result of the large pixel fill factor and absence of polysilicon layer found in CCDs and photogate pixels.

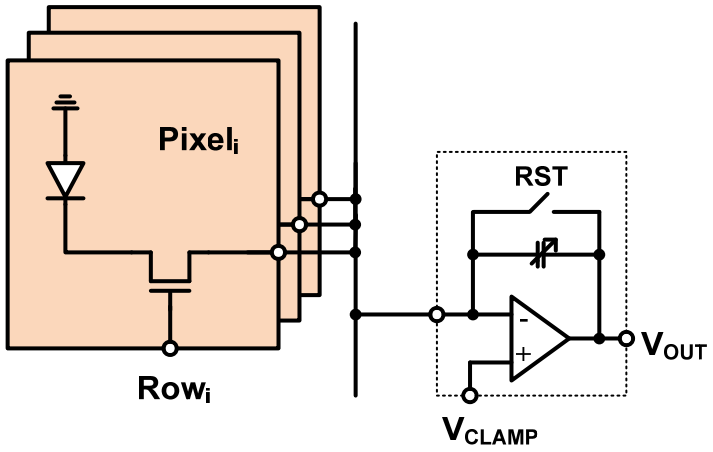


Figure 2-3 Passive CMOS pixel schematic and column amplifier.

The readout noise is the biggest problem with the passive pixel. Readout noise in a passive pixel is typically on the order of hundred(s) of electrons r.m.s. while it is less than few electrons r.m.s. in a CCD. Another issue is scaling problem. The passive pixel also does not scale well to larger array sizes and or faster pixel readout rates since more pixels connected to a column bus increases the bus capacitance. Increased bus capacitance and faster readout speed results in higher readout noise and higher power consumption. Passive pixel sensors also suffer from large fixed pattern noise from column amplifiers.

2.3.1.2 *Active Pixels*

Buffering the photodiode voltage via an in-pixel amplifier eliminates the performance issues with the passive pixel. A sensor with an in-pixel amplifier is known as an active pixel sensor (APS). The source follower type in-pixel amplifiers are typically used in APS pixels. The pixel source followers are enabled only during pixel readout. Therefore, the power consumption of pixels is relatively low despite the use of active amplifiers.

2.3.1.2.1 Photodiode Type CMOS APS

The photodiode-type APS was proposed for solving the issues with passive pixel in 1968, [16]. However, the first high-performance PD-APS was demonstrated in 1995 by JPL researchers, [24]. A circuit diagram of a typical photodiode-type (PD) APS is shown in Figure 2-4. The photodiode-type APS pixels have high quantum efficiency as there is no overlying polysilicon. Typical photodiode-type APS uses three transistors (3T) per pixel. M1 is the reset transistor, M2 is the pixel source follower and M3 is the row select transistors.

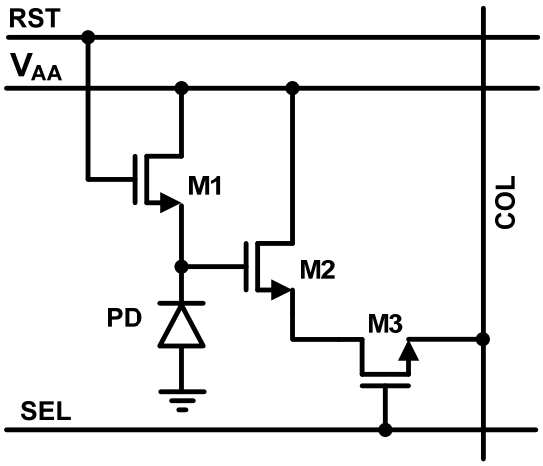


Figure 2-4. Schematic of a there transistor (3T) photodiode type CMOS APS pixel.

Reset transistor sets the photodiode node to a known voltage (V_R) at the beginning of integration period. This voltage is stored on the depletion capacitance of the photodiode. The stored negative bias increases the built-in electric field from N-region to P-region in the PN-junction. During the integration period, reset transistor is turned off, photodiode is floating and exposed to light. Light exposure creates excess electron hole pairs. The built in electric field drifts photo generated electrons to N-region and holes to the grounded P-region. Drifted photo generated charges discharge the photodiode capacitance during the integration period. Thus, at the end of integration period, the final voltage across the photodiode depends on the light level. Pixels receiving more light will discharge faster than those receiving less light. Pixel source follower transistor is basically a voltage buffer for driving the capacitive column bus isolating the floating photodiode node from the readout electronics and allowing non-destructive readout. Row select transistor connects the pixels in selected row to the column bus. More complex CMOS APS pixel structures with added transistors for improving performance are also available. However, all CMOS active pixels have the similar basic operation.

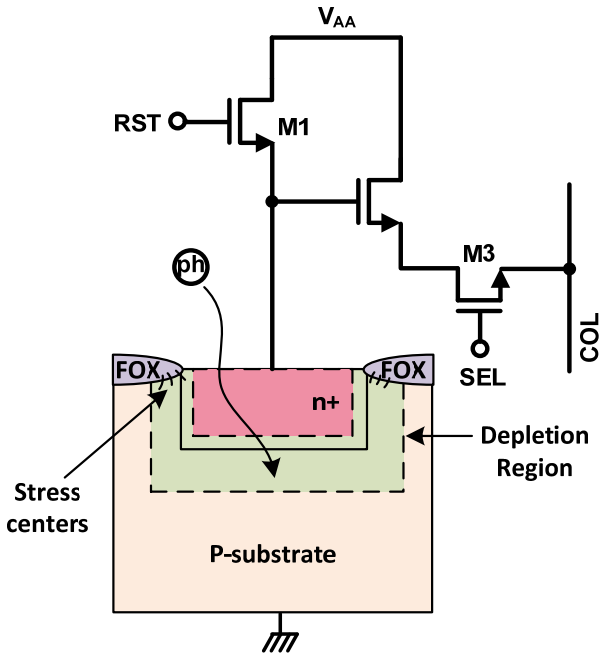


Figure 2-5. Cross sectional view of photodiode in 3T CMOS APS Pixel.

Cross sectional view of a photodiode is shown as shown on Figure 2-5. Extended field oxide (FOX) formed around n+ regions in standard sub-micron CMOS processes induce dark currents due to stress centers, [25]. Surface defects and surface recombination centers are other sources of dark current which also cause quantum loss in shorter wavelengths. These surface recombination centers absorb photo generated charges created close to the surface. Since the short wavelength photons are absorbed close to the surface, the photodiode response to blue/UV spectrum is poor.

Blue response and dark current issues related to surface defects are improved by burying the n-region under a thin surface p+ region as shown in Figure 2-6. This structure is known as buried photodiode or pinned photodiode and requires special manufacturing process. The doping concentrations have to be very well controlled to shape the photodiode's potential well correctly, [23]. The potential well in the buried photodiode allows complete

charge transfer from the photodiode to a floating diffusion. Therefore, a floating diffusion node and a transfer gate are added to the pixel for low noise readout. FD node is reset and the reset level is read. After that, the buried photodiode charge is transfer to the FD node by turning the TX gate on. The floating diffusion node is read again representing the signal level. The difference between these values is the absolute signal proportional to the light. This readout scheme is known as correlated double sampling (CDS) readout and it suppresses thermal noise from pixel reset, 1/f noise from the in-pixel source follower, and fixed pattern noise due to pixel-to-pixel variation in pixel transistors.

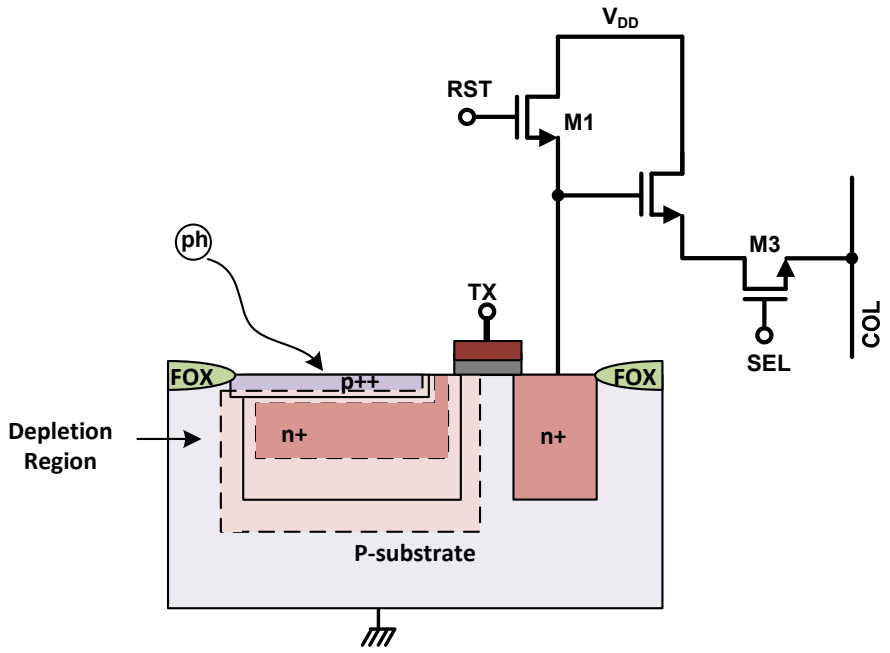


Figure 2-6. Cross sectional view of a buried (pinned) photodiode in CMOS APS pixel.

2.3.1.2.2 Photogate Type CMOS APS

The photogate type APS was developed in 1993 for high performance scientific imaging and low light applications at JPL, [26]–[28]. Photogate concept was adapted from CCD technology for low noise charge collection. The photogate type APS pixel schematic is shown in Figure 2-7.

When a positive voltage is applied to the photogate (PG) electrode, the holes are repelled and a depletion layer is formed under the gate oxide. The depletion region collects photo generated electrons while the holes flow to the ground due to the internal electric field across the depletion region. The charge collection region in a photogate extends to surface of silicon just like the photodiode. However, in photogate, the surface or the MOS device channel has better quality than that of the photodiode leading to lower surface dark current. In addition, there is no stress related dark current component in photogate. These lead to a very low dark current. The surface effects can be reduced even more by using buried photogate.

Signal charge is integrated under the photogate while the floating diffusion node (FD) and transfer gate (TX) are added to the pixel for correlated double sampling and low noise readout. The photogate-type APS is typically larger than the photodiode-type APS due to the added components.

FD node is reset and the reset level is read first. Then the charge under the photogate is transfered to the FD node by pulsing the photogate and turning the TX gate on. The FD node voltage is read after the charge transfer again. The difference between the values before and after charge transfer is the absolute signal value accumulated under the PG during integration period.

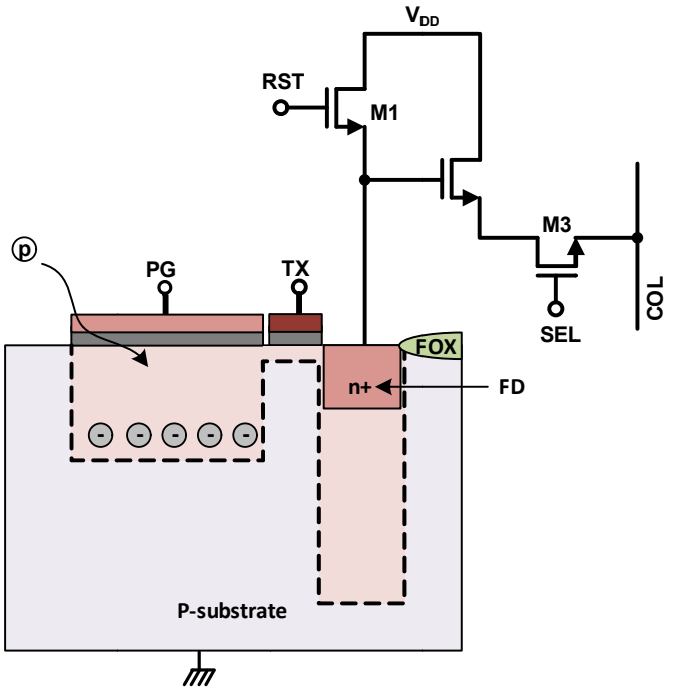


Figure 2-7. Cross sectional view of a photogate (PG) type CMOS APS pixel.

2.3.2 **Analog Signal Processing (ASP)**

A charge integration amplifier is used for readout in passive pixel sensors and sample and hold circuits are used for active pixel sensors. Once the voltage at the source follower output is stored on sample and hold capacitors, pixel readout is completed. Reset noise, 1/f noise, and FPN due to the pixel-to-pixel process parameter variations are largely suppressed by correlated double sampling (CDS) operation performed in the ASPs, [1]. Typically, sample and hold circuit is followed by a programmable gain charge amplifier in the ASP. After the CDS and gain operations in ASP, the pixel data is sent to the analog-to-digital converters. Other analog signal processing functions such as level shifting, offset cancellation, delta-double sampling etc. may also be implemented in the ASP.

2.3.3 **Analog-to-Digital Converter (ADC)**

Processed analog pixel outputs can be converted to digital code in a CMOS imager. Depending on the system architecture, a single global ADC operating at high speed, column ADCs operating at lower speeds or in pixel ADCs might be used.

On-chip ADC is desirable for several reasons. Digital signals have better noise immunity compared to analog one. Integrating more components on a single chip reduces component count and overall system cost. Since powerful amplifiers are not needed to drive analog output pads and off chip capacitive loads, lower system power can be achieved.

The ADC must support video data rates depending on the resolution and frame rate. The ADC must have at least 8-bit resolution with low integral non-linearity (INL) and differential non-linearity (DNL) so that the image quality is not degraded. The ADC must consume minimal power and chip area. The ADC must be well isolated from the pixel array and analog components so that the switching noise from the ADC does not couple to these blocks and reduce image quality.

The ADC can be implemented as a single high speed ADC running serially or multiple lower speed ADCs running in parallel. Column parallel architecture is widely used in which each pixel column has its own ADC. The speed requirement of the ADC is reduced by the number of columns in the array. A column parallel architecture is preferred for high-resolution, high-speed and low-power operation. However the ADC size needs to be compact. Ramp ADCs are usually used in this architecture due to its compact size. Successive approximation (SAR) ADCs consume less power compared to ramp ADCs. However, they require a larger area and they are hard to fit into small column pitches. The column parallel architecture allows low bandwidth readout resulting in lower noise images, [29], [30]. They

have also been shown to have lower overall power consumption, [31]. Column parallel architecture is preferred also because of the higher speed of multiplexing digital data compared to the multiplexing analog signals, [30].

Introduction of high speed analog-readout circuits allowed faster analog multiplexing and implementing high speed serial readout channels, [30]. Column series architecture uses a single global charge amplifier and ADC for the whole imager. A single ADC runs at higher speed and it is not practical to build high resolution and high speed imagers. However a single global ADC avoids the addition of fixed pattern noise and it saves chip area.

Comparison of different topologies available for CMOS image sensor integration are listed and compared in Table 2-1.

Table 2-1. Comparison of ADC topologies for CMOS image sensors.

ARCHITECTURE	RESOLUTION	POWER	ENERGY PER SAMPLE	CLOCK CYCLE	SPEED	ADVANTAGES / DRAWBACKS
FLASH	8 bits	>50 mW	~50 nJ/S	1	10 Msps –1 Gsps	+ Extremely fast + High input bandwidth - Highest power consumption - Large die size - High input capacitance - Expensive - Sparkle codes*
SUCCESIVE-APPROXIMATION REGISTER (SAR)	8 bits–16 bits	~100 μW	~100 pJ/S	N	75 Ksps –2 Msps	+ High resolution and accuracy + Low power consumption + Few external components - Low input bandwidth - Limited sampling rate - VIN must remain constant during conversion
INTEGRATING / RAMP	>14 bits	~1 mW	~10 nJ/S	2^N	< 100 Ksps	+ High resolution + Low supply current + Excellent noise rejection - Low speed
SIGMA-DELTA (Σ-Δ)	>14 bits	>10 mW	~5 nJ/S	$<2^N$	> 200 Ksps	+ High resolution + High input bandwidth + Digital on-chip filtering - External T/H - Limited sampling rate
PIPELINE	10 bits–14 bits	>10 mW	10 nJ/S	N+1	10 Msps –100 Msps	+ High throughput rate + Low power consumption + Digital error correction and on-chip self-calibration - Requires 50% duty cycle typical - Requires minimum clock frequency

2.4 Summary

An overview CMOS image sensors was presented in this chapter. A brief historical background on image sensors was followed by a comparison of CMOS active pixel sensor (APS) technology and CCD technology. Finally, CMOS image sensor and its functional blocks were introduced. Pixel circuits, analog signal processing, and analog-to-digital converter were discussed in detail.

CHAPTER 3 - LOW-POWER CMOS IMAGE SENSOR DESIGN

Many modern mobile applications require image sensors to operate in off-limit areas for extended durations. Such systems are expected to provide reliable operation without human interference Examples of such systems include, but are not limited to, retinal prosthesis, and wireless sensors operating in remote, hard to access areas. Powering these systems is a serious challenge. Limited battery capacity is a serious constraint limiting the operation lifetime of such systems. Moreover, the physical size of the battery is limited by the specifications of these applications. Therefore, energy efficiency is the key design priority not only for designing these systems but also for the image sensors that would be integrated in these remote wireless sensors systems.

Compact and fully integrated active pixel sensor (APS) imagers can be built in standard CMOS manufacturing technology. Integrating all components of the imager electronics on-chip results in smaller interconnect capacitances and lower overall dynamic power consumption. While, ultra-low power high-speed image sensor sub-systems can be designed at relatively low cost in scaled CMOS technologies. [1]

Low-power CMOS image sensor design requires a well-defined design methodology to handle the power budget. Cost, power, speed, and performance tradeoffs need to be considered to achieve the specifications with minimal power.

In this chapter, the factors contributing to total power consumption in a CMOS image sensor are presented first. Second, energy figure of merit (*e*FoM) for comparing power consumption of different CMOS image sensor designs is introduced. Third, low-power design

methodology in CMOS image sensors is described at different levels of abstraction. Fourth, low voltage image sensor design techniques in the literature are reviewed. Finally, all are summarized at the end of the chapter.

3.1 Power Consumption in CMOS Circuits

There are four main components of power consumption in a CMOS image sensor. These are dynamic power consumption ($P_{dynamic}$), static power power consumption (P_{static}), short circuit power consumption (P_{short}), and leakage power consumption ($P_{leakage}$). The average power consumed in a CMOS circuit is given in (3.1).

$$P_{average} = P_{dynamic} + P_{static} + P_{short} + P_{leakage} \tag{3.1}$$

Dynamic power consumption is the power consumed by a digital gate while switching. During input transition, the digital gate charges the load capacitance voltage from one voltage level to another charging or discharging the energy stored on the parasitic load capacitor. This charge flow from power supply to ground is repeated every time when the digital gate output is switched. In general, the output of a gate will not switch at every clock period. Power is consumed only when the output node(s) is switched not the input node(s). Average number of transitions for the output node per clock cycle is known as transition probability (α). The average power consumed in a CMOS circuit due to this charge flow during output transitions is given in (3.2).

$$P_{dynamic} = \alpha \cdot f \cdot C_L \cdot V_{DD} \cdot V_{swing} \tag{3.2}$$

α is the transition probability of the output, f is the operating frequency, C_L is the equivalent load capacitance, V_{dd} is the power supply voltage, V_{swing} is the voltage swing at the output node, [32].

Static power is consumed by analog blocks such as amplifiers, voltage references, and constant current sources. These analog blocks consume power from supply as long as they are turned on. Therefore, they are powered off when they are not actively used to prevent unnecessary static power consumption. The average static power consumed by an analog block is given in (3.3).

$$P_{average} = \beta \cdot V_{DD} I_{static} \tag{3.3}$$

β is the duty cycle of blocks consuming static power and I_{static} is the bias current.

During output transition of digital circuits, pullup and pulldown transistors are simultaneously on for a short duration due to finite rise and fall times of the logic gate input signals. This creates a short circuit path from power supply to ground. The power consumed due to this short circuit is given by (3.4).

$$P_{short} = V_{DD} I_{short} \tag{3.4}$$

I_{short} is the mean current flowing from power supply to ground during the output transition, [33]. This current can be minimized using high threshold devices. When sum of the thresholds of PMOS and NMOS transistors are larger than the supply voltage, PMOS and NMOS transistor will not be on at the same time. Therefore, short circuit current will be minimized since it flows only when the pull up and pull down transistors are on simultaneously.

Leakage currents of reverse biased PN-junctions in MOS transistors and the subthreshold conduction of transistors in cut off mode are the source of leakage power consumption, [34]. Leakage power consumed in a circuit is given by (3.5).

$$P_{leakage} = V_{DD} I_{leakage} \tag{3.5}$$

$I_{leakage}$ is the equivalent total leakage current drawn from power supply. Leakage power is consumed as long as the circuit is connected to power supply bus even though no input is actively applied unlike dynamic, short circuit, and static power consumptions which are consumed only when the circuit has active inputs or outputs.

Effective ways to reduce dynamic power consumption are to reduce the load capacitance, the power supply voltage, the operating speed, and the output activity. Technology scaling contributes to power reduction by lowering both the supply voltage and the parasitic device capacitances. Reducing the supply voltage reduces switching, static, short circuit and leakage power consumptions all together. However, there are limitations to supply voltage scaling. Performance of a circuit is reduced as supply voltage is lowered. The performance degradation is partially compensated by higher doping levels and lower threshold voltages. Reduced transistor threshold voltages allow supply voltage reduction. In practice there are limits to the minimum allowable threshold voltage due to reduced noise margins and exponentially increasing subthershold leakage current. Moreover, threshold voltage variations become more severe as threshold voltage is reduced. Therefore, supply voltage scaling has a limit, [35]–[38].

3.2 Power Consumption Figure of Merits

Power consumption of imagers change with array size and frame rate. In order to compare the power consumption performance of different CMOS image sensor architectures, an energy figure of merit (*e*FoM) is used. The energy figure of merit is defined as the energy consumed for capturing and digitizing light information by a single pixel. This measure is a good indicator of the relative power performance for different image sensor architectures operating at different frame rates and array sizes.

Energy consumed by an image sensor for capturing one frame is given by (3.6).

$$E_{frame} = \frac{P_{Total}}{FR} \tag{3.6}$$

P_{Total} is the total power consumption of the imager IC including all electronics and pads, and FR is the frame rate. The *e*FoM is obtained by dividing the frame energy by the array size. Thus, the *e*FoM is given by (3.7).

$$e\text{FoM} = \frac{P_{Total}}{FR \cdot m \cdot n} \tag{3.7}$$

m and n are the pixel array size on X- and Y-directions.

The *e*FoM could be used for image sensors with both analog and digital outputs. Other figure of merits are also used for digital output image sensors. The image sensor figure of merit (iFoM) is defined for CMOS image sensors that have on chip analog-to-digital converters (ADCs) and provide n-bit digital output [10]. The iFoM quantifies the total energy

consumption per pixel for one code quantization of effective pixel signals and for driving them off chip. Thus, total power consumption of the chip is used for calculating iFoM in Joule per pixel per quantization level or code. The iFoM is given with (3.8).

$$i\text{FoM} = \frac{P_{Total}}{FR \cdot m \cdot n \cdot 2^{K}} \qquad \text{(Joule/pixel*code)} \tag{3.8}$$

K is the resolution of the ADC used in the image sensor. Typically, bit resolution of an ADC (N_{ADC}) does not reflect true effective bit resolution. Effective number of bits (ENOB) at sampling frequency to maintain the frame rate has to be used in iFoM equation instead of N_{ADC} for truly quantifying the energy consumption per quantization level.

3.3 Low-Power Circuit Design Methodology

Reducing the power consumption of a system requires optimization of power consumption on every level of abstraction. Supply voltage might be reduced through process level, circuit level, architectural level or system level optimizations. Tradeoffs between power, performance and area must be carefully evaluated to achieve optimal design. The performance should satisfy design specifications despite aggressive scaling of the power. Freedom of design choices depend on design specifications. Power optimization methodology in each level of abstraction is introduced in this section.

3.3.1 **Reducing Power Consumption at Process Level**

Technology scaling had been the driving force for advances in semiconductor industry. Technology scaling increases transistor density and performance while reducing

power consumption and manufacturing cost through scaling transistor dimensions, operating voltage, and doping.

Starting with early 1970s, gate length (L), width (W), gate oxide thickness (t_{ox}) and diffusion depth has been decreasing by 0.7 times every three years. This corresponds to doubling of number transistors on a given silicon area. The supply voltage needs to be scaled down as the lateral and the vertical dimensions of a MOS device are scaled down in order to keep the internal electric field constant. When a voltage (V) is applied across two terminals separated by a distance d, the electric field magnitude (E) is given by (3.9).

$$\left|\vec{E}\right| = \frac{V}{d} \tag{3.9}$$

Since the gate oxide thickness and channel length are scaled with a scaling factor k, voltages applied across the gate oxide (V_{GB}) and channel (V_{DS}) needs to be scaled down proportionally. Additionally doping concentrations are increased with the same scaling factor k to make up for the reduced voltages. Reduced oxide thickness, supply voltage and increased doping concentration results in threshold voltages scaled by the same scaling factor, k. Drain current (I_D) both in saturation and linear regions are also scaled by the same scaling factor as a result of scaled W, L, t_{ox}, V_{GS}, V_{DS}, and V_{th} if mobility μ_n stays constant and channel length modulation factor λ is much smaller than 1 as shown in equations (3.10) and (3.11).

$$I_D' = \frac{\mu_n \varepsilon_{ox}}{t_{ox}/k} \cdot \frac{W/k}{L/k} \cdot \left[\left(V_{GS}/k - V_{th}/k \right) \cdot V_{DS}/k - \frac{\left(V_{DS}/k \right)^2}{2} \right] \cong I_D/k \tag{3.10}$$

$$I_D = \frac{1}{2} \cdot \frac{\mu_n \varepsilon_{ox}}{t_{ox}/k} \cdot \frac{W/k}{L/k} \cdot \left[\left(V_{GS}/k - V_{th}/k \right)^2 \cdot \left(1 + \lambda \cdot \left(V_{DS}/k \right) \right) \right] \cong I_D/k \tag{3.11}$$

As the feature sizes are scaled down, transistor and interconnect capacitances are decreased proportionally. Moreover, increased number of metal layers in advanced process technologies reduce the interconnect capacitances to ground. Reduced capacitances are driven by the unchanged device resistances (V/I). Therefore, transistor delay is scaled by the same scaling factor as shown in equation (3.12).

$$T_D' = \frac{V/k \cdot C/k}{I/k} = T_D/k \tag{3.12}$$

Technology scaling has a quadratic effect on power dissipation of individual transistors due to the reduced voltage and current levels as shown on Table 3-1. The power delay product is reduced by k^3, [39].

Table 3-1. Effects of technology scaling on device parameters.

Parameter	Scaling Factor
W, L, t_{ox}	$1/k$
V_{dd}, V_{th}	$1/k$
C_{ox}	$1/k$
Parasitic Capacitance	1/k
I_D	$1/k$
Delay (T_D)	$1/k$
Substrate Doping (N_A)	K
Power Consumption	$1/k^2$
Power-Delay Product	$1/k^3$

The next 15 year's forecast for scaling physical gate size and supply voltage are shown in Table 3-2, [40]. The most advanced technology should be chosen for low-power consumption as evident from the scaling laws.

Digital circuits can benefit most from the next generation technology for reducing area, speed, and power. However, performance of imaging blocks and analog blocks are more sensitive to adverse effects of technology scaling than digital circuits. CMOS image sensors require a stable, well-characterized technology. For example, voltage supply reduction has a serious impact on the signal-to-noise ratio and dynamic range of the imager.

Table 3-2. 15 years' feature size and power supply scaling forecast for CMOS processes.

Year of Production	2011	2012	2013	2014	2015	2016	2017	2020	2023	2026
DRAM ½ Pitch (nm)	36	32	28	25	23	20	17.9	12.6	8.9	6.3
ASIC Physical Gate Length (nm)	26	24	21	19	18	16	14.5	10.8	8.1	5.8
Power Supply (V)	0.90	0.87	0.85	0.82	0.80	0.77	0.75	0.68	0.62	0.57

Power consumption of CMOS APS image sensors are expected to decrease as supply voltages decrease with technology scaling in CMOS processes. CMOS image sensors will benefit from technology scaling by reducing pixel size, increasing resolution, and integrating more analog and digital circuits on the same chip with the sensor, [41].

Shallow junctions and high doping concentrations result in low photoresponsivity. Shallow trench isolation (STI), thin gate oxide layer, and salicide layers result in unacceptably high dark current. In-pixel transistor leakage is another significant source of dark current and it increases as technology scales down. Increased number of interconnect layers and the slow

scaling of inter connect layers increase the relative vertical distance from IC surface to the photo detector area. This effect together with the use of silicon dioxide/nitride materials reduces light transmission to the photo detector. Reduced photoresponsivity, limited voltage swing at the photo diode node, increased dark current, increased switch resistances, decreased performance of analog blocks and similar design challenges associated with technology scaling and supply voltage reduction drastically affect the performance of CMOS image sensor, [41] [42].

3.3.2 Reducing Power Consumption at Circuit Level

Digital circuits can be optimized by careful selection of transistors sizes to achieve performance specifications such as signal to noise ratio (SNR) and delay for the circuit. The switching activity can be reduced by well controlled timing. Limiting the output voltage swing of digital circuits helps reducing power consumption, [43]. Optimizing the clock and bus loading is also effective in lowering the switching power consumption. Place and route optimization of the digital blocks results in shorter interconnection wires and lower load capacitances.

Analog blocks such as operational amplifiers (OPAMPs) limit minimum supply voltage (V_{dd}) that could be used in image sensor. Therefore, designing these analog blocks to operate with low supply voltages is critical for power optimization, [44]. Moreover, shutting unused analog blocks down helps further reduce the power consumption.

3.3.3 Reducing Power Consumption at Architecture Level

Power consumption can be reduced by resource-sharing at the architecture level. Another method for power reduction at architecture level is partitioning the chip architecture into sub blocks and selectively enabling or powering these blocks.

Parallelism in the readout structures and ADCs in CMOS image sensors reduces the power consumption, [45]. Image sensor readout channel can be built using pixel parallel, column parallel, column series and pixel series architectures.

Rows of pixels are readout in parallel in both column parallel and column series architectures. The difference is in the column readout and analog to digital conversion. In column parallel architecture, digital conversion is run in parallel while digital conversion is performed sequentially in column series architecture. The column-parallel approach has the advantage of using slow data converters to achieve a high conversion rate. The column parallel architecture have also been shown to have lower overall power consumption, [29]–[31]. Even though the serial ADC in column series architecture runs at higher speed and consumes more power, serial readout architecture is preferred for reducing chip size, and FPN, [30].

3.3.4 Reducing Power Consumption at System Level

Designing the imager sensor IC for low supply voltage operation reduces the power consumption of the whole camera. Designing the system to tolerate variable supply and reference voltages reduce power consumption by eliminating the power hungry regulator circuits. Operating the system with low voltage and boosting the supply voltage for the blocks requiring high supply voltage reduces overall power consumption of the system, [46].

3.4 Low-Voltage Image Sensor Design

Traditional CMOS pixel structures have serious supply voltage limitations and they are not suitable for low-voltage operation. Gate to source voltage drop across the pixel reset and source follower transistors limit the dynamic range of the image sensor pixel and readout electronics following it. In this section supply voltage limitations of a 3T CMOS APS pixel (Figure 3-1) will be analyzed which can be generalized for other CMOS APS pixel structures.

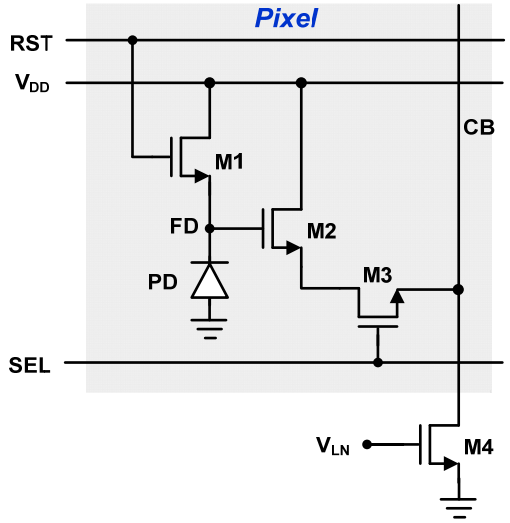


Figure 3-1. 3T pixel structure and current sink load

When the reset transistor in a 3T pixel turns on, it pulls the FD node to the reset level. Ideally this reset level should be power supply voltage. However, there is a threshold voltage drop from reset transistor gate to its source. The maximum voltage at FD node of a pixel driven by a standard reset signal is given in (3.13).

$$V_{FD,\max} = V_{rst} = V_{DD} - V_{TH,M1} \tag{3-13}$$

The pixel source follower buffers the photodiode node to the column bus (CB). The voltage at CB node is given in (3.14). The minimum voltage at the CB node for the source follower to stay in the proper operating region is given in (3.15).

$$V_{CB} = V_{FD} - V_{th,M2} - V_{OD,M2} - V_{DS,M3} \tag{3-14}$$

$$V_{CB,\min} = V_{OD,M4} \tag{3-15}$$

$V_{OD,M2}$ and $V_{OD,M4}$ are the overdrive voltages of pixel source follower and current mirror load transistors, respectively, while $V_{DS,M3}$ is the drain to source voltage across the select transistor M3. Overdrive voltages are set by the column bias current and they are constant for saturated transistors conducting constant drain current.

The absolute minimum voltage at the FD node that is detectable by the source follower is given in (3.16). Dynamic range of an imager is given in (3.17).

$$V_{FD,\min} = V_{th,M2} \tag{3-16}$$

$$DR = V_{DD} - V_{th,M1} - V_{th,M2} \tag{3-17}$$

The threshold voltage of a transistor with non-zero source to bulk voltage is increased because of body effect. Therefore, the threshold voltages of both reset and source follower transistors are increased significantly for higher values of V_{FD}. These voltage drops significantly limit the usable range of photodiode node voltage or dynamic range (DR).

Considering a process with threshold voltage of 0.5V, the dynamic range would be reduced by more than 1V. Therefore, minimum supply voltage for building an image sensor in such a process would be around 1.8V to achieve a reasonable pixel dynamic range of 0.5-0.6V.

Low threshold transistors could be used to decrease the minimum supply voltage. Modern submicron processes provide low threshold devices, but these devices have serious subthreshold leakage currents. Therefore, low-leakage high threshold voltage transistors are typically preferred for low power applications. [46]. Moreover, leakages in pixel transistors result in high dark currents. Several methods have been proposed to overcome the limitations on minimum supply voltage while maintaining wider dynamic range.

3.4.1 PMOS Reset

One method proposed for improving dynamic range is using PMOS reset transistor as shown on Figure 3-2, [47], [48]. PMOS transistor allows resetting the photodiode node to supply voltage. Therefore, the dynamic range for PMOS reset pixel is given in (3.18).

$$DR = V_{DD} - V_{GS,M2} \tag{3-18}$$

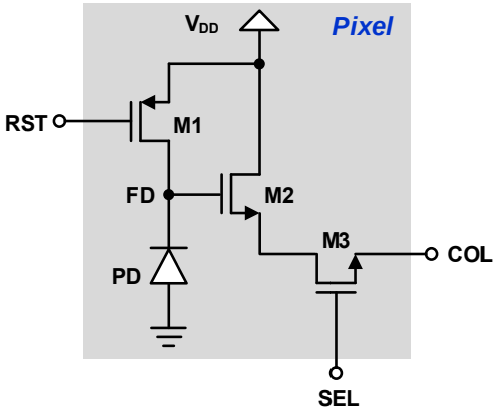


Figure 3-2. 3T CMOS pixel with PMOS reset transistor

Pixels with a PMOS reset transistor are very large and have low fill factor due to the size requirements of n-well and minimum distance requirements between n-well and n+ diffusion regions.

3.4.2 Bootstrapped Reset

Bootstrapped reset switch is another method for improving the dynamic range by removing the gate to source voltage drop of reset switch as shown on Figure 3-3. Bootstrapping method allows applying a gate voltage higher than supply voltage at the gate. However, in case supply voltage is close to process maximum voltage, bootstrapping results in hot-carrier degradation issues in CMOS transistors, [49][50]. The dynamic range for bootstrapped reset pixel is given in (3.19).

$$DR = V_{DD} - V_{GS,M2} \tag{3-19}$$

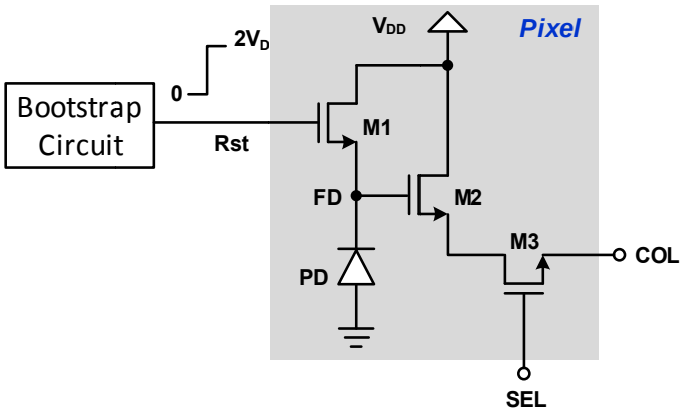


Figure 3-3. 3T CMOS pixel with bootstrapped reset clock.

3.4.3 **Complimentary Pixel**

Complimentary pixel structure is an improved implementation of PMOS reset idea. The dynamic range limitation imposed by both reset transistor and source follower gate to source voltage drops are eliminated. Complementary pixel solves the source-follower input range limitation by utilizing a pair of complementary source followers in the pixel to achieve rail-to-rail input and output swing as shown in Figure 3-4. A PMOS source follower is added in parallel with the NMOS source follower, so that at least one source follower is active over all input voltage ranges. The size of source followers must be arranged carefully to get identical gain for maximum linearity, [51][52]. For the complementary structure to work as expected V_{DD} has to satisfy (3.20).

$$V_{DD} \geq V_{THN} + |V_{THP}| \tag{3-20}$$

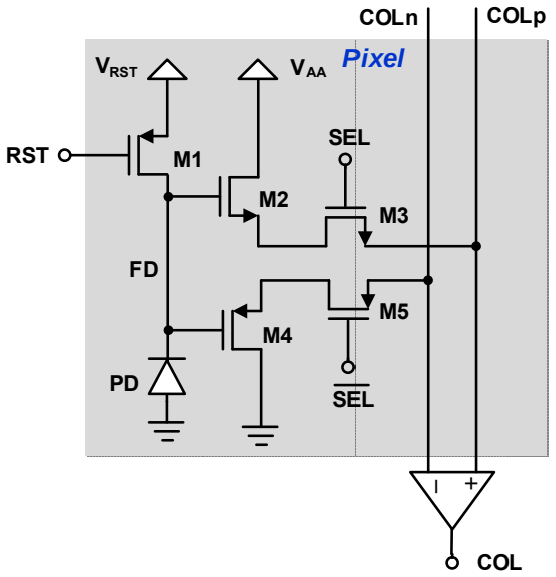


Figure 3-4. Complimentary pixel structure

As a result of the increase in the available input and output voltage swing, the saturation level of the pixel, dynamic range and signal to noise ratio are effectively improved. However, the pixel becomes very large compared to a regular 3T pixel because of the three added PMOS transistors and thus the pixel fill factor is reduced considerably.

3.4.4 Digital Output Pixels

The primary problem with voltage mode image sensors with 3T pixels is the limited capacitance and voltage swing of the photo sensitive element that limits the dynamic range of the sensor. Pixels with digital outputs have been proposed to overcome these issues and operate with very low supply voltages, [53].

Idea of converting light intensity into frequency has been around for a long time [54]. Asynchronous self-resetting pulse width modulation pixels (Figure 3-5) convert light level into frequency instead of voltage as in regular 3T APS pixel. Pixel is composed of a photodiode, a voltage comparator, a reset transistor, a digital counter/register, a feedback network, and other readout and control circuits. Photo generated current discharges the photodiode during the integration period. As the photodiode discharges below the reference voltage, the comparator switches and photodiode is reset through a PMOS transistor achieving hard reset operation.

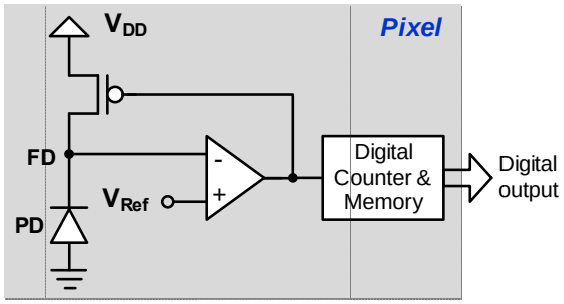


Figure 3-5. Pulse width modulation pixel

As the light intensity increases, the photodiode discharges faster and the comparator switches faster increasing the frequency of the output signal. The comparator performance has a major effect on pixel performance. The most important parameter of the comparator is lowest minimum detectable input voltage to improve low-light sensitivity and increase frame rate. Another desired attribute is small delay to reduce reset-induced nonlinearity and extend the saturation frequency at the high-illumination levels. The comparator must have wide operating frequency range to ensure good performance at high frame rates. It is also important to simplify the comparator circuit in order to reduce the pixel area, while maintaining the fill factor and to have the comparator operate at low-supply voltages, [55]–[57]. Alternative digital image sensor structures based on pulse width modulation (PWM) have also been proposed [21]. PWM based pixels operate with supply voltages as low as 0.45V [59].

Time based imagers (Figure 3-6) have been proposed as an alternative to PWM imagers [23][24]. The time based image sensors measure the time it takes for the photodiode node to fall below a reference voltage.

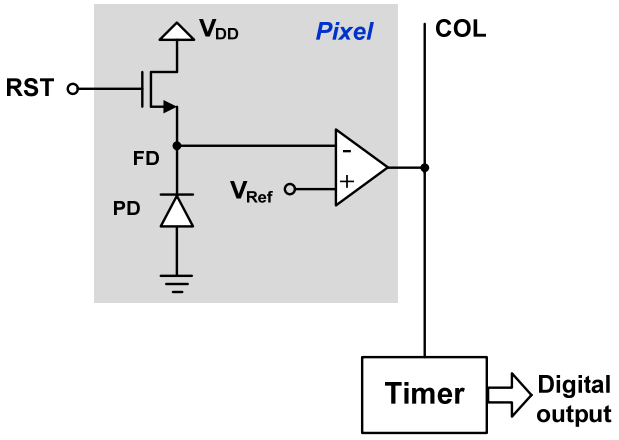


Figure 3-6. Time based pixel

Pixel to pixel offset and gain variations are serious issues for digital output pixels. Offset and gain variations contribute to FPN. Correlated double sampling is not possible with digital pixels. Pixel structures using current mode reset instead of voltage mode reset remove the effects of source follower transistor threshold variations [62]. Even though the pixel to pixel variations are not completely removed with current mode reset, they are reduced significantly. Current mode resetting method can be applied to in pixel comparator to improve the FPN of the imager [61].

3.4.5 Supply Boosting

Since low threshold devices increase the leakage power considerably, high threshold devices are preferred for low power design. However, high threshold voltages in low leakage processes limit minimum usable supply voltage. Digital circuits can be operated with satisfactory performance at low supply voltages despite high threshold voltages. But, low supply voltages will have adverse effects on the performance of analog blocks, especially on the circuits between pixel and digital output pads.

Low voltage pixel designs and readout techniques discussed so far increase complexity and size of the pixel and readout electronics impeding scaling capability of the APS pixel. Supply boosting technique applied to pixel source followers (PSF) of CMOS APS imagers achieve low-power and wide operating range for PSF when the supply voltage is reduced below the minimum pixel supply voltage.

Dynamic range of PSF and analog readout is improved by boosting reset signal, select signal, and pixel power supply. Boosting technique allows using a single low voltage supply and generating a boosted supply voltage and boosted clocks for blocks requiring higher voltage such as pixel source follower and ADC comparator(s).

Supply booster circuit is composed of 3 inverters, a PMOS switch and a capacitor as shown in

Figure 3-7. The booster circuit doubles the supply voltage when the input clock goes high. Booster circuit is a highly efficient single-shot voltage converter.

Boosting the reset signal increases the maximum voltage input to the source follower. Boosted reset signal sets the maximum voltage at the source follower input to V_{DD}. When the pixel supply voltage and reset clock are boosted together, the maximum source follower input is given by equation (3.21) and dynamic range is given by equation (3.22).

$$V_{PD,\max} = V_{rst} = 2 \cdot V_{DD} - V_{th,M1} \tag{3-21}$$

$$DR = 2 \cdot V_{DD} - V_{th,M1} - V_{th,M2} \tag{3-22}$$

Boosting the Select signal decreases the voltage drop across the select transistor and further increases the dynamic range at the pixel output. [46]

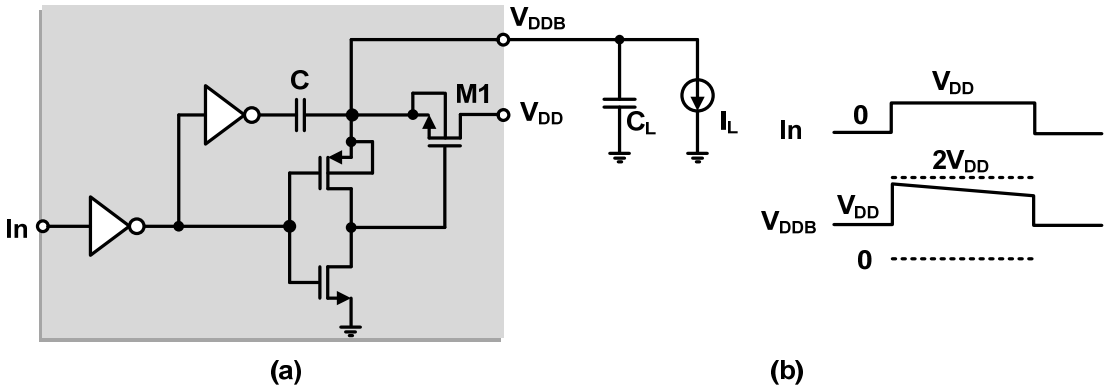


Figure 3-7. (a) Voltage booster circuit schematic, (b) associated waveforms.

Boosted supply voltage (V_{DDB}) is actually less than $2V_{DD}$ due to the capacitive voltage division between the boosting capacitance and the capacitive load. The actual initial value of boosted supply voltage ($V_{DDB,i}$) is given by (3.23).

$$V_{DDB,i} = V_{DD} + V_{DD}\frac{C}{C + C_L} \tag{3-23}$$

This voltage will decrease as the circuit draws current from the boosting capacitor. V_{DDB} value Δt seconds after the boosting clock edge is given by (3.24).

$$V_{DDB} = V_{DD} + V_{DD}\frac{C}{C + C_L} - \Delta V = V_{DD} + V_{DD}\frac{C}{C + C_L} - \frac{I_L \cdot \Delta t}{C + C_L} \tag{3-24}$$

The boosting capacitance should be large enough to minimize the effects of capacitive loading on the boosting voltage and ΔV.

3.5 Summary

Power dissipation is the prime design constraint for portable systems. The low-power system design requires optimization at all levels – technology, circuit and logic, architecture, algorithm, and system level. Low supply voltage design methods are emphasized for low-power CMOS image sensors design. Low voltage image sensor design techniques reported in literature have been presented. A summary of current state-of-the-art low power imagers is presented in Table 3-3.

Table 3-3. Comparison of state-of-the-art low power imagers

PARAMETER	[57] **Kagawa**	[59] **Hanson**		[85]**Cho**	[61] **Chung**		[8] **Law**	[10] **Ay**
Technology	0.35µm (2P3M)	0.13µm Bulk		0.13µm (1P4M)	0.18µm (1P6M)		0.35µm (2P3M)	0.5µm (2P3M)
Pixel Pitch	10µm	5µm		3.4µm	10µm		15µm	21µm
Array Size	128x96	128x128		128x128	64x40		32x32	54x50
Fill Factor	18.50%	32%		38.00%	25.40%		21.00%	32%
ADC Resolution	9 bit - Ramp	10 bit - Ramp		10 bit - Ramp	10 bit - Ramp		8 bit - Ramp	10 bit - SAR
Supply Voltage	1.35 V	0.5 V		0.75 V	0.5 V		1.5 V	1.2 V
Temporal Noise (Dark)(rms)	0.95 LSB	55.30 LSB		1.92 LSB	0.65 LSB		NA	0.98 LSB
Pixel FPN (Dark) (rms)	0.61 LSB/ 0.12%	NA		6.76 LSB/ 0.66%	0.56 LSB/ 0.055%		NA	NA
Column FPN (Dark) (rms)	0.15 LSB/ 0.03%	NA		0.61 LSB/ 0.06%	0.16 LSB/ 0.016%		NA	NA
Total FPN (Dark) (rms)	NA	67.58 LSB / 6.6%		NA	NA		47.16LSB/ 18.42%	1.23 LSB/ 0.12%
Energy Harvesting (µW)	Not capable	Not capable		Not capable	Not capable		0.0356 @29klux	3.35 @60klux 2.10 @20klux
Energy Harvesting (µW/mm^2)	Not capable	Not capable		Not capable	Not capable		0.155 @29klux	2.81 @60klux 1.76 @20klux
Frame Rate (fps)	9.6	0.5	8.5	15	11.8	78.5	21	7.4
Power Consumption (Pixel Array) (µW)	0.42	NA	NA	1.6	0.45	0.6	NA	0.0264
Power Consumption (Imager Core) (µW)	NA	0.7	1.24	NA	NA	NA	NA	NA
Power Consumption (Whole Chip) (µW)	55.2	NA	NA	65.2	4.95	29.6	15.8	14.25
iFOM (Pixel Array) (pJ/frame*pixel)	3.56	NA	NA	6.51	14.8	2.98	NA	1.32
iFOM (Pixel Array) (pJ/frame*pixel)	NA	85.4	8.6	NA	NA	NA	NA	NA
eFOM (Whole Chip) (pJ/frame*pixel)	467.9	NA	NA	265.3	163.9	147.3	734.7	713.2

CHAPTER 4 - ENERGY HARVESTING IMAGE SENSORS

Many modern wireless sensor applications require sensors to operate in isolated, dangerous, or remote areas for extended period of time. Typically, it is very difficult to access these sensor systems to replace power sources. Thus, it is required that the devices have to operate with extreme energy efficiency while providing the demanded performance putting battery lifetime as the top design priority. On the other hand, even the operation lifetime of very low-power, low-leakage, and energy-efficient systems are limited by the finite energy stored and/or left on a power source or battery. Therefore, it is desirable for the sensor systems to harvest ambient energy in the environment to assist the power source and/or eliminate the need for one.

Among all different kinds of energy harvesters, photovoltaic (PV) energy converter is one viable choice due to its high conversion efficiency and compatibility with standard CMOS processes [2]–[4]. Fortunately, the level of illumination required for operating an image sensor to capture images is sufficient enough for powering the imaging system if the light energy is harvested efficiently. Furthermore, the same PN-junction structures used for image capturing in modern semiconductor image sensor pixels could be configured for harvesting ambient energy eliminating the need for dedicated solar energy harvester structures. Integrating energy harvesting capability into image sensor enables reducing the system cost and, volume [8]–[11]. Thus, the design of the energy autonomous electronic systems is possible combining highly efficient on-chip energy harvesting structures and ultra-low power circuits.

This chapter presents the energy harvesting image sensor topologies in the literature and a comparison of different micro solar cell structures designed, fabricated and tested in this study.

4.1 PN-Junctions under Illumination

The core of an image sensors and solar cells is a PN-junction photodiode. Integration type image sensors utilize PN-junction in reverse bias configuration. Solar cells on the other hand are basically forward bias PN-junctions.

The unilluminated PN-junction is in equilibrium (Figure 4-1). The N-region has a higher concentration of electrons and P-region has higher concentration of holes. A region

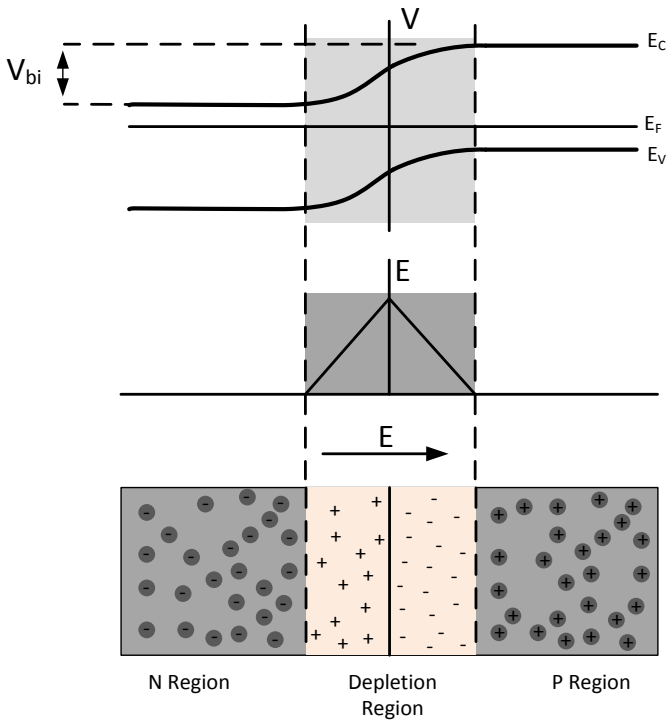


Figure 4-1. Energy band diagram and built in electric field in a PN-junction under equilibrium.

depleted of carriers is formed on both sides of the metallurgical junction. A built in electric field directed from N-region to P-region is formed in the depletion region due to ionized donor and acceptor atoms. Drift current due to the built in potential and diffusion current due to the carrier concentration gradient are balanced and equilibrium is established while the Fermi level is constant through the semiconductor, [63].

When the PN-junction is illuminated with visible light, excess electron-hole pairs are generated in the semiconductor (Figure 4-2). The concentration of these photo generated carriers is larger than the equilibrium concentration of minority carriers. Therefore, the concentration of minority carriers increases significantly. This increase in the concentration of minority carriers leads to the flow of the minority carriers across the depletion region into the qausi-neutral regions. Holes will move from N-region to P-region and electrons will move from the P-region to N-region. Thus, a photo generated current (I_{ph}) will start to flow from N-region to P-region as a result of excess carrier flow. The photo generated current is given by (4-1).

$$I_{ph} = AJ_{ph} = A\left(qG\left(L_N + W_D + L_P\right)\right) \tag{4-1}$$

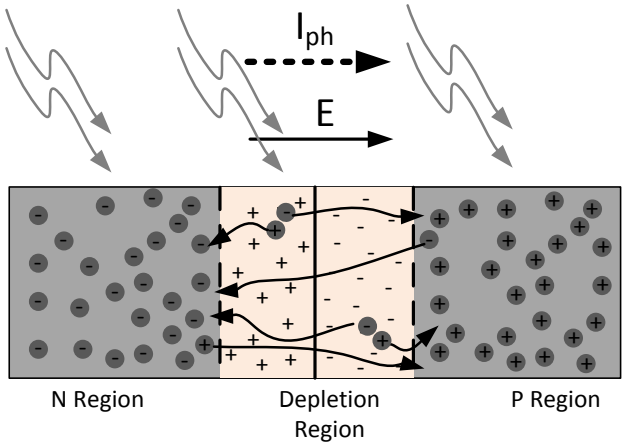


Figure 4-2. Flow of photo generated carriers across the depletion region.

G is the photo carrier generation rate, q is the electron charge, L_N and L_P are the diffusion lengths of minority carriers, W_D is the width of depletion region and A is the junction area. The equation reflects the fact that junctions with wider depletion regions and longer diffusion lengths have larger photo generated current density. Equation (4-1) also shows that junctions with larger area have larger photo currents, [64].

The excess carriers building up in the semiconductor will disturb the equilibrium and the Fermi level will not be constant throughout the semiconductor. The difference between quasi Fermi levels in N-region and P-region will lower the built-in potential barrier across the depletion region (Figure 4-3). The lowered potential barrier will allow flow of increased diffusion current known as recombination current from P-region to N-region, [64].

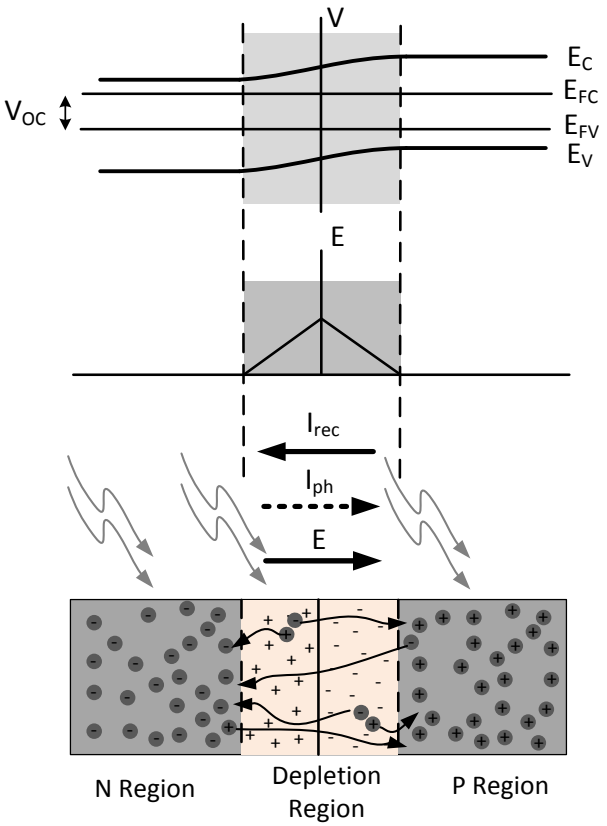


Figure 4-3. Energy band diagram and built in electric field in a PN-junction under illumination.

When a reverse bias voltage is applied across the junction, the built-in barrier increases further. Recombination current is reduced to zero as potential barrier increases. The thermally generated current and photo generated current flows from N-region to P-region.

When a forward bias is applied to the PN-junction, the potential barrier is lowered allowing flow of forward current (recombination current). When the forward bias is larger than the open circuit voltage, the forward current suppresses the photo generated current. The modified Schockley equation for illuminated PN-junction is given in (4-2).

$$I(V_a) = I_s\left(\exp\left(\frac{qV_a}{kT}\right) - 1\right) - I_{ph} \tag{4-2}$$

$I(V_a)$ is the current flowing into the p terminal of the PN-junction and V_a is the potential difference between P-terminal and N-terminal. Net current flowing through the junction drops to zero for a positive value of V_a commonly referred to as the open-circuit voltage (V_{oc}).The corresponding current voltage (I-V) curves of PN-junction illuminated with different light levels are shown in Figure 4-4.

In the open-circuit condition, no net current can flow inside the PN-junction. The photo current and the thermal generation current are balanced by the recombination current flowing from P-region to N-region. The electrostatic-potential barrier across the junction is lowered by an amount of V_{oc}. V_{oc}.is the potential difference between the two terminals of the PN-junction and can be measured by a voltmeter.

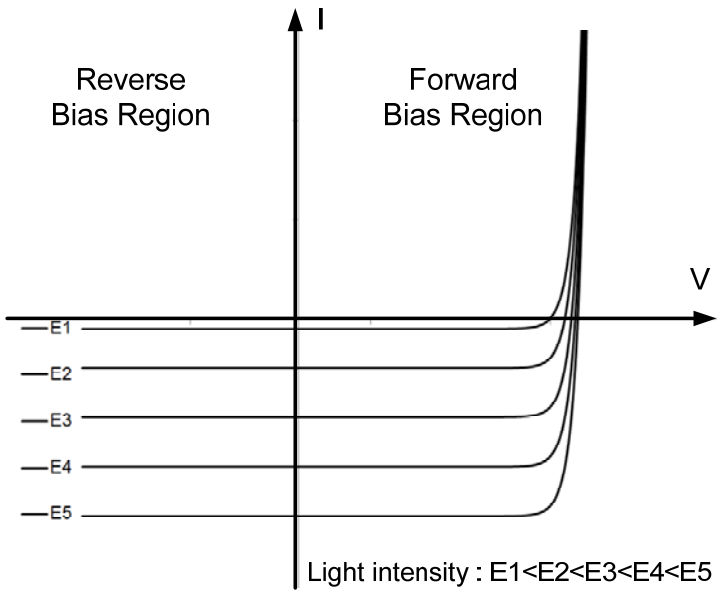


Figure 4-4. I-V curve of PN-junctions under different illumination levels.

When an external load circuit is connected to PN-junction, part of the carriers that cross the depletion region will flow through the external circuit. Therefore, excess carier build up and Fermi level disturbance is less. As a result built in potential barrier is lowered less than the open circuit voltage and less recombination current flows through the junction.

Under the short-circuit condition, the N-region and P-region are at the same potential. Therefore, the built in potential is unchanged. The recombination current is insignificant and photo generated current flows through the external wire. This current referred as short circuit current (I_{sc}) is the maximum current output from the illuminated PN-junction.

4.2 Solar Energy Harvesting

Energy generated by solar cells can be characterized measuring the voltage and current output from the solar cell under different loading conditions. Power measurement setup for solar cell is shown in Figure 4-5.

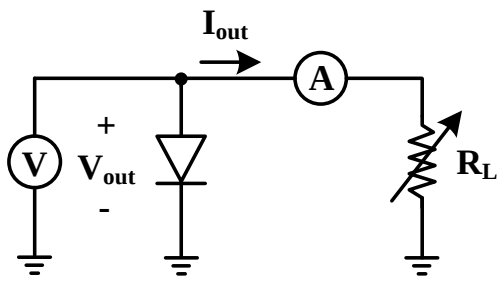


Figure 4-5. Power measurement setup of a solar cell.

Relation between output current (I_{out}) and voltage (V_{out}) is obtained from (4.2). Direction of output current is opposite to the diode current. The solar cell I-V equation is given by (4.3).

$$I_{out}(V_{out}) = I_{ph} - I_s\left(\exp\left(\frac{qV_{out}}{kT}\right) - 1\right) \tag{4-3}$$

It is evident from (4.3) that the output voltage of a solar cell decreases as the load current increases. The power output for a specific output voltage V_{out} is given by (4.4).

$$P(V_{out}) = \left(I_{ph} - I_s \cdot \left(\exp\left(\frac{qV_{out}}{kT}\right) - 1\right)\right) \cdot V_{out} \tag{4-4}$$

Power output from the solar cell is zero both at open circuit (I_{out}=0) and short circuit (V_{out}=0) conditions. Therefore, it is necessary to operate the photodiodes at a point that they will deliver the maximum power. V_{out} corresponding to maximum power output (V_{MPP}) can be calculated by setting the derivative of (4-4) to zero. The relation between V_{MPP} and other solar cell parameters is given in (4.5).

$$\frac{I_{ph}+I_s}{I_s}=\left(1+\frac{qV_{MPP}}{kT}\right)\cdot\left(\exp\left(\frac{qV_{MPP}}{kT}\right)\right) \tag{4-5}$$

Boltzmann's constant k and electronic charge q are universal constants and thermal current I_s is constant for a given PN-junction. Photo generated current I_{ph} depends on illumination linearly. Therefore, V_{MPP} is a logarithmic function of light level as shown in (4-5). The open circuit voltage for a specific illumination can be calculated using (4-3).

$$V_{oc}=\frac{kT}{q}\ln\left(\frac{I_{ph}+I_s}{I_s}\right) \tag{4-6}$$

It is not possible to get simple closed form algebraic solution for the maximum power point voltage (V_{MPP}) and current (I_{MPP}) values in terms of other parameters. However, the relations can be calculated numerically using (4-5) and (4-6). There is an approximately linear dependence between the V_{MPP} and V_{oc} as expressed in (4-7) [65].

$$V_{MPP}=k_v\times V_{OC} \tag{4-7}$$

k_v is called the voltage fraction. Even though k_v increases slightly as illumination increases, it is fairly constant over wide ranges of illuminations. This equation is the basis of fractional voltage maximum power point tracking (FVMPPT) algorithm. Alternatively, a current based approach can be taken. The ratio of I_{MPP} and short circuit current (I_{SC}) of the solar cell structure called current fraction (k_c) can be used for MPPT instead of k_v. This method is called fractional current maximum power point tracking (FCMPPT) algorithm. However, voltage based method is easier to implement and is preferred over the current based method.

The FVMPPT operation is very simple. The voltage fraction constant is determined by measurements under various illumination levels. The MPPT circuit measures the open-circuit

voltage V_{oc} either by interrupting the normal operation of the system and storing the measured value or by using an identical solar cell (pilot cell) to measure the V_{oc} real time. Open circuit voltage is multiplied by the fraction constant by a very simple voltage divider circuit to generate a reference voltage. Load of the solar cell is adjusted to set the output voltage equal to this reference voltage.

As every auxiliary system, the circuits implementing MPPT consumes power from the energy source while maximizing the power delivered to the load. The power consumed by MPPT circuits increase with increased tracking algorithm complexity. Naturally, it is desirable that the MPPT circuits consume minimal power, so that it doesn't affect the overall power efficiency of the energy harvesting system. The fractional voltage based MPPT algorithm and associated circuits are the simplest and most energy efficient.

4.3 Solar Energy Harvesting Image Sensors: An Overview

Several different energy harvesting CMOS image sensor topologies capable of harvesting energy from the ambient light sources have been proposed,[6]–[11]. Self-powered sensor (SPS) concept proposed in [6] and [7] has a dedicated power generating photodiode (PGPd) and a dedicated imaging photodiode. The cathode of a power generating photodiode (PGPd) is connected to the pixel power supply and the anode is connected to the floating power harvesting bus. Figure 4-6(a) shows the general structure of pixels based on SPS concept. There are several short comings of this pixel topology. The SPS concept is not intended for self-powered operation despite its name. The PGPd acts as a battery in series with the circuit power supply generating a voltage higher than the circuit main supply. Since the PGPd is current limited, the maximum current PGPd can provide to the pixel is the short circuit current of the PGPd. If the pixel tries to draw more current, the effective pixel supply

voltage V_{DD}^* drops below V_{DD} and current is limited with the reverse saturation current of PGPd. Therefore, when the pixel does not receive enough light to provide the necessary current, the regular imager operation is compromised.

The pixel structure proposed in [8] and [9] is based on reconfigurable photodiode concept. Same photodiode is used for harvesting and imaging. Energy harvesting and imaging modes run sequentially. Figure 4-6(b) shows the general structure of these sequential pixels. The power output is meaningful. However, two in pixel switches connected to the anode side of the forward biased photodiodes cause considerable leakage reducing power generation efficiency.

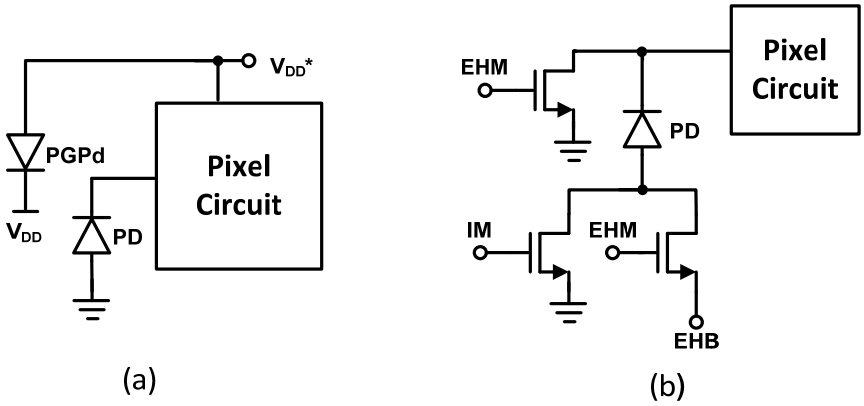


Figure 4-6. Pixels based on (a) SPS concept [6], [7], (b) sequential energy harvesting pixel [8], [9].

4.4 The Energy Harvesting and Imaging (EHI) Sensor

The CMOS energy harvesting and imaging (EHI) active pixel sensor (APS) proposed in [10] and [11] is shown in Figure 4-7. The pixel does not need a battery supply during energy harvesting. The anodes of energy harvesting photodiodes are connected to a global bus and the global bus is switched instead of switching anodes of individual photodiodes. Unlike

in pixel switches, these global switches do not receive light and their leakage is insignificant. Therefore, possible leakage paths on energy harvesting bus are minimized. Energy harvesting photodiode in each pixel acts as micro solar cell producing useful power from light incident on the pixel array.

The pixel is composed of a reconfigurable photodiode (PD2) and four NMOS transistors (M1-M4). However, the presence of the permanently grounded substrate introduces a second photodiode PD1. Reset (M1), pixel source follower (M2) and row select (M3) transistors are the typical transistors in a 3T CMOS APS pixel. M4 shorts the parasitic photodiode PD1 to ground in energy harvesting mode (EHM), and it is turned off in imaging mode (IM). Both photodiodes are reverse biased during imaging mode (IM) and PD2 is forward biased during energy harvesting mode (EHM). [66]

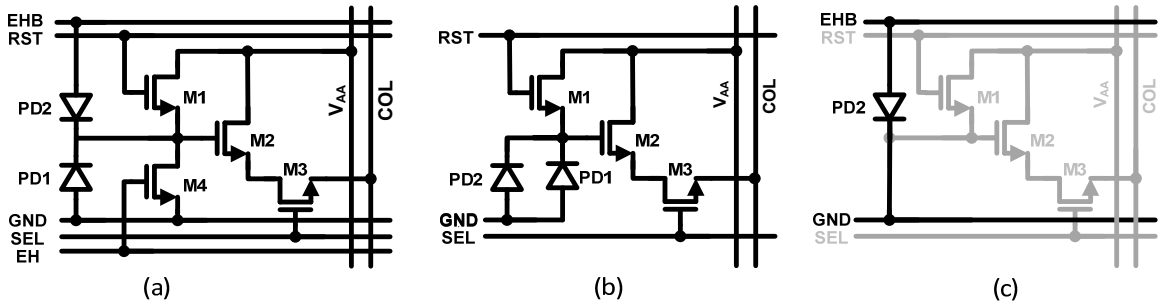


Figure 4-7. (a) Energy Harvesting and Imaging (EHI) pixel, (b) imaging mode, (c) energy harvesting mode [10], [11], [66].

Core of the energy harvesting image sensor structure is the reconfigurable floating PN-junction PD2. In standard CMOS process, several different types of PN-junction diodes can be built using combinations of P-substrate, N+ diffusion, P-diffusion, and N-well layers. The PN-junction formed using P-substrate and N+ diffusion or N-well junctions are permanently reverse-biased since P-substrate is always connected to most negative potential.

These junctions are suitable for CMOS image sensors, but not for an energy harvesting photodiode or micro solar cell. Therefore, energy harvesting PN-junctions are formed using P-diffusion and N-well layers.

In energy harvesting mode the photodiode connected between floating diffusion node and a global energy harvesting bus (EHB) is forward biased and works as a micro solar cell harvesting light energy. M4 is off and global Energy Harvesting Bus is grounded in imaging mode. The photodiode is reverse biased with its anode grounded and its cathode connected to FD node. The cross sectional view of the energy harvesting and imaging (EHI) pixel is shown in Figure 4-8.

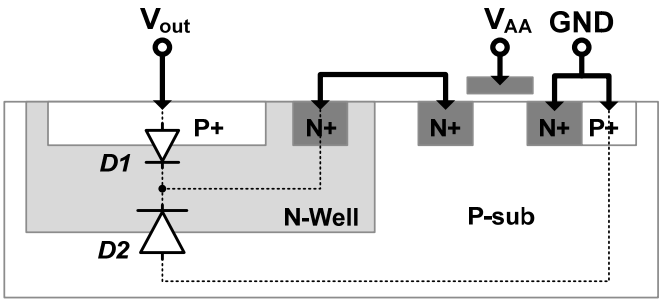


Figure 4-8. First generation EHI sensor pixel cross section, [10], [66].

The first generation EHI sensor achieved very low power operation consuming only 13.5µW. EHI sensor is built in 2P3M 0.5µm CMOS manufacturing process. The pixel array size is 54x50. The power consumption of the energy harvesting imager is minimized by lowering supply voltage without sacrificing the performance of pixel. Imager was built in a high voltage process. Threshold voltages of NMOS and PMOS transistors used in this image sensor operating at 1.2 V are 0.8 V and -0.9 V, respectively. The ASP is designed for low-voltage and low-power operation. Supply boosting technique [46], [67] was used in both pixel

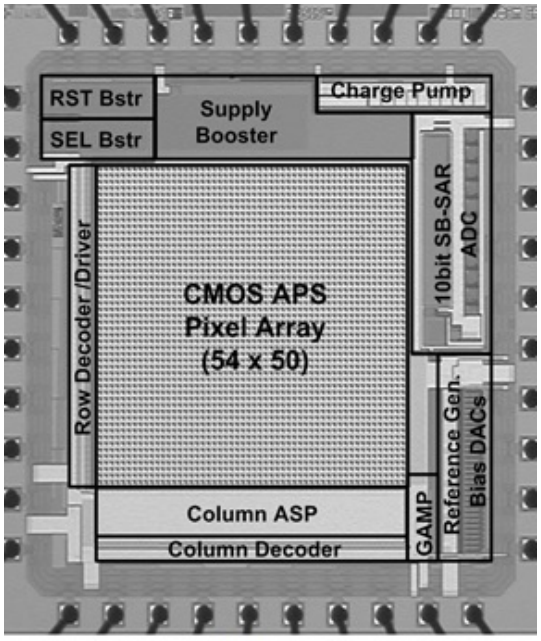
source follower (PSF) and analog to digital converter (ADC). The pixel reset and select signals were also boosted to improve linearity and voltage range of the pixel source follower.

Column series single channel global voltage readout is employed to reduce the power consumption. The pixel output from each row is first sampled on a column sample and hold (S&H) circuit. The absolute pixel signal after correlated-double-sampling (CDS) is amplified by a global charge amplifier and converted into digital code by a 10-bit successive approximation register (SAR) ADC.

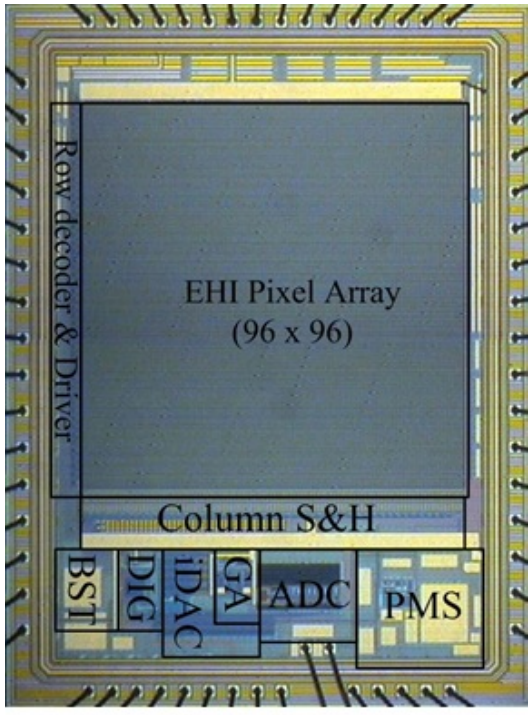
4.5 Energy Harvesting Capacity of On-chip Photodiodes

The energy harvesting capacity of the imager was limited by the insufficient energy generation capacity of the P-diffusion /N-well diode. Second generation EHI sensor was built in 2012. Sensor was fabricated in triple well 0.18μm 1P6M CMOS process. The energy harvesting capacity was increased by using P-well layer in triple well process, [11]. Chip micrographs of the first and second generation EHI imagers are shown in Figure 4-9.

The main difference between the first and second generations is the layers used for building the photodiodes. This structure has 3 different diodes contrary to the 2 diodes in the 1st generation EHI sensor. N-well/P-sub junctions form the PD1, while the N+ diff/P-well and N-well/P-well junctions form the PD2. P-well type energy harvesting and imaging (EHI) pixel is shown in Figure 4-10. This EHI pixel just like N-well type EHI pixel is based on three-transistor (3T) standard APS structure.

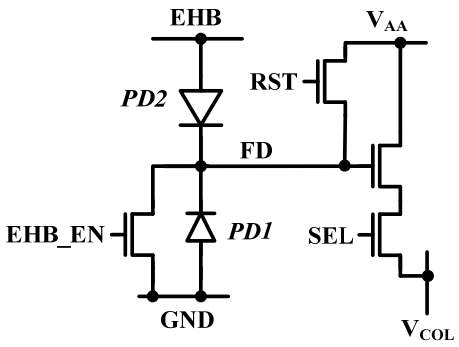


(a)

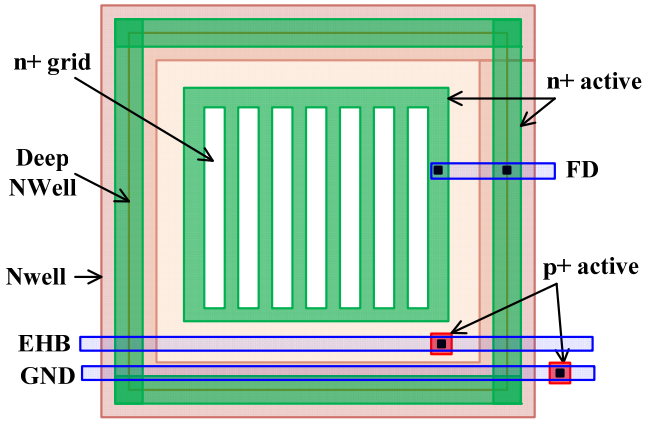


(b)

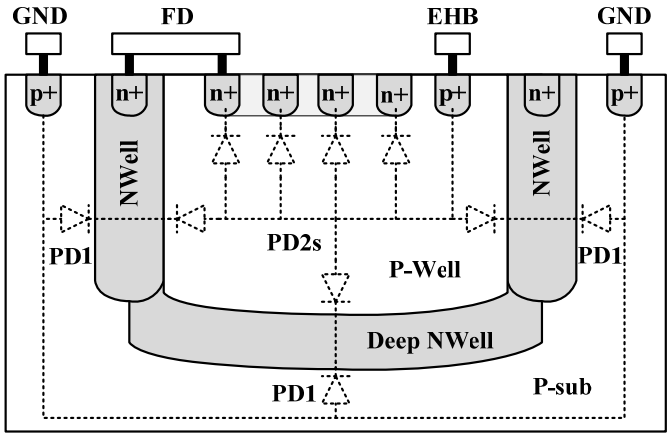
Figure 4-9. Chip micrographs of; (a) 1st generation EHI sensor [10], [66], (b) 2nd generation EHI sensor [11].



(a)



(b)



(c)

Figure 4-10. Second generation EHI sensor pixel (a) schematic, (b) layout, (c) cross section,[11].

The N-well ring decreases the size of P-well considerably. Therefore, the P-well /N+ diffusion diode is smaller than the P-diffusion /N-well diode in the N-well type pixel. However, the added P-well/N-well junctions increase total junction area for the energy harvesting photo diode PD2 resulting in a larger harvesting diode. Moreover, the deep P-well/N-well junction captures photons in red visible spectrum which could not be captured by the shallow junction improving the energy conversion efficiency even more.

Energy-harvesting efficiency and current-voltage-power (IVP) characteristics of the two EHI pixels in energy harvesting mode were measured under different illumination conditions corresponding to different day light conditions (5,000lux to 50,000lux). Figure 4-11 shows the I-V-P curves for the two pixel arrays, [12]. Since the two pixel arrays have different sizes, both measurements were normalized for a $1mm^2$ pixel array.

Table 4-1 summarizes the maximum power delivered by each array for the given illumination condition. Measurements confirm that the P-well type structure making use of the large junction area of the P-well delivers more power in a given wafer area proving that using deeper PN-junctions improve energy harvesting capacity. [12]

Table 4-1. Output power versus light illumination, [16].

Illuminance (Lux)	***Maximum Power Delivered to Load (μW)***	
	N-Well Pixel	**P-Well Pixel**
5,000	0.16	0.36
10,000	0.34	0.79
20,000	0.70	1.46
40,000	1.17	3.05
50,000	1.66	3.96

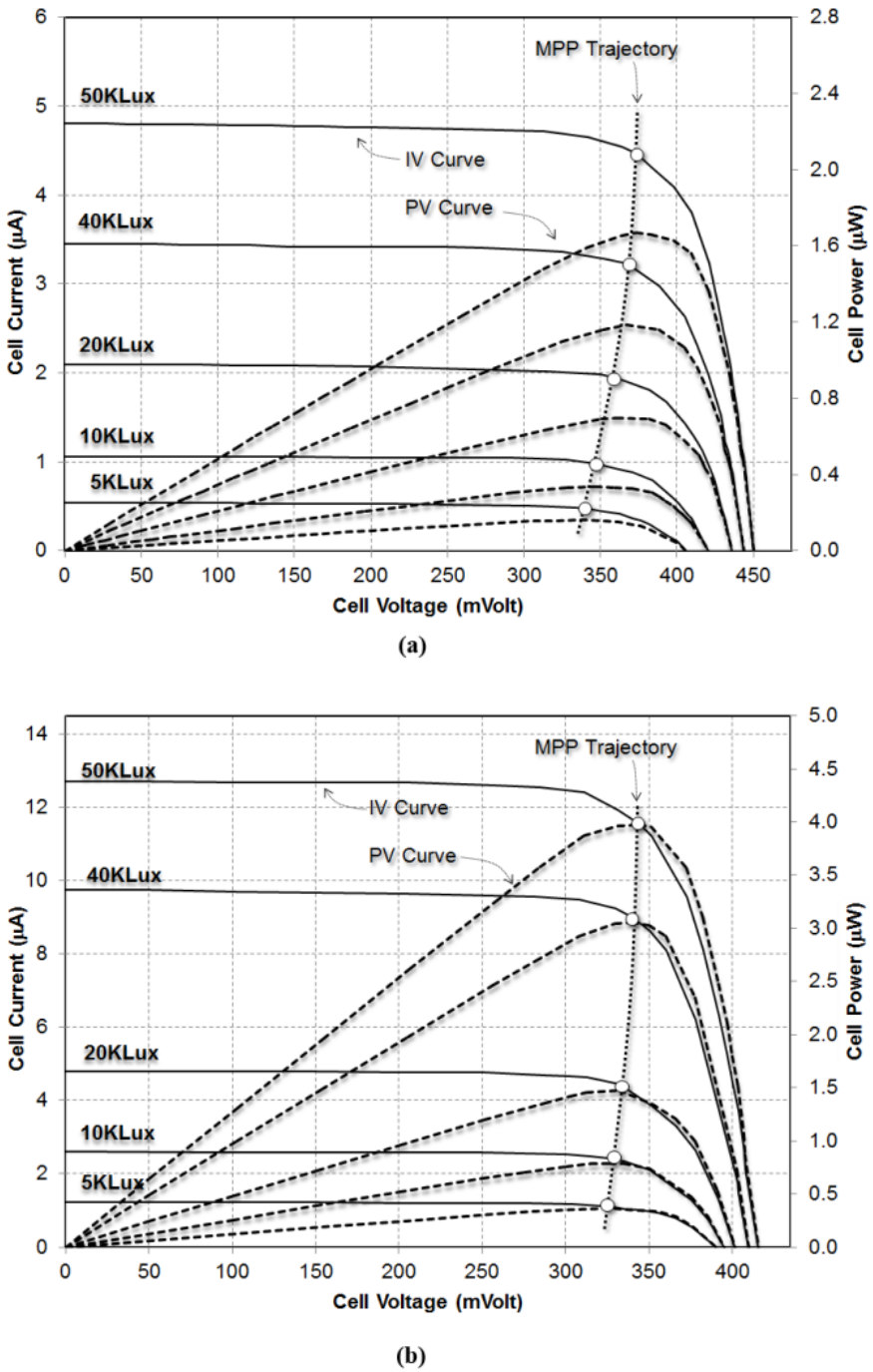


Figure 4-11. Measured current-voltage-power (IVP) curves of the EHI pixel structures; (a) 1st generation EHI pixel, (b) 2nd generation EHI pixel, [12]

4.6 On Chip Power Management System

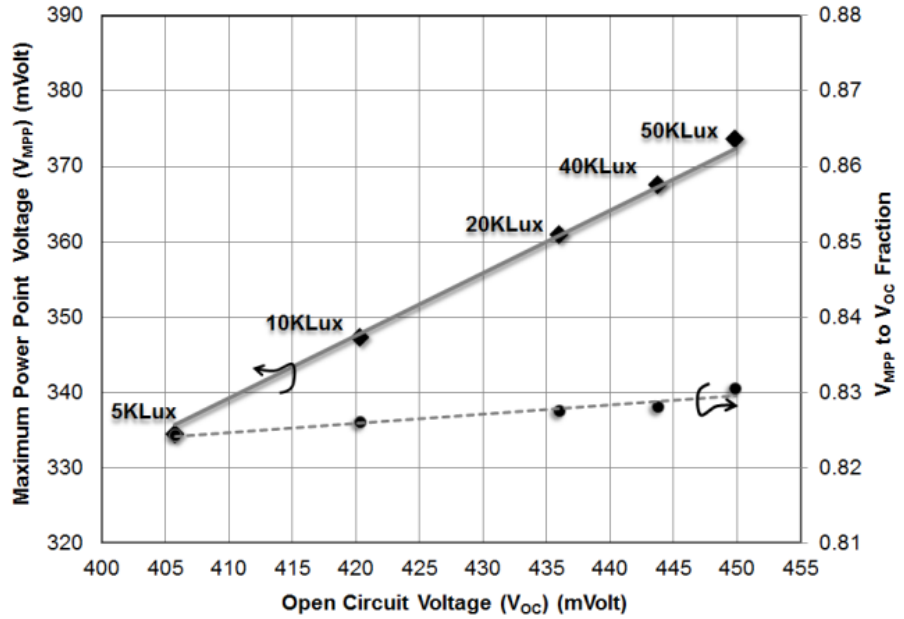
The measured relation between V_{MPP} and V_{oc} and the voltage fraction k_v for different illumination levels is shown in Figure 4-12. Even though k_v increases with illumination, the value is relatively constant over a very wide illumination range. Therefore, simple fractional MPPT method can be used for managing the power output from the EHI sensors. MPPT system can be built using only a simple resistive voltage divider and comparator [68].

The power management system (PMS) in [68] is integrated into the 2nd generation EHI sensor. The PMS harvests solar energy with the maximum power efficiency, stores the harvested energy, boosts the output voltage level to the regulated level and eventually switches the chip supply from battery to the harvested power whenever it is available. The PMS is composed of four major components: MPPT circuit, inductive boost converter, regulator, and power management decision block as shown in Figure 4-13.

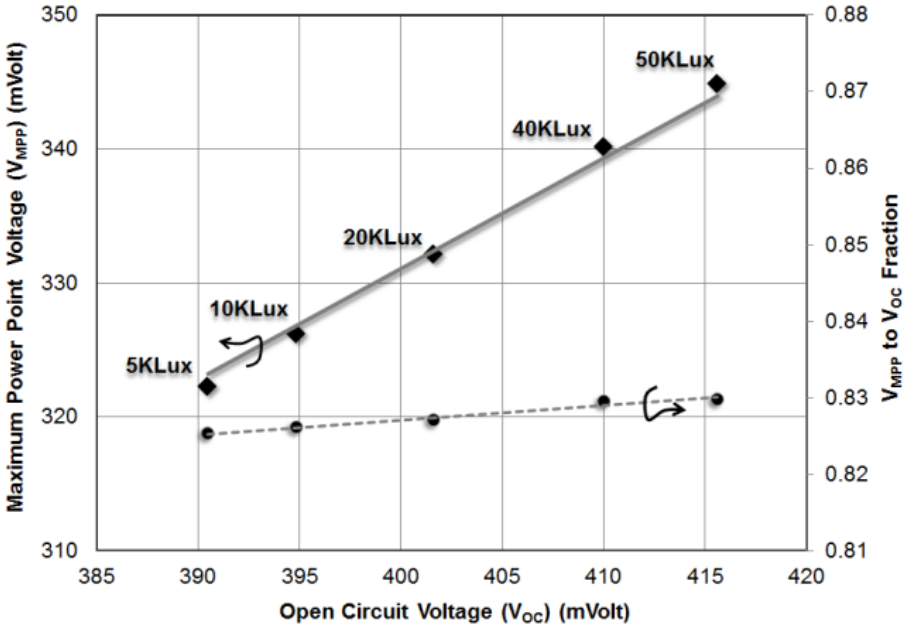
MPPT circuit is composed of a comparator and a 4-bit programmable resistive voltage divider. A pilot solar cell structure surrounding the EHI pixel array generates the open circuit voltage. Open circuit voltage of the pilot solar cell (V_{PILOT}) is equal to V_{oc} of the pixel array. V_{MPP} is generated by applying the V_{PILOT} to a large on-chip resistive voltage divider. Thus, V_{MPP} is given by (4.8).

$$V_{MPP} = \frac{R_2}{R_1 + R_2} \times V_{PILOT} = \frac{R_2}{R_1 + R_2} \times (\alpha \times V_{OC}) \tag{4-8}$$

$$k_v = \frac{R_2}{R_1 + R_2} \times \frac{V_{PILOT}}{V_{OC}} \tag{4-9}$$



(a)



(b)

Figure 4-12. Relation between V_{MPP} and k_v and V_{oc} for different illumination levels for (a) 1st generation EHI pixel, (b) 2nd generation EHI pixel.

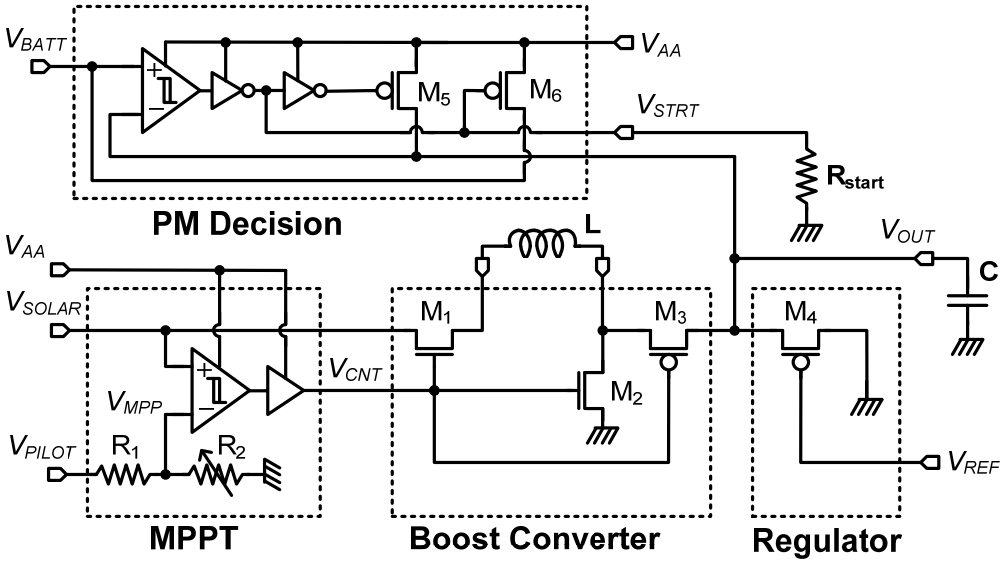


Figure 4-13. On-chip power management system (PMS) in 2nd gen. EHI sensor, [11], [68].

Even though R_1 and R_2 are set large enough to minimize the current drawn from the pilot cell, the output voltage of the pilot cell is less than V_{oc}. The voltage fraction is reduced below the resistive divider ratio by a factor α due to the finite equivalent input resistance of resistive voltage divider. The voltage divider ratio is programmable to compensate for this error. The resistive divider is adjusted through scan chain registers.

The comparator output compares the V_{SOLAR} and V_{MPP} and generates a control output (V_{CNT}) driving the boost converter. The effective current drawn by boost converter from the solar cell keeps solar cells at V_{MPP}. When V_{SOLAR} is less than V_{MPP}, the comparator output is "low" and M1 and M2 of the boost converter are off. V_{SOLAR} rises towards V_{OC} with no loading until the comparator output switches. When comparator output switches, M1 and M2 turn on and V_{SOLAR} decreases as a result of the current drawn from the photodiode array. V_{SOLAR} settles at V_{MPP} as the boost converter turns ON and OFF. Fractional Voltage MPPT technique is a

very low power and simple technique. Its low power operation compared to more sophisticated methods makes up for any minute deviations from MPP.

Solar cell current flows through the inductor to ground when the M1 and M2 are turned on. The output voltage of solar cell (V_{SOLAR}) drops as the current drawn from the solar cell increases. When the current reaches the maximum available current (or short circuit current) V_{SOLAR} is 0V. MPPT circuit tries to keep the current at the optimum level by sensing the V_{SOLAR}. When V_{SOLAR} drops below V_{MPP}, the MPPT comparator turns the NMOS switches off and turns the PMOS switch M3 on. As a result, the inductor is floating with 1 terminal connected to the storage capacitor. Since the inductor current cannot change instantly, the floating inductor supplies a decaying current. Thus, the solar energy stored in the inductor is transferred to large external storage capacitor. Since there is no load connected to photodiode array, V_{SOLAR} rises. When it rises one hysteresis voltage above V_{MPP}, the output of MPPT comparator is toggled again starting a new cycle. This operation continues charging the storage capacitor with the maximum efficiency. Note that the switches in the boost converter are driven by MPPT circuit. This integrated topology requires no clocks to drive the switches. As such, the circuit can efficiently operate with low power compared to switched-capacitor based charge pumps.

In order to regulate the harvested voltage output at V_{OUT} with low power consumption, a charge-skimming regulation technique is utilized. As the floating inductor acting like a current source pumps charge to the capacitor, the voltage across the capacitor (V_{OUT}) increases. It decreases when load removes charge from the capacitor. If the current consumed from the capacitor by the load is larger than the current supplied, the capacitor will eventually discharge. However, when the supplied current is larger, voltage will go on increasing. The

charge-skimming gate is a simple switch that turns on when V_{OUT} reaches a preset maximum value.

$$V_{OUT,MAX} = V_{REF} + |V_{THP}| \tag{4-10}$$

The charge skimming gate dumps the excess charge to ground. As the excess charge is dumped and the voltage level falls, the switch will turn OFF. The output voltage might have a small ripple due to the transistor switching, which is acceptable for power supply of self-powered CMOS image sensor.

PMS decision block switches chip power supply (V_{AA}) between the energy storage node (V_{OUT}) and the battery (V_{BATT}) voltages. It compares the V_{OUT} and V_{BATT} with a hysteresis. If V_{OUT} is one hysteresis voltage (V_{HYST}) above the V_{BATT} voltage, then M5 turns on, and M6 turns off allowing self-power operation. Meanwhile, MPPT and boost converter continue to transfer charge from solar cells to the external capacitor keeping V_{OUT} high. At start up, gate of PMOS switch M6 is grounded by a large off-chip resistor (R_{START}>5MΩ) and M6 connects V_{AA} to V_{BATT}.

4.7 Summary

Harvesting energy from environment is an important tool for powering low power electronic systems. Solar energy harvesting is suitable for powering image sensors. Since image sensors operate in illuminated environments, light energy is readily available. Moreover, the photodiodes used in pixels can be used for harvesting the solar energy. Energy autonomous image sensors can be built integrating high efficiency solar energy harvesting structures with low power image sensors.

A power management system harvests maximum available power from the pixel array, converts the pixel array output to a usable voltage, regulates the converted voltage and stores the generated energy for powering the image sensor and switches between battery power and harvested power based on the availability of harvested power.

CHAPTER 5 - ULTRA-LOW POWER ENERGY HARVESTING AND IMAGING (EHI) TYPE CMOS APS IMAGER DESIGN

This chapter presents an ultra-low power CMOS active pixel sensor (APS) image sensor designed with energy harvesting capability and operating at 1V supply voltage. The energy harvesting and imaging (EHI) APS imager dissipates an order of magnitude lower power than the current state of the art low-power CMOS APS imagers reported.

Besides low-power operation, the power harvesting capacity of the new EHI pixel is increased one order of magnitude. The low-power CMOS image sensor described in this chapter harvests sufficient energy to power the imager with the amount of ambient light illumination needed for capturing the scene images. The image sensor architecture and details of the blocks with underlying circuits used in imaging and energy harvesting modes are described in detail.

5.1 Image Sensor Architecture

The EHI-type CMOS APS concept is based on the fact that the pixel photodiodes used for imaging and solar cells are physically identical. An image sensor is basically an array of reverse biased PN-junctions. A solar cell is a photodiode operating in forward bias region. Therefore, the same PN-junction can be used as an imaging photodiode while reverse biased and as a micro solar cell while forward biased. First and second generation EHI-type CMOS APS pixels were developed based on this principle of operation and described in previous chapter. The 3rd generation EHI-type CMOS APS pixel described in this chapter generates

enough energy for imaging operation so that the EHI imager does not need a battery supply. As stated before, the physical construction of energy harvesting photodiode affects the energy harvesting capacity considerably [12]. The proposed 3rd generation EHI imager uses a completely new approach in building the energy harvesting photodiode in each pixel.

Block diagram of the proposed 3rd generation EHI APS imager is shown in Figure 5-1. The EHI imager system is composed of a 64(H) x 45(V) pixel array, low-power readout electronics and a novel charge pump. Pixel pitch is 18μm. A low-leakage and mature 0.35μm 2P4M/3.3V CMOS process was used for fabrication.

The pixel array is addressed row by row. Rows are selected with a shift register type

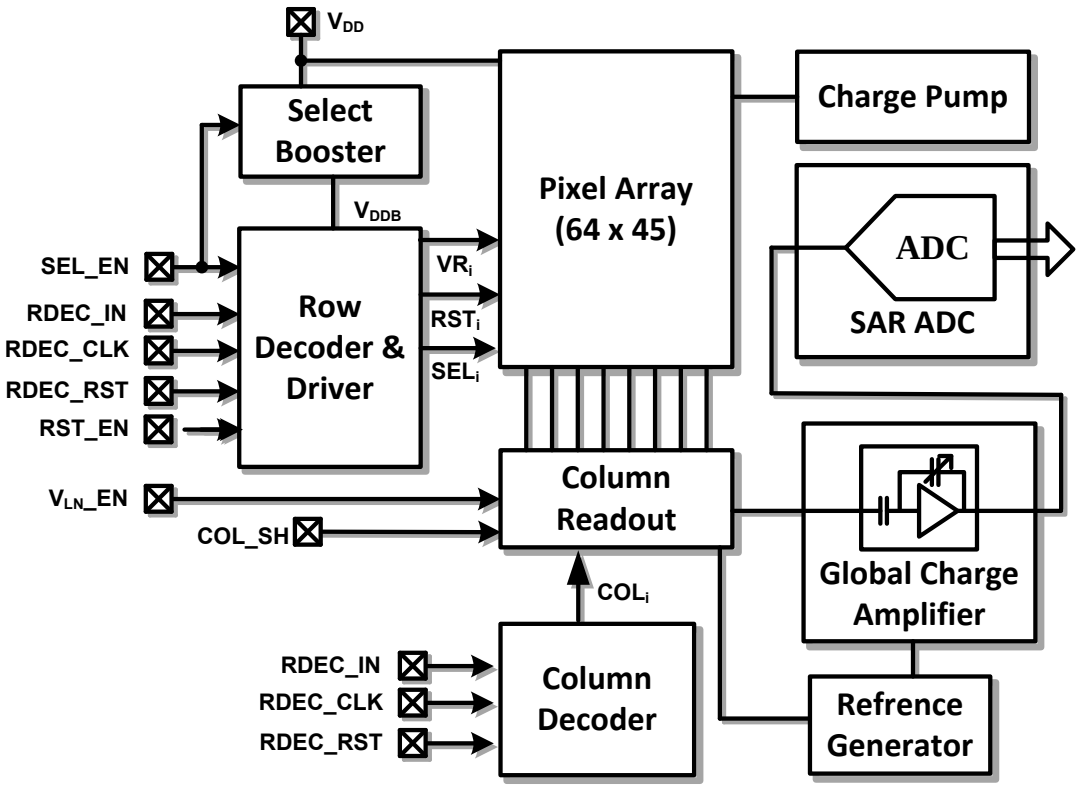


Figure 5-1. Block diagram of the 3rd generation EHI-type CMOS APS image sensor.

row decoder and row driver. All pixels in the selected row are read out in parallel and are stored on the column sample and hold (S&H) capacitors. Column readout circuit together with the global charge amplifier performs correlated double sampling (CDS) function. CDS reduces the 1/f noise, thermal noise and FPN caused by the threshold voltage, doping concentration, and physical dimension variations of the pixel transistors.

A shift register based column decoder is used for selecting columns sequentially. The S&H capacitor in the selected column is connected to the global charge amplifier (GCA). GCA converts the absolute pixel signals stored on S&H capacitors into voltage. GCA also introduces gain to the readout channel increasing signal to noise ratio (SNR).

GCA output is sampled by an on-chip successive approximation (SAR) type ADC. ADC converts the GCA output into 8-bit digital output. Both analog and digital outputs are available from the imager.

Row select signal is boosted in the proposed EHI imager to improve linearity for the pixel source follower [69]. Reset or supply boosting was not used due to the fact that a PMOS reset switch was used in the pixel. A very low power reference generator was developed to provide on-chip bias currents for the pixel source followers and the GCA.

The harvested energy was boosted by a novel on-chip charge pump which not only provides high voltage output but also changes the polarity of the harvested energy.

5.2 The 3rd Generation Energy Harvesting and Imaging (EHI) Pixel

5.2.1 **P-Sub/N-Well Photodiode**

In a twin well CMOS manufacturing process, layers available for building a PN-junction are; P-substrate (p-sub), N-well, N diffusion (N+diff) and P diffusion (P+diff). Triple well CMOS processes additionally have a P-well layer in which an isolated NMOS transistor

could be built. The P-sub layer is permanently grounded. Therefore, anodes of P-sub/N+diff and P-sub/N-well junctions are permanently grounded while both terminals of P-well/N+diff, P-well/N-well and N-well/P+diff can be connected freely to any potential. The p-sub/n-well photodiode generates much larger photo current than the other junctions in CMOS processes. The photo generated current in a PN-junction is given by (5.1)

$$I_{ph} = A \cdot J_{ph} = A \cdot \left(q \cdot G \cdot \left(L_N + W_D + L_P \right) \right) \tag{5-1}$$

G is the photo carrier generation rate, q is the electron charge, L_N and L_P are the diffusion lengths of minority carriers, W_D is the width of depletion region, and A is the junction area.

It is evident from (5-1) that junctions with larger area, wider depletion regions and longer diffusion lengths have larger photo generated current, [64]. Since the P-sub/N-well junction has very deep sidewalls, the junction area is much larger than other available junctions. Moreover, depletion regions extend deeper into lightly doped regions. Since both P-sub and N-well layers are lightly doped compared to N+ or P+ diffusion layers, the depletion region is much wider in P-sub/N-well junction. All these factors lead to a much larger photo generated current in the P-sub/N-well junction.

Since anode of a solar cell is more positive than its cathode, P-sub/N-well photodiode can only generate a negative voltage at its cathode. Therefore, in previous EHI pixel approaches (1st generation EHI in [18] and 2nd generation EHI in [1]), only the floating anode photodiodes were used for energy harvesting photodiodes. The inevitable P-sub/N-well junction was treated as a parasitic and shorted to ground during energy harvesting. A very large power generation capacity is wasted in these approaches.

In the proposed 3rd generation EHI image sensor, the energy harvesting pixel structure generates a negative voltage and it is safely handled in a twin well process. This new approach of generating and handling negative micro solar cell voltages increases the harvested power approximately 10 times.

There are some issues associated with handling negative voltages in an integrated circuit. Since NMOS transistors have P-type bulks and N-type source and drain regions, PN-junctions are formed at the interfaces. It is desired that all current entering the drain flows through the channel into source. A large current will flow from the bulk to source and drain if these junctions are forward biased. The magnitude of the forward bulk to source and bulk to drain currents can be calculated using the Schockley diode model as given in (5-2), [63].

$$I_D = I_s\left(\exp\left(\frac{V_D}{n \cdot V_T}\right) - 1\right) \tag{5-2}$$

I_s is the reverse saturation current, n is the diode non ideality factor and V_T is the thermal voltage. Since the PN-junction forward current is an exponential function of the forward bias voltage, it can suppress the drain to source current preventing the regular operation of the NMOS transistor. Therefore, the substrate of a NMOS transistor has to be kept at the most negative potential in the system, [70]. In a standard CMOS process with no P-well, permanently grounded substrate is the bulk of all NMOS transistors. Therefore, handling a negative voltage with these transistors is an unconventional practice.

As long as the bulk of the transistor is kept at the most positive system voltage, there will be no leakage problem from source and drain nodes of a PMOS transistor. However, turning the PMOS switch on requires a voltage even more negative than the negative voltage applied to its drain or source. Charge pump circuits that could generate such negative voltages

are available, but they increase circuit complexity and power consumption of the imager. Thus, using NMOS switches are a more practical despite the forward bias currents running from bulk to source (I_{BS}) and bulk to drain (I_{BD}). The magnitude of the substrate leakage currents are not significant for the range of negative voltage values generated on chip. Rationale of using NMOS switches for handling the generated negative voltage is discussed in detail in section 5.5.1.

Since P+diff layer can be placed in the N-well with no area penalty, a P+diff/N-well photodiode (PD2) can be vertically stacked with the P-sub/N-well photodiode (PD1). The second photodiode works as an extra energy harvester in the energy harvesting mode. In imaging mode, PD1 and PD2 operating in parallel results in a much wider spectral response compared to a typical photodiode type CMOS APS utilizing shallow P-sub/N+diff junction only. The deep P-sub/N-well junction (PD1) is more sensitive to red photons while shallow P+diff/N-well junction PD2 is more sensitive to green photons. The pixel fill factor is very high since two parallel photodiodes are built in the same area in a vertically stacked fashion. Cross section of the new EHI photodiodes designed in 0.35µm 2P4M CMOS process is shown in Figure 5-2.

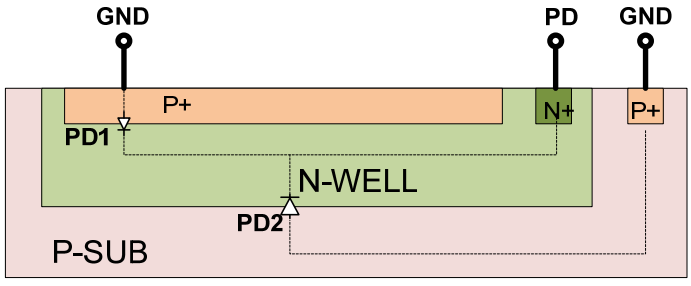


Figure 5-2. Cross sectional view of the photodiodes in new EHI pixel.

5.2.2 **EHI Pixel Circuit**

The EHI pixel schematic is shown in

Figure 5-3(a). The pixel is composed of two photodiodes (PD1, PD2 as described in previous section), one PMOS transistor (M1) and three NMOS transistors (M2-M4). M1 is the reset transistor used for resetting the floating diffusion (FD) node. M2 is the pixel source follower (PSF) and M3 is the row select transistors. These three transistors are the typical transistors in a photodiode type 3T CMOS APS pixel with a PMOS transistor, [71]. M4 is the EHI enable switch.

When an NMOS transistor is used as a reset switch, drain of the NMOS reset transistor is connected to pixel supply voltage (V_{DD}) and source is connected to the floating

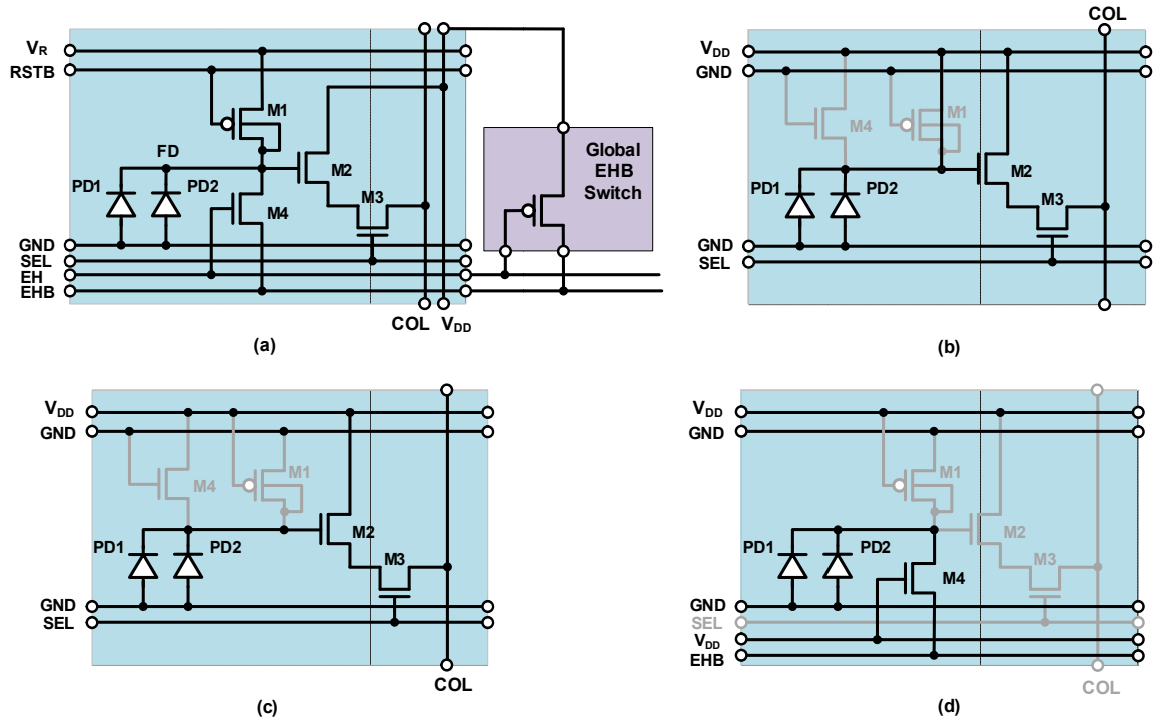


Figure 5-3. (a) EHI pixel circuit and the global EHB switch, (b) pixel configuration during reset, (c) pixel configuration during integration, (d) pixel configuration during energy harvesting mode.

diffusion (FD) node. High level of RST signal should be at least one threshold voltage above the supply voltage for resetting the pixel to V_{DD}. On the other hand, a PMOS reset transistor can pull the PD node to V_{DD} with no threshold voltage drop contrary to a NMOS device. Since the PMOS source is fixed at supply voltage, reset transistor will turn on by applying ground level to its gate.

PMOS reset transistor has its drawbacks as well. Since a PMOS device has its own n-well, it is much larger than an NMOS transistor with the same channel width and length. The carrier mobility in P-type transistor is less than that of an N-type transistor. Therefore, the channel width must be larger to achieve same conductivity with a PMOS reset transistor. Using a PMOS transistor as switch in a conventional CMOS active pixel reduces the fill factor of the pixel considerably and is not preferred in commercial applications. Moreover, the large N-Well to substrate junction in the pixel will have considerable leakage from power supply to ground under illumination.

In the proposed EHI pixel, the PMOS transistor is built in the N-well used for building the photodiodes (PD1, PD2). A very compact PMOS reset transistor can be built this way. However, the bulk of the PMOS is connected to its drain in this circuit configuration. During the reset phase, the source and drain are shorted. Therefore, connecting the bulk to source or drain does not cause a problem during reset. However, the source to bulk junction is forward biased as N-well potential drops from V_{DD} during the integration period if the source is fixed at supply voltage. As a result, the forward biased junction will leak current to FD node from power supply and stop integration.

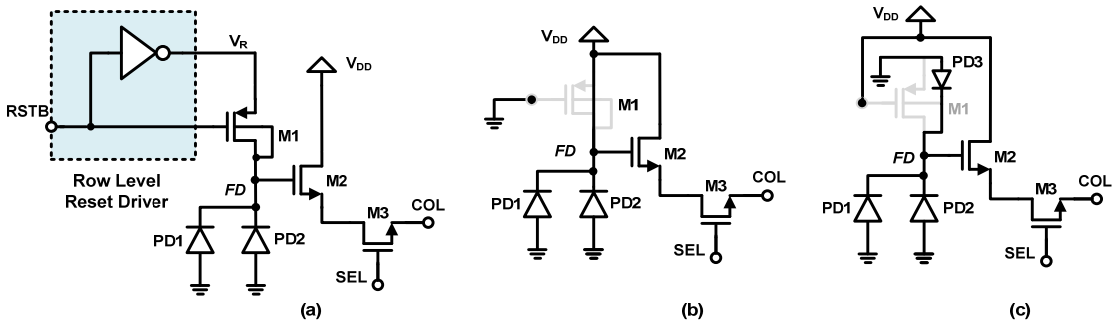


Figure 5-4. (a) Reset driver circuit driving the new EHI pixel, (b) reset transistor configuration during pixel reset operation, (c) reset transistor configuration during integration period.

This problem is overcome using a row level reset driver circuit as shown in Figure 5-4(a). The reset driver switches the V_R node to supply voltage only during reset phase and switches it to ground at all other times. The source to bulk junction of the PMOS reset transistor acts as a third photodiode (PD3) in parallel with PD1 and PD2. The PD3 contributes to the integration operation in imaging mode and harvests energy in energy harvesting mode.

The FD and energy harvesting node of the pixel are the same node. In the imaging mode, M4 is turned off and FD nodes are disconnected from the energy harvesting bus (EHB). In imaging mode, EH signal is LOW and EHB is connected to power supply (V_{DD}) using a global PMOS transistor in order to make sure M4 transistors are completely turned off. M4 switch is configured just like an NMOS reset switch in the imaging mode. Therefore, it can be used as a soft reset switch in imaging mode. It is possible to achieve soft reset with M4 and hard reset with M1. Applying first hard reset and then soft reset reduces the thermal noise, [23]. This can be easily achieved adding a simple digital gate to the row driver. During the energy harvesting mode, EH signal is high. M4 switches are turned on shorting FD nodes in all pixels to EHB and global EHB switch is turned off. All photodiodes deliver the energy generated in pixel to EHB.

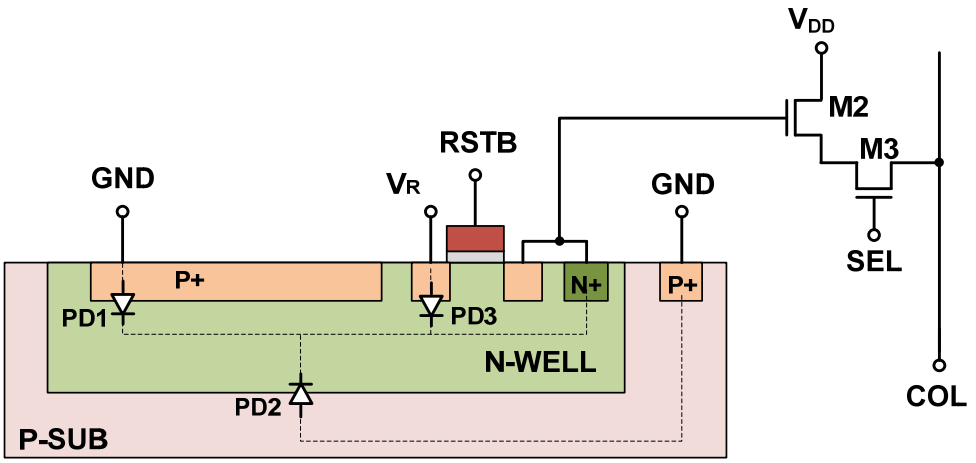


Figure 5-5. Cross section and schematic of the 3rd generation EHI pixel in imaging mode.

During imaging mode, the incident photons are absorbed by the pixel photodiodes and converted to voltage. The P+diff /N-well and P-sub/N-well photodiodes are used in parallel for imaging. The P+diff /N-well photodiode has a short minority carrier diffusion length in the P+diff region due to the high doping concentration of the P+diff layer. Electron-hole (e-h) pairs generated in the P+diff region will recombine before they arrive at the depletion region. Therefore, the blue response of the EHI pixel is poor. Moreover, e-h pairs generated by absorption of red photons deep in the substrate recombine before they reach the depletion region of the shallow junction. The P-sub/N-well photodiode has longer diffusion lengths both in the N-well and P-sub due to the low doping concentrations of both regions. Depletion regions of the side wall junctions of the p-sub/ n-well junction are also wider and these depletion regions extend to the surface. Therefore, blue response of the p-sub/n-well junction is relatively better than the shallow junction photodiodes.

The photodiode voltage is buffered by the pixel source follower. Outputs of all pixels in a column are connected to the same column bus through the row select transistor. The row

select transistor in the selected row is on and all others are off. Therefore, only one pixel is connected to a column bus at a time. The voltage drop across the select transistor decreases for larger overdrive voltages. This also improves gain linearity of the pixel source follower, [69]. Therefore, the select transistor is driven with a boosted select signal.

5.3 Analog Building Blocks

Analog signal chain from pixel photodiode node to global charge amplifier (GCA) output is shown in Figure 5-6. Incident photons are captured and converted to a voltage signal by the pixel photodiode. The photodiode voltage is buffered by the pixel source follower. Source follower output is sampled by the column readout circuit. Column outputs are amplified by the GCA and analog output is generated.

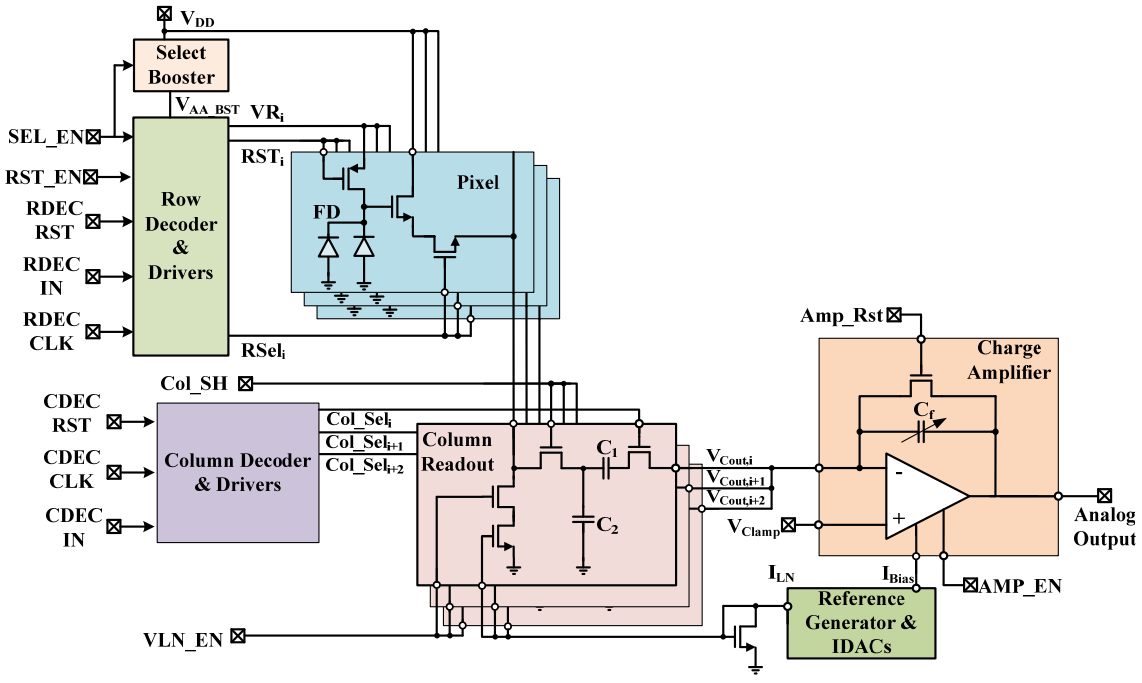


Figure 5-6. Analog signal chain for imaging mode operation.

Figure 5-7 shows the timing diagram for the EHI imager during imaging mode. Row readout starts with selecting a row. Outputs of all pixel source followers in the row are sampled by the column sample and hold (S&H) circuits. After the signal readout, all pixels in the row are reset. Pixel source follower outputs right after the reset are sampled by the column S&H circuit. Once the pixel outputs are sampled, the column S&H capacitors are connected to the GCA one by one. GCA outputs are sampled by the SAR ADC and then converted to digital. After conversion of 64 columns, the row readout is complete and the next row is selected. In this readout scheme, integration time of a pixel is the frame time.

When imager is running at 5 frames per second (FPS), it is clocked with a 2.08 MHz master clock. ADC sampling and conversion time for each column is 135 clock periods (64.8 µs). Column sampling time is 392 clock periods (188.2 µs). Total row time is 9032 (392 + 64 x 135) clock periods (4.34 ms). Pixel column current sources biasing the pixel source follower are controlled by the VLN_EN signal. The current sources are turned on only during column S&H.

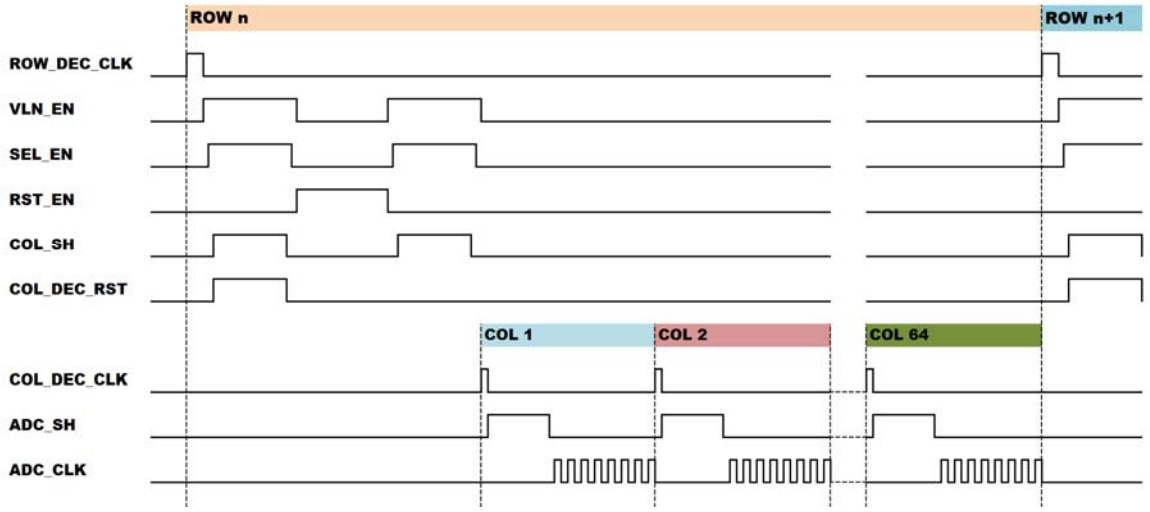


Figure 5-7. EHI imager timing during imaging mode.

5.3.1 **Analog Readout Channel**

Pixel source follower transistor (M2) is connected to the column current source through select transistor (M3). Column bias current could be as low as 12.5nA for lower frame rates. For 5 FPS, it is set to 25nA. A source follower can pull its source to the biased level with unlimited current. Therefore, source follower bias current does not have any effect on the sampling time as long as the initial voltage on the S&H capacitor is lower than the source follower output voltage.

Pixel outputs are processed by the analog readout channel. Analog readout channel is composed of column readout circuits and global charge amplifier. The column read out circuits and global charge amplifier effectively function as a switched capacitor amplifier as shown in Figure 5-8.

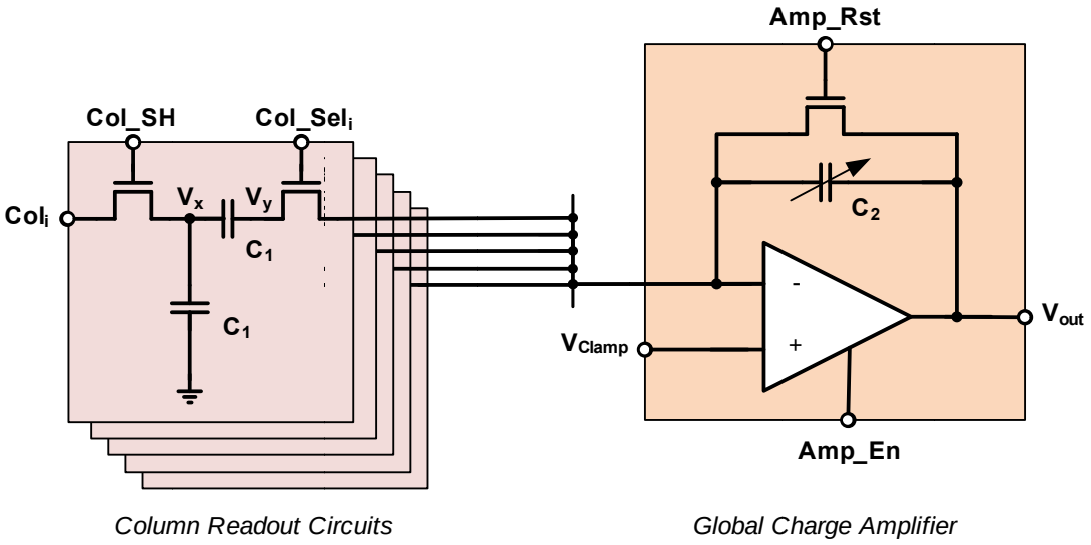


Figure 5-8. Analog readout channel

The charge amplifier dissipates a considerable portion of the total power of the imager. Therefore, it is important to minimize the power consumption of the charge amplifier.

A simple amplifier structure with minimum number of branches is preferred for power efficiency. The settling time of the amplifier output is inversely proportional to output current of the amplifier. Therefore, more amplifier bias current is needed for higher operating frequencies.

5.3.1.1 *Column Readout Circuit*

The pixel source follower outputs in the whole row are sampled on column sample and hold (S&H) capacitors (C1, C2) at the end of integration (signal level) and right after reset (reset level). The differential sampling scheme is known as correlated double sampling (CDS). CDS eliminates thermal noise, 1/f noise and pixel FPN caused by pixel to pixel variations due to threshold voltage, doping concentration, and physical size variations of pixel transistors (M1-M3). The CDS function is performed basically by subtracting reset level from signal level for each pixel. True CDS is achieved subtracting the reset level and signal level in the same frame. True CDS is not possible in 3T CMOS APS pixel. However, a pseudo CDS, where the signal value is subtracted from the reset level of the next frame, is performed using the column readout circuit together with the global charge amplifier, [71]–[73].

At the end of integration, all column select switches and amplifier reset switch are turned on simultaneously setting the top plates of C_1 capacitors in all columns to the reference voltage applied to the non-inverting input of the amplifier denoted as V_{Clamp}. Simultaneously, column sample and hold switches are also turned on sampling the pixel output voltage on the bottom plate of C_1 and top plate of C_2 capacitors. The pixel output sampled at this instance is the signal level at the end of integration. The voltage across the sample and hold capacitor is given by (5-3).

$$V_{c1} = V_y - V_x = V_{Clamp} - V_{sig} \tag{5-3}$$

Consequently, all pixels in the row are reset. When sample and hold switches are turned on, the top plate of the sample and hold capacitors are set to the pixel output at pixel reset level. At this instance top plate of the sample and hold capacitor C_1 is given by (5-4).

$$V_y = V_{Clamp} + V_{rst} - V_{sig} = V_{Clamp} + V_{eff} \tag{5-4}$$

5.3.2 **Global Charge Amplifier**

Global charge amplifier (GCA) performs several critical functions in the analog signal chain. The GCA provides gain for the analog signal chain. The pixel and column readout circuits attenuate the signal. GCA restores the lost signal swing. The added gain also increases signal to noise ratio (SNR). The GCA also functions as a buffer between the column S&H capacitor and the ADC S&H capacitor. However, the most critical function of the global amplifier is its role in correlated double sampling (CDS).

Once the differential sampling of the columns are completed, column select switches are turned on one by one connecting each column S&H circuit to the GCA. When the switch is turned on, the amplifier forces V_y in column readout circuitry to V_{Clamp}. The excess charge is moved to the initially discharged feedback capacitor C_f. The output of the amplifier is connected to an analog pad, and the on-chip ADC. Output capacitance of the column readout circuit is given by (5-5).

$$C_{Out} = \frac{C_1 C_2}{C_1 + C_2} \tag{5-5}$$

Therefore, the amplifier output voltage is given by (5-6).

$$V_{out} = V_{Clamp} - \frac{C_1 C_2}{C_f (C_1 + C_2)} V_{eff} + \left(1 + \frac{C_1 C_2}{C_f (C_1 + C_2)}\right) \frac{V_{offset}}{1 + A_o} \tag{5-6}$$

Global charge amplifier gain in EHI imager can be set to 4x, 2x, 1.33x and 1x.

Amplifier is the most power hungry block in a CMOS image sensor. Designing a very low power charge amplifier is challenging due to the trade-offs between power consumption, settling time and bandwidth.

Global charge amplifier in the CMOS APS imager may be implemented using several amplifier topologies including Miller compensated two-stage OPAMP [74], balanced current mirror OTA [75], [76], folded cascode differential amplifier [77], and multi-stage amplifier. Despite their lower gain, balanced current mirror OTA and Miller compensated OPAMP topologies are preferred over folded cascade amplifiers and multi stage amplifiers due to power, area, bandwidth and slew rate considerations, [44], [72].

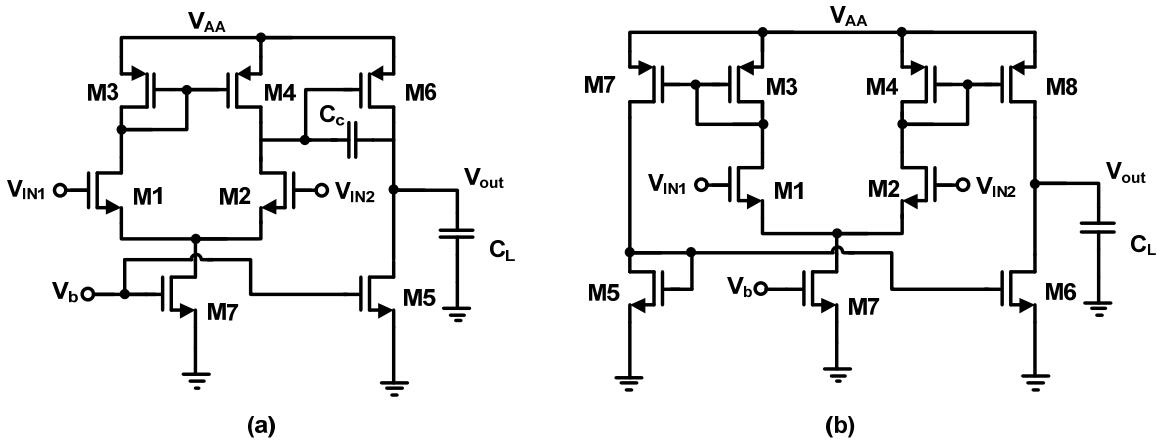


Figure 5-9. Schematic of (a) Miller compensated OPAMP and (b) balanced current mirror OTA.

Schematic diagram of the Miller compensated OPAMP and balanced current mirror OTA are shown in Figure 5-9. Power consumption of balanced current mirror OTA is shown

to be lower than miller compensated two-stage OPAMP with equal gain, slew rate, gain bandwidth product and phase margin, [44]. Most important reason for the higher power consumption in a Miller compensated OPAMP is the power consumed while charging and discharging the compensation capacitance. Since the major part of the voltage gain is achieved at the output node in a single stage amplifier, no compensation capacitance is needed, [72]. The balanced current mirror OTA is a single stage amplifier with high current driving capability and large output swing. Therefore, it is the preferred amplifier structure for GCA implementations in image sensors. The current mirror OTA circuit implementation used in the EHI imager's GCA is shown in Figure 5-10.

Since only the output stage current determines the bandwidth, slew rate and settling time, a (1:10) current-mirror ratio is used for decreasing the unnecessary power consumption on half of the signal path. The overall transconductance of the amplifier is given by (5-7).

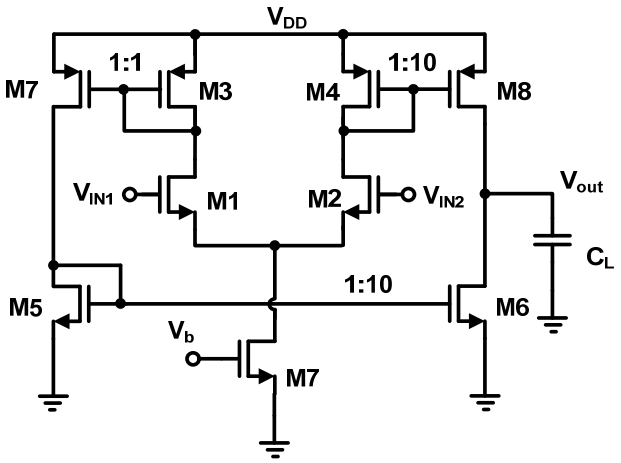


Figure 5-10. Current Mirror OTA schematic used in EHI imager's GCA.

$$g_m = 10 \cdot g_{m1} \tag{5-7}$$

The single stage amplifier driving a load capacitor C_L is a low pass filter with a dominant pole at its output node. The amplifier's time constant, unity gain frequency, 3dB frequency and slew rate are given in (5-8) to (5-11).

$$\tau = C_L / g_m \tag{5-8}$$

$$\omega_u = 1/\tau_u = g_m / C_L \tag{5-9}$$

$$\omega_{3dB} = \frac{1}{\tau_{3dB}} = \frac{1}{[(r_{o6} \parallel r_{o8})C_L]} \tag{5-10}$$

$$SR = 10 \cdot i_{bias} / C_L \tag{5-11}$$

5.3.3 **Successive Approximation ADC**

An 8-bit successive approximation register (SAR) type ADC is used for converting the amplifier output to a digital code in the EHI imager. SAR ADCs consume relatively low power offering a good balance of chip area and bit resolution. They are suitable image sensor topologies for medium to high resolution applications where ADCs need to operate at a relatively medium speed.

Even though fully differential SAR ADCs have better rejection of common mode noise and even order harmonic distortion, they require doubling the number of switches, two capacitive DACs, more complicated sample and hold circuits and consume more power compared to single ended SAR ADCs. Therefore, single ended SAR ADCs are preferred for low power applications, [78], [79]

Energy efficient dynamic comparator [80] is used to minimize power consumption of the SAR ADC. Schematic diagram of the comparator is shown in Figure 5-11. This dynamic

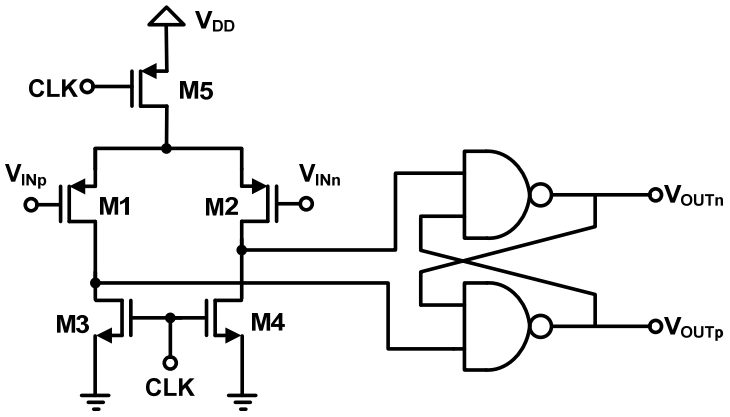


Figure 5-11. Dynamic Latched Comparator

comparator does not consume static power while easily achieving 100kS/s speed for 1V power supply in 0.35µm CMOS process that is chosen for the EHI imager. This speed meets the requirement of the CMOS image sensors with smaller array sizes less than 10Kpixels for low-power applications for up to 20 FPS.

Operation principle of a SAR ADC is based on binary search. Sampled input voltage (V_{in}) is compared against the output of a digital-to-analog converter (DAC). The SAR ADC used in this design uses a binary-weighted capacitor array for DAC to generate binary weighted quantization levels. SAR logic implements the binary search algorithm. The direction of the binary search is determined by the comparator output, [81]. The number of comparison steps is reduced to ADC resolution using binary search. Block diagram of the SAR ADC integrated is seen in Figure 5-12.

The schematic of the 8-bit successive approximation ADC with the binary-weighted capacitor array DAC is shown in Figure 5-13. The capacitive DAC is initially discharged. The

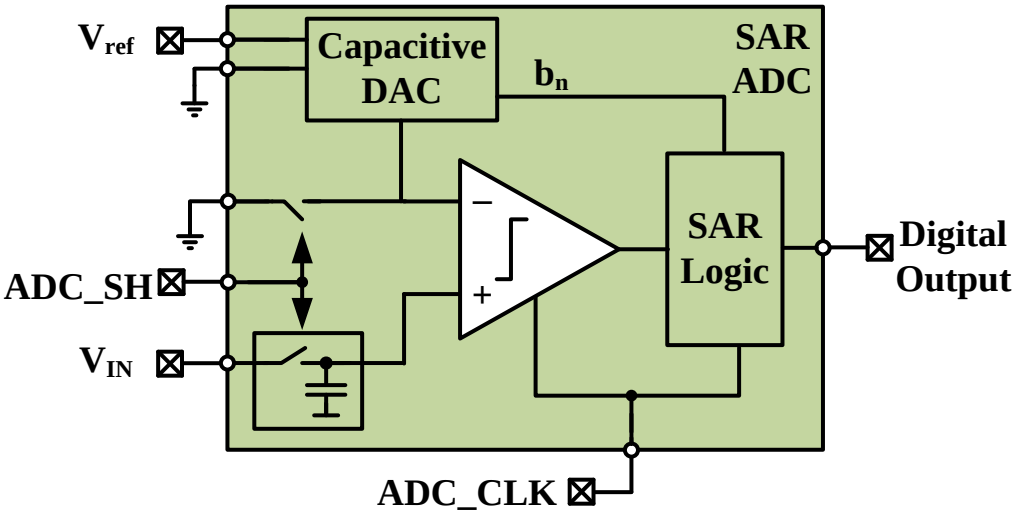


Figure 5-12. Block diagram of the successive approximation ADC.

GCA output is sampled onto the S&H capacitor (C_{SH}). After sampling the input, the bottom plates of DAC capacitors are successively connected to the ADC reference voltage (V_{ref}). This switching changes the top plate voltage proportional to the relative size of the capacitor to the total capacitance of the network. The voltage V_x at the top plates is given by (5-12).

$$V_x = \frac{C_1}{C_T - C_1} V_{ref} \tag{5-12}$$

C_1 is the total value of capacitors switched to V_{ref} and C_T is the total value of DAC capacitors.

When largest capacitor in the DAC is switched to V_{ref} at first comparison step, the sampled input is compared against the $V_{ref}/2$. Depending on the comparator output, this capacitor is kept at V_{ref} or switched back to ground. When the second capacitor is switched to V_{ref} at the second step, V_{in} is compared against either $3V_{ref}/4$ or $V_{ref}/4$ depending on what the comparator output was after the first step. The comparator output at each step determines comparison value in the next step.

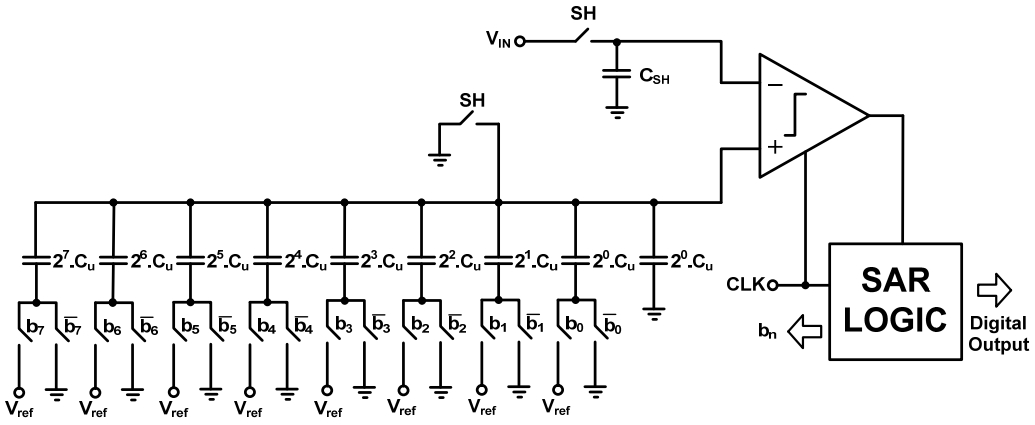


Figure 5-13. The 8 bit SAR ADC schematic used in the EHI imager.

The SAR ADC completes conversion in 8 clock cycles. There is no static power consumption in the ADC since a clocked comparator with output latch is used. Main component of power consumption is the switching power dissipated for charging and discharging the capacitors between GND and V_{REF}. Since V_{REF} is set by the charge amplifier output range and the clock frequency is determined by the frame rate, the only way to reduce switching power of the SAR ADC is minimizing the unit capacitor size. Minimum size polysilicon-insulator-polysilicon (PIP) capacitors are used for building the capacitive DAC to minimize the switching power.

Absolute minimum capacitor size is set by thermal noise of the capacitors. The thermal noise should be less than half LSB. The minimum capacitance for this particular application is calculated to be 3fF. However, there are practical limitations for the unit capacitance size. Since capacitor matching is very critical for ADC linearity, physical dimensions of the unit capacitor is chosen larger than the minimum size for good matching. Unit capacitor size was chosen as 13fF.

5.3.4 **Reference Circuit**

The reference current in a circuit is expected to be insensitive to process, voltage, and temperature variations. Normally bandgap references are used to generate such an invariant current. For low power operation, the reference voltage needs to be very low power as well. Therefore, a bandgap reference cannot be used in the EHI imager. A supply independent beta multiplier current reference generator is used in the EHI imager instead of a power hungry bandgap reference. A novel reference generator that consumes 50nA total supply current was designed. However, generating 12nA reference current reliably with a standard beta multiplier reference generator would require very large on-chip resistors. Therefore, the resistor is replaced with triode region transistors. This makes building a very low power reference generator possible with small area, [82].

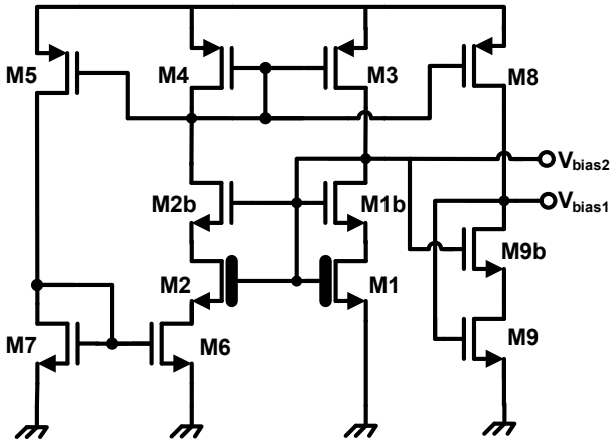


Figure 5-14. Very low-power beta multiplier reference current generator.

The proposed reference current generator used in the EHI imager is shown in Figure 5-14. Gate to source voltages (V_{GS}) of MOSFET transistors decrease with increasing temperature under constant bias current, i.e. it is complementary to absolute temperature

(CTAT). Sub threshold MOSFETs behave as exponential devices just like BJTs. Therefore, difference between V_{GS} of two MOSFETS (ΔV_{GS}) is proportional to absolute temperature (PTAT). High threshold voltage NMOS transistors (M1 and M2) are used as the bottom pair to ensure deep sub threshold mode operation and building self-biased low voltage cascoded current mirrors. If the triode transistor was an ideal resistor, a PTAT current would be generated. $V_{GS,M6}$ decreases with increasing temperature for a constant drain current through M7 ($I_{D,M7}$). Even though channel resistance of triode transistor M6 (R_{M6}) decreases with temperature for a constant $V_{GS,M6}$, decreasing $V_{GS,M6}$ increases the channel resistance of triode transistor M6 (R_{M6}). Unlike a physical resistor, the temperature coefficient of R_{M6} can be controlled by transistor sizing. Increasing channel resistance balances the increasing voltage across it (ΔV_{GS}). This feedback loop results in a relatively temperature independent current when transistor sizes are chosen properly.

A reference generator is expected to have high power supply rejection. Regular threshold NMOS transistors (M1b and M2b) are used for building a self-biased low voltage cascoded current mirror. Since theses transistors have smaller threshold voltage, M1 and M2 are still saturated when the gates are connected together. M1b and M2b limits the change in drain voltages of M1 and M2 as supply voltage changes and the reference current generated is more stable as supply voltage changes. The generated current is run into diode connected transistor M9 and bias voltage V_{bias1} is generated to mirror the generated current to analog blocks such as column current mirrors and GCA. M9b is connected its drain for building a low voltage cascoded current mirror. M9b is biased with the gate voltage of M1 (V_{bias2}). Bias voltages V_{bias1} and V_{bias2} generated by the reference generator are used in 6-bit programmable current DACs for generating bias currents of circuits.

5.3.5 Current Steering DACs

The reference current from the reference generator is mirrored to column circuits and charge amplifier. Column and charge amplifier are biased with the minimum bias current while good quality images with low fixed pattern noise for low-power operation captured.

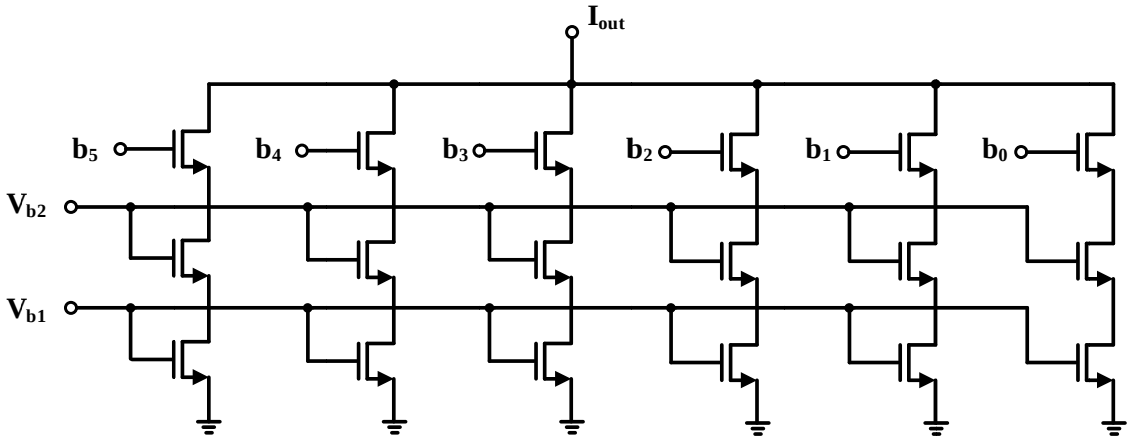


Figure 5-15. 6-bit current steering DAC schematic.

The bias currents are set via 6 bit programmable current steering DACs as shown in Figure 5-15. The current steering DAC control code is stored on a scan chain. DAC output increases 12.5nA when control code increases 1 bit. The current range could be set between 0A and 787.5nA in the EHI imager.

5.4 Digital Building Blocks

5.4.1 Row and Column Select Logic

The row and column addressing circuits in the ultra-low power EHI imager are implemented with shift registers. Shift register based addressing circuit selects rows and

columns sequentially. Therefore, window readout and randomly accessing pixels is not possible with this addressing scheme. These functions are nonessential for low resolution ultra-low power image sensors. Shift registers reduce circuit complexity, silicon area, number of interconnects and most importantly power consumption.

5.4.2 Row Select Logic

The row select logic in the EHI sensor is a chain of 45 back to back shift registers as shown in Figure 5-16. The shift registers are controlled by non-overlapping clocks ϕ_1 and ϕ_2.

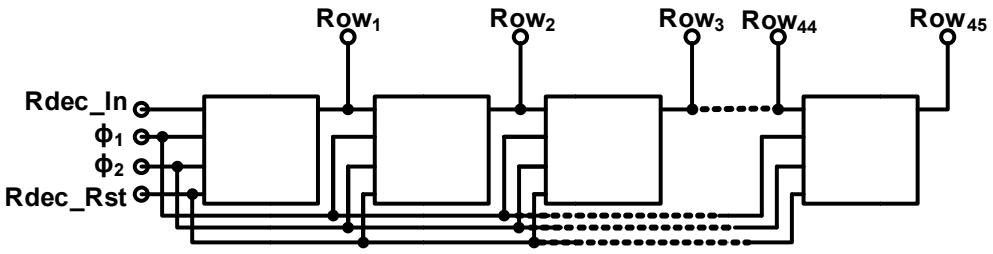


Figure 5-16. Shift register based row addressing circuit

At the beginning of frame readout, all shift registers in the row addressing circuit are reset. The outputs of all shift registers are low. The next row is selected at each rising clock edge. 45 clock edges are applied to the decoder and all rows are selected by this shifting operation.

5.4.3 Row Driver

The row driver gets the RST_EN, SEL_EN signals and shift register output Row_i as input and generates SEL_i, $RSTB_i$ and V_{Ri} signals. SEL_i and Vr_i signals are kept low and $RSTB_i$ is kept high unless the individual row is selected by the shift register. Select signal is

boosted by a level shıfter. The secondary supply voltage of level shifter is boosted by the global select booster. The voltage drop across the select transistor decreases and improves linearity when the select signal is boosted. When RST_EN signal is applied, RSTB signal for the selected row switches to low and V_R signal for the selected row switches to high.

5.4.4 Select Booster

Turning switches on and reducing switch resistance is a major challenge in low voltage circuit design. Increasing the amplitude of the clock signals beyond the supply voltage is a necessary to decrease switch resistance. Figure 5-17 shows a schematic of the select booster circuit [67], [83].

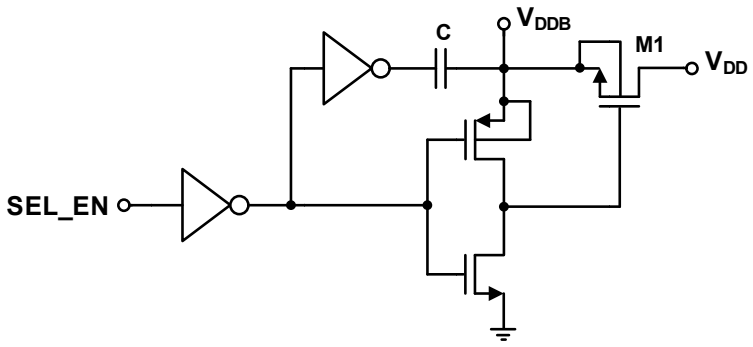


Figure 5-17. Select booster circuit

When SEL_EN signal is low, V_{DDB} is shorted to V_{DD}. The capacitor *C* is charged to V_{DD}. When SEL_EN signal is high, PMOS switch M1 is off and V_{DDB} is equal to $2V_{DD}$ for the unloaded select booster. When select booster is driving a capacitive load C_L, V_{DDB} is given by (5-13).

$$V_{DDB} = \left(\frac{C_L}{C_L + C} + 1 \right) \cdot V_{DD} \tag{5-13}$$

5.4.5 **Column Select Logic**

The column select logic in the EHI sensor is a chain of 64 back to back shift registers as shown in Figure 5-18. Non-overlapping clocks ϕ_1 and ϕ_2 control the shift registers.

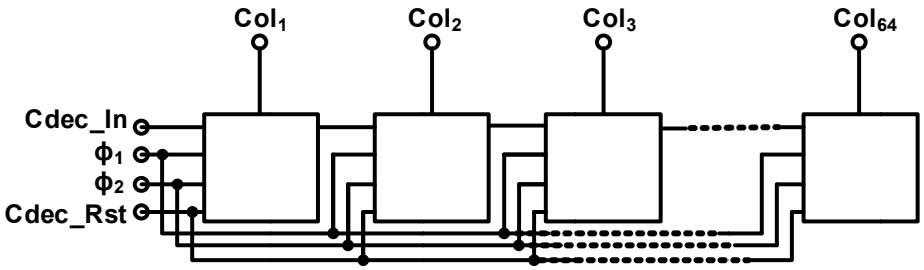


Figure 5-18. Shift register based column addressing circuit

All columns are selected during column decoder reset. When cdec_rst is low, Col_i are equal to shift register output. Only one of the shift register outputs and column select signals (Col) are high and all others are low at a time. Shifting operation is same as the row decoder.

5.5 ENERGY HARVESTING MODE CIRCUITS AND OPERATION

When imager is in standby, all imaging circuits are powered down and EH signal is high. In this mode, the global EHB switch is disconnected from V_{DD} and M4 transistors in all pixels turn on connecting photodiodes in all 2880 pixels to EHB. The generated power is applied to a charge pump and converted to a usable voltage. The charge pump output is stored on a storage capacitor. The energy harvesting mode circuits are shown in Figure 5-19.

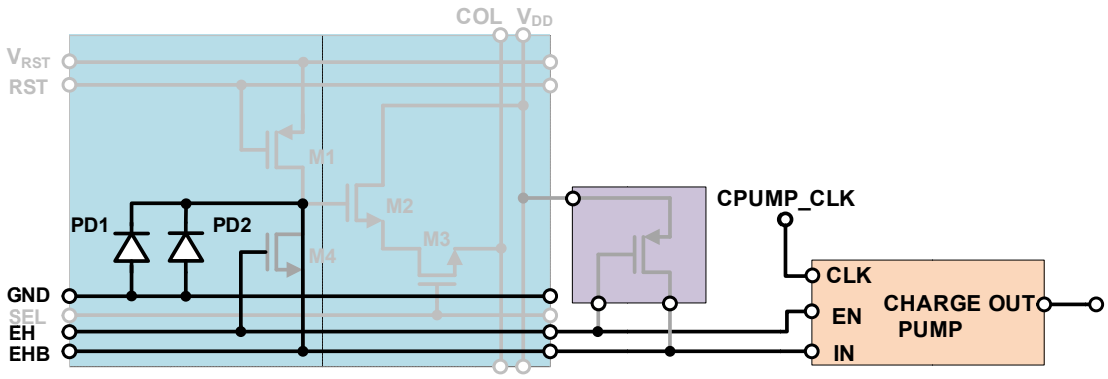


Figure 5-19. Energy harvesting mode circuits

5.5.1 Handling Generated Negative Voltage with NMOS Switches

Since the voltage generated on chip is negative, bulk to source and bulk to drain leakage is expected when NMOS transistors are connected to this negative voltage. The magnitude of the forward bulk current can be calculated using the Schockley diode model as given in (5-2). I_s for the source and drain junctions of a reasonably sized transistor in the manufacturing process used for the 3rd and 4th generation EHI sensors is between 10^{-18} and 10^{-17} A depending on the transistor size.

Maximum value of the negative voltage applied to the source and drain of an NMOS switch is the open circuit voltage (V_{oc}) of the energy harvesting photodiodes under normal illumination. V_{oc} is -470 mV under 40kLux illumination. Because of the logarithmic dependence of V_{oc} on light level, V_{oc} will increase slightly for increasing illumination. V_{oc} increases to -479mV under 60Klux illumination.

The leakage current of the in pixel EH transistor (W= 1 µm and L=0.35 µm) and the transistors used in charge pump circuit (W= 30 µm and L=0.35 µm) for different forward bias

voltages are listed in Table 5-1. The forward junction current that could be observed from bulk to source junction of a reasonably sized NMOS transistor is less than 100 pA for 0.45V forward bias voltage and reaches just 1nA for forward bias larger than 0.5V for pixel EH switch transistor. Thus, when a non-illuminated NMOS transistor is used as a switch connected to the cathode of a photodiode array generating negative voltage, leakage current from ground to the source and drain of the switch will cause an insignificant drop in energy efficiency. Therefore, an NMOS transistor can be used safely used in negative energy harvesting pixel. It was reported that the sources of NMOS transistors have been connected to $-V_{oc}$ and complicated digital circuits have been operated in standard CMOS process confirming this analysis, [84].

The leakage current is reduced further by allowing the NMOS transistors receive light. PN-junctions receiving light behave differently. The relation between diode current and diode voltage under illumination is given by (5-14).

Table 5-1. Leakage Current of NMOS Transistor with $V_{BS}>0$.

APLLIED NEGATIVE VOLTAGE	**FORWARD CURRENT**	
	1µm/0.35µm transistor	**30µm/0.35µm transistor**
700mV	1.13µA	17.62 µA
650mV	178.2nA	2.79 µA
600mV	24.79nA	386.6nA
550mV	3.76nA	58.60nA
500mV	515.9pA	8.03nA
450mV	81.03pA	1.25nA
400mV	12.79pA	187.97pA
350mV	3.00pA	37.51pA
300mV	1.30pA	12.96pA

$$I_D = I_s\left(\exp\left(\frac{V_D}{n \cdot V_T}\right) - 1\right) - I_{ph} \tag{5-14}$$

where I_{ph} is photogenerated current, [64]. The PN-junctions in illuminated NMOS transistors act as solar cells themselves and I_{ph} running from cathode to anode suppresses forward bias current. The PN-junction is not truly forward biased until the forward bias voltage exceeds the open circuit voltage of these PN-junctions. Open circuit voltage is independent of junction area unlike the short circuit current. Even though V_{oc} will be different for transistor junctions and photodiodes due to diode parameter differences, the difference will be minute and generated negative voltage will exceed the V_{oc} of the transistor junctions by a few mili volts if they exceed at all. When the generated voltage is less than their open circuit voltage, the transistor junction will provide its photo generated current to EHB instead of stealing current from it. Therefore, the source to bulk junction in an illuminated NMOS transistor connected to the energy harvesting bus or the cathodes of energy harvesting photodiodes will not leak the harvested energy. Instead its junctions will act like parallel solar cells and it will contribute to energy generation efficiency. Therefore, the generated negative voltage can be processed on-chip with CMOS transistors without any serious leakage problems especially if the transistors are exposed to light.

5.5.2 **Charge Pump Operation**

Since the voltage output of the micro solar cell array is negative, a novel charge pump which inverts the polarity was designed. The circuit diagram of the charge pump is shown in Figure 5-20. Charge pump is driven by a standard clock. Since the transistors connected to EHB cannot be turned off simply by applying 0V to its gate, the clock should be boosted to

negative voltages. The clock is level shifted to negative voltages using a cross coupled inverter. When one of the cross coupled inverter outputs are high, gate of the NMOS on the other side is high and it turns on. Since sources of the cross coupled NMOS transistors are connected to EHB, the output is pulled to EHB voltage. The cross couple inverter outputs have slow edges. Therefore, the two outputs are not high simultaneously. When these outputs are buffered using standard inverters, non-overlapping clocks are obtained. Non-overlaping clocks ensure there is no reverse leakage during clock transitions.

Timing diagram in Figure 5-21 summarizes the charge pump operation. Power supply is needed only for powering the inverters. When CLK 1 is high, bottom plates of C1 and C3 are switched from ground to EHB trying to decrease the voltage on their top plates by V_{oc}. Bottom plates of C2 and C4 are switched from EHB to ground trying to increase the voltage

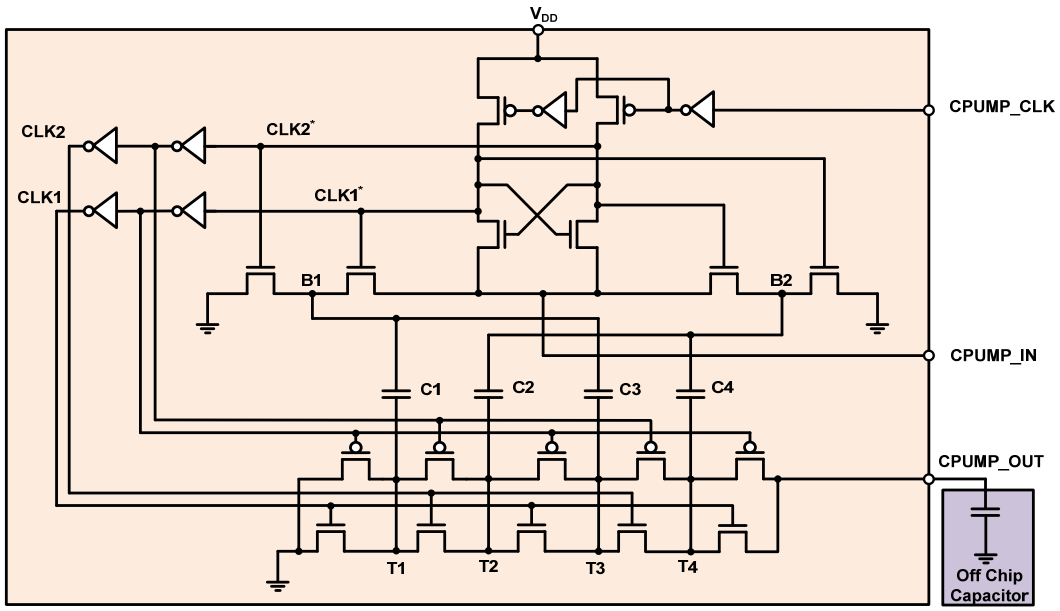


Figure 5-20. Polarity Inverting Charge Pump

on their top plates by V_{oc}. Top plate of C1 is connected to ground, top plates of C2 and C3 are shorted and top plate of C4 is connected to the storage capacitor. As a result of this switching, charge is dumped from ground to C1 top plate, C2 top plate to C3 top plate and C4 top plate to storage capacitor. When CLK2 goes high, bottom plates of C1 and C3 are switched from EHB to ground trying to increase voltage at their top plates by V_{oc}. Bottom plates of C2 and C4 are switched from ground to EHB trying decrease voltage at their top plates down by a voltage of V_{oc}. Top plates of C1 and C3 are connected to top plates of C2 and C4 respectively. This switching pumps charge from top plates of C1 and C3 to top plates of C2 and C4. The storage capacitor has very large capacitance for storing sufficient energy to run the imager in imaging mode.

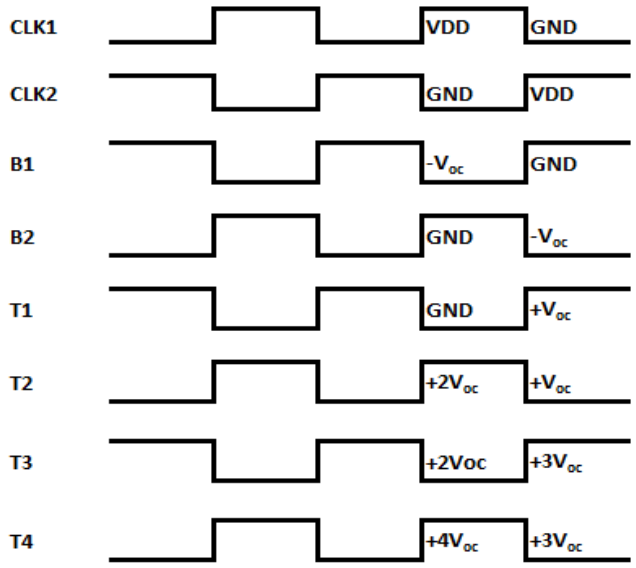


Figure 5-21. Charge pump node voltages

5.6 Summary

The prototype 3rd generation EHI sensor was presented in detail. The ultra-low power imager is designed to run with a 1V supply voltage. This image sensor could be powered by a watch battery for years. The image sensor architecture and details of analog and digital building blocks of the imagers was described. Power dissipation is the main design constraint for this image sensor. Low-power design methodology is considered at all levels of design. The energy harvesting mode circuits of the image sensor were also presented in detail. Details of the pixel configuration in energy harvesting mode and the inverting charge pump were presented.

Overall, four major differences between the new EHI pixel and other pixels with energy harvesting capability were listed. First of all, battery power is needed only for driving the gate of EH enable transistors (M4) in the EHI pixels and the EHB switch all other imaging circuits are turned off during energy harvesting mode. Secondly, leakage paths on energy harvesting bus on the pixel array side and charge pump side are insignificant compared to generated power. Thirdly, PMOS reset transistor is used with no fill factor penalty and no reset clock boosting is needed. The fill factor is further improved by vertically stacking p+diff/n-well and p-sub/n-well junction photodiodes in the EHI pixel. Fourthly, the energy harvesting efficiency is increased by an order of magnitude compared to earlier EHI sensor [10]. Thus, it is possible to run EHI imager completely by the energy harvested while it is inactive.

CHAPTER 6 - A 0.8V ULTRA-LOW POWER CMOS EHI-APS IMAGER WITH CONTINUOUS ENERGY HARVESTING

This chapter presents the 4th generation energy harvesting and imaging (EHI) APS designed for 0.8V operation and extremely low power consumption with continuous time energy harvesting capability.

Even though energy harvesting improved considerably, power consumption reduction was limited in the 3rd generation EHI image sensor due to the power hungry analog readout channel. Solving the power consumption issues related to the readout channel has been the primary motivation while designing the 4th generation EHI sensor. A new breed of CMOS image sensor with fully digital readout is developed for this new image sensor to achieve ultra-low power consumption. The 4th generation EHI imager design achieves lower power consumption than any image sensor reported in the literature today.

N-well/p-sub junctions are utilized in the new pixel to harvest large power as in the 3rd generation EHI sensor. The micro solar cells and imaging photodiodes are built separately resulting in a continuous time energy harvesting operation unlike the previous EHI sensors.

The image sensor architecture and details of the imaging and energy harvesting mode blocks are described in detail in this chapter.

6.1 Image Sensor Architecture

Digital image sensor architectures such as pulse width modulation imagers [57], [59] and time based imagers [61], [85] do not consume static power and they can be operated at lower supply voltages compared to active pixel sensor (APS) imagers. However, the digital

pixels in these imagers are noisy and image quality is poor. Especially, switching noise due to in pixel comparator, charge injection and clock feed through affects the image quality. Reducing pixel to pixel variations and improving image quality requires complicated compensation schemes [61].

CMOS APS imagers have superior image quality. Therefore, low power APS imagers are preferred over the digital image sensors. Pixel to pixel variations can be eliminated easily by an analog subtraction operation known as by correlated double sampling (CDS) [86]. However, bulky sampling capacitors and other analog components in the analog readout channel of CMOS APS imagers consume power and silicon area. Especially, the operational amplifiers consume considerable static power. Moreover, these analog blocks limit the minimum imager supply voltage.

In a typical APS imager, pixel reset and signal values are stored on sample and hold capacitors and the stored values are buffered to the sample and hold capacitor of analog to digital converter (ADC). Typically, a global charge amplifier performs the buffering and CDS operations utilizing column sample and hold capacitors. Thus, global charge amplifier is the most active, fast, and power hungry block in the low-power APS imagers.

Proposed image sensor is a new breed of image sensor combining the benefits of digital and CMOS APS imagers. The high image quality is accomplished using the APS pixels and power consumption is reduced using a fully digital global readout channel. The proposed image sensor achieves low-power operation by eliminating the need of a global charge amplifier while achieving the required performance. The proposed readout channel is composed of eight (8) global SAR ADCs working in parallel. The new EHI imager has larger pixel array size of 96(H)x96(V), low-power readout electronics and a novel charge pump.

Pixel pitch is 14μm which is smaller than any other EHI pixel sizes. A low-leakage and mature 0.35μm 2P4M/3.3V CMOS process was also used for design and fabrication of the new EHI imager.

A considerable power is dissipated while charging and discharging column sample and hold capacitors during pixel readout. Therefore, not only the global charge amplifier but also these column capacitors are removed from the readout channel to further save imager power. Moreover, storing pixel source follower output on a sample and hold capacitor and then using this value as input to the ADC requires a voltage buffer which consumes considerable static power, too. Thus, new pixel series readout architecture is developed to directly sample pixel outputs into ADC. One pixel is sampled and converted at a time by an ADC. The pixels in a row are not readout or reset in parallel as in column parallel and column series image sensor architectures. Therefore, a standard 3 transistor APS pixel topology cannot be used in the proposed pixel series architecture. The new ASP pixel has row and column reset switches in series for X-Y addressing.

Block diagram of the proposed architecture is shown in Figure 6-1. The rows are addressed one by one through row decoder and row drivers. Once a row in the pixel array is selected, column decoder selects 8 consequent pixels in the row at a time. Selected pixels are readout in parallel and sampled by the global SAR ADCs. Subsequently, the selected pixels are reset. The reset values are readout and sampled by the SAR ADCs. SAR ADCs convert the difference between the pixel outputs sampled before and after pixel reset into 8 bit digital codes. The ADC performs correlated double sampling (CDS) of columns function as well as the quantization. The digital outputs of 8 ADCs are stored in 64 bit memory and shifted out sequentially.

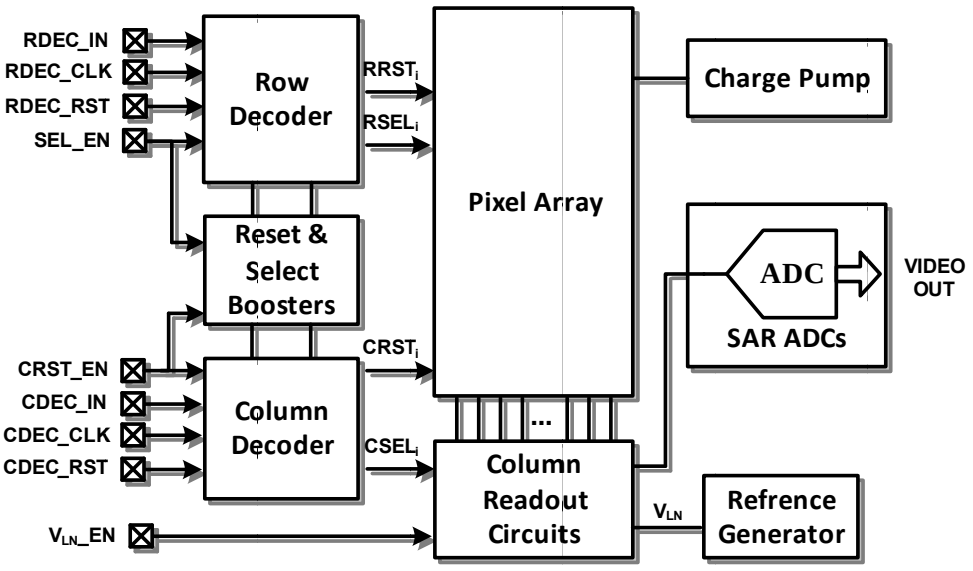


Figure 6-1. Block diagram of the 4th generation EHI imager with pixel series architecture.

The pixel source follower amplifiers and the reference generator are the only blocks consuming static power. The reference generator consumes 46nA on 0.8V supply voltage while the pixel source followers are biased with only 12nA current. The pixel source followers are turned on only during sampling of pixel signals. They are turned off during ADC operation.

6.2 The New EHI Pixel Circuits

6.2.1 Energy Harvesting Photodiode

No area was wasted for building energy harvesting photodiode in the sequential mode 1st, 2nd, and 3rd generation EHI sensors since the energy harvesting and imaging photodiodes were the same. The pixel structure in the 4th generation EHI imager has a dedicated energy harvesting photodiode. Energy harvesting and imaging operations run in parallel. Energy

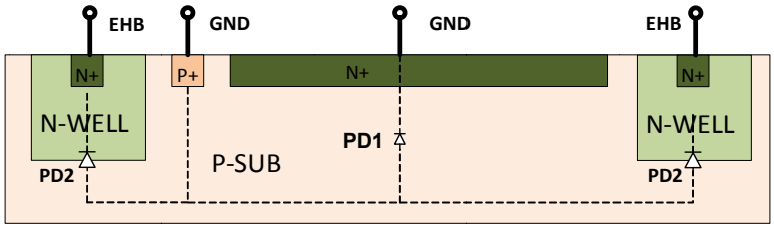


Figure 6-2. Cross sectional view of the photodiodes

harvesting photodiodes are implemented using minimum size n-wells placed around pixel structure as shown in Figure 6-2.

Certain areas are occupied by interconnects in all pixels. The energy harvesting n-wells are placed under these interconnect areas. Since the n-well layers take a little more area compared to interconnect layers, it decreases the pixel fill factor slightly. The metal layers used for interconnects are physically above the silicon surface, and photons incident with an angle can easily reach under these metal layers. Therefore, even though metal wires running over the energy harvesting photodiodes cause some shading and reduce the energy harvesting efficiency, this reduction is not very significant.

6.2.2 EHI Pixel Circuit

The 4th generation EHI pixel schematic is shown in Figure 6-3. The pixel is composed of imaging photodiode (PD1), energy harvesting photodiode (PD2) and four NMOS transistors (M1-M4). M1 and M2 are the series reset transistors used for resetting the floating diffusion (FD) node. M3 is the pixel source follower (PSF) and M4 is the row select transistors. Column reset switch M1 is added in series to the regular 3T reset transistor for selectively resetting the pixels in a row.

Since reset transistors M1 and M2 are NMOS transistors, the maximum voltage at the floating diffusion node (FD) is one threshold voltage below their gate voltage. Boosted clocks are needed for driving both row and column reset switches due to dynamic range concerns. Row and column reset clocks are boosted for resetting the photodiode to V_{DD}, and improving the signal dynamic range of the EHI pixel.

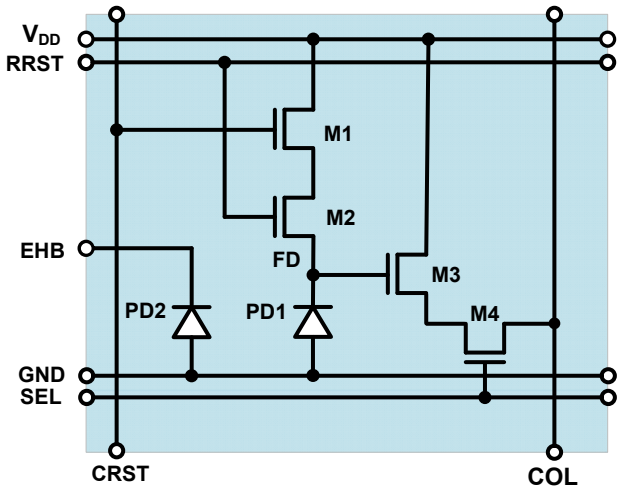


Figure 6-3. XY- Addressable Pixel Used in 4th Generation EHI Imager

6.3 Readout Channel

Analog readout channels in typical CMOS APS imagers consume significant power. It is composed of large sample and hold (S&H) capacitors and active analog components. Since pixel outputs are stored on column sample and hold capacitors, voltage buffers are needed to drive output pads or ADCs. If the on-chip ADC sample and hold capacitor is connected directly to the column S&H capacitor eliminating the voltage buffer, there will be a charge sharing and dynamic range will be reduced significantly. In case of off-chip analog to digital conversion, it is impossible to drive the analog output pad with the column capacitor without

an active voltage buffer. In early CMOS APS imagers pixel outputs at reset and signal levels were stored on two column level S&H capacitors and the voltages stored on these capacitors were buffered using two matched source followers [22], [86], [87]. Closed-loop global operational amplifiers were added to the readout channel to improve the performance of imagers. Source follower type voltage buffers add more attenuation to the readout channel since source follower gain is less than unity. Using a closed loop operational amplifier introduces gain to the readout channel and restores the conversion gain reduced due to readout channel losses and attenuation of source followers. Source followers also increase the FPN due to mismatches between the two source followers [88].

Charging the large column S&H capacitors used for storing the pixel outputs consume significant amount of power. The analog voltage buffers implemented with either the source followers or the operational amplifiers results in significant static power consumption. Especially the operational amplifier type charge amplifier(s) consume more power than any other component in the imager. Therefore, eliminating the amplifier is very critical for achieving low power operation.

The main challenge in removing the charge amplifier from the signal chain is the problem of driving the ADC S&H capacitors. Going back to source follower type voltage buffers is not an option in low voltage operation since signal range is already limited and introducing more attenuation to the readout channel will severely reduce image quality. Therefore, the need for a voltage buffer has to be eliminated completely for low-power operation. In the proposed structure the column S&H capacitors are removed and the reset and signal values are stored on the capacitive digital to analog converters (DACs) of the SAR

ADC directly. The ADC is driven by the pixel source followers and no voltage buffer is needed.

Removing column S&H and the global charge amplifier with programmable gain has a drawback of reduced signal chain gain which degrades the signal to noise ratio (SNR). The pixel source follower introduces approximately 15% to 25% attenuation on the signal path. Since the simplified signal path has no other sources of attenuation other than the passive losses, power savings justify this signal attenuation and the reduced SNR.

6.3.1 Column Readout Circuit and Timing

96 columns are sampled by 8 global SAR ADCs sequentially. Each ADC processes 12 columns. ADC #1 for example processes columns 0, 8, 16, 24, 32, 40, 48, 56, 64, 72, 80, 88, and 96. 96 column buses are connected to twelve (12) input multiplexers and multiplexer outputs are connected to column bias circuit and ADC inputs. The column multiplexers and the column bias current mirrors are shown in Figure 6-4. Column select signals (COL_SELi) are boosted for reducing the on resistance of the column select transistors.

Figure 6-5 shows the timing diagram for the 4th generation EHI imager readout. Row readout starts with selecting a row during which RRST signal is pulled high. Group of 8 columns on the selected row are also selected consequently. Row select and column select switches are turned on by applying SEL_EN signal. The pixel outputs are sampled by the 8 global ADC when the signal sample and hold signal (SHS) is applied.

After the signal readout, all selected pixels are reset. CRST signal is set high by applying RST_EN signal to reset the photodiode. CRST and RRST signals are boosted when RST_EN signal is applied. Pixel outputs right after the reset are sampled by the global ADCs also when the reset sample and hold signal (SHR) is applied.

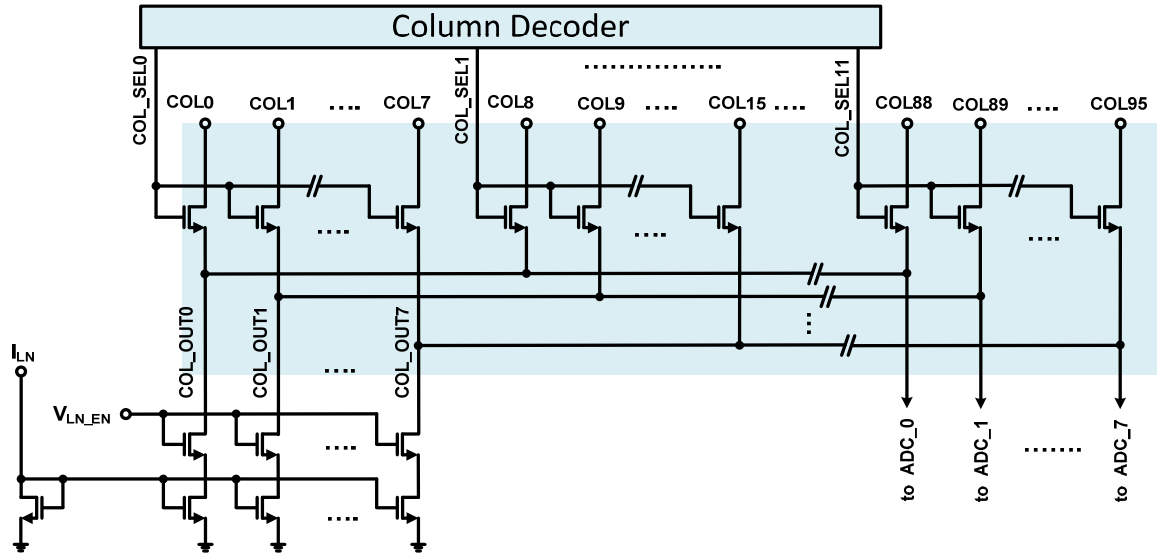


Figure 6-4. Column readout circuit schematic.

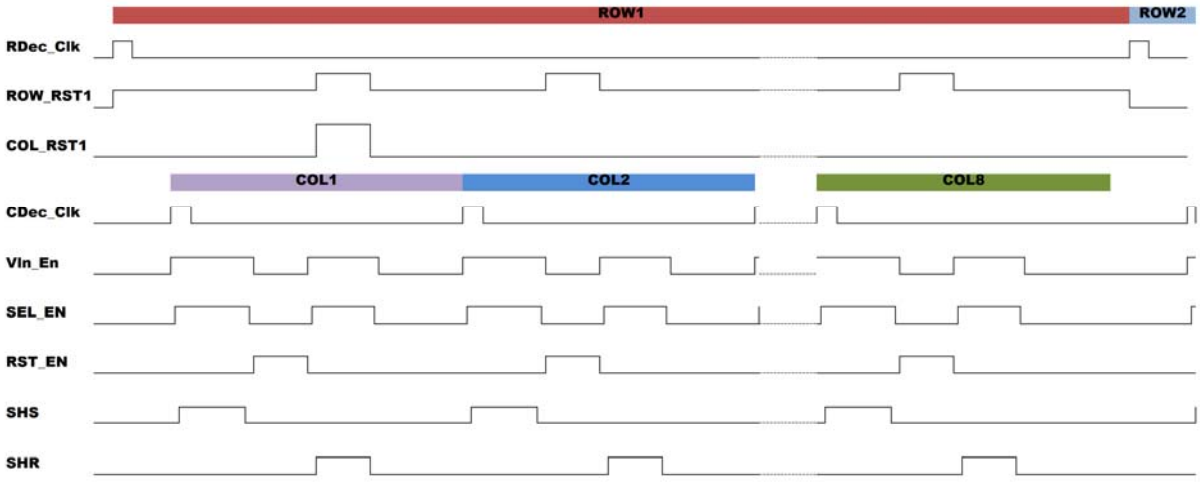


Figure 6-5. Timing diagram for the 4th generation EHI imager readout.

Once the pixel outputs are sampled, the SAR ADCs convert the difference between two sampled levels of pixel to digital word. The 8 bit content of the 8 global ADC totaling 64 bits are shifted out of the imager sequentially while the next 8 column of pixels are sampled by the ADC S&H circuits.

6.3.2 **Successive Approximation Register ADCs**

8-bit successive approximation register (SAR) ADCs are used for sampling pixel voltages before and after pixel reset and converting the difference between the two levels into a digital code. 8 global SAR ADCs working in parallel process the selected columns. The outputs of the ADCs are stored on a 64 bit shift register and shifted out serially. Block diagram of 8 global SAR ADCs are shown in Figure 6-6.

A novel single-ended 8-bit SAR ADC consuming ultra-low power is used in the 4th generation EHI imager. The SAR ADC samples the pixel signal level onto the first binary weighted capacitive DAC when sample and hold signal (SHS) is pulsed. After the Pixel reset, the sample and hold reset (SHR) is pulsed high and the pixel reset level is sampled onto the other capacitive DAC. The effective input (V_{eff}) of the SAR ADC is the difference between the two sampled signals. SAR ADC uses a single reference voltage (V_{ref}) and can digitize effective inputs in the range of 0 to $2V_{ref}$ using a novel switching method.

6.3.2.1 *Single-Ended Correlated Double Sampling (CDS) SAR ADC Circuit*

Circuit diagram of the proposed novel single-ended SAR ADC that is capable of performing correlated double sampling operation is shown in Figure 6-7. The SAR ADC is composed of two binary-weighted capacitive digital to analog converters (DACs), a comparator and a SAR logic controlling the DAC switches.

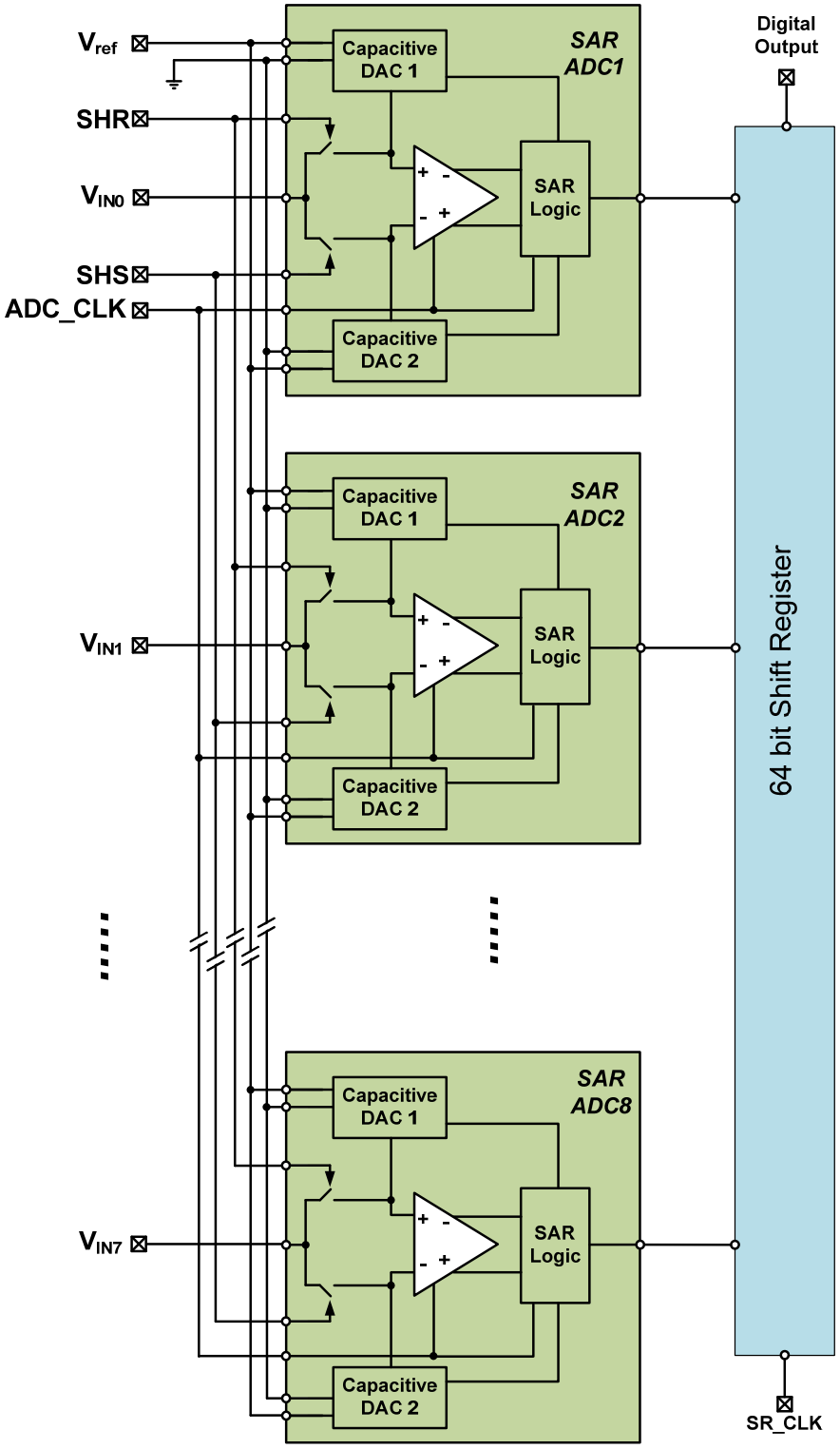


Figure 6-6. Block diagram of the successive approximation register (SAR) ADCs in the imager.

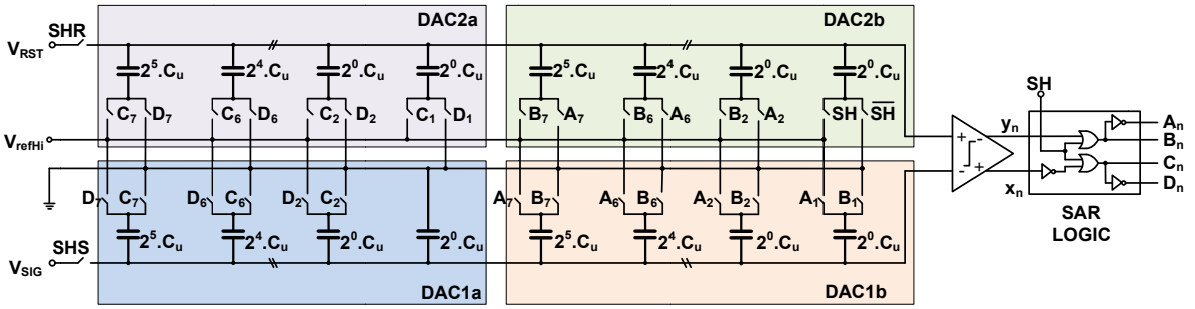


Figure 6-7. Single-ended correlated double sampling (CDS) SAR ADC schematic.

Each capacitive DAC has a total of 128 unit capacitor ($128C_u$). Each DAC has 2 symmetric capacitive sub-DACs with a total capacitance of 64 unit capacitors ($64C_u$) each. Same energy efficient dynamic comparator used in 3rd generation EHI image sensor is used in the SAR ADC. The SAR ADC has a novel switching technique that optimizes the dynamic power consumption.

6.3.2.2 *Proposed SAR ADC Switching Method*

In a conventional SAR ADC the reference voltage is equal to the maximum input range of the ADC. The novel switching method used in this SAR ADC reduces the reference voltage to the half of the input voltage range. Single ended SAR ADCs using half the reference voltage have been proposed before [89]. The switching method in the EHI image sensor is a relatively simple switching method optimized for correlated double sampling of pixel outputs and minimum switching power consumption.

Power consumed to switch a capacitor from ground to V_{ref} at a certain switching frequency (f_{sw}) is given by (6-1).

$$P = f_{sw} \cdot C \cdot V_{ref}^2 \tag{6-1}$$

The power dissipated for switching the capacitive DAC reduces to a quarter of the power consumed by conventional switching method when V_{ref} is reduced to one half.

The ADC samples the pixel output (V_{Sig}) on the top plates of binary-weighted capacitors in capacitive DAC1. Bottom plates are grounded during signal sampling. The pixel output after pixel reset (V_{Rst}) is sampled on the top plates of binary-weighted capacitors in capacitive DAC2. Bottom plates are connected to V_{ref} during reset sampling. Once SHR is completed, bottom plates of second sub-DAC in DAC2 (DAC2b) are switched to ground and bottom plates of second sub-DAC in DAC1 (DAC1b) are switched to V_{ref}.

The effective input of the ADC is compared to V_{ref} and most significant bit (MSB) is determined. Inputs of the comparator at this instance are given by (6-2) and (6-3).

$$V_p = V_{Rst} - \frac{V_{ref}}{2} \tag{6-2}$$

$$V_n = V_{Sig} + \frac{V_{ref}}{2} \tag{6-3}$$

$32C_u$ capacitors in DAC2a and DAC1a are switched if MSB is 1. $32C_u$ capacitors in DAC2b and DAC1b are switched if MSB is 0. $16C_u$ capacitors in DAC2a and DAC1a are switched if 7^h bit is 1. $16C_u$ capacitors in DAC2b and DAC1b are switched if 7^{th} bit is 0. Switching goes on until LSB is determined. Comparator inputs for MSB comparison are preset when SHR and SHS signals go low. Therefore, SAR ADC completes conversion in 7 clock cycles after the SHR and SHS go low. Details of the novel switching are explained for 3 bit SAR ADC example in Figure 6-8.

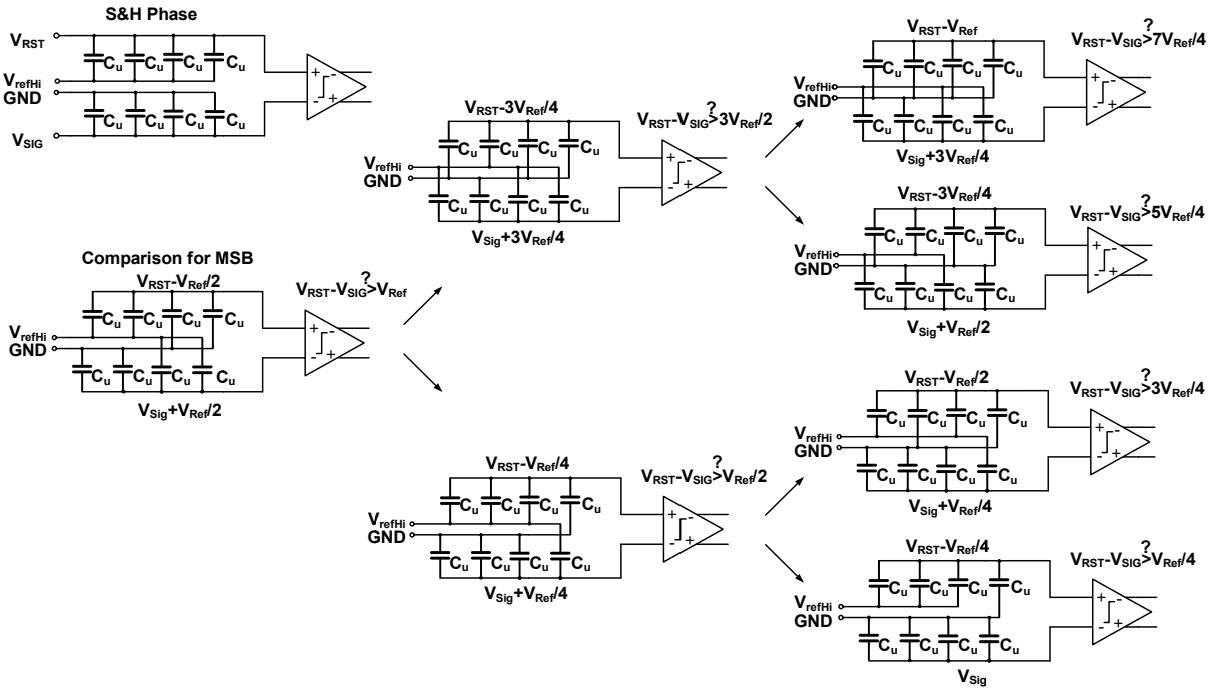


Figure 6-8. Flowchart of the proposed novel switching method in a 3-bit SAR ADC example.

6.3.3 **Reference Generator Circuit**

A simpler version of the current reference circuit used in 3rd generation EHI imager is used for generating the on-chip bias current for the pixel source followers. The reference generator circuit is shown in Figure 6-9. Since the only circuit requiring static bias current is column source followers, reference current requirements are relaxed in 4th generation imager.

The column bias current I_{LN} is mirrored from PMOS transistor M4 with a programmable PMOS current DAC in order to avoid current consumption in unnecessary branches. Therefore, cascode transistors M1b and M2b are removed from the original design.

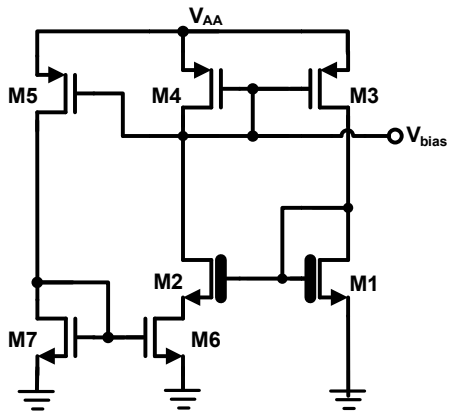


Figure 6-9. Nano-watt, supply independent reference current generator circuit.

6.3.4 **Current Steering DAC**

The current generated by the reference generator is mirrored to column current sources. Columns are biased with the minimum bias current while capturing good quality images with low fixed pattern noise. The bias current is set via 7 bit programmable current steering DAC as shown in Figure 6-10.

The current steering DAC control code is stored on a scan chain. DAC output increases 12.5nA when control code increases 1 bit. The current range is from 0A to 1587.5 nA.

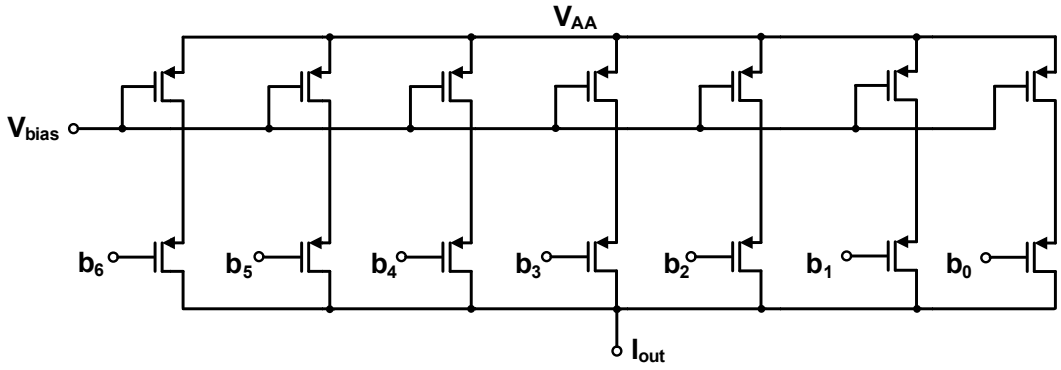


Figure 6-10. 7-bit programmable current steering DAC.

6.4 Digital Building Blocks

6.4.1 Row Select Logic

The row select logic in the EHI sensor is composed of a chain of 96 shift registers as shown in Figure 6-11. The shift registers are controlled by non-overlapping clocks ϕ_1 and ϕ_2. Input of the shift registers are moved to their output at every rising edge of ϕ_1. At the beginning of frame readout, all shift registers in the row addressing circuit are reset. The outputs of all shift registers are low. The next row is selected at each rising clock edge.

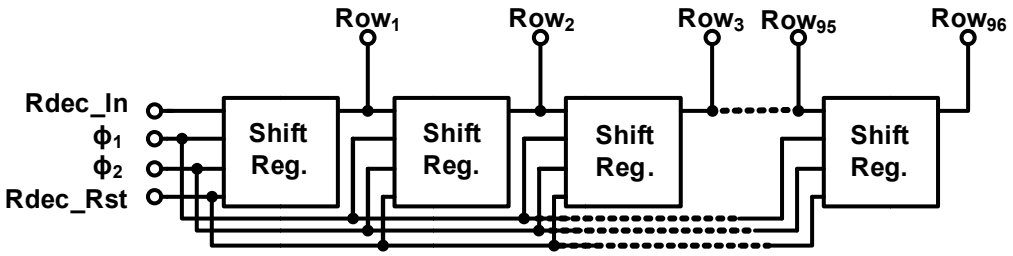


Figure 6-11. Shift register based row addressing circuit.

6.4.2 Row Driver

The row driver gets the SEL_EN signal and shift register output Row$_i$ as input and generates RSEL$_i$ and RRST$_i$ signals. RSEL$_i$ and RRST$_i$ signals are low unless the individual row is selected by the shift register. Row reset and select signals are boosted by level shifters. The supply voltage of the level shifters is boosted by the reset and select boosters.

Row reset signal has to be boosted in order to pull the photodiode FD node to V_{DD} when pixel is reset. The row reset switch is in series with column reset switch. The photodiode is reset only when column reset and row reset signals are both high. Therefore,

row reset signal needs to be boosted only when column reset signal is boosted. Therefore, a single reset booster is used for both row reset and column reset signals.

The voltage drop across the row select transistor decreases when the select signal is boosted. The pixel is readout when row select and column select switches are both on. Therefore, row select and column reset signals are boosted by same select booster.

6.4.3 Column Select Logic

The column select logic is a chain of 12 back to back shift registers as shown in Figure 6-12. The shift registers are identical to the shift registers in the row select logic. At the beginning of each row, all shift registers in column addressing circuit are reset. Column shift registers operate exactly like the row shift registers and next column is selected at each clock edge.

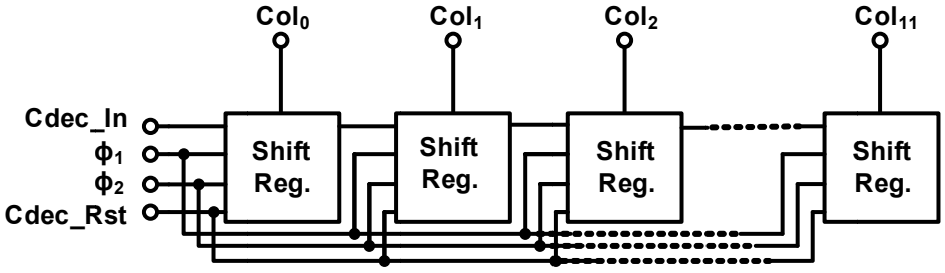


Figure 6-12. Shift register based column addressing circuit

6.4.4 Column Driver

The column driver gets the select enable (*SEL_EN*) and reset enable (*RST_EN*) signals and shift register output Col_i as input and generates column select ($CSEL_i$) and column reset

($CRST_i$) signals. $CSEL_i$ and $CRST_i$ signals are low unless the individual column is selected by the shift register.

Column reset and column select signals are boosted by level shifters. The supply voltage of the level shifters is boosted by the global reset and select boosters.

6.4.5 Select and Reset Boosters

The same select booster used in 3rd generation EHI sensor is used for boosting the select and reset signals in the 4th generation EHI sensor. Figure 6-13 shows the schematic of the booster circuit. When *SEL_EN* signal is high, V_{DDB}_SEL is equal to $2V_{DD}$ for the unloaded select booster. Reset booster circuit is identical to the select booster circuit. When *RST_EN* signal is high, V_{DDB}_RST is equal to $2V_{DD}$ for the unloaded reset booster.

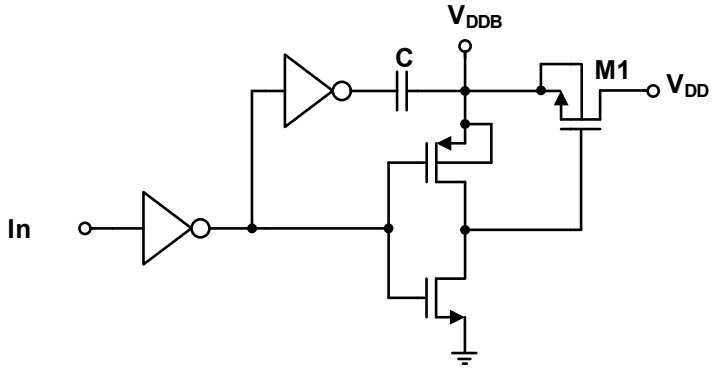


Figure 6-13. Booster circuit for select and reset boosting

6.5 Energy Harvesting Mode Circuits and Operation

Energy harvesting circuits in 4th generation EHI sensor are very simple. Imaging and energy harvesting photodiodes are built independent of each other. Therefore, imaging and energy harvesting modes run in parallel. There is no need to reconfigure pixels between imaging and energy harvesting modes. All the energy harvesting photodiodes are connected to the energy harvesting bus (EHB) directly. The generated energy is stored on a storage capacitor (C1). The energy harvesting circuits are shown in Figure 6-18. Energy much larger than the energy needed to run the imager is continuously harvested. The circuit can operate free of batteries autonomously.

6.5.1 Energy Harvesting Photodiodes

Depletion regions formed at the sidewalls of photodiodes results in a total junction area larger than the physical area of the photodiode. This phenomenon is known as edge effect and it becomes very significant for small photodiodes, [25], [90]–[97]. Total junction area of an n-well/p-sub junction photodiode is given by (6-4).

$$A_T = A_L + A_V = A_L + P_J \cdot D_J \tag{6-4}$$

Total area is the sum of the lateral (A_L) and the sidewall junction (A_V) areas of the n-well. Sidewall junction area is the product of n-well junction depth (D_J) and the perimeter (P_J). Placing multiple minimum size n-wells in a given lateral area rather than a single n-well covering the whole area results in a larger total junction area and energy collection centers since the n-well depth is larger.

The total area covered by the 96x96 4th generation EHI pixels is 1.83 mm^2. 0.72 mm^2 of the total pixel array is used for the energy harvesting photodiodes. The actual lateral area of

the n-wells is 0.58 mm^2 and the rest is wasted because of the distance requirements between two n-well layers. The total perimeter of the n-wells is 649.5mm. Considering the n-well junction depth and sidewalls, total n-well junction area available for energy harvesting is 2.36 mm^2. [1] If same size pixel were built with stacked photodiodes as in 3rd generation EHI sensor, the n-well/p-substrate photodiodes would occupy total area of 1.02 mm^2 and have a total perimeter of 388 mm. The resulting total junction area would be 2.1 mm^2. Therefore, a larger junction area is achieved in a small lateral silicon area by maximizing the junction perimeter in 4th generation EHI imager.

6.5.2 Charge Pump

The Energy stored on C1 is processed by a charge pump and converted to a positive usable voltage. The charge pump output is stored on the storage capacitor C2. Same polarity inverting charge pump is used as in 3rd generation EHI sensor.

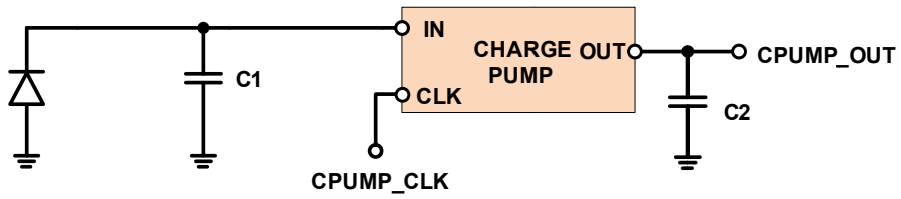


Figure 6-14. Energy harvesting mode circuits

[1] Sidewall depth used for the junction area calculations is extracted from the diode parameters for the manufacturing process.

6.6 Summary

The prototype 4th generation EHI sensor was presented in detail. Imager has a completely digital readout channel. Digital circuits can operate with lower supply voltages compared to analog circuits. The ultra-low power imager runs with 0.8 V supply voltage despite the high threshold voltages.

Removal of analog readout channel reduces the imager power consumes significantly. Imager noise is very low and image quality is very good despite removal of the amplifier from the signal chain.

The energy harvesting circuits of the image sensor were also presented in detail. Pixel structure allowing continuous energy harvesting and imaging is presented in detail. Polarity inverting charge pump for converting the harvested energy into usable supply voltage was also presented.

CHAPTER 7 - MEASUREMENT RESULTS OF THE EHI IMAGERS

Test and measurement results for the 3rd and 4th generation EHI sensors are presented in this chapter. First, imaging mode performance of the 3rd generation EHI sensor is presented and images captured are provided. The energy harvested by the new sequential EHI pixels in energy harvesting mode for varying load currents and light levels are presented next. Following, the novel charge pump circuit measurements including efficiency are presented. Second, imaging and energy harvesting mode performances of the 4th generation EHI sensor is presented and captured test images are provided. Imaging performance of the new 3rd and 4th generation EHI imager topologies are compared with the previously reported imagers. The main comparison merits are power consumption and image quality. Energy harvesting capacity of the four generation EHI sensors are compared among them and similar imagers in literature that have energy harvesting capability.

7.1 3rd Generation EHI Sensor Measurements

7.1.1 Sensor Implementation

3rd generation EHI sensor is built in a mature 0.35μm 3.3V CMOS opto electronic manufacturing process that has 2 poly-silicon and 4 metal layers (2P4M). Threshold voltages for NMOS and PMOS transistors are +0.45V and -0.7V, respectively. The micrograph of the 3rd generation EHI sensor is shown in Figure 7-1. Physical size of image sensor core is about 1.5mm x 1.2mm. Total chip size together with the pad frame is 2.2mm x 1.6mm. Chip is packaged in 68 pin ceramic leadless chip carrier (LCC68).

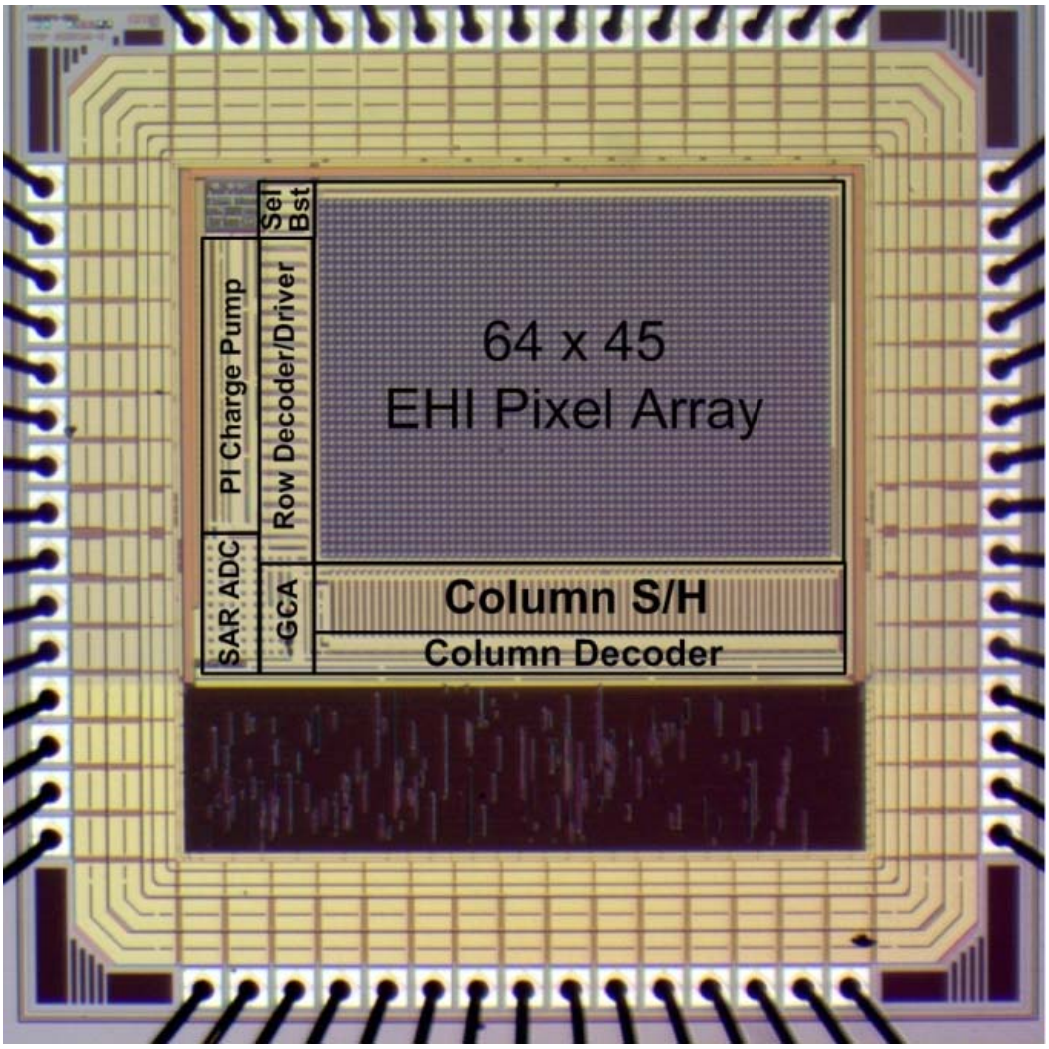


Figure 7-1. Micrograph of the 3rd generation EHI image sensor fabricated in 0.35μm 2P4M CMOS OPTO process.

7.1.2 3rd Generation EHI Sensor Imaging Mode Measurements

The EHI sensor is designed to operate at low supply voltage for minimal power consumption. The high threshold voltages of transistors in selected CMOS process impede aggressively lowering the supply voltage. Digital circuit blocks and SAR ADC can operate at supply voltages lower than 1V. The image quality is acceptable at a minimum supply voltage of 1V. Table 7-1 summarizes the EHI imager chip specifications.

Table 7-1. 3rd Generation EHI imager specifications.

PARAMETER	SPECIFICATIONS
Process Technology	0.35μm Technology
Pixel Pitch	18 μm x 18 μm
Pixel Type	EHI type photodiode APS
Pixel Fill Factor	65% for PD1; 42.5% for PD2
Pixel Array Resolution	64(H) x 45(V)
Imager Die Size	1.5mm x 1.2mm
ADC Type	8-bit SAR ADC
Supply Voltage	1.0 – 3.3V
Maximum Frame Rate	21 fps
Sensor Output Format	8-bit parallel (digital), 1 channel (analog)

Image quality of 3rd generation EHI sensor is characterized with noise measurements. Imager noise is measured at 1V and 1.2V power supply voltages at 8 frames per second (fps). Noise measurements are summarized in Table 7-2. All measured noise levels are less than 0.5% of the full scale, thus imager noise could not be observed by the human eye.

Table 7-2. Noise measurements for 1V and 1.2V supply voltage at 8 fps.

PARAMETER	MEASUREMENT RESULTS	
Supply Voltage	1.0 V	1.2 V
Temporal Noise (Dark)	0.70 LSB	0.50 LSB
Dark Signal Non-Uniformity (DSNU)	1.20 LSB / 0.47%	0.86 LSB / 0.34%
Pixel FPN (Dark)	1.17 LSB / 0.46%	0.84 LSB / 0.33%
Column FPN (Dark)	0.15 LSB / 0.060%	0.11 LSB / 0.043%
Row FPN (Dark)	0.24 LSB / 0.092%	0.17 LSB / 0.066%
Temporal Noise (Half Well)	1.21 LSB	0.95 LSB
Photo Response Non-Uniformity (PRNU) (Half Well)	0.78 LSB / 0.30%	0.57 LSB / 0.22%
Pixel FPN (Half Well)	0.73 LSB / 0.29%	0.52 LSB / 0.20%
Column FPN (Half Well)	0.20 LSB / 0.080%	0.18 LSB / 0.071%
Row FPN (Half Well)	0.17 LSB / 0.068%	0.12 LSB / 0.049%

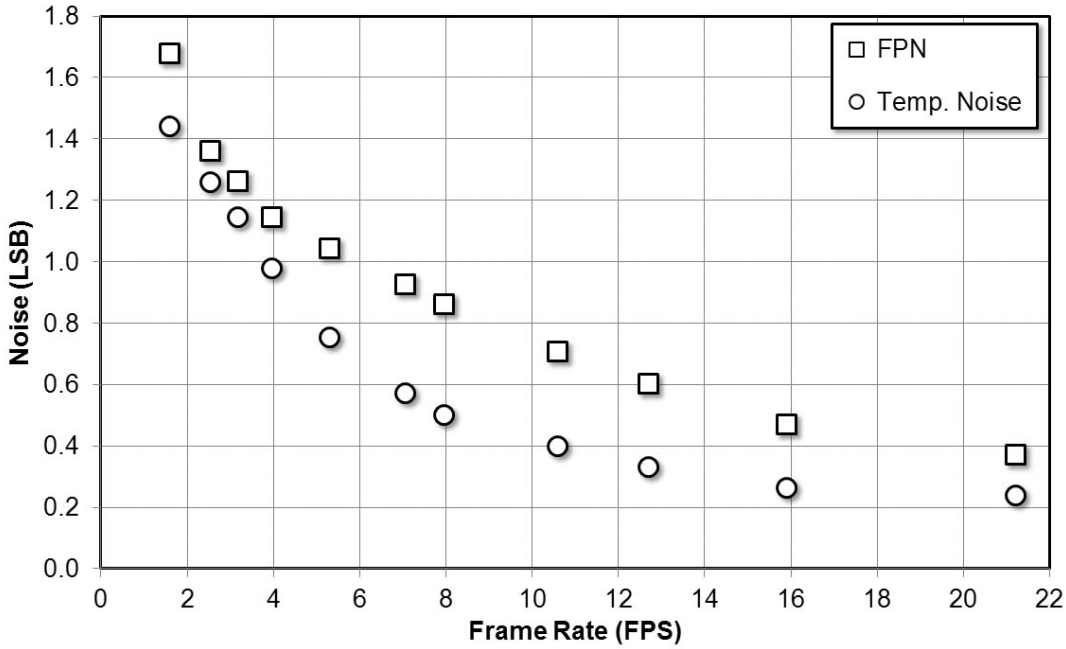


Figure 7-2. Dark signal non-uniformity and dark temporal noise variation with frame rates.

The measured temporal and fixed pattern noise of the image sensor decrease with increasing frame rate. Figure 7-2 shows the measured dark signal non-uniformity (DSNU) which is the fixed pattern noise (FPN) measured in dark and temporal noise for different frame rates at 1.2V supply voltage. As expected, both noises are reduced because as integration time decreases (or frame rate increases) the dark current accumulation decreases and resulting dark current shot noise reduce accordingly.

Photo response non-uniformity (PRNU) is measured at half full-well illumination level. Figure 7-3 shows the measured photo response of the image sensor, temporal noise, and photo response non-uniformity (PRNU) as a function of light exposure at 8 fps and 1.2V supply voltage. Pixel photodiode characteristics including conversion gain could be extracted from the temporal noise measurement. Imager signal chain is very linear and produces low-noise images.

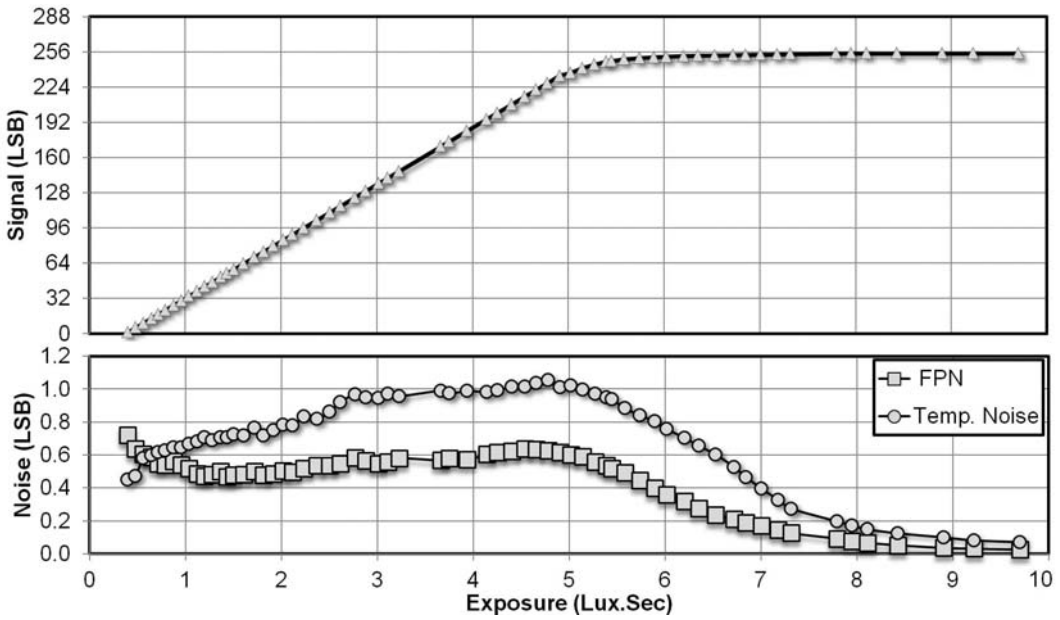


Figure 7-3. Measured photo response curve and noise performance at 8fps and 1.2V supply.

The image sensor consumes only 9 μW at 21.2 frames per second (fps) at lower supply voltage of 1V that good images could still be produces. This measured figure includes the whole chip power consumption counting in pixel array, row and column select logic, row driver, analog column readout, SAR ADC, reference generator and pad frame. Measured full-chip power consumptions of the 3rd generation EHI sensor at 1.6 fps and 21.2 fps for 1.0V power supply are summarized in Table 7-3.

Table 7-3. Measured low and high frame rate power consumptions and figure of merits.

PARAMETER	MEASUREMENTS	
Frame Rate (fps)	1.6	21.2
Power Consumption (Whole Chip) (μW)	0.92	9.04
Power Consumption (Pixel Array Chip) (μW)	0.034	0.202
Figure of Merit (Whole Chip) (pJ/frame*pixel)	200.9	148.1
Figure of Merit (Pixel Array) (pJ/frame*pixel)	7.38	3.32

Power consumption increases with increasing frame rate for two reasons. First, dynamic power consumption of digital circuits increases with increased clock frequency. Second, slew rate and settling time of the OPAMP in the global charge amplifier has to be increases for higher frame rates which could be achieved only by increasing the bias current of the OPAMP or increasing the power consumption. Figure 7-4 shows the measured power consumption and energy figure of merit (eFOM) as a function of frame rate for 1.0V supply voltage.

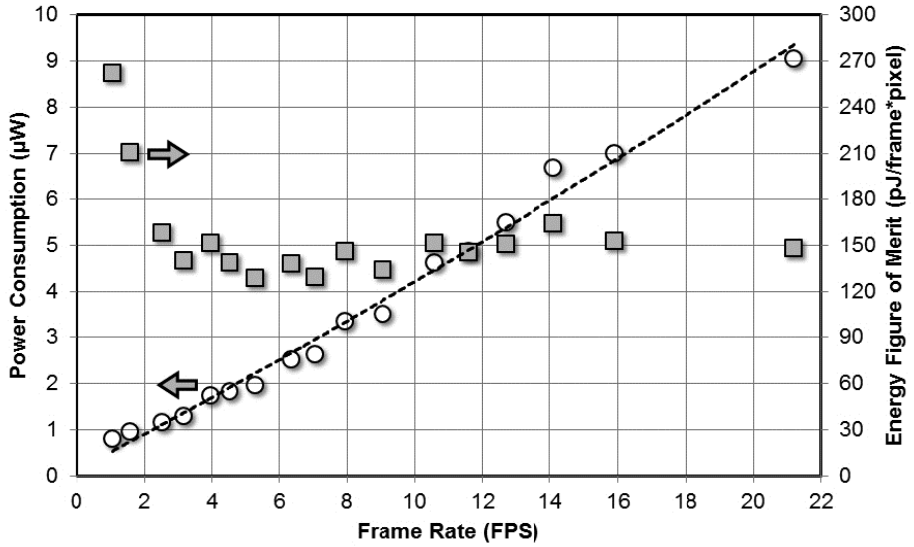


Figure 7-4. Measured whole chip power consumption and energy figure of merit as a function of frame rate at 1.0V supply voltage.

7.1.3 **Captured Test Images**

Images captured by the 3rd generation sensor at different frame rates for 1V and 1.2V power supply voltages are shown in Figure 7-5 and Figure 7-6, respectively. Image quality improves with increased supply voltages, and it could be observed on captured images by a human eye. Lower the frame rate worst the quality gets due to the increased DSNU.

(a)

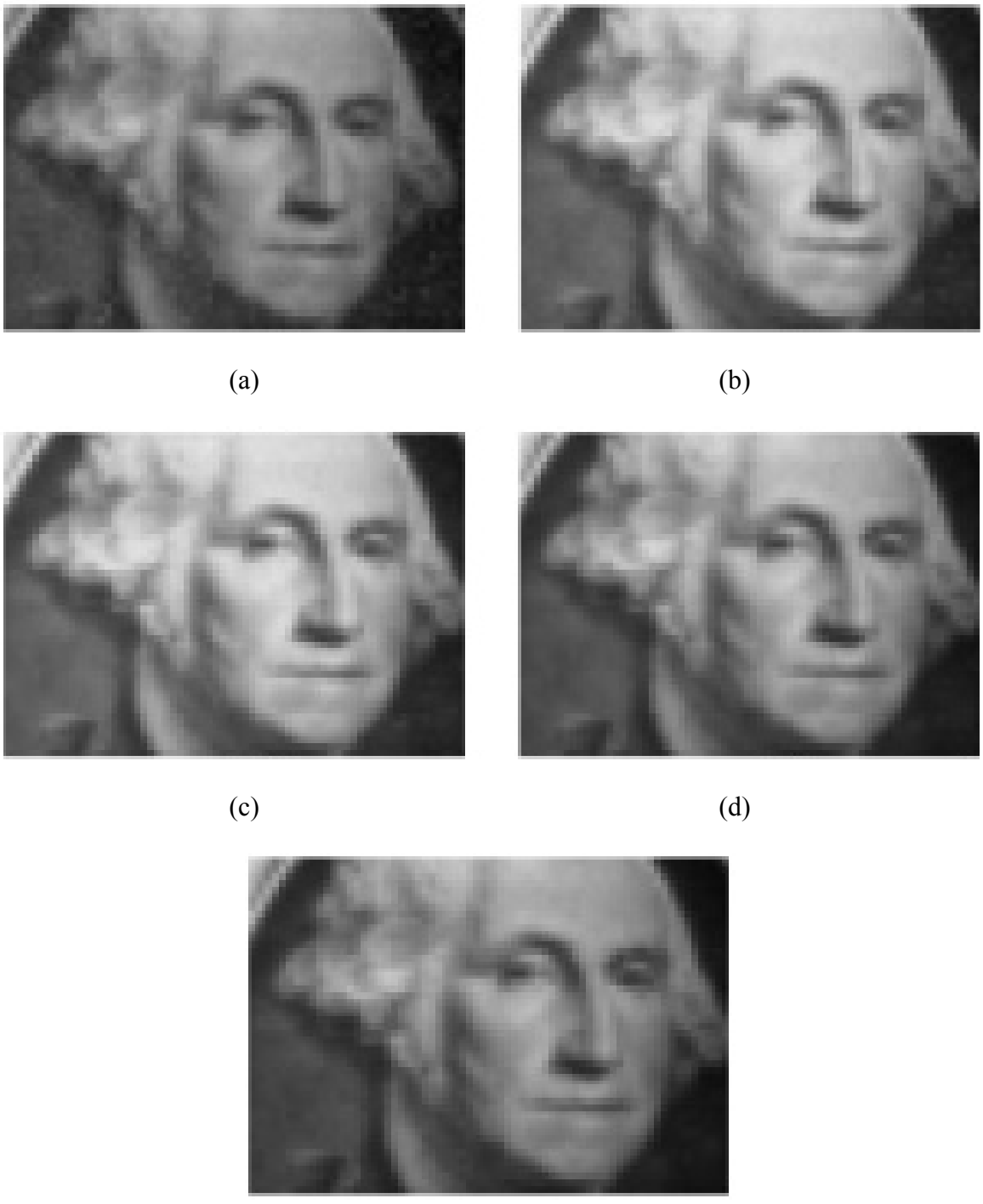
(b)

(c)

(d)

(e)

Figure 7-5. Test images capture at different frame rates and 1.0V power supply voltage. (a) 2.5 fps (b) 5.3 fps (c) 8 fps (d) 12.7 fps (e) 21.2 fps



(a) (b)

(c) (d)

(e)

Figure 7-6. Test images capture at different frame rates and 1.2V power supply voltage. (a) 2.5 fps (b) 5.3 fps (c) 8 fps (d) 12.7 fps (e) 21.2 fps

7.1.4 3rd Generation EHI Sensor Energy Harvesting Mode Measurements

Total 2880 pixels occupy an IC die area of 0.93 mm^2. Current-voltage-power (IVP) characteristics of the EHI pixel array in energy harvesting mode was measured under different illumination conditions as shown in Figure 7-7. During measurement, on-chip charge pump circuitry was turned off and an external variable load resistor (R_L) is connected directly to the energy harvesting bus (EHB). Load resistor is varied from low (~0Ω) to high impedance (5MΩ) forcing the micro solar cells in the EHI pixels to short and open circuit conditions. At the maximum power point (MPP) operation, EHI pixel array delivers 114.5μA current while the load voltage is 402mV delivering a total power of 45.97μW for 57,000lux illumination. Delivered power drops to 16.75μW and 4.18μW for 20,000lux and 5,000lux illuminations, respectively.

Charge pump efficiency was measured by operating the charge pump at different clock frequencies under constant loading condition. Load resistor (R_L) is picked to keep the solar cell array near MPP. Charge pump efficiency is calculated as the ratio of its output power and input power. Overall efficiency of energy harvesting structures in the EHI pixels is calculated by finding the ratio between output power and maximum power output of the solar cell array. Maximum efficiency point of charge pump and maximum power point of micro solar cells in the EHI pixel array do not exactly overlap. Therefore, the overall efficiency of the energy harvesting circuits is reduced. For this measurement, a 1000 μF storage capacitor was used. Focal plane illumination level was set to 39KLux. Charge pump efficiency of 75% was achieved while delivering 16.65 μA at 1.26V output voltage. The overall efficiency of energy harvesting structure is 65.3% as shown on Figure 7-8. The unloaded output voltage of the novel charge pump is 1.85V.

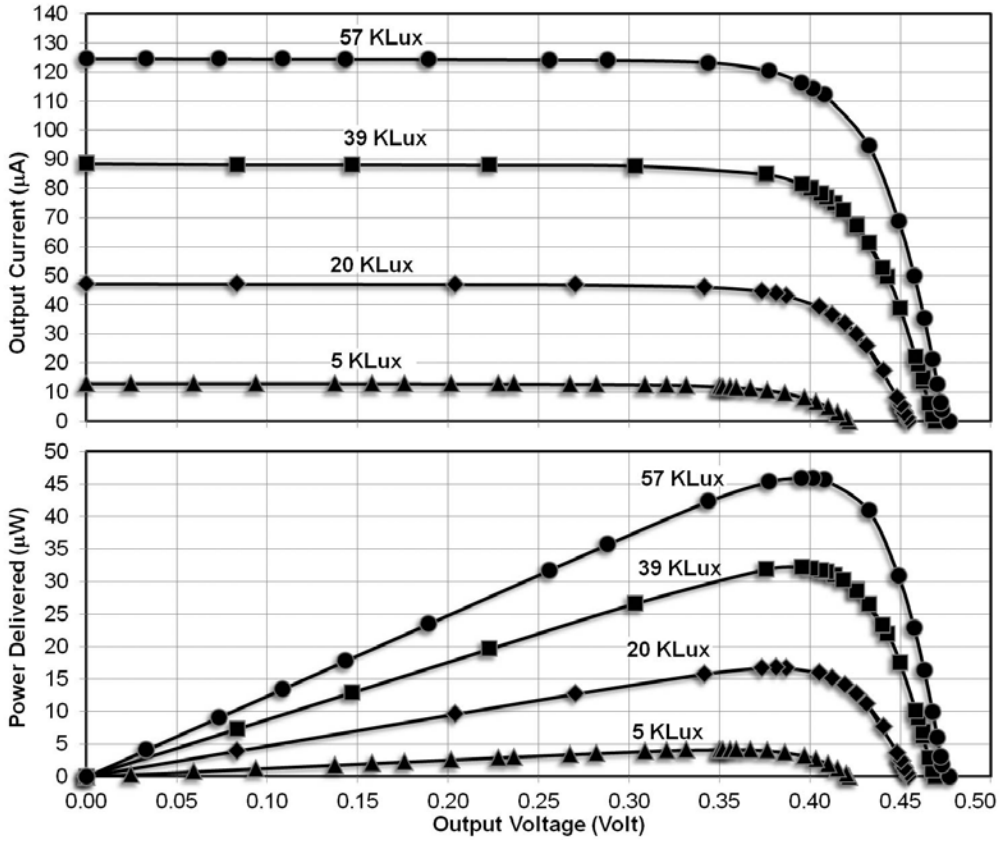


Figure 7-7. Measured current-voltage-power (IVP) curves of the 3rd generation EHI pixel array at various illumination levels.

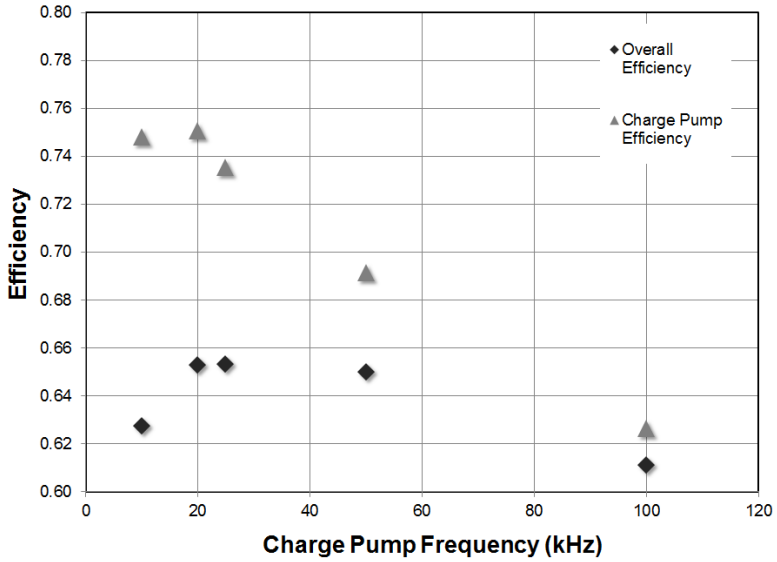


Figure 7-8. Charge pump input output efficiency and overall energy harvesting efficiency

7.2 4th Generation EHI Sensor Measurements

7.2.1 Sensor Implementation

4th generation sensor is built in the same CMOS process as the 3rd generation EHI imager. The micrograph of the 4th generation EHI sensor is shown in Figure 7-9. Physical size of image sensor core is about 1.7 mm x 1.6 mm. Total chip size together with the pad frame is 2.5 mm x 2.1 mm. Chip is packaged in 84 pin grid array package (PGA84).

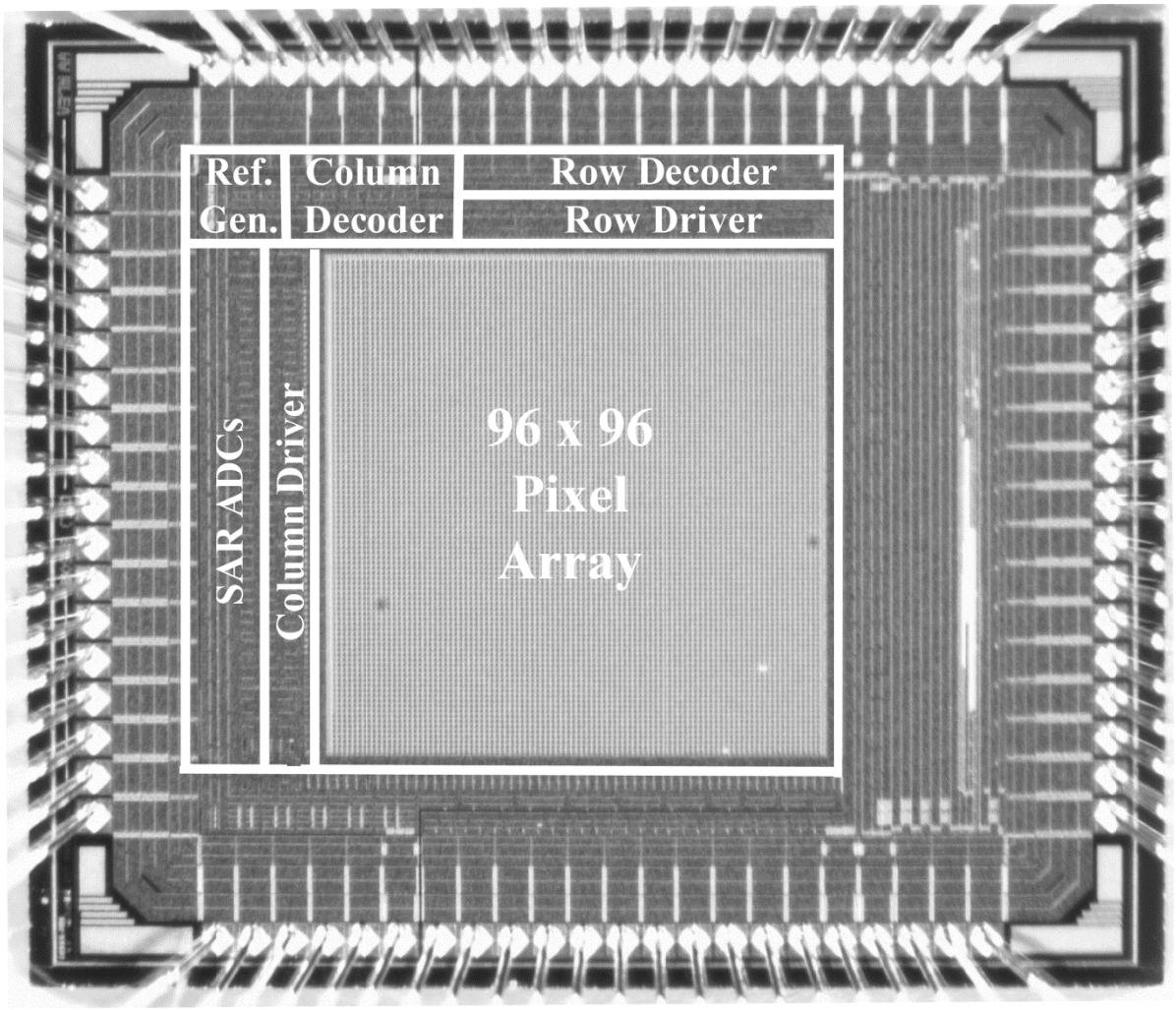


Figure 7-9. Micrograph of the 4th generation EHI image sensor fabricated in 0.35μm 2P4M CMOS OPTO process.

.

7.2.2 4th Generation EHI Sensor Imaging Mode Measurements

The EHI sensor is designed to operate at low supply voltage for minimal power consumption. Despite high threshold voltages of transistor in selected CMOS process, supply voltage of the EHI imager could be reduced down to 0.8V. This is achieved by the new readout architecture removing OPAMP based charge amplifier from the analog signal chain/ Test chip specifications are summarized in Table 7-4.

Table 7-4. 4th Generation EHI imager specifications.

PARAMETER	SPECIFICATIONS
Process Technology	0.35μm, 2P4M CMOS Optoelectronics
Pixel Pitch	14 μm x 14 μm
Pixel Type	EHI type photodiode APS
Pixel Fill Factor	30%
Pixel Array Resolution	96(H) x 96(V)
Imager Die Size	1.7mm x 1.6mm
ADC Type	8-bit SAR ADC
Supply Voltage	0.8 – 3.3V
Maximum Frame Rate	22.4 fps
Sensor Output Format	8-bit series (digital)

Image quality of 4rd generation EHI sensor is characterized with noise measurements. Imager noise is measured at 0.8V and 1.2V power supply voltages at 11.2 frames per second (fps). Noise measurements are summarized in Table 7-5. All measured noise levels are less than 0.5% of the full scale, thus imager noise could not be observed by the human eye.

Table 7-5. Noise measurements for 0.8V, 1.2V and 2.0V supply voltage at 11.2 fps.

PARAMETER	MEASUREMENT RESULTS		
Supply Voltage	0.8 V	1.2 V	2.0 V
Temporal Noise (Dark)	0.20 LSB	0.19 LSB	0.09 LSB
Dark Signal Non-Uniformity (DSNU)	0.25 LSB / 0.097%	0.20 LSB / 0.078%	0.11 LSB / 0.042%
Pixel FPN (Dark)	0.062 LSB / 0.024%	0.037 LSB / 0.015%	0.018 LSB / 0.007%
Column FPN (Dark)	0.24 LSB / 0.094%	0.20 LSB / 0.076%	0.10 LSB / 0.041%
Row FPN (Dark)	0.010 LSB / 0.004%	0.011 LSB / 0.004%	0.010 LSB / 0.004%
Temporal Noise (Half Well)	0.79 LSB	0.51 LSB	0.32 LSB
Photo Response Non-Uniformity (PRNU) (Half Well)	0.85 LSB / 0.33%	0.62 LSB / 0.24%	0.42 LSB / 0.17%
Pixel FPN (Half Well)	0.74 LSB / 0.29%	0.52 LSB / 0.20%	0.33 LSB / 0.13%
Column FPN (Half Well)	0.37 LSB / 0.014%	0.29 LSB / 0.11%	0.19 LSB / 0.076%
Row FPN (Half Well)	0.19 LSB / 0.075%	0.17 LSB / 0.065%	0.18 LSB / 0.071%

Noise of the imager is observed to decrease as supply voltage increases as shown in Figure 7-10. Main reason for this is the decreased pixel dynamic range, reduced ADC input voltage range and subthreshold operation of transistors.

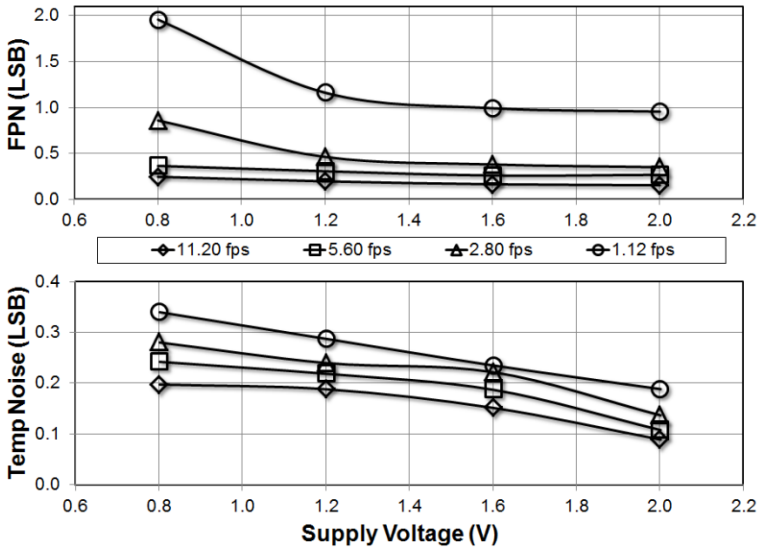


Figure 7-10. Measured FPN and temporal noise variations for different supply voltages and frame rates in dark.

The image sensor noise is observed to decrease with increasing frame rate. Figure 7-11 shows how dark signal non-uniformity and temporal noise changes with frame rate at 0.8V, 1.2V, 1.6V, and 2.0V supply voltages.

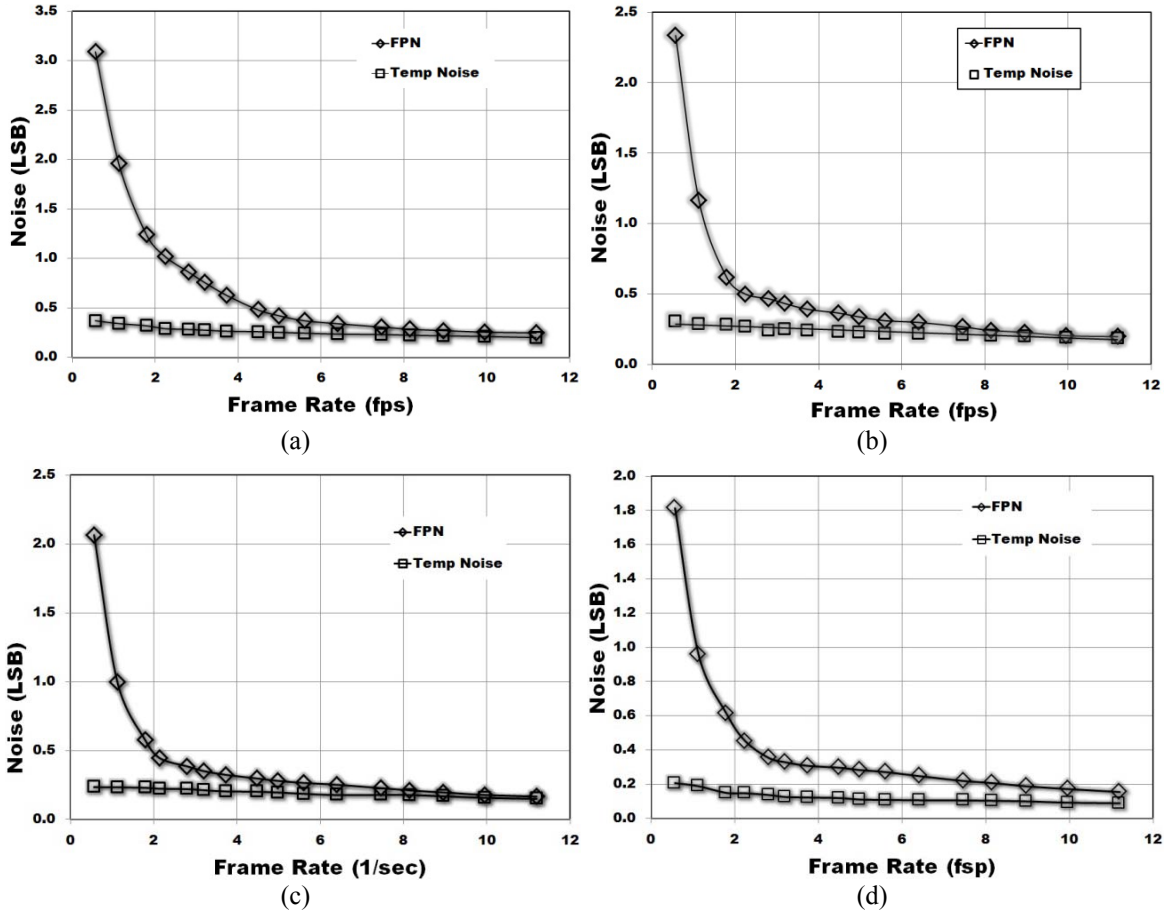


Figure 7-11. Dark signal non-uniformity (DSNU or FPN) and temporal noise variation at different frame rate and supply voltages for; (a) 0.8V supply voltage, (b) 1.2V supply voltage, (c) 1.6V supply voltage, (d) 2.0V supply voltage

Photo response non-uniformity (PRNU) is observed to fluctuate with illumination instead of following a general trend. The main reason for this is the mismatches between parallel ADC channels. Peak noise corresponds to the pixel values where largest capacitors in the sub DACs are supposed to switch. Figure 7-12 shows the measured photoresponse, temporal noise and photo response non-uniformity as a function of light exposure at 5.6 fps.

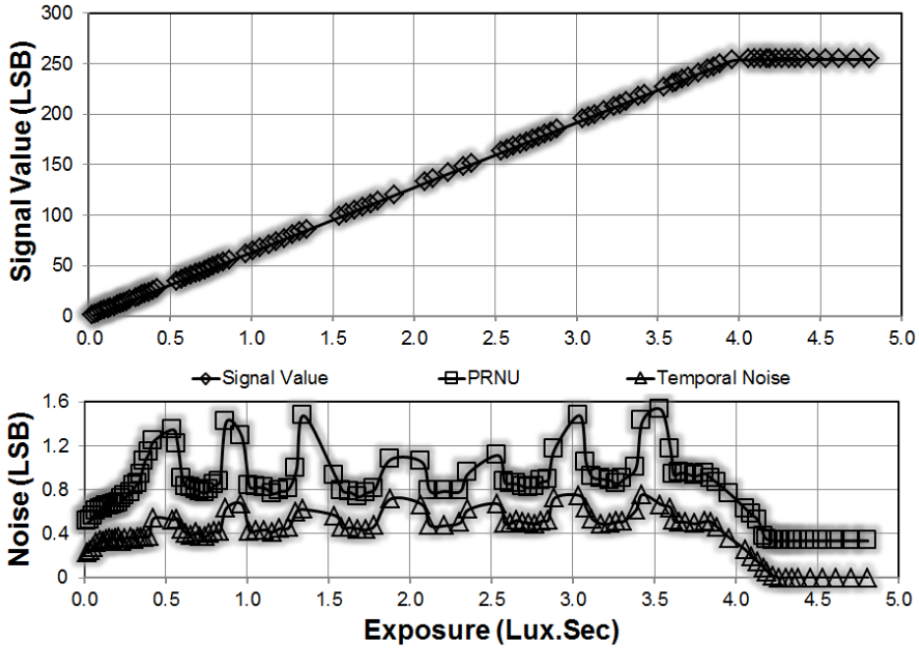


Figure 7-12. Measured photoresponse and noise performance of 4th generation EHI imager at 5.6 fps and 1.2V supply voltage.

At 0.8V supply voltage, the image sensor core consumes only 0.14 µW and 2.07 µW at 0.56 and 22.1 frames per second (fps), respectively. This power consumption includes the pixel array, row and column select logic, row and column drivers, SAR ADCs, and reference generator. Power consumption together with the pad frame and digital pad outputs increases to 0.27 µW and 5.11 µW at 0.7 and 22.4 fps, respectively. Power consumption of the EHI sensor at 0.7 and 22.4 fps for 0.8 V power supply are summarized in Table 7-6.

Switching power of the digital blocks dominate the power consumption of the imager. Therefore, the power consumption of the imager has an approximately quadratic dependence on power supply voltage. Figure 7-13 shows the variation of energy figure of merit with increasing supply voltage.

Since the image sensor consumes very low static power, dependence of power

Table 7-6. Measured power consumptions and figure of merits at 0.8V supply voltage.

PARAMETER	MEASUREMENTS	
Frame Rate (fps)	0.70	22.4
Power Consumption (Pixel Array) (µW)	0.0225	0.131
Power Consumption (Excl. pads) (µW)	0.14	2.07
Power Consumption (Whole Chip) (µW)	0.27	5.11
Figure of Merit (Pixel Array) (pJ/frame*pixel)	3.49	0.63
Figure of Merit (Excl. pads) (pJ/frame*pixel)	21.46	10.02
Figure of Merit (Whole Chip) (pJ/frame*pixel)	41.47	24.73

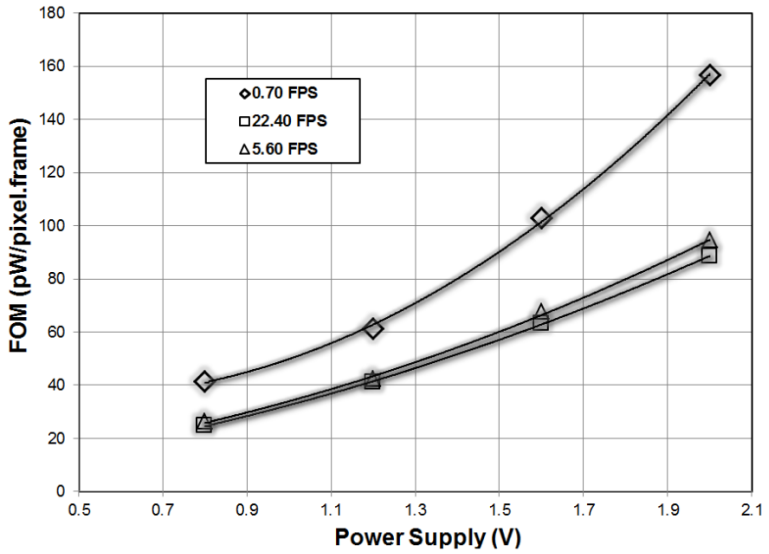
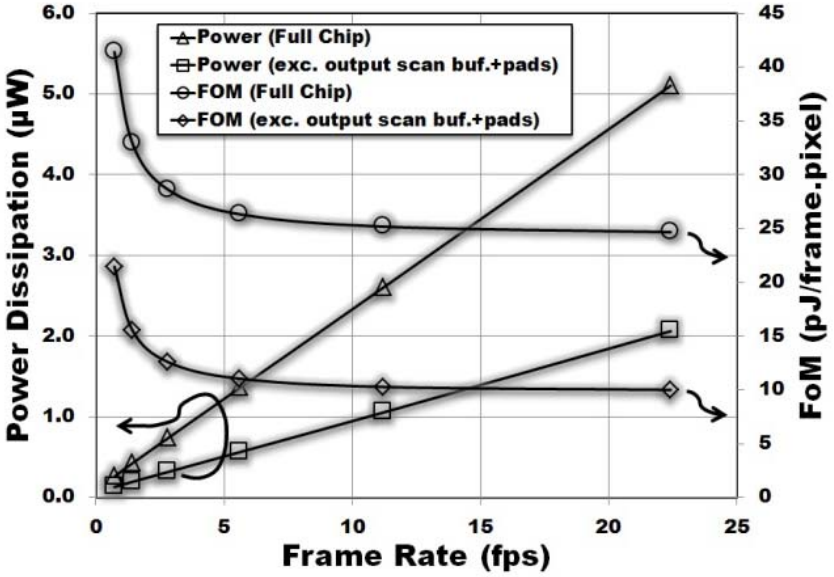


Figure 7-13. Measured energy figure of merit as a function of supply voltage.

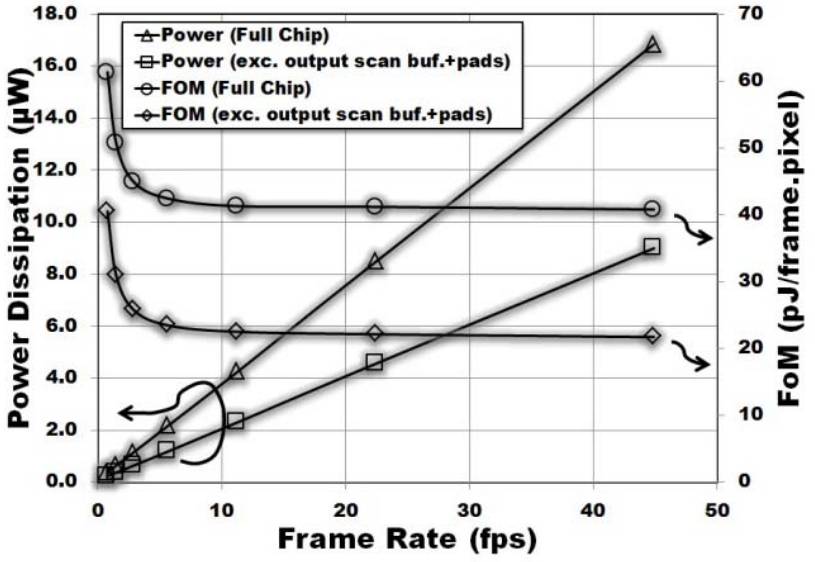
consumption on frame rate is approximately linear. Power consumption at lower frame rates decreases significantly. Figure 7-14 and Figure 7-15 shows the measured power consumption and energy figure of merit as a function of frame rate.

Power consumption of different blocks in the 4th generation EHI sensor chip at different frame rates are listed in Table 7-7. Since the power consumption of digital blocks

linearly increase with frequency while the power consumption of analog circuits are more or less constant, power consumption at higher frame rates is dominated by digital blocks.

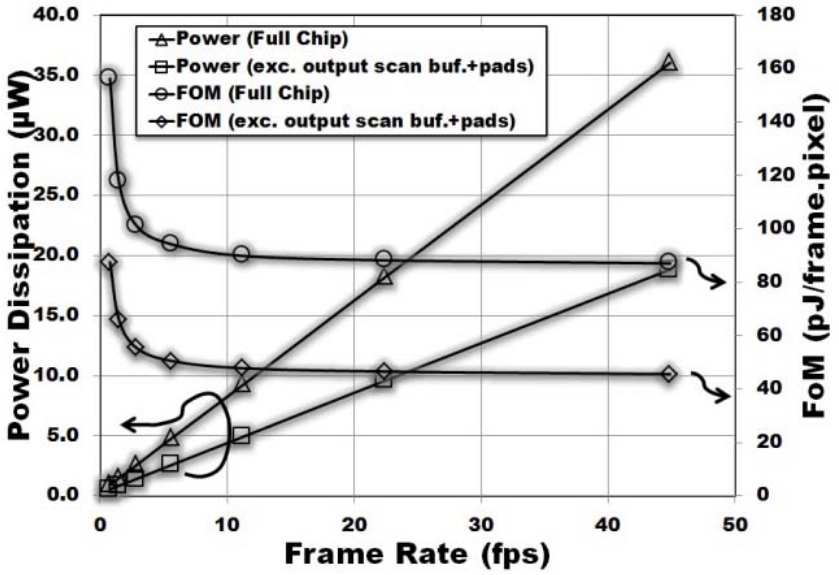


(a)

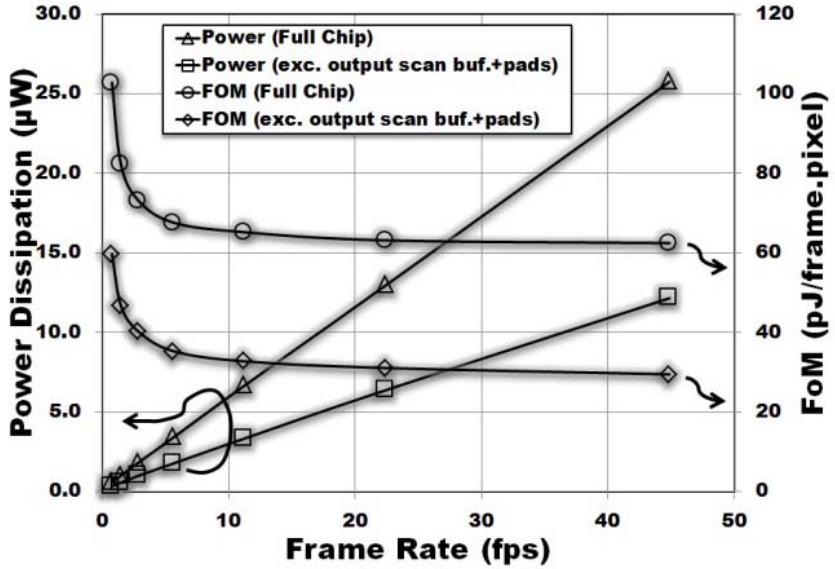


(b)

Figure 7-14. Measured power consumption and energy figure of merit as a function of frame rate at different supply voltages: (a) 0.8V, (b) 1.2V.



(a)



(b)

Figure 7-15. Measured power consumption and energy figure of merit as a function of frame rate at different supply voltages: (a) 1.6V, (b) 2.0V.

Table 7-7. Power consumption of circuit blocks in EHI imager.

Frame Rate	0.7 FPS	5.6 FPS	22.4 FPS
Pixel Array	8.41%	3.45%	2.57%
Reference Generator, Column Bias Circuits, Row and Column Drivers	16.11%	4.59%	2.29%
8x ADCs	27.23%	33.83%	35.65%
64-bit Shift Register	29.79%	39.89%	42.70%
Digital Pads	18.46%	18.24%	16.79%
Total	100%	100%	100%

7.2.3 **Captured Test Images**

Images captured by the 4th generation sensor at 0.8V and 1.2V power supply voltages are shown in Figure 7-16. Image quality improvement with increasing supply voltage can be seen in images.

Figure 7-16. Test images captured at (a) 0.8V supply voltage, (b) 1.2V supply voltage.

7.2.4 4th Generation EHI Sensor Energy Harvesting Mode Measurements

0.72 mm^2 area out of 1.38 mm^2 total pixel array area is used for the energy harvesting photodiodes in the 4th generation EHI sensor. The total junction area including the sidewalls is 2.36 mm^2. Current-voltage-power (IVP) characteristics of the energy harvesting photodiodes were measured under different daylight conditions as shown in Figure 7-17. The charge pump was shut down and EHB was loaded directly with a variable load resistor (R_L). R_L is varied from short circuit to open circuit condition. At the maximum power point (MPP), pixel array delivers 80.9 µA current while the load voltage is 388 mV delivering a total power of 31.36 µW power for 60,000 lux illumination. Maximum delivered power drops to 20.59 µW, 11.07 µW and 2.76 µW for 40,000 lux, 20,000 lux and 5,000 lux illuminations, respectively.

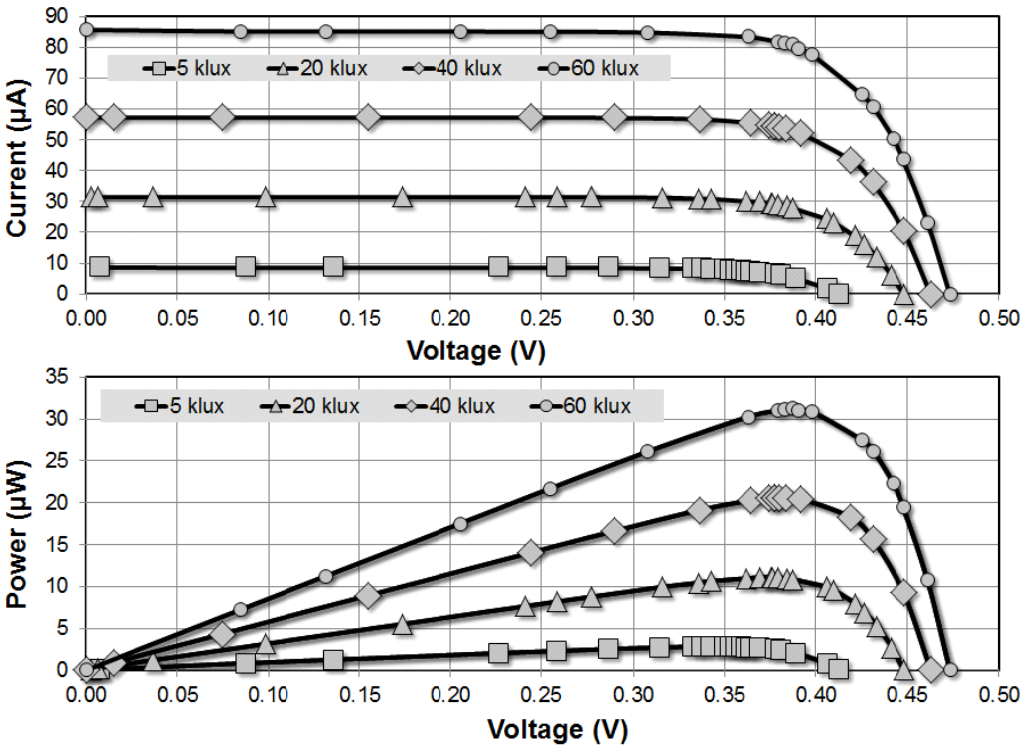


Figure 7-17. Measured current-voltage-power curve of the 4th generation EHI pixel array.

7.3 Comparison of 3rd and 4th Generation EHI Pixels

A comparison of the 3rd and 4th generation EHI sensors are shown in Table 7-8. The new imager structure with digital readout used in 4th generation EHI sensor has lower power consumption than the CMOS APS structure with analog readout channel used in 3rd generation EHI imager as expected. Noise performance of the 4th generation EHI sensor is also better than the noise performance of 3rd generation EHI sensor.

The energy harvesting capacity of 4th generation EHI imager is not as high as the 3rd generation EHI sensor. In the 3rd generation EHI sensor, the photo diodes consume 65% of total pixel array area. Since the energy harvesting photodiodes are made by placing minimum size n-wells in the empty areas between pixels, the energy harvesting photodiode area is smaller in 4th generation EHI sensor. The energy harvesting photodiodes are mostly shaded by pixel interconnects running over them and energy harvesting efficiency is reduced.

Table 7-9 shows the comparison of 3rd and 4th generation EHI sensors with the state-of-the-art low power CMOS image sensors. The image sensors used in comparison are built with different pixel and readout structures. Digital pixels used in image sensors with pulse width modulation (PWM) [57], [59] and time based readout [61], [85] can operate at very low voltages compared to source follower based active pixels. Therefore, these imagers typically have lower power consumption. 3rd generation EHI sensor consumes lower power than the imagers with analog readout [8], [10] and two of the digital image sensors. Considering the power hungry analog blocks, achieving lower power consumption than digital image sensors is a remarkable performance. Energy figure of merit of 3rd generation EHI sensor is comparable to the time based imager operating at 0.5V supply voltage in [61]. Therefore, it can be argued that building the same imager structure in a process with lower threshold

Table 7-8: Comparison of the first-and the second-generation sensors.

PARAMETER	3rd Generation EHI	4th Generation EHI
Process Technology	0.35µm, 2P4M CMOS	0.35µm, 2P4M CMOS
Pixel Pitch	18 µm x 18 µm	14 µm x 14 µm
Pixel type	EHI type Photodiode APS	EHI type Photodiode APS
Pixel fill factor	65% for PD1; 42.5% for PD2	30%
Resolution	64(H) x 45(V)	96(H) x 96(V)
Imager size	1.5mm x 1.2mm	1.7mm x 1.6mm
ADC Type	8-bit SAR ADC	8-bit SAR ADC
Supply Voltage	1.0 – 3.3V	0.8 – 3.3V
Maximum frame rate	21 fps	22.4 fps
Sensor output	8-bit parallel digital	8-bit series digital
Harvested Power (µW)	46.0 @ 57 klux 16.7 @ 20 kLux	31.36 @ 60 klux 11.07 @ 20 klux
Harvested Power Density (µW /mm^2)	49.3 @ 57 kLux 17.9 @ 20 kLux	17.14 @ 60 klux 9.78 @ 20 klux
Temporal Noise (Dark)	0.50 LSB @ 1.2V	0.19 LSB @ 1.2V
Dark Signal Non-Uniformity (DSNU)	0.86 LSB @ 1.2V	0.20 LSB @ 1.2V
Pixel FPN (Dark)	0.84 LSB @ 1.2V	0.037 LSB @ 1.2V
Column FPN (Dark)	0.11 LSB @ 1.2V	0.20 LSB @ 1.2V
Row FPN (Dark)	0.17 LSB @ 1.2V	0.011 LSB @ 1.2V
Temporal Noise (Half Well)	0.95 LSB @ 1.2V	0.51 LSB @ 1.2V
Photo Response Non-Uniformity (PRNU) (Half Well)	0.57 LSB @ 1.2V	0.62 LSB @ 1.2V
Pixel FPN (Half Well)	0.52 LSB @ 1.2V	0.52 LSB @ 1.2V
Column FPN (Half Well)	0.18 LSB @ 1.2V	0.29 LSB @ 1.2V
Row FPN (Half Well)	0.12 LSB @ 1.2V	0.17 LSB @ 1.2V
Power Consumption (Pixel Array) (µW)	0.034 @ 1V, 1.6fps	0.0225 @ 0.8V,0.7fps
Power Consumption (Excl. pads) (µW)	NA	0.14 @ 0.8V, 0.7fps
Power Consumption (Whole Chip) (µW)	0.92 @ 1V, 1.6fps	0.27 @ 0.8V, 0.7fps
Energy Figure of Merit (Pixel Array) (pJ/frame*pixel)	3.32 @ 1V, 21.2fps	0.63 @ 0.8V, 22.4fps
Energy Figure of Merit (Excl. pads) (pJ/frame*pixel)	NA	10.02 @ 0.8V,22.4fps
Energy Figure of Merit (Whole Chip) (pJ/frame*pixel)	148.1 @ 1V, 21.2fps	24.73 @ 0.8V, 22.4fps

Table 7-9. Comparison of EHI sensors to other low power imagers

PARAMETER	[57] **Kagawa**	[59] **Hanson**		[85]**Cho**	[61] **Chung**		[8] **Law**	[10] **Ay**	**3rd Gen. EHI**		**4th Gen. EHI**	
Technology	0.35µm (2P3M)	0.13µm Bulk		0.13µm (1P4M)	0.18µm (1P6M)		0.35µm (2P3M)	0.5µm (2P3M)	0.35µm (2P4M)		0.35µm/3.3V (2P4M)	
Pixel Pitch	10µm	5µm		3.4µm	10µm		15µm	21µm	18µm		14µm	
Array Size	128x96	128x128		128x128	64x40		32x32	54x50	45x64		96x96	
Fill Factor	18.50%	32%		38.00%	25.40%		21.00%	32%	65% for PD1; 42.5% for PD2		30%	
ADC Resolution	9 bit - Ramp	10 bit - Ramp		10 bit - Ramp	10 bit - Ramp		8 bit - Ramp	10 bit - SAR	8 bit - SAR		8 bit - SAR	
Supply Voltage	1.35 V	0.5 V		0.75 V	0.5 V		1.5 V	1.2 V	1.0 V		0.8 V	
Temporal Noise (Dark)(rms)	0.95 LSB	55.30 LSB		1.92 LSB	0.65 LSB		NA	0.98 LSB	0.50 LSB		0.19 LSB	
Pixel FPN (Dark) (rms)	0.61 LSB/ 0.12%	NA		6.76 LSB/ 0.66%	0.56 LSB/ 0.055%		NA	NA	0.84 LSB/ 0.330%		0.037 LSB/ 0.015%	
Column FPN (Dark) (rms)	0.15 LSB/ 0.03%	NA		0.61 LSB/ 0.06%	0.16 LSB/ 0.016%		NA	NA	0.11 LSB / 0.043%		0.20 LSB/ 0.076%	
Total FPN (Dark) (rms)	NA	67.58 LSB / 6.6%		NA	NA		47.16LSB/ 18.42%	1.23 LSB/ 0.12%	0.86 LSB/ 0.340%		0.20 LSB/ 0.078%	
Energy Harvesting (µW)	Not capable	Not capable		Not capable	Not capable		0.0356 @29klux	3.35 @60klux 2.10 @20klux	46.0 @57klux 16.7 @20klux		31.36 @ 60klux 11.07 @ 20klux	
Energy Harvesting ($\mu W/mm^2$)	Not capable	Not capable		Not capable	Not capable		0.155 @29klux	2.81 @60klux 1.76 @20klux	49.3 @57klux 17.9 @20klux		17.14 @ 60klux 9.78 @ 20klux	
Frame Rate (fps)	9.6	0.5	8.5	15	11.8	78.5	21	7.4	1.59	21.2	0.7	22.4
Power Consumption (Pixel Array) (µW)	0.42	NA	NA	1.6	0.45	0.6	NA	0.0264	0.034	0.202	0.0225	0.131
Power Consumption (Imager Core) (µW)	NA	0.7	1.24	NA	NA	NA	NA	NA	NA	NA	0.14	2.07
Power Consumption (Whole Chip) (µW)	55.2	NA	NA	65.2	4.95	29.6	15.8	14.25	0.92	9.04	0.27	5.11
iFOM (Pixel Array) (pJ/frame*pixel)	3.56	NA	NA	6.51	14.8	2.98	NA	1.32	7.38	3.32	3.49	0.63
iFOM (Pixel Array) (pJ/frame*pixel)	NA	85.4	8.6	NA	NA	NA	NA	NA	NA	NA	21.46	10.02
eFOM (Whole Chip) (pJ/frame*pixel)	467.9	NA	NA	265.3	163.9	147.3	734.7	713.2	200.9	148.1	41.47	24.73

voltages could result in a much better power consumption performance. The power consumption of PWM imager in [59] has a much lower energy figure of merit, but the noise of this imager sensor is unreasonably high and the image quality is very low compared to the 3rd generation EHI sensor.

4th generation EHI sensor has an extra ordinarily low power consumption. Its energy figure of merit is comparable to the PWM imager in [59]. The energy figure of merit is much lower than all other image sensors. However, comparing 4th generation image sensor to [59] needs a deeper analysis. First of all, 4th generation sensor achieves a much lower noise and better image quality. Power consumption of the same image sensor could be further reduced if it is manufactured in a process with lower threshold voltages.

7.4 Summary

The measurement results of the two EHI sensors designed for ultra-low power consumption and high energy harvesting capacity were presented.

The 3rd generation EHI sensor in imaging mode of operation is a low power CMOS APS imager with analog readout channel. It operates at 1V power supply and consumes 920 nW total chip power while capturing 64 (H) x 45 (V) resolution video at 1.59 fps. In the energy harvesting mode EHI imager can harvest 49.3 μW power per 1 mm^2 pixel array area. The power harvesting capacity of the 3rd generation EHI imager is far better than previous energy harvesting imager structures.

The 4th generation EHI sensor is a novel low power CMOS APS imager topology with fully digital readout channel. Core imager operates at 0.8V power supply and consumes only 140 nW power while capturing 96 (H) x 96 (V) resolution video at 0.7 fps. 4th

generation EHI sensor can harvest energy continuously unlike the previous EHI structures. 4^{th} generation EHI imager can harvest 17.14 μW power per 1 mm^2 total pixel array area.

4th generation EHI Sensor consumes one-to-two orders of magnitude less power than the state of the art CMOS active pixel sensors. Its power consumption is better than most digital imagers operating at supply voltages as low as 0.45V. The imager topology can be used to build extremely low power image sensors in processes with lower threshold voltages.

CHAPTER 8 - CONCLUSION

Harvesting power from ambient sources is vital for sensors and systems deployed in hard to access environments where battery replacement is difficult, if not impossible, to extend operating lifetime. Ambient sources can power an electronic system as long as the ambient energy source is persistent and harvested efficiently, potentially leading to an infinite operational lifetime. Beside efficient energy harvesting, various schemes have been proposed to eliminate the need for batteries in portable electronics and wireless sensors.

The most viable ambient energy source for powering an image sensor is solar energy bearing in mind both image sensors and solar cells could operate only under sufficient lighting conditions. With this to consider, an energy harvesting and imaging (EHI) sensor could be developed harvesting solar energy on its focal plane to power an ultra-low power CMOS APS imager. Thus, this study was focused on developing ultra-low power design techniques at all hierarchical levels of a CMOS APS imager while maximizing the harvested energy on the focal plane in an attempt to achieve continuous and self-powered operation.

The research is divided into four research objectives. The first objective is the investigation of fundamental principles, limits, and problems associated with photovoltaic energy harvesters. The second objective is the investigation and development of continuous mode energy harvesting and imaging pixel structures as opposed to the current state-of-the-art EHI pixels that could harvest energy and capture images sequentially. The third objective is to develop and integrate micro power management circuits, systems, and techniques that can condition the harvested energy as a usable power source. The fourth objective is

designing an ultra-low power CMOS APS imager which could be powered by the harvested energy on the focal plane.

The energy harvesting capacity of the original EHI sensor [10] is improved substantially using N-well/P-sub photodiode for energy harvesting, [12]. The N-well/P-sub photodiode increases energy harvesting capacity by more than an order (15x) of magnitude compared to the P+diff/N-well diode used in original EHI imager, [10]. The 3rd generation EHI imager can harvest up to 46 µW power under bright sunlight of 57KLux.

Continuous time energy harvesting is achieved in 4th generation EHI pixel by implementing energy harvesting micro solar cells and imaging photodiodes independently in each pixel. The energy harvesting micro solar cells and imaging photodiodes were built with maximum area efficiency using special design methods.

A unique polarity inverting charge pump is developed for converting the negative voltage generated on-chip to a usable positive voltage. The charge pump operates with high energy efficiency (~75%) while generating +1.85V without load and +1.26V delivering 16.65 µA load current.

An ultra-low power CMOS APS imager which dissipates an order of magnitude less power than state-of-the-art CMOS APS imagers could be powered with a watch battery for decades. In order to achieve this goal, an ultra-low power design methodology has been developed and used at all levels of abstraction. The 3rd generation EHI sensor was built with a 64 x 45 array of 3rd generation EHI type CMOS APS pixels, with standard analog readout, and on-chip 8-bit SAR ADC operating at 1V power supply. Power consumption is minimized at every circuit block. The prototype imager chip is built in a 0.35µm 2P4M CMOS technology. The imager dissipates only 9µW of power at 21.2 fps frame rate. This

power consumption includes the pixel array, row and column logic, row driver, analog readout, bias circuits, SAR ADC, and pad frame. This power consumption is very low compared to other CMOS APS imagers reported to date. However, the power hungry blocks in the analog readout channel prevent further power consumption reductions.

The 4th generation EHI sensor was implemented as a special ultra-low power 96 x 96 CMOS APS with fully digital readout and parallel on-chip 8-bit SAR ADCs operating at 0.8V power supply. Removal of analog circuits on the readout channel decreases power consumption significantly. Power consumption is minimized at every circuit block. The prototype sensor chip was also built in 0.35 µm 2P4M CMOS technology. The imager core dissipates only 2.07µW power at 22.1 fps frame rate. The core power consumption includes the pixel array, row and column logic, row and column drivers, bias circuits and 8 parallel SAR ADCs. The power consumption of the complete chip is 5.11µW power at 22.1 fps frame rate including the power consumed by 64 bit output shift registers and the pad frame. This power consumption is very low compared to other CMOS imagers reported to date.

The important technical achievements of the designed CMOS APS imager chip in this research are as follows:

- Low-voltage (0.8V) image sensor operation was achieved with very good image quality despite high threshold voltage transistors in 0.35µm CMOS process. Power supply voltage can be further reduced using modern CMOS manufacturing processes.
- Extremely low-power consumption is achieved through the ultra-low power design methodology and new image sensor readout architecture developed in this research. The imager core consumes only 140nW while capturing images at 0.7 fps frame rate with good image quality in 4th generation EHI imager. At same frame rate, full-chip power

consumption achieved is 270nW. These power consumptions are significantly lower than the existing CMOS APS imagers today. They could also be further reduced by using modern low threshold CMOS process.

- Digital readout channel architecture developed in this research increases system robustness and simplifies the system design. It eliminates the need for analog blocks and reference generators needed for operating these analog blocks. Autonomous System-On-a-Chip (ASoC) imager operation can be achieved easily adding a digital timing block. Adding the digital timing generator will drop the pad count to 4 pads. Eliminating the pads will reduce power consumption further.
- The developed image sensor offers exceptional reduction of system cost and increased system robustness and far more reduction of power consumption than earlier sensors reported. The energy harvesting capability integrated into the EHI sensor makes energy autonomous image sensors possible. The EHI sensor can be operated without a need for battery replacement for decades.

8.1 Future Directions

There are four directions of future work for EHI sensor design.

The first is integrating a digital timing generator to achieve autonomous camera-on-a-chip (ASoC) with only 4 pads: power, ground, digital output, and power output. Reducing the pad count will reduce the power consumption by approximately 20%. The timing generator will add to the power consumption, but the power savings due to the removal of pads will be more than the power dissipated by the timing generator.

The second research direction is implanting the CMOS APS imager structure with fully digital readout channel in a process with lower threshold voltage transistors. This will allow reduction of supply voltage. Thus, power consumption will be reduced significantly.

The third research direction is designing alternative image sensor structures that can operate at lower supply voltages and consume less power than CMOS APS imagers.

The fourth area is to improve the power management system. Improving the efficiency of the on-chip DC-DC converter and integrating a maximum power point tracking (MPPT) circuit into the power management system will improve energy harvesting efficiency.

REFERENCES

[1] E. R. Fossum, “CMOS image sensors: electronic camera on a chip,” in Electron Devices Meeting, 1995. IEDM ’95., International, 1995, pp. 17–25.

[2] M. Ferri, D. Pinna, E. Dallago, and P. Malcovati, “Integrated micro-solar cell structures for harvesting supplied microsystems in 0.35-μm CMOS technology,” in *Sensors, 2009 IEEE ,* vol., no., pp.542,545, 25-28 Oct. 2009.

[3] B. Plesz, L. Juhasz, and J. Mizsei, “Feasibility study of a CMOS-compatible integrated solar photovoltaic cell array,” in *2010 Symposium on Design Test Integration and Packaging of MEMS/MOEMS (DTIP)*, 2010, pp. 403–406.

[4] E. G. Fong, N. J. Guilar, T. J. Kleeburg, H. Pham, D. R. Yankelevich, and R. Amirtharajah, “Integrated Energy-Harvesting Photodiodes With Diffractive Storage Capacitance,” *IEEE Trans. Very Large Scale Integr. VLSI Syst.*, vol. 21, no. 3, pp. 486–497, 2013.

[5] N. J. Guilar, T. J. Kleeburg, A. Chen, D. R. Yankelevich, and R. Amirtharajah, “Integrated Solar Energy Harvesting and Storage,” *IEEE Trans. Very Large Scale Integr. VLSI Syst.*, vol. 17, no. 5, pp. 627–637, 2009.

[6] A. Fish, S. Hamami, and O. Yadid-Pecht, “CMOS Image Sensors With Self-Powered Generation Capability,” *IEEE Trans. Circuits Syst. II Express Briefs*, vol. 53, no. 11, pp. 1210–1214, 2006.

[7] C. Shi, M. K. Law, and A. Bermak, “A Novel Asynchronous Pixel for an Energy Harvesting CMOS Image Sensor,” *IEEE Trans. Very Large Scale Integr. VLSI Syst.*, vol. 19, no. 1, pp. 118–129, 2011.

[8] M. K. Law, A. Bermak, and C. Shi, "A Low-Power Energy-Harvesting Logarithmic CMOS Image Sensor With Reconfigurable Resolution Using Two-Level Quantization Scheme," *IEEE Trans. Circuits Syst. II Express Briefs*, vol. 58, no. 2, pp. 80–84, 2011.

[9] F. Tang, Y. Cao, and A. Bermak, "An ultra-low power current-mode CMOS image sensor with energy harvesting capability," in *ESSCIRC, 2010 Proceedings of the ,* vol., no., pp.126,129, 14-16 Sept. 2010.

[10] S. U. Ay, "A CMOS Energy Harvesting and Imaging (EHI) Active Pixel Sensor (APS) Imager for Retinal Prosthesis," *IEEE Trans. Biomed. Circuits Syst.*, vol. 5, no. 6, pp. 535–545, 2011.

[11] T. Wang, X. Huang, M. Yan, H. Yu, K. S. Yeo, I. Cevik, and S. Ay, "A 96x96 1V ultra-low power CMOS image sensor for biomedical application," in *Circuits and Systems (APCCAS), 2012 IEEE Asia Pacific Conference on*, vol., no., pp.13,16, 2-5 Dec. 2012.

[12] I. Cevik, S. U. Ay, J. Wang, and M. Yan, "Power Generation Capability of CMOS Image Sensors with on-Chip Energy Harvesting Pixels," in *Circuits and Systems (MWSCAS), 2013 IEEE 56th International Midwest Symposium on*, vol., no., pp.313,316, 4-7 Aug. 2013.

[13] Nakamura, Junichi. *Image Sensors and Signal Processing for Digital Still Cameras*. Boca Raton, FL: Taylor & Francis, 2005.

[14] G. P. Weckler, "Operation of p-n Junction Photodetectors in a Photon Flux Integrating Mode," *IEEE J. Solid-State Circuits*, vol. 2, no. 3, pp. 65–73, Sep. 1967.

[15] R. H. Dyck and G. P. Weckler, "Integrated arrays of silicon photodetectors for image sensing," *IEEE Trans. Electron Devices*, vol. 15, no. 4, pp. 196–201, Apr. 1968.

[16] P. J. W. Noble, "Self-scanned silicon image detector arrays," *IEEE Trans. Electron Devices*, vol. 15, no. 4, pp. 202–209, Apr. 1968.

[17] S. G. Chamberlain, "Photosensitivity and Scanning of Silicon Image Detector Arrays," *IEEE J. Solid-State Circuits*, vol. 4, no. 6, pp. 333–342, Dec. 1969.

[18] P. W. Fry, P. J. W. Noble, and R. J. Rycroft, "Fixed-pattern noise in photomatrices," *IEEE J. Solid-State Circuits*, vol. 5, no. 5, pp. 250–254, Oct. 1970.

[19] W. S. Boyle and G. E. Smith, "Charge Coupled Semiconductor Devices," *Bell Syst. Tech. J.*, vol. 49, no. 4, pp. 587–593, 1970.

[20] A. Krymski, D. Van Blerkom, A. Andersson, N. Bock, B. Mansoorian, and E. R. Fossum, "A high speed, 500 frames/s, 1024x1024 CMOS active pixel sensor," in *VLSI Circuits, 1999. Digest of Technical Papers. 1999 Symposium on*, vol., no., pp.137-138, 17-19 June 1999.

[21] E. R. Fossum, "Digital camera system on a chip," *IEEE Micro*, vol.18, no.3, pp.8,15, May/Jun 1998.

[22] E. R. Fossum, "Ultra low power imaging systems using CMOS image sensor technology," *Adv. Microdevices Space Sci. Sens. Proc SPIE*, vol. 2267, pp. 107–111, 1994.

[23] Ay, Suat U. *Large Format Cmos Image Sensors: Performance and Design*. Saarbrücken: VDM, Verlag Dr. Müller, 2008.

[24] R. H. Nixon, S. E. Kemeny, C. O. Staller, and E. R. Fossum, "128x128 CMOS photodiode-type active pixel sensor with on-chip timing, control and signal chain electronics," in *Proc. SPIE Charge-Coupled Devices and Solid-State Optical Sensors V*, 1995, vol. 2415, pp. 117–123.

[25] S. U. Ay, “Photodiode Peripheral Utilization Effect on CMOS APS Pixel Performance,” *IEEE Trans. Circuits Syst. Regul. Pap.*, vol. 55, no. 6, pp. 1405–1411, Jul. 2008.

[26] S. K. Mendis, S. E. Kemeny, and E. R. Fossum, “A 128×128 CMOS active pixel image sensor for highly integrated imaging systems,” in *Electron Devices Meeting, 1993. IEDM '93. Technical Digest., International*, vol., no., pp.583,586, 5-8 Dec. 1993.

[27] S. Mendis, S. E. Kemeny, and E. R. Fossum, “CMOS active pixel image sensor,” *IEEE Trans. Electron Devices*, vol. 41, no. 3, pp. 452–453, Mar. 1994.

[28] S. K. Mendis, S. E. Kemeny, R. C. Gee, B. Pain, C. O. Staller, Quiesup Kim, and E. R. Fossum, “CMOS active pixel image sensors for highly integrated imaging systems,” *IEEE J. Solid-State Circuits*, vol. 32, no. 2, pp. 187–197, Feb. 1997.

[29] S. Yoshihara, Y. Nitta, M. Kikuchi, K. Koseki, Y. Ito, Y. Inada, S. Kuramochi, H. Wakabayashi, M. Okano, H. Kuriyama, J. Inutsuka, A. Tajima, T. Nakajima, Y. Kudoh, F. Koga, Y. Kasagi, S. Watanabe, and T. Nomoto, “A 1/1.8-inch 6.4 MPixel 60 frames/s CMOS Image Sensor With Seamless Mode Change,” *IEEE J. Solid-State Circuits*, vol. 41, no. 12, pp. 2998–3006, Dec. 2006.

[30] A. I. Krymski, N. E. Bock, N. Tu, D. Van Blerkom, and E. R. Fossum, “A high-speed, 240-frames/s, 4.1-Mpixel CMOS sensor,” *IEEE Trans. Electron Devices*, vol. 50, no. 1, pp. 130–135, Jan. 2003.

[31] M.-S. Shin, J.-B. Kim, M.-K. Kim, Y.-R. Jo, and O.-K. Kwon, “A 1.92-Megapixel CMOS Image Sensor With Column-Parallel Low-Power and Area-Efficient SA-ADCs,” *IEEE Trans. Electron Devices*, vol. 59, no. 6, pp. 1693–1700, Jun. 2012.

[32] A. P. Chandrakasan, S. Sheng, and R. W. Brodersen, “Low-power CMOS digital design,” *IEEE J. Solid-State Circuits*, vol. 27, no. 4, pp. 473–484, 1992.

[33] H. J. M. Veendrick, “Short-circuit dissipation of static CMOS circuitry and its impact on the design of buffer circuits,” *IEEE J. Solid-State Circuits*, vol. 19, no. 4, pp. 468–473, Aug. 1984.

[34] W. M. Gosney, “Subthreshold drain leakage currents in MOS field-effect transistors,” *IEEE Trans. Electron Devices*, vol. 19, no. 2, pp. 213–219, Feb. 1972.

[35] D. Liu and C. Svensson, “Trading speed for low power by choice of supply and threshold voltages,” *IEEE J. Solid-State Circuits*, vol. 28, no. 1, pp. 10–17, 1993.

[36] S.-W. Sun and P. G. Y. Tsui, “Limitation of CMOS supply-voltage scaling by MOSFET threshold-voltage variation,” *IEEE J. Solid-State Circuits*, vol. 30, no. 8, pp. 947–949, 1995.

[37] Z. Chen, J. Shott, J. Burr, and J. D. Plummer, “CMOS technology scaling for low voltage low power applications,” in *Low Power Electronics, 1994. Digest of Technical Papers., IEEE Symposium*, vol., no., pp.56,57, 10-12 Oct. 1994.

[38] H.-S. Wong, “Technology and device scaling considerations for CMOS imagers,” *IEEE Trans. Electron Devices*, vol. 43, no. 12, pp. 2131–2142, 1996.

[39] R. H. Dennard, F. H. Gaensslen, V. L. Rideout, E. Bassous, and A. R. LeBlanc, “Design of ion-implanted MOSFET’s with very small physical dimensions,” *IEEE J. Solid-State Circuits*, vol. 9, no. 5, pp. 256–268, Oct. 1974.

[40] “INTERNATIONAL TECHNOLOGY ROADMAP FOR SEMICONDUCTORS, 2012 UPDATE.” .

[41] A. El Gamal, “Trends in CMOS image sensor technology and design,” in *Electron Devices Meeting, 2002. IEDM '02. International ,* vol., no., pp.805,808, 8-11 Dec. 2002.

[42] A. El Gamal and H. Eltoukhy, “CMOS image sensors,” *IEEE Circuits Devices Mag.*, vol. 21, no. 3, pp. 6–20, 2005.

[43] A. Rjoub and O. Koufopavlou, “Low voltage swing gates for low power consumption,” in *Proceedings of the 1999 IEEE International Symposium on Circuits and Systems, 1999. ISCAS ’99*, pp.234,237 vol.1, Jul 1999.

[44] W. Gao and R. Hornsey, “Low power realization in main blocks of CMOS APS image sensor,” presented at the SPIE Photonics North, 2005, pp. 261–269.

[45] C. Zhongjian, L. Xiaoyong, J. Lijiu, H. Jianzhong, and Y. Songlin, “An improved low power CMOS readout circuit for focal plane array,” in *4th International Conference on ASIC, 2001. Proceedings*, 2001, pp. 854–857.

[46] S. U. Ay, “Boosted readout for CMOS APS pixels,” in *2011 IEEE International Symposium on Circuits and Systems (ISCAS)*, 2011, pp. 2205–2208.

[47] C. Xu, W. Zhang, and M. Chan, “A low voltage hybrid bulk/SOI CMOS active pixel image sensor,” *IEEE Electron Device Lett.*, vol. 22, no. 5, pp. 248–250, 2001.

[48] S.-Y. Ma and L.-G. Chen, “A single-chip CMOS APS camera with direct frame difference output,” *IEEE J. Solid-State Circuits*, vol. 34, no. 10, pp. 1415–1418, 1999.

[49] H.-S. P. Wong, R. T. Chang, E. Crabbe, and P. D. Agnello, “CMOS active pixel image sensors fabricated using a 1.8-V, 0.25- mu;m CMOS technology,” *IEEE Trans. Electron Devices*, vol. 45, no. 4, pp. 889–894, 1998.

[50] K.-B. Cho, A. Krymski, and E. R. Fossum, “A 1.2 V micropower CMOS active pixel image sensor for portable applications,” in *Solid-State Circuits Conference, 2000. Digest of Technical Papers. ISSCC. 2000 IEEE International*, 2000, pp. 114–115.

[51] C. Xu, W. Zhang, W.-H. Ki, and M. Chan, “A 1.0-V VDD CMOS active-pixel sensor with complementary pixel architecture and pulsewidth modulation fabricated with a 0.25-μm CMOS process,” *IEEE J. Solid-State Circuits*, vol. 37, no. 12, pp. 1853–1859, 2002.

[52] H.-C. Chow and J.-B. Hsiao, “A new rail-to-rail readout circuit of CMOS image sensor for low power applications,” in *48th Midwest Symposium on Circuits and Systems, 2005*, 2005, pp. 1019–1022 Vol. 2.

[53] L. G. McIlrath, “A low-power low-noise ultrawide-dynamic-range CMOS imager with pixel-parallel A/D conversion,” *IEEE J. Solid-State Circuits*, vol. 36, no. 5, pp. 846–853, 2001.

[54] K. P. Frohmader, “A novel MOS compatible light intensity-to-frequency converter suited for monolithic integration,” *IEEE J. Solid-State Circuits*, vol. 17, no. 3, pp. 588–591, 1982.

[55] X. Wang, W. Wong, and R. Hornsey, “A High Dynamic Range CMOS Image Sensor With Inpixel Light-to-Frequency Conversion,” *IEEE Trans. Electron Devices*, vol. 53, no. 12, pp. 2988–2992, 2006.

[56] A. Kitchen, A. Bermak, and A. Bouzerdoum, “PWM digital pixel sensor based on asynchronous self-resetting scheme,” *IEEE Electron Device Lett.*, vol. 25, no. 7, pp. 471–473, 2004.

[57] K. Kagawau, S. Shishido, M. Nunoshita, and J. Ohta, “A 3.6pW/frame·pixel 1.35V PWM CMOS Imager with Dynamic Pixel Readout and no Static Bias Current,” in *Solid-State Circuits Conference, 2008. ISSCC 2008. Digest of Technical Papers. IEEE International*, 2008, pp. 54–595.

[58] S. Hanson, Z. Foo, D. Blaauw, and D. Sylvester, “A 0.5 V Sub-Microwatt CMOS Image Sensor With Pulse-Width Modulation Read-Out,” *IEEE J. Solid-State Circuits*, vol. 45, no. 4, pp. 759–767, 2010.

[59] S. Hanson and D. Sylvester, “A 0.45-0.7V sub-microwatt CMOS image sensor for ultra-low power applications,” in *2009 Symposium on VLSI Circuits*, 2009, pp. 176–177.

[60] J. Choi, S. Park, J. Cho, and E. Yoon, “A 1.36 μW adaptive CMOS image sensor with reconfigurable modes of operation from available energy/illumination for distributed wireless sensor network,” in *Solid-State Circuits Conference Digest of Technical Papers (ISSCC), 2012 IEEE International*, 2012, pp. 112–114.

[61] M.-T. Chung, C.-L. Lee, C. Yin, and C.-C. Hsieh, “A 0.5 V PWM CMOS Imager With 82 dB Dynamic Range and 0.055% Fixed-Pattern-Noise,” *IEEE J. Solid-State Circuits*, vol. 48, no. 10, pp. 2522–2530, 2013.

[62] F. Boussaid, A. Bermak, and A. Bouzerdoum, “An ultra-low power operating technique for mega-pixels current-mediated CMOS imagers,” *IEEE Trans. Consum. Electron.*, vol. 50, no. 1, pp. 46–53, 2004.

[63] B. Streetman, in *Solid State Electronic Devices*, Fourth Ed., Prentice Hall, pp. 130–190.

[64] M. A. Green, *Solar Cell Operating Principles Technology and System Applications*. Prentice Hall, 1981.

[65] M. A. S. Masoum, H. Dehbonei, and E. F. Fuchs, “Theoretical and experimental analyses of photovoltaic systems with voltageand current-based maximum power-point tracking,” *IEEE Trans. Energy Convers.*, vol. 17, no. 4, pp. 514–522, Dec. 2002.

[66] S. U. Ay, “A 1.32pW/frame.pixel 1.2V CMOS energy-harvesting and imaging (EHI) APS imager,” in *Solid-State Circuits Conference Digest of Technical Papers (ISSCC), 2011 IEEE International*, 2011, pp. 116–118.

[67] S. U. Ay, “A sub-1 Volt 10-bit supply boosted SAR ADC design in standard CMOS,” *Analog Integr. Circuits Signal Process.*, vol. 66, no. 2, pp. 213–221, Feb. 2011.

[68] A. Kanago, V. Barry, B. Sprague, I. Cevik, and S. Ay, “A low power maximum power point tracker and power management system in 0.5µm CMOS,” 2012, pp. 238–241.

[69] S. U. Ay, “Boosted CMOS APS Pixel Readout for Ultra Low-Voltage and Low-Power Operation,” *IEEE Trans. Circuits Syst. II Express Briefs*, vol. 60, no. 6, pp. 341–345, Jun. 2013.

[70] B. Razavi, *Design of Analog CMOS Integrated Circuits*. McGraw-Hill Science/Engineering/Math, 2000.

[71] E. R. Fossum, “CMOS image sensors: electronic camera on a chip,” pp. 17–25.

[72] Kwang-Bo Cho, A. I. Krymski, and E. R. Fossum, “A 1.5-V 550-µW 176 x 144 autonomous CMOS active pixel image sensor,” *IEEE Trans. Electron Devices*, vol. 50, no. 1, pp. 96–105, Jan. 2003.

[73] Kwang-Bo Cho, A. Krymski, and E. R. Fossum, “A 1.2 V micropower CMOS active pixel image sensor for portable applications,” pp. 114–115.

[74] J. Ruiz-Amaya, M. Delgado-Restituto, and A. Rodriguez-Vazquez, "Accurate Settling-Time Modeling and Design Procedures for Two-Stage Miller-Compensated Amplifiers for Switched-Capacitor Circuits," *IEEE Trans. Circuits Syst. Regul. Pap.*, vol. 56, no. 6, pp. 1077–1087, Jun. 2009.

[75] P. Perez-Nicoli, F. Veirano, C. Rossi-Aicardi, and P. Aguirre, "Design method for an ultra low power, low offset, symmetric OTA," in *2013 7th Argentine School of Micro-Nanoelectronics, Technology and Applications (EAMTA)*, 2013, pp. 38–43.

[76] L. Yao, M. Steyaert, and W. Sansen, "A 0.8-V, 8-µW, CMOS OTA with 50-dB gain and 1.2-MHz GBW in 18-pF load," in *Solid-State Circuits Conference, 2003. ESSCIRC '03. Proceedings of the 29th European*, 2003, pp. 297–300.

[77] S. Mallya and J. H. Nevin, "Design procedures for a fully differential folded-cascode CMOS operational amplifier," *IEEE J. Solid-State Circuits*, vol. 24, no. 6, pp. 1737–1740, Dec. 1989.

[78] M. D. Scott, B. E. Boser, and K. S. J. Pister, "An ultralow-energy ADC for Smart Dust," *IEEE J. Solid-State Circuits*, vol. 38, no. 7, pp. 1123–1129, Jul. 2003.

[79] L. S. Y. Wong, S. Hossain, A. Ta, J. Edvinsson, D. H. Rivas, and H. Naas, "A very low-power CMOS mixed-signal IC for implantable pacemaker applications," *IEEE J. Solid-State Circuits*, vol. 39, no. 12, pp. 2446–2456, Dec. 2004.

[80] M. Van Elzakker, E. Van Tuijl, P. Geraedts, D. Schinkel, E. Klumperink, and B. Nauta, "A 1.9 µW 4.4fJ/Conversion-step 10b 1MS/s Charge-Redistribution ADC," in *Solid-State Circuits Conference, 2008. ISSCC 2008. Digest of Technical Papers. IEEE International*, 2008, pp. 244–610.

[81] Zhimin Zhou, B. Pain, and E. R. Fossum, "CMOS active pixel sensor with on-chip successive approximation analog-to-digital converter," *IEEE Trans. Electron Devices*, vol. 44, no. 10, pp. 1759–1763, Oct. 1997.

[82] H. Oguey and D. Aebischer, "CMOS Current Reference without Resistance," in *Solid-State Circuits Conference, 1996. ESSCIRC '96. Proceedings of the 22nd European*, 1996, pp. 104–107.

[83] D. Senderowicz, G. Nicollini, S. Pernici, A. Nagari, P. Confalonieri, and C. Dallavalle, "Low-voltage double-sampled ΣΔ converters," *IEEE J. Solid-State Circuits*, vol. 32, no. 12, pp. 1907–1919, Dec. 1997.

[84] Y. Arima and M. Ehara, "On-chip solar battery structure for CMOS LSI," *IEICE Electron. Express*, vol. 3, no. 13, pp. 287–291, 2006.

[85] K. Cho, D. Lee, J. Lee, and G. Han, "A 0.75V CMOS image sensor using time-based readout circuit," in *2009 Symposium on VLSI Circuits*, 2009, pp. 178–179.

[86] R. H. Nixon, S. E. Kemeny, C. O. Staller, and E. R. Fossum, "128 x 128 CMOS photodiode-type active pixel sensor with on-chip timing, control and signal chain electronics," in *Charge-Coupled Devices and Solid-State Optical Sensors V, Proc. SPIE*, 1995.

[87] E.-S. Eid, A. G. Dickinson, D. A. Inglis, B. D. Ackland, and E. R. Fossum, "A 256x256 CMOS active pixel image sensor," in *Charge-Coupled Devices and Solid-State Optical Sensors V, Proc. SPIE*, 1995.

[88] Z. Zhou, S. E. Kemeny, B. Pain, R. C. Gee, and E. R. Fossum, "A CMOS Active Pixel Sensor with Amplification and Reduced Fixed Pattern Noise," in *Program of 1995 IEEE Workshop on CCDs and Advanced Image Sensors*, Dana Point, CA, 1995.

[89] W. Hu, Y.-T. Liu, T. Nguyen, D. Y. C. Lie, and B. P. Ginsburg, "An 8-Bit Single-Ended Ultra-Low-Power SAR ADC With a Novel DAC Switching Method and a Counter-Based Digital Control Circuitry," *IEEE Trans. Circuits Syst. Regul. Pap.*, vol. 60, no. 7, pp. 1726–1739, Jul. 2013.

[90] J. Shappir and A. Kolodny, "The response of small photovoltaic detectors to uniform radiation," *IEEE Trans. Electron Devices*, vol. 24, no. 8, pp. 1093–1098, Aug. 1977.

[91] T. I. Kamins and G. T. Fong, "Photosensing Arrays with Improved Spatial Resolution," *IEEE J. Solid-State Circuits*, vol. 13, no. 1, pp. 80–85, Feb. 1978.

[92] H. Holloway, "Theory of lateral-collection photodiodes," *J. Appl. Phys.*, vol. 49, no. 7, pp. 4264–4269, Jul. 1978.

[93] S. Kirkpatrick, "Modeling diffusion and collection of charge from ionizing radiation in silicon devices," *IEEE Trans. Electron Devices*, vol. 26, no. 11, pp. 1742–1753, Nov. 1979.

[94] H. Holloway and A. D. Brailsford, "Peripheral photoresponse of a p-n junction," *J. Appl. Phys.*, vol. 54, no. 8, pp. 4641–4656, Aug. 1983.

[95] L. M. Sander, "Exact solution for the peripheral photoresponse of a p-n junction," *J. Appl. Phys.*, vol. 57, no. 6, pp. 2057–2059, Mar. 1985.

[96] J. S. Lee and R. I. Hornsey, "Photoresponse of photodiode arrays for solid-state image sensors," *J. Vac. Sci. Technol. Vac. Surf. Films*, vol. 18, no. 2, pp. 621–625, Mar. 2000.

[97] J. S. Lee, R. I. Hornsey, and D. Renshaw, "Analysis of CMOS Photodiodes. II. Lateral photoresponse," *IEEE Trans. Electron Devices*, vol. 50, no. 5, pp. 1239–1245, May 2003.