Space Vector Modulation of a Brushless DC Motor and Resolver Position Sensor for a Force-Feedback Application

A Thesis
Presented in Partial Fulfillment of the Requirements for the
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by

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AUTHORIZATION TO SUBMIT THESIS

This thesis of Anthony L. Crawford, submitted for the degree of Master of Science with a Major in Electrical Engineering and titled "Space Vector Modulation of a Brushless DC Motor and Resolver Position Sensor for a Force-Feedback Application" has been reviewed in final form. Permission, as indicated by the signatures and dates given below, is now granted to submit final copies to the college of Graduate Studies for approval.

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ABSTRACT

The focus of this thesis is the control of a three phase brushless direct current (BLDC) motor to drive a force feedback (haptic) robotic hand in a radiological environment. This thesis presents both the theory behind, and the specific hardware and software, implemented to operate the BLDC motor and resolver. The discussion associated with the hardware includes the primary considerations of operating electronics in a radiation environment, selected brushless motor, selected resolver, developed Printed Circuit Board (PCB) implementing the three half bridge driver and resolver-to-digital circuit, and supporting LabVIEW Field-Programmable Gate Array (FPGA) system.

The associate software includes the LabVIEW code programmed on the fast/dependable operating, but restricted space, FPGA system. The developed code effectively implements Space Vector Pulse Width Modulation (SVPWM) and position data acquisition using unique techniques to account for the restricted space available on the FPGA system. Such techniques include small memory switching/comparison logic operators and simple operations such as addition, multiplication, and bit number truncation to execute operations traditionally performed via floating point operations and trigonometric functions.

Additional evaluation is also presented regarding the means of selecting a suitable Pulse Width Modulation (PWM) duty cycle to ensure that the dynamics associated with the BLDC motor components as well as the digital resolver-to-digital converter are accounted for in order to generate smooth motion and position accuracy while minimizing the probability of overheating. Overheating is more prevalent in haptic finger torque control applications where a high torque, stall like position may be applied for extended periods of time.

The thesis concludes with a discussion of future work including the implementation of Field Oriented Control (FOC) and measuring the three phase currents using a single current signal and its relationship to the PWM signal profile.

ACKNOWLEDGEMENTS

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DEDICATION

I would like to dedicate this thesis to my wife, without her support this endeavor would not have been possible.

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LIST OF ABBREVIATIONS

FPGA	Field-Programmable Gate Array
FOC	Field Oriented Control
SVM	Space Vector Modulation
PID	Proportional Integral Derivative
PWM	Pulse Width Modulation
SVPWM	Space Vector Pulse Width Modulation
ASIC	Application Specific Integrated Circuit
PCB	Printed Circuit Board

CHAPTER 1: INTRODUCTION

1.1 Overview

The focus of this thesis is to develop the circuitry necessary to drive BLDC motors embedded in a force-feedback (haptic) robotic hand under unconventional constraints. These constraints are primarily imposed by the radiation environment in which the motors will operate. The BLDC motors are applicable for this application because the brushes associated with conventional DC brushed motors cause impurities which are disadvantageous [1] and difficult to clean up in some radiation environments. It is also more difficult to perform any maintenance (including motor change-out) in a radiation environment (which is required more often for brushed DC motors). Additionally the BLDC motors have a higher torque to volume ratio. The resolver position sensor is applicable for this application because of the ill effects that radiation has on most sensors conventionally employed to control the motors (e.g. Hall Effect sensors, encoders). In summary, this thesis presents a force-feedback system capable of operating a BLDC motor utilizing a resolver shaft position sensor in a radiation environment.

The primary challenge associated with this scenario is that conventional controllers are not designed to accommodate the unique combination of requirements. The typical controllers that complement a brushless motor whose size is appropriate for this application (based on the application's desired size and torque requirements) only accommodate Hall Effect sensor or encoder feedback and are primarily limited to position or speed control rather than the torque control deemed necessary for this force feedback application.

Although a system appropriate for this application would be able to implement some established technologies/practices (brushless motors, space vector modulation, resolvers, reading digital position signals, etc.), some novel techniques are required in order to fully integrate the these technologies together.

The items of particular importance include the integration of the technologies into a flexible platform that can be adjusted/optimized/customized for use in human-machine interaction haptic hand studies. The performance requirements to realize effective, robust, and dependable tele-operation transparency between a user and a robotic device in a radiological environment finds its way into every subpart of this project including motor selection, driver techniques, position sensing, and current feedback.

A system that has the most potential for such an application is LabVIEW's FPGA system which is characterized by fast, reliable, customizable functionality and is able to collect the operation of the multiple entities (motors, force sensors, and user information) into a single unit. CAN serial systems also have the potential to control multiple motors but such systems are subject to time lags when communicating with multiple motors. Given such a characteristic, the CAN system does not hold as much potential for use in a haptic system compared to the FPGA system. This is because time lags are especially detrimental for applications that seek to produce a transparent experience between a user and a tele-operated robotic hand system. However, the price for the advantages associated with the FPGA system is the limited available space in which to program the functions necessary to control all 21 motors, which are completely controlled within the FPGA system due to the lack of a

commercial microcontroller with the ability to directly control torque and read resolver signals.

The space restriction aspects associated with FPGA systems are especially important to consider because BLDC motor commutation techniques, such as SVM, which are characterized by higher performance attributes, traditionally use embedded operations that would require a substantial amount of space on an FPGA system (e.g. lookup tables of the space vector modulated profiles, floating point operations, trigonometric function, simple division, etc.).

The novelty associated with this thesis includes the selection of complementary products necessary to accommodate the unique application of haptics within a radiological environment and the application of unique techniques to guarantee the associated operations are performed at a sufficient rate to produce effective haptic performance.

1.2 Thesis Layout

This thesis is organized such that it discusses the background, implemented technology, results, and then future work to fully realize this system.

The background section discusses:

- Radiation environment effects on electrical equipment including circuit board structures and difficulties associated with maintenance activities that drive the need for more dependable equipment.
- Force-feedback theory as it applies to the robotic hand which will implement the brushless motor system described in this thesis.
- Brushless motor theory including a discussion of the three phase construction as it applies to the employed motors.
- Resolver theory as it applies to conventional structure associated with employed device.
- Brushless motor driver circuitry theory.
- Brushless motor commutation (trapezoidal, sinusoidal, space vector modulation).
- Field Oriented Control theory.

The implementation section discusses the hardware and software required to implement the above mentioned theories and includes:

- The general components (haptic hand user interface and associated robotic hand) implemented in this force-feedback system.
- The employed brushless motor and the criteria that drove its selection.
- The employed brushless motor driver and the associated hardware (microchips, electrical component, PCB based on microchip application schematic) and software (LabVIEW programs) necessary to achieve its implementation.
- The employed resolver.
- The employed circuitry required to read the employed resolver (microchips, electrical component, PCB board design based on microchip application schematic) and its suitability for this application.
- The LabVIEW field oriented controller that would be applicable for this application that was extracted from a National Instruments forum post as presented and developed by Dr. Ben Black from National Instruments.
- The proposed three phase current measurement system based on single bus signal.

The results section discusses the implemented system's ability to accommodate the performance criteria imposed by the haptic and radiological constraints, including:

- Smooth and reversible rotary motion (extensive discussion on the implications of this simple performance exhibition is included in the results section).

This thesis reports future work required to fully realize this system's application in the proposed haptic application including:

- The modification of an acquired LabVIEW Field Oriented Control program acquired from National Instruments to be applied for torque control rather than speed control.
- The measurement of the three phase currents from a single bus signal current profile via its correlation to the applied PWM signals and how the system dynamics need to be considered via adjustments in the PWM period.
- Experiments to validate that the proposed system will drive the haptic system adequately when performing tasks such as grasping and manipulation.

1.3 Background

1.3.1 Radiation Environment Limitations

Radiation environments influence both the mechanical and electrical performance properties of materials. The primary phenomenon that drives this influence is that the energetic radiation particles and photons produce atomic displacements, electronic excitations, or both [2]. These actions can disrupt a semiconductor's crystal structure or damage the insulator resulting in leakage. Such damage can shift voltages within the circuit and cause devices which are designed to turn on/ off at well-defined operating points to function improperly [3].

These phenomena are applicable to the circuitry associated with the Hall effect sensors and encoders employed in typical motor applications. Table 1 [4] provides guidance with regard to the types of systems that can be employed with respect to radiation levels. As shown effect, anything above a category D level recommends that no electronics be used.

Table 1: Indicative Radiation Scale for Typical Nuclear Tele-Operated Applications [4].

Table 1
Indicative radiation scale for typical nuclear teleoperated applications

Category	Dose rate (Gy/h)	Total dose (Gy)	Type of intervention
A	<0.01	<10	Most maintenance work in low radiation environments. Light decontamination operation. Teleoperation is an alternative to hands-on work. No radiation hardening is needed.
B	<10	<1000	Most decontamination work. Interventions on primary loop components. Some cell work. Teleoperation is required. Special material choice. Rad-hard electronics available.
C	<1000	<1 MGy	Reactor vessel intervention. Dismantling work. Hot cell tasks. Very narrow material and electronics choice.
D	<10 000	<1 MGy	In-core and fusion reactor maintenance. Fuel manipulations. No electronics. Critical material choice.

To some effect, the research associated with this project is attempting to circumvent this limitation and identify a means by which electric motors with electronic driver and control can be employed in such an environment. In order to achieve this end, *special set-ups are therefore needed, with remote electronics, radiation-hardened transducers, and adapted signal processing. Resolvers are more reliable under radiation than their optical counterpart. A gamma radiation tolerance up to 10 MGy (which reaches far into category D as identified in Table 1) is achievable with proper design of the coils and the supply cables [4].*

ASTM standard C1615-10 [1] provides exceptional guidance with regard to implementing technology, including electronics and motors, in a radiation environment. Like the resolvers, discussed above, BLDC motors have a similar internal makeup (e.g. winding and lack of brushes) and the standard identifies them as being applicable in radiation environments due to their high power density, reversibility, and long life in high irradiation fields for applications including robotics and precision positioning. As such, these components have similar robustness in a radiation environment as resolvers.

The lack of brushes in BLDC motors also limits the amount of impurities that are undesirably introduced into some radiological environments. This is not the case for conventional brushed DC motors which tend to produce graphite dust [1]. These impurities are disadvantageous because some of these environments have purity restrictions and the brush shavings are very difficult to clean up from such environments. The difficulties associated with cleanup are also a huge factor in general system maintenance (including motor change-out). Because BLDC motors are more robust and reliable than their brushed DC motor

counterpart they are more ideal in this application. It is also recommended in reference [1] that BLDC motors be used in applications where horsepower requirements are below 3750 watts. For power levels above 3750 watts, it is recommended that an AC motor be used. Motors in the recommended applications for hot cells are presented in Table 2.

Table 2: Motors and Their Recommended Applications in Hot Cells [1]

TABLE 1 Motors and Their Recommended Applications for Hot Cells

Type	Horsepower (1 Hp = 750 watts)	Typical Size (dia.)	Application	Comments
AC Shaded Pole 115/208-2300-VAC	0 -1	3″ – 6″	Fans and blowers	• Inexpensive • Non reversible • Light duty • Low starting torque • Simple controller • Non-precision positioning • No position or velocity feedback • Applications requiring small motors
AC capacitor start, 115 VAC, single phase	½ - Up	6″- Up	Pumps and blowers	• Inexpensive • General purpose motor • Fixed speed • High current per horsepower • Moderate to high starting torques • Light duty
AC Three-phase 208-230 VAC	½ - Up	6″ - Up	pumps, blowers, fans, compressors, agitators, hoists, general purpose motor	• Inexpensive • Reversible • High starting torque • Requires three-phase source • Generally fixed speed, but variable speed can be achieved by using variable freq.drive (VFD)
DC brush (permanent magnet)	1/16 - 1	1″ – 8″	Variable speed drives, mixers, conveyors, high torque small gearmotors	• Can be low voltage • Inexpensive motor and controller • Variable speed • No position feedback • Non-precision positioning • Brushes may require replacement with high altitude brushes for longer life
DC Brushless – (permanent magnet/servo)	1/32 - 5	1″ - 8″	High torque small gearmotors, robotics, linear actuators	• Compact • Expensive • Precision positioning • Reversible • Velocity control • Can be low voltage • Long life in high radiation fields if the drive electronics are moved out of cell
DC Shunt-Wound	5 - Up	6″ - Up	Larger loads requiring variable speed, direction, and position control	• Variable speed/torque control available • Larger motors operated at low speeds require forced cooling • Limited use
Stepper (Brushless DC)	¼ – ½	3″ - 5″	Robotics	• Consumes power to hold position (heat buildup) • Requires feedback for closed-loop position indication • Requires computer/micro processor control system • Can be operated open-loop • Expensive motor controls
Universal AC or DC	Fractional	3″ - 6″	Power tools and vacuum cleaners	• High torque available in a small motor • Inexpensive • Low efficiency • Brushes may require replacement if motor is used in low moisture or inert gas environment • Normally powered by 120 VAC

1.3.2 Force-Feedback Theory

The force-feedback (haptic) system, in which the product of this thesis will be employed, is embedded in the system generated and patented by the author [5] (Figure 1). The left portion of this figure is the user interface (additionally shown in Figure 2 and Figure 3) that monitors the configuration of the user's hand and communicates the forces experienced by the robotic hand (right portion of the figure) back onto the user. The user interface used brushed DC motors as it will be used outside of the radiation environment and its hardware is not subject to the same radiological concerns as the robotic hand shown on the right of Figure 2. The robotic hand on the right of the figure (also shown in Figure 4 and Figure 5), will employ the BLDC motor, resolver, resolver to digital converter, brushless motor driver, and proposed torque control presented in this thesis.

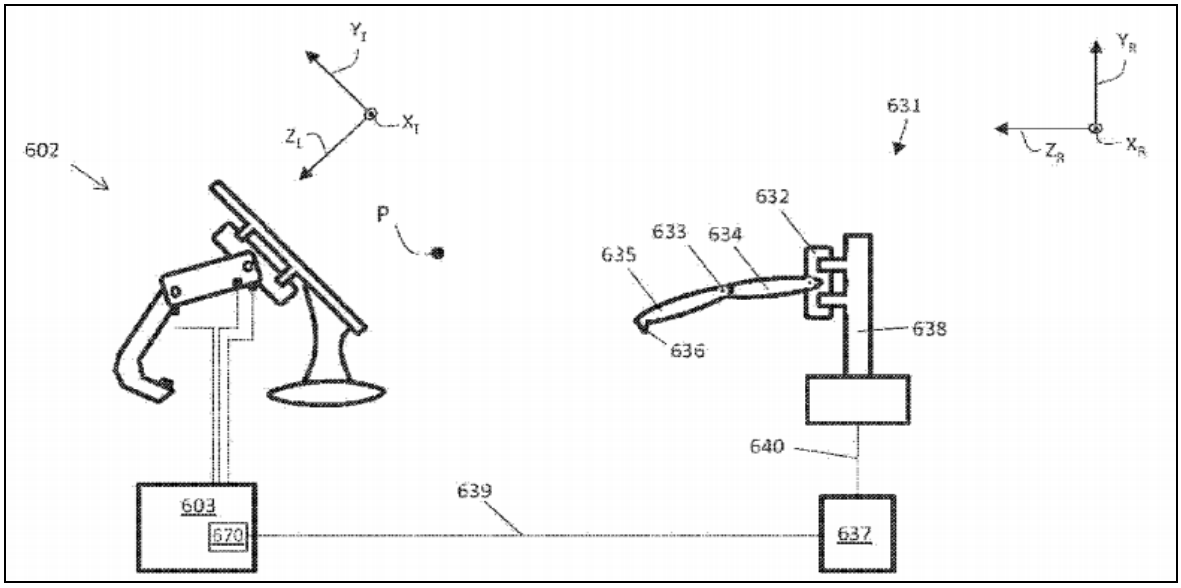

Figure 1: Force-Feedback Robotic Hand System.

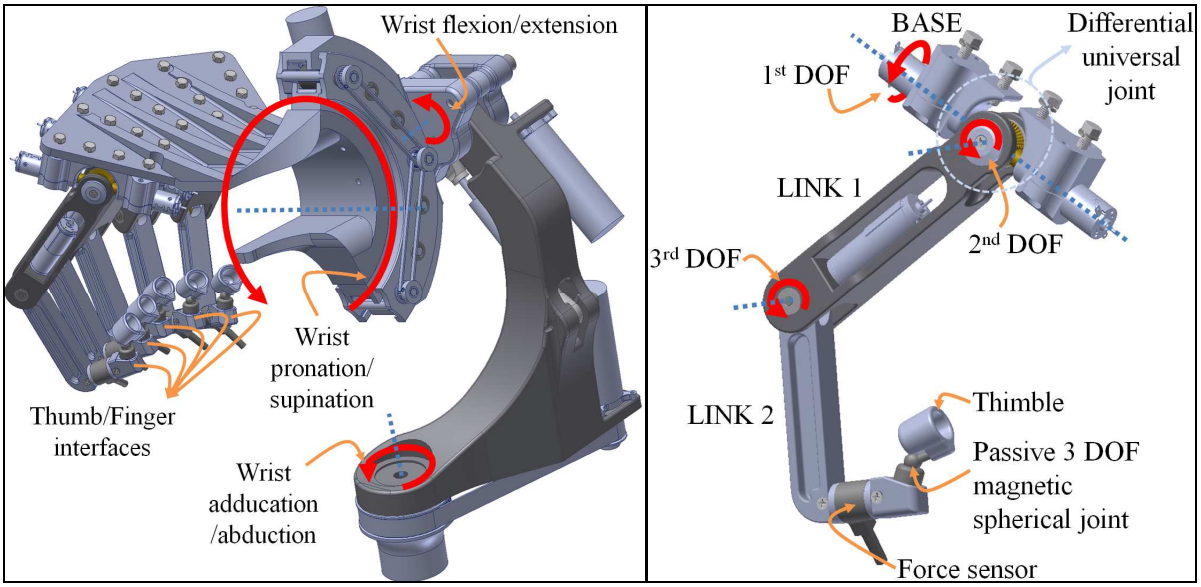

Figure 2: CAD Model of Developed Haptic User Interface Using Brushed Motors and Force Sensors.

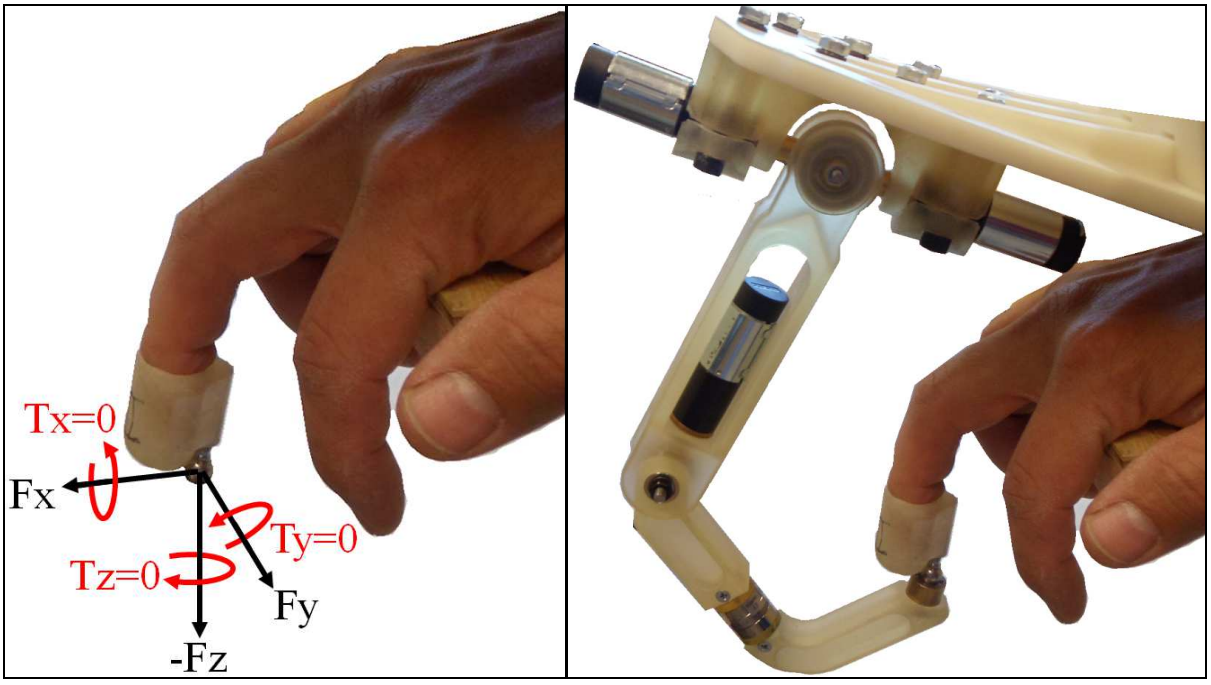

Figure 3: Developed Haptic User Interface as Shown Being Employed by User.

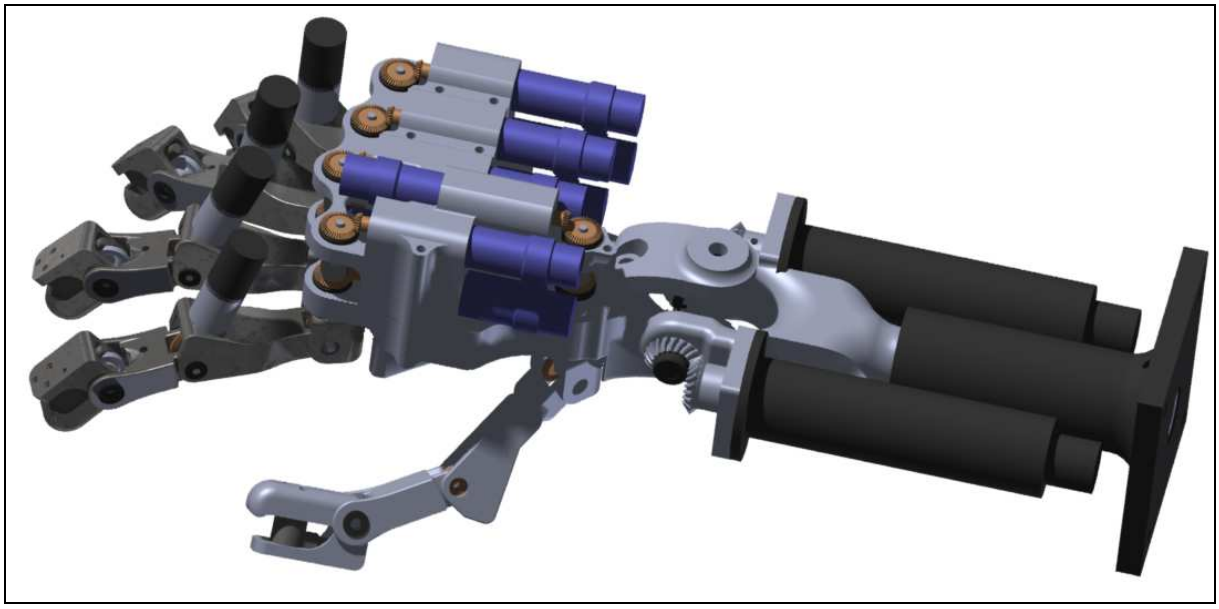

Figure 4: CAD Model of Developed Robotic Hand Employing BLDC Motors.

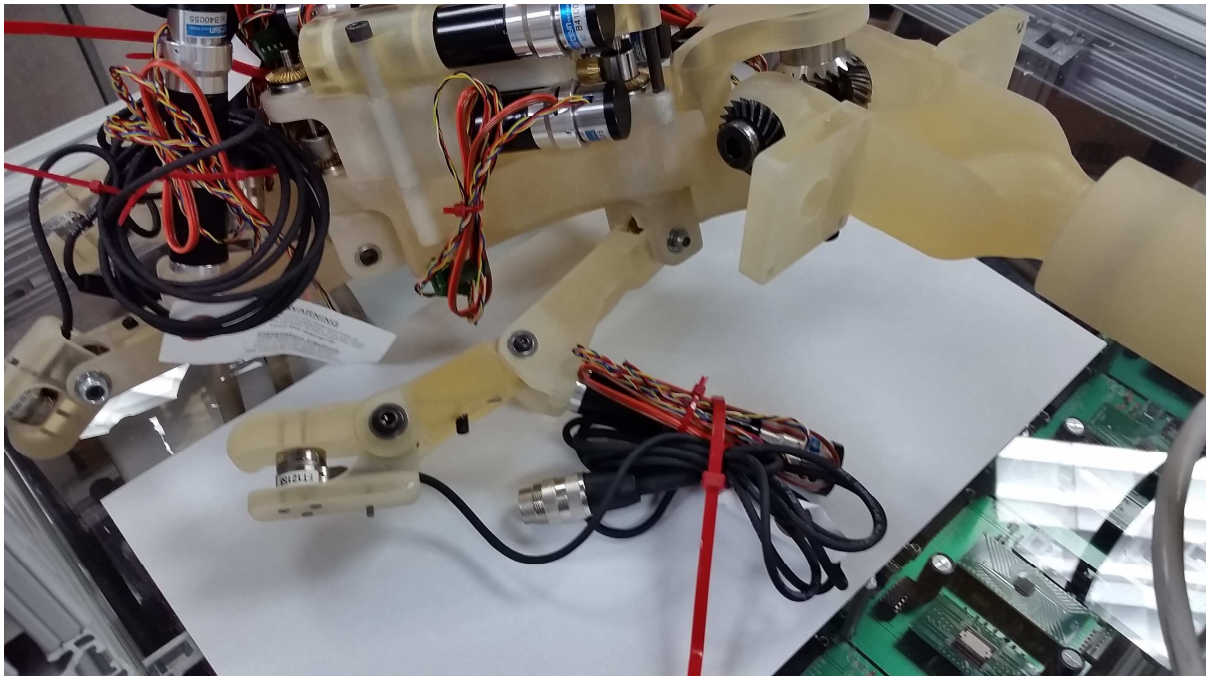

Figure 5: Developed Haptic Robotic Hand Employing BLDC Motors.

Feedback control as it applies to the device will appropriately utilize the general n-link manipulator dynamic equation as shown in (1). In (1) $M(\theta)$ is the inertia matrix, $C(\theta,\dot{\theta})\dot{\theta}$ is the Coriolis and centripetal torques, $V(\theta,\dot{\theta})$ is the friction (coulomb, viscous, etc.) related torques, $G(\theta)$ is the gravitational related torques, and τ is the control torque. The employed control law will be that shown in (2). Extensive description of the system, including a thorough survey of the type of haptic systems available in the associated control algorithm implemented to achieve the haptic behavior, is included in references [6] and [7].

$$M(\theta)\ddot{\theta} + C(\theta,\dot{\theta})\dot{\theta} + G(\theta) + V(\theta,\dot{\theta}) = \tau \tag{1}$$

$$\tau = J^T\left(K_1 f_e + f_{des_{L,NL}}\right) - \hat{G}(\theta) - \hat{V}(\theta,\dot{\theta}) \tag{2}$$

Additionally, one of the most important aspects of haptic systems, as it pertains to this thesis research, is that the system must exhibit a reliable 1kHz communication rate in order to appear seamless to the user [8]. This requirement drives the system to perform at a frequency higher than this (without delays) in order to produce reliable performance.

1.3.3 Resolver Theory

The primary components of a resolver, like the brushless motor, are the rotor and stator. The resolver implemented in this thesis is a transformer consisting of three windings, one on the rotor and two on the stator (known as a classical resolver as shown in Figure 6). The rotor winding is supplied an AC sine wave input and depending on the position of the rotor relative to the stator the voltage across each of the two secondary windings will be scaled by a factor of either cosine or sine of the rotor angle. The equations relating the input to the output are shown in Figure 6 and the graphical representation of these equations from both the resolver vendor and the resolver to digital converter vendor are shown in Figure 7 [9] and Figure 8 [10] (both figures are included to validate both resolver and the resolver-to-digital converter produce/read similar signals).

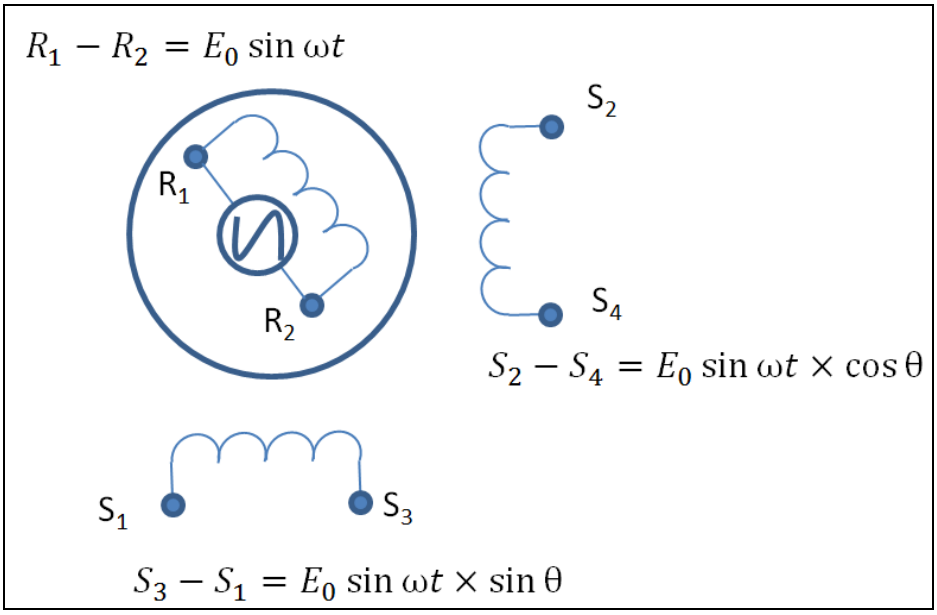

Figure 6. Primary Components Associated with Classical Resolver.

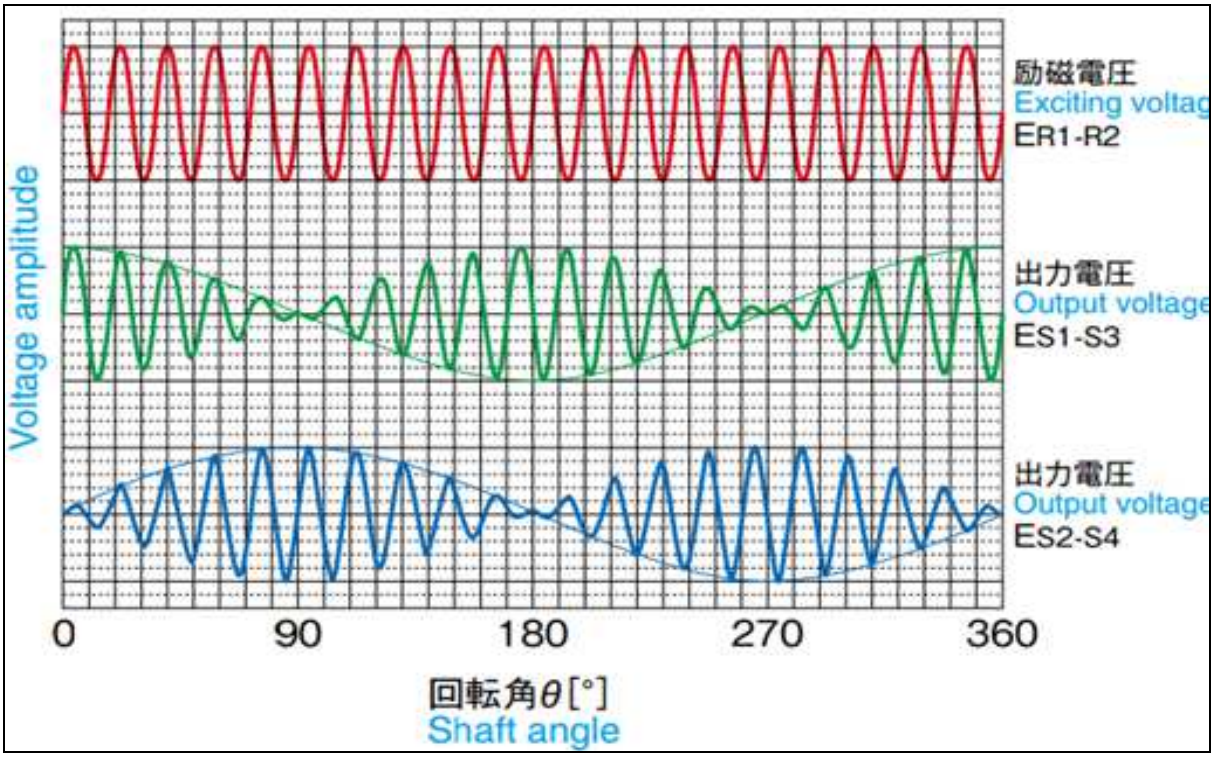

Figure 7. Characteristics of Excitation and Output Voltages as Supplied by Employed Resolver's Vendor [9].

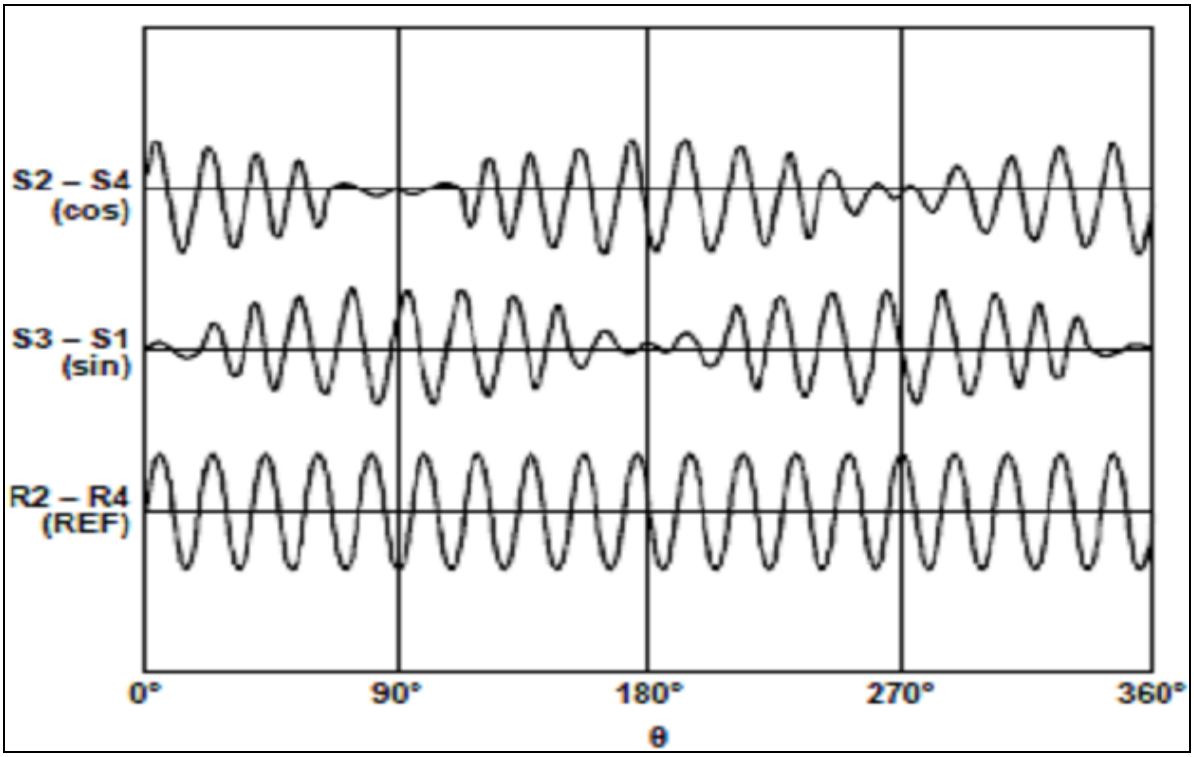

Figure 8. Characteristics of Excitation and Output Voltages as Supplied by Employed AD2S1210 Resolver to Digital Converter [10].

Figure 7 also includes a larger sinusoidal wave over the high frequency wave which represents the ratio between the outputs and the input excitation signal. The overall angle can be extracted by taking the inverse tangent of the two signals divided by one another. This process is shown in the following equation.

$$\theta = \arctan\left(\frac{S_3 - S_1}{S_2 - S_4}\right) \tag{3}$$

1.3.4 Resolver Signal Reading Theory

Because the resolver is an analog system, reading the position requires a device capable of reading such signals. However, current data acquisition systems are primarily comprised of digital inputs/outputs because these signals are able to communicate information at much lower voltages and currents, thus requiring less substantial hardware than analog inputs and outputs.

If a resolver were to be directly operated, up to two analog outputs and four analog inputs would be required. However, there are resolver-to-digital chips available which provide the resolver with a sinusoidal analog input, read the corresponding analog output data, and convert the data into a digital signal. As is true with any digital chip the format complexity required to communicate with the device depends on the device. However, what is consistent is that these chips are also subject to the laws of physics and also exhibit dynamic responses within them. Thus when communicating with these devices it is important to recognize that in order to send/receive a digital signal from such a device they must wait for the dynamics to settle out in order to achieve more reliable performance.

However, to the benefit of these digital chips, most mechanical systems with which these chips can be implemented possess mechanical time constants much longer than those embedded within the chip. This affords one to send/receive a signal to/from such a device, wait for the dynamics associated with that action to die out, write/read the steady state signal, and proceed to the next step (such as reading the next bit in a 10 bit number) an enormous number of times before the frequency of the data that they communicate has an adverse effect on the overall system itself. This behavior holds for resolver-to-digital converters.

1.3.5 Brushless Motor Theory

The primary components as well as the supporting components associated with the Maxon EC brushless motor employed in this thesis can be seen in Figure 9 [11]. BLDC motors consist of two primary components, the stator and rotor (permanent magnet). The rotor embodies a permanent magnet and the stator is comprised of a three phase winding. The various commutation methods associated with BLDC motors are dependent on the rotor position in order to apply the proper fluxes to the proper phases in order to generate the proper movement.

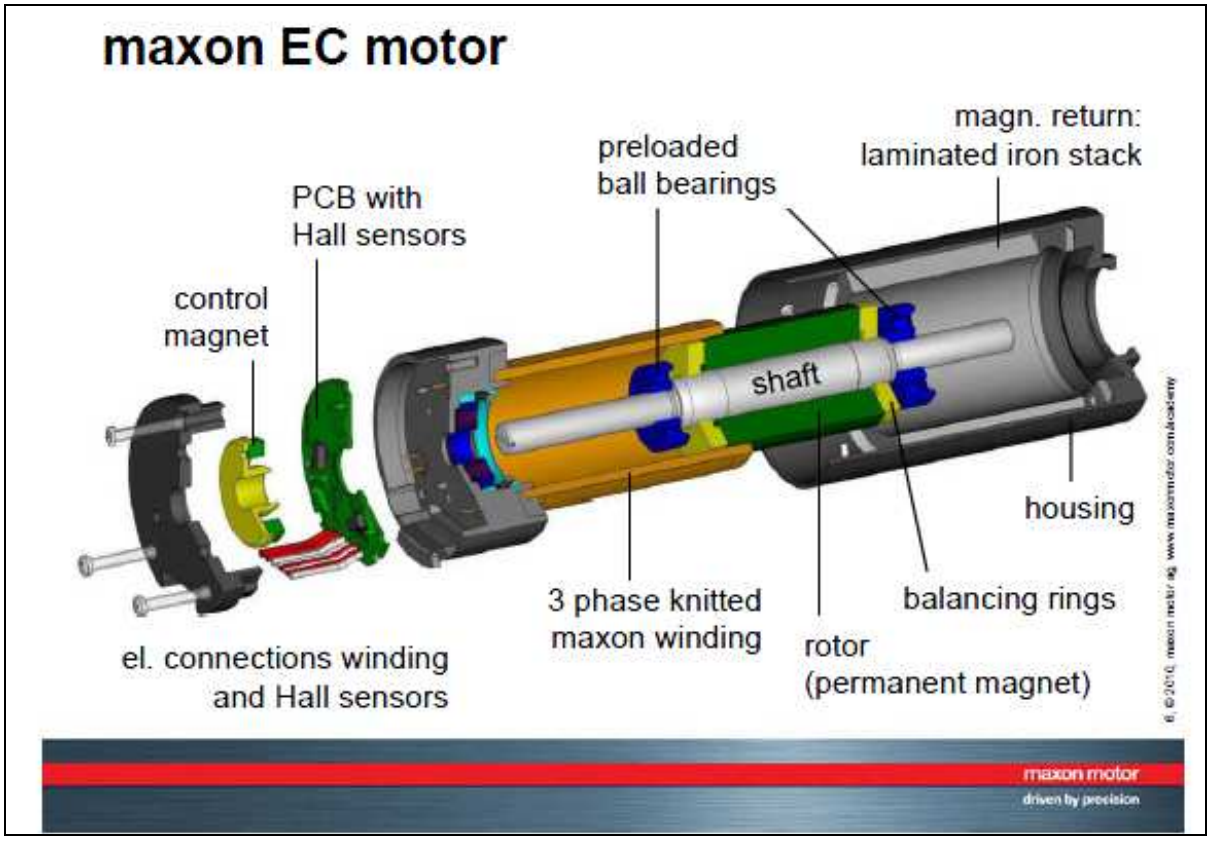

Figure 9: Primary BLDC Motor Components [11].

The advantages of the BLDC motor over the conventional brushed motor according to references [11] and [12] consist of:

- Excellent torque characteristics (similar torque profiles as conventional DC motors)
- High power density (BLDC motors have the highest running torque per cubic inch of any DC motor).
- Extremely wide speed range (A BLDC motor can operate at speeds above 10,000 rpm under loaded and unloaded conditions).
- Outstanding controllability.
- Responsiveness and quick acceleration (Inner rotor BLDC motors have low rotor inertia, allowing them to accelerate, decelerate, and reverse direction quickly).
- High reliability/lifespan (BLDC motors do not have brushes, meaning they are more reliable and have life expectancies of over 10,000 hours. This results in fewer replacements and repairs with less overall down time).

Disadvantages include:

- More complex three phase control which will be discussed in section 1.3.7: Brushless Motor Commutation Theory.

As included in the lists of advantages and disadvantages, BLDC motors have relatively good power density, reliability, and responsiveness. However, these advantage are more applicable for the motors being implemented in higher speed applications rather than slow speed (if not fixed position) torque control applications such as the target haptic finger. As such, the performance of the motor at stall conditions is an important consideration. In the stall condition one or more of the phases can experience sustained currents that may overheat and damage the device. Given this characteristic, BLDC motor vendors provide a plot (Figure 10 [13]) which outlines the recommended operating ranges for continuous and short term operation thus recognizing that stall conditions are allowable but only for short durations.

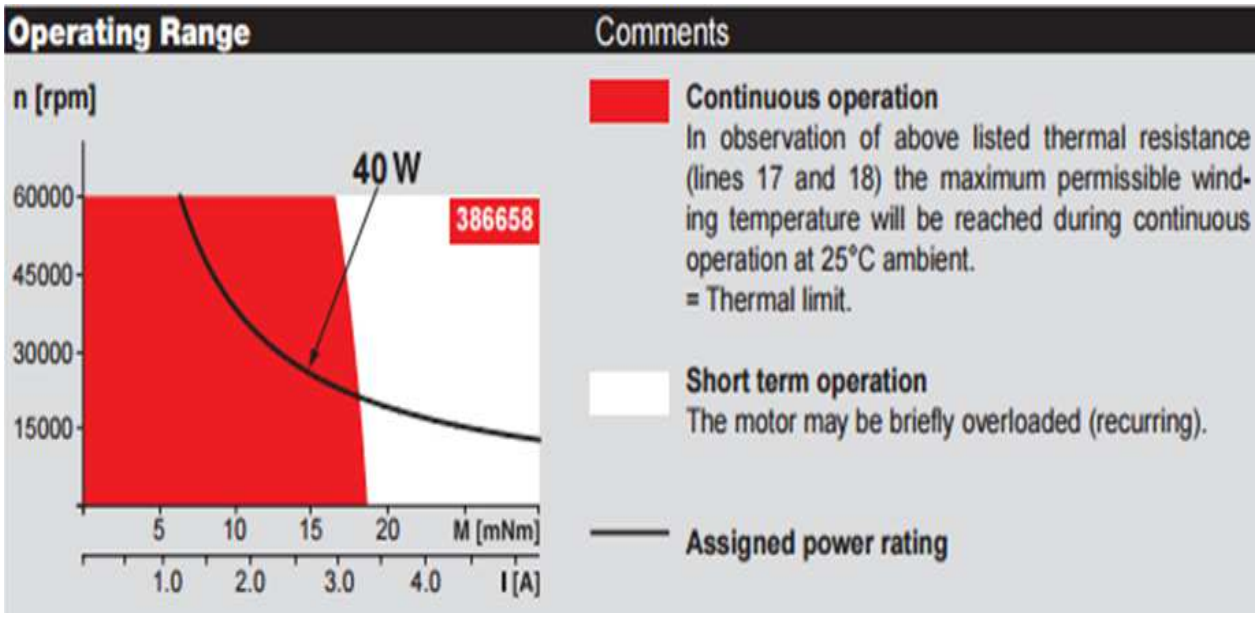

Figure 10: Operating Range Associated with a Sample BLDC Motor [13, pg. 209]

In addition to operating range plots, BLDC motor vendors also report motor characteristics that can be used to size the motor based on application conditions. Some important characteristics include:

- Continuous motor torque
- Stall torque
- Speed limitation
- Nominal voltage
- Speed torque gradient
- Torque constant

1.3.6 Brushless Motor Driver Circuitry Theory

In order to drive a three phase brushless motor, a circuit implementing six independent half bridges is required. Each bridge is comprised of a combination of two FETs (1 p-type and one n-type). A graphic of the three independent half bridge layout of the switching amplifier implemented in this research is shown in Figure 11.

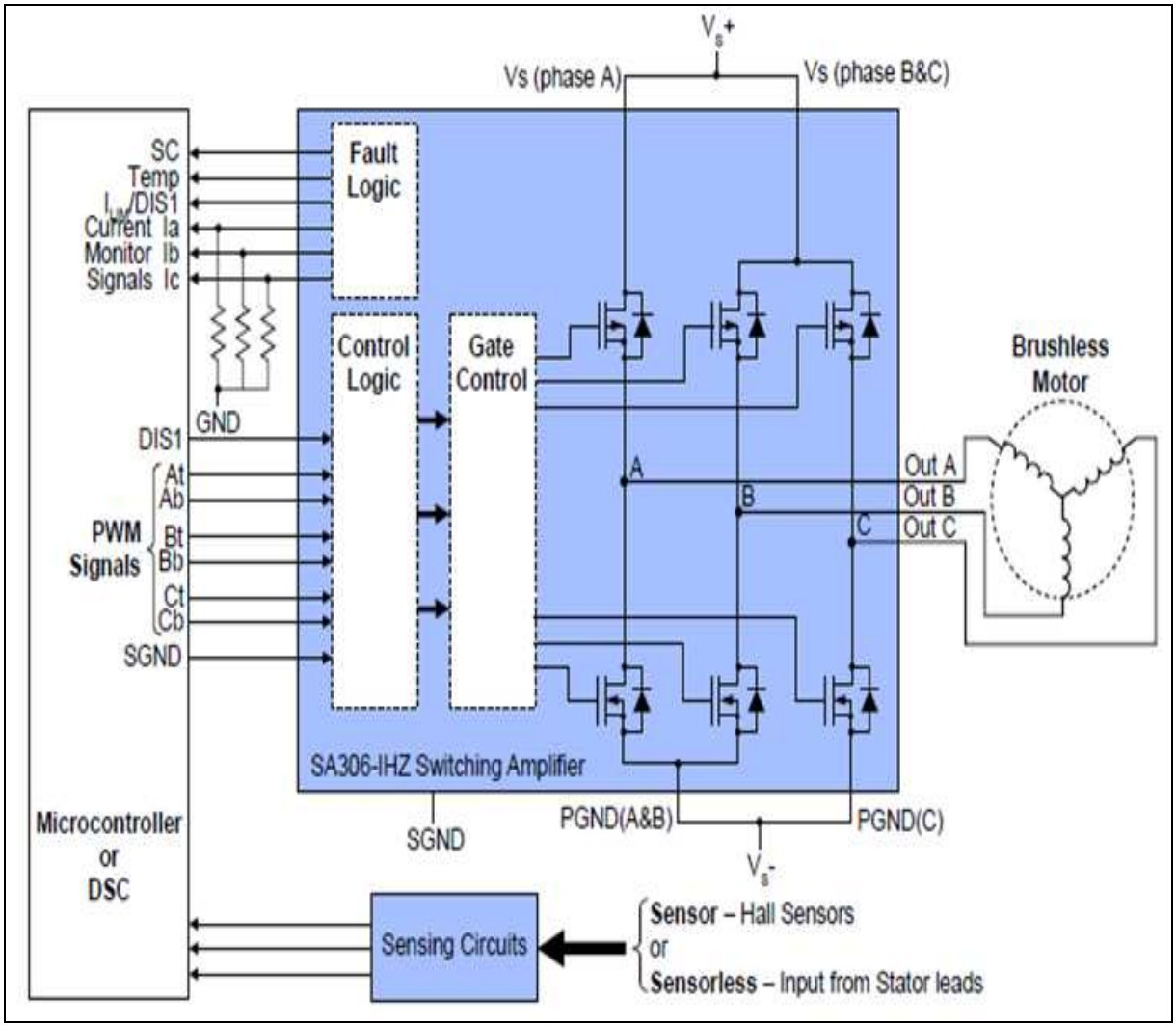

Figure 11: General SA306-IHZ Switching Amplifier Layout, Including the Three Independent Half Bridge Circuits to Drive the Brushless Motor [14].

Combinations of these FETs are implemented to provide magnetic imbalance within the brushless motor. These combinations are driven by PWM signals, of which the widths of each phase are driven by the strategies discussed in section 1.3.7. These combinations route the current through the appropriate phases. An example of the FET on/off activations is shown in Figure 12 and can be viewed as four different segments:

- Segment 1: 1H, 2H, 3H active
- Segment 2: 2H, 3H, 1L active
- Segment 3: 2H, 1L, 3L active
- Segment 1: 1H, 2H, 3H active

It can also be seen in Figure 12 that there is a slight delay between when a high FET becomes active and its corresponding low FET becomes inactive. If both a high FET and low FET, in the same phase, are active at the same time, a short can be created, resulting in current being shot though the FETs. The resulting high current can cause damage to the FETs.

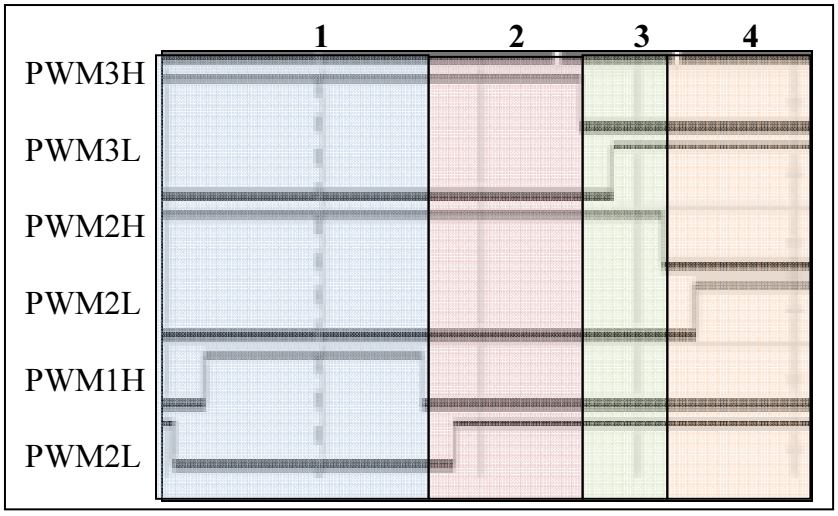

Figure 12: Example FET On/Off Activation Profile as they Pertain to the Driver's Three Half Bridge Configuration. [22].

While surveying available technology for brushless motor drivers two versions of the three half bridge circuit were found which employ discrete components [15][16]. The schematics associated with these systems (Figure 13 and Figure 14) show the three half-bridges fabricated with discrete components. Implementing a driver comprised of discrete components would provide more flexibility when designing a circuit in order to accommodate the idiosyncrasies with a motor system (e.g. high current levels) that may not be accommodated by a commercial product such as the single-chip driver referenced in Figure 11.

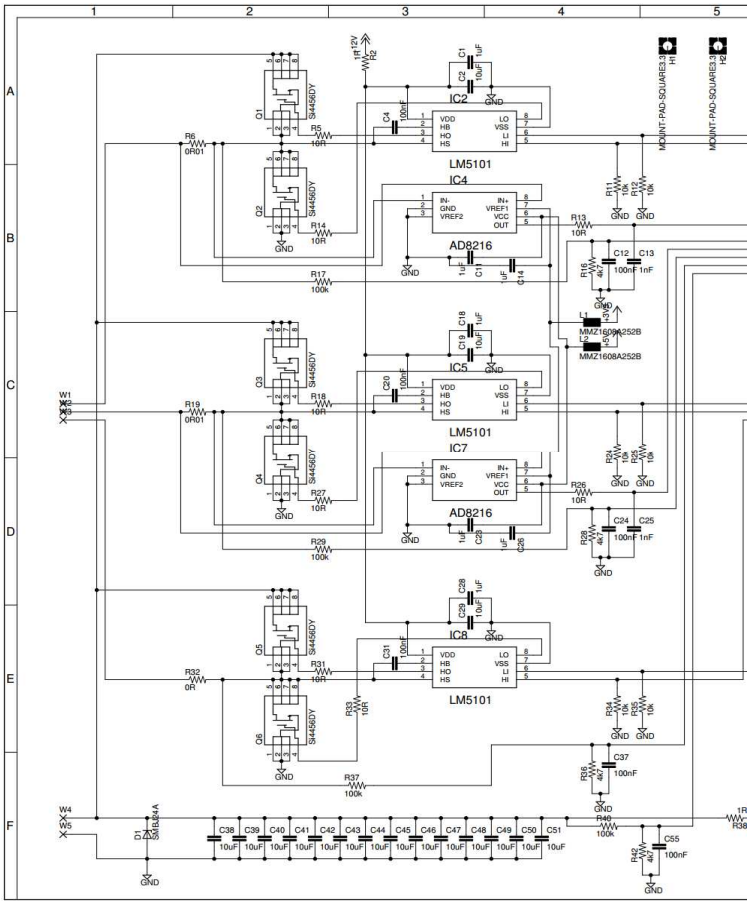

Figure 13: Brushless Motor Controller – Dan Strother's Design Schematic [15].

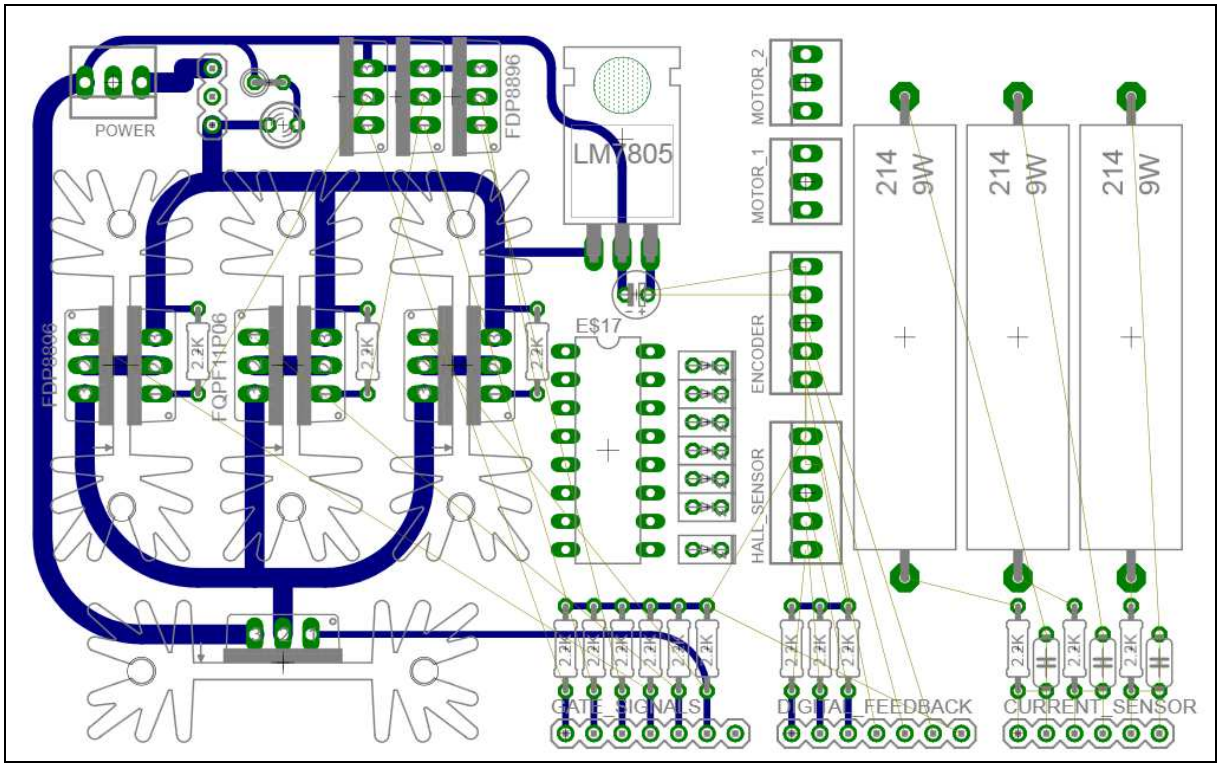

Figure 14: Brushless Motor Controller – Schematic Associated with Dr. Ben Black Design [16].

1.3.7 Brushless Motor Commutation Theory

There are several means to operate a BLDC motor using the three independent half bridge circuit layout discussed in section 1.3.6. The ones considered for this research include the six phase (trapezoidal or block), sinusoidal, and SVM. Each of these techniques relates the rotor position to each of the stator phases and identifies a flux that will pull on the rotor and generate torque. These commutation theories range from a relatively simple but less efficient (six phase), to more complex but smoother and more efficient (sinusoidal), to most complex but still smooth and most efficient by about 15% (SVM). More details associated with each of these techniques will be discussed in the following sections.

1.3.7.1 Six Phase (Trapezoidal) Commutation

Six phase trapezoidal commutation divides motor into six phases per revolution. Within each phase the current is directed through the three independent half bridge circuit by turning on/off the high/low sides of each circuit such that the rotor observes the appropriate flux that leverages the rotor to rotate. Although simple and effective, the discrete nature of this technique provides a varying torque throughout the motor motion resulting in motion that is not as smooth as the other commutation techniques discussed below. Figure 15 and Figure 16 demonstrate the implementation of trapezoidal control given position inputs from Hall sensors.

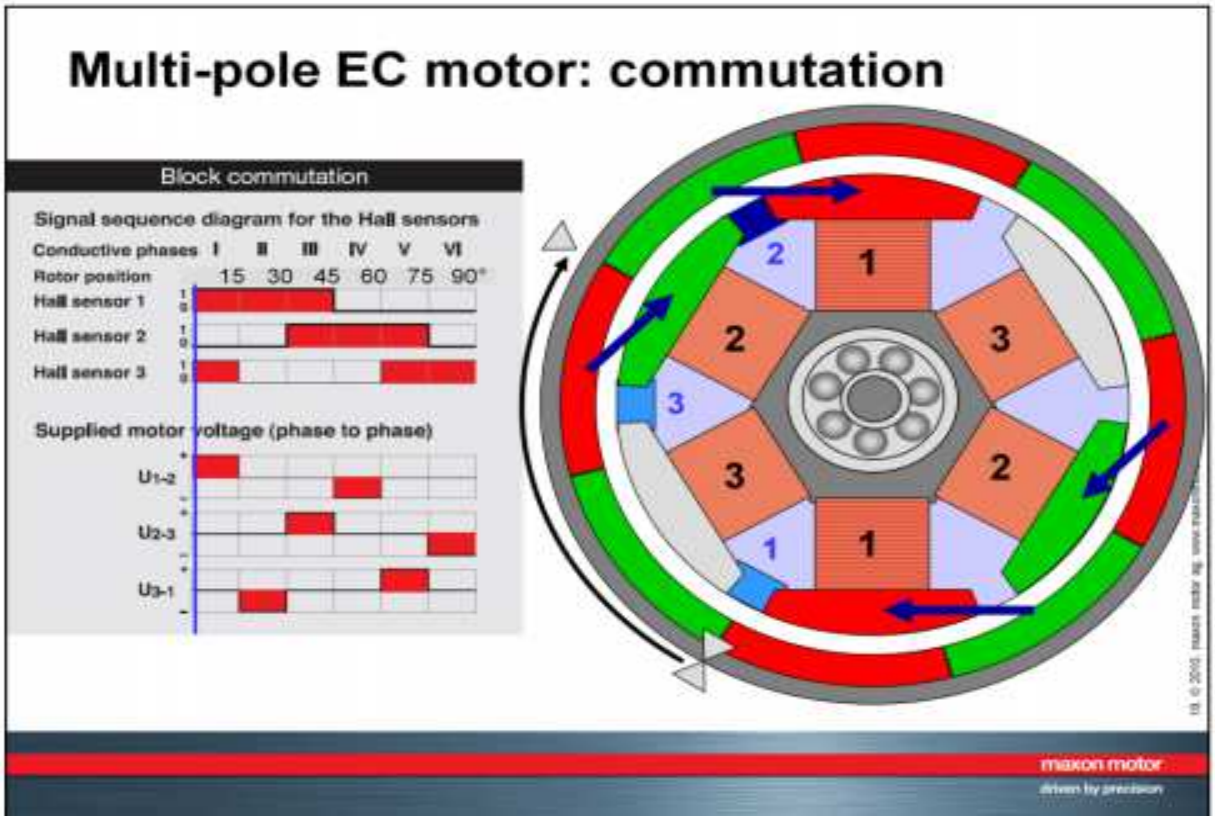

Figure 15. Trapezoidal Commutation of a Maxon Multi-Pole EC Motor Relating Hall Sensor Response to Circuit Output [11].

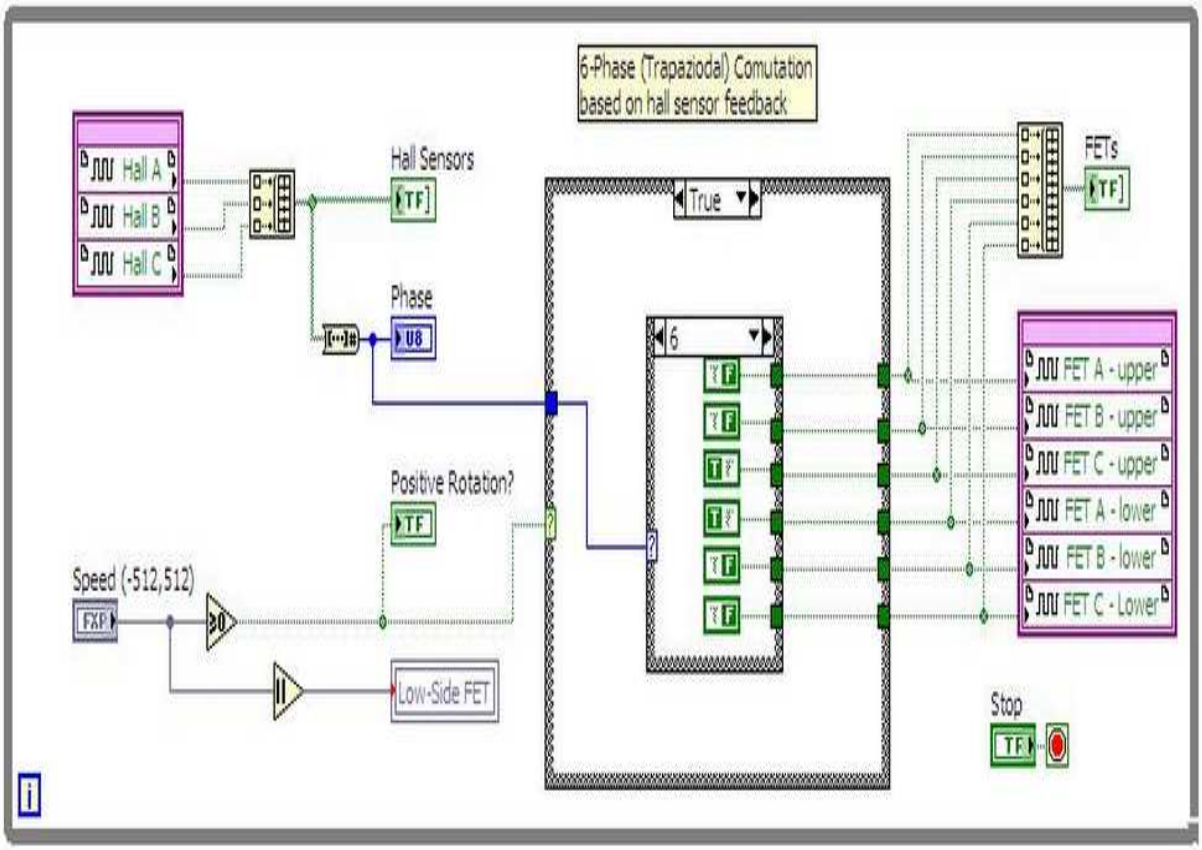

Figure 16. Trapezoidal Commutation Technique Implemented in LabVIEW Relating Hall Sensor Response (Top Left), to a Phase Which Activates the Appropriate FET Activation Combination in the Condition Block Which Feeds into the Circuit Outputs [16].

In Figure 15 and Figure 16 the input provided to the motor is achieved via Hall sensors. Depending on which one or two of the three Hall sensors is active drives which FETs are active. For instance, in Figure 15 if Hall sensor 3 is active the rotor is in conductive phase VI and FET B upper and FET C lower are active. Figure 16 shows inputs from the Hall sensors which identifies the rotor as being in phase 6 which activates the upper FET C and lower FET A (the full set of conditions for this LabVIEW program is shown in Table 3). As can be seen when comparing these two they are slightly different which can be attributed to a different

Hall sensor arrangement or directionality (clockwise or counter-clockwise), thus it is important to understand the Hall sensor arrangement when applying this strategy. Regardless, the primary means to generate motion in trapezoidal commutation is to activate one high FET and one low FET corresponding with the position of the rotor to get a magnetic leverage to create the torque that causes the rotor to rotate.

Table 3: Trapazoidal Commutation FET Combinations Given Hall Sensor Data.

Hall A	*Hall B*	*Hall C*	*FET A Upper*	*FET B Upper*	*FET C Upper*	*FET A Lower*	*FET B Lower*	*FET C Lower*
1	1	0	OFF	ON	OFF	OFF	OFF	ON
0	1	0	OFF	ON	OFF	ON	OFF	OFF
0	1	1	OFF	OFF	ON	ON	OFF	OFF
0	0	1	OFF	OFF	ON	OFF	ON	OFF
1	0	1	ON	OFF	OFF	OFF	ON	OFF
1	0	0	ON	OFF	OFF	OFF	OFF	ON

1.3.7.2 Sinusoidal Commutation

Sinusoidal control relates the amplitude of current supplied by each phase to the rotor angle. For one rotation the current amplitudes for the three phases represent three sinusoidal profiles that are 120 degrees out of phase from each other as shown in Figure 17. This provides much smoother operation than trapezoidal commutation but also requires more precise rotor position measurement than can be achieved with Hall sensors as further explained in Figure 17.

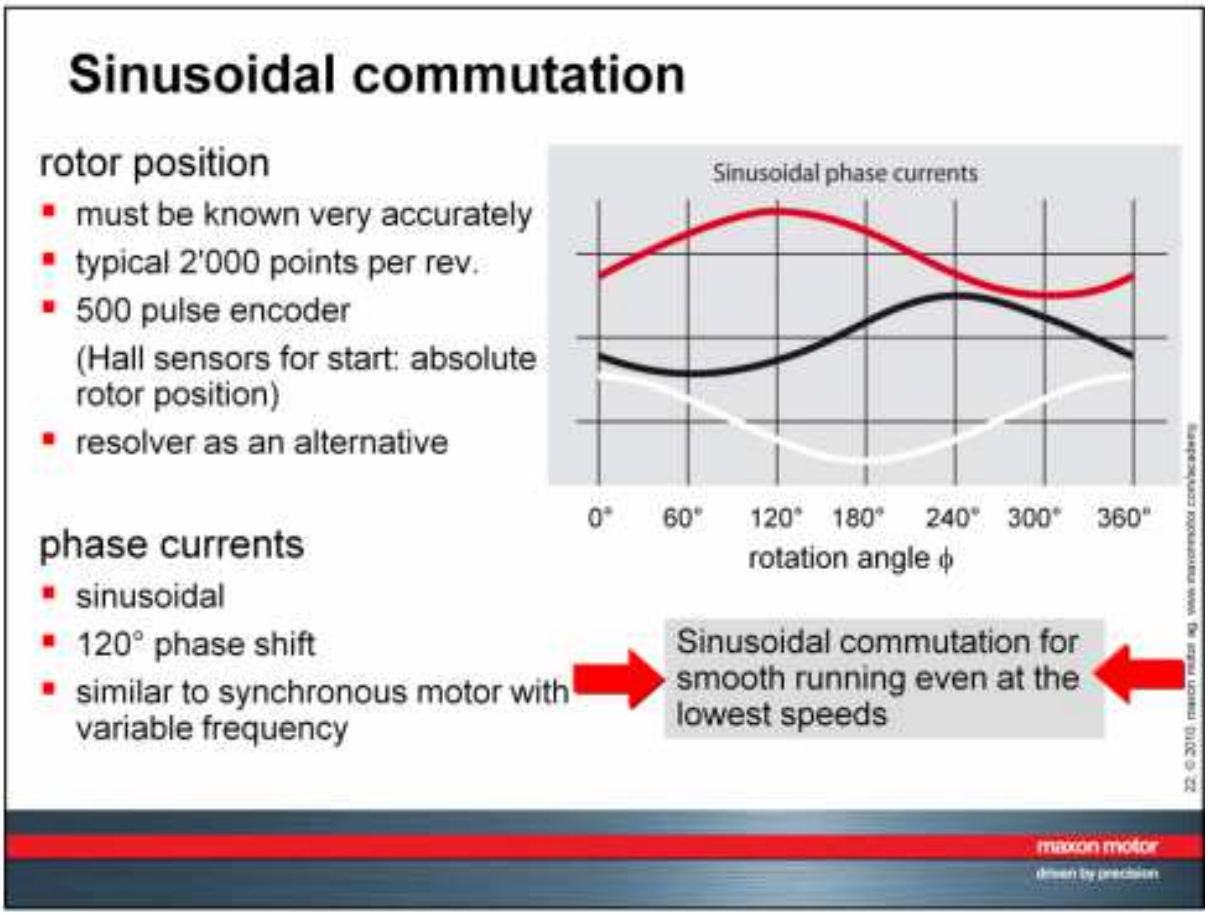

Figure 17. Sinusoidal Commutation of a Maxon EC Motor Relating Rotation Angle to Phase Current Magnitudes [11].

1.3.7.3 Space Vector Modulation Theory

The profile comparison between the sinusoidal and space vector modulated commutation is shown in Figure 18 and Figure 19 [17]. As shown, the space vector modulated profile form in Figure 19 (repeated in Figure 20) has a unique shape. However, when correlated to the line-to-line voltage (e.g. PWM1 - PWM2 → VA – VB), a sinusoidal voltage relationship transpires (which relates to a sinusoidal current profile) as shown in Figure 21.

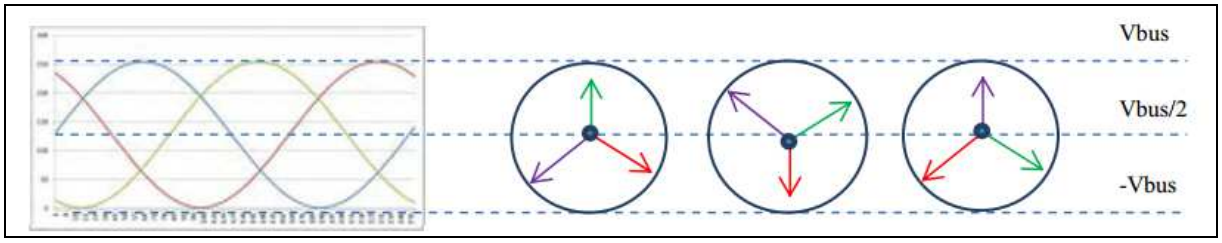

Figure 18: Center Voltage of Sinusoidal Commutation Does Not Float in Space [17].

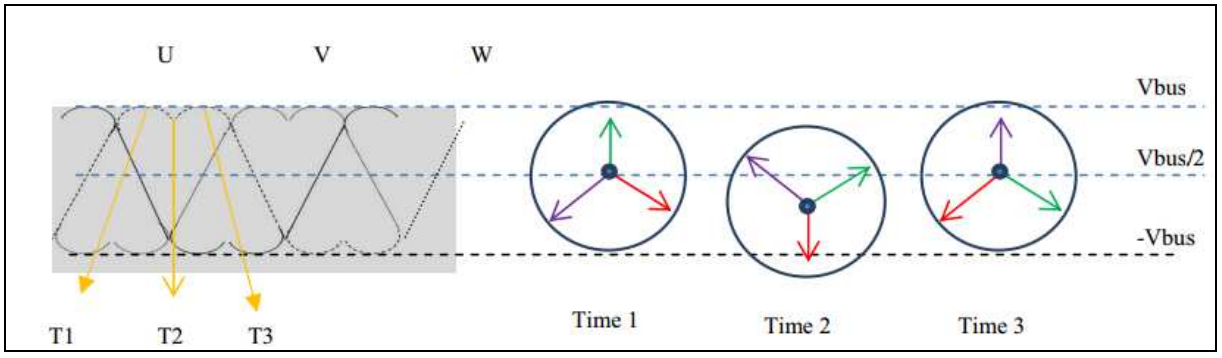

Figure 19: Center Voltage of Space Vector Floats in Space [17].

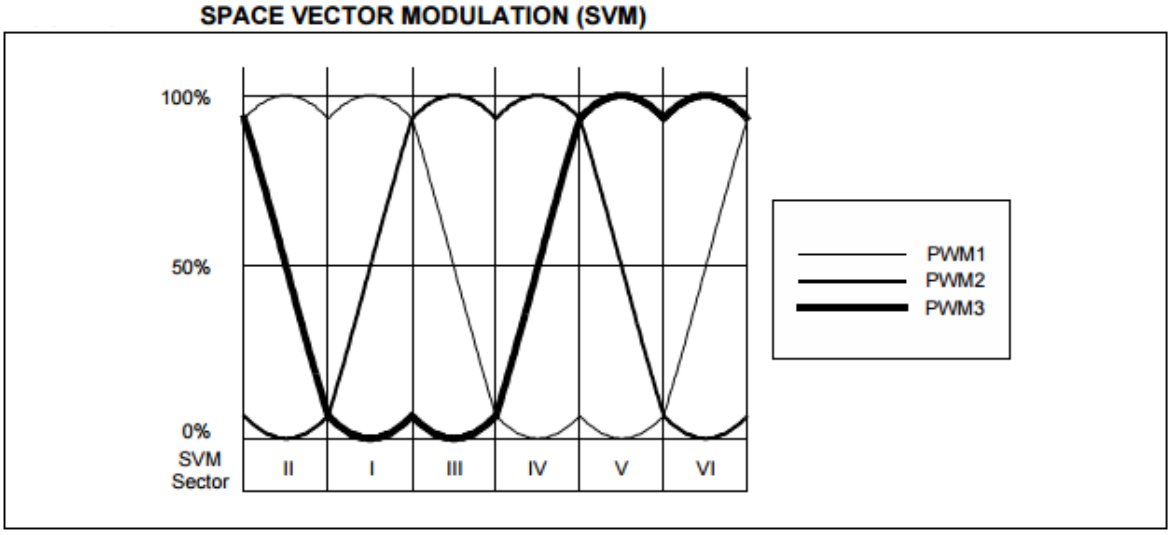

Figure 20: Space Vector Modulation Profile [22].

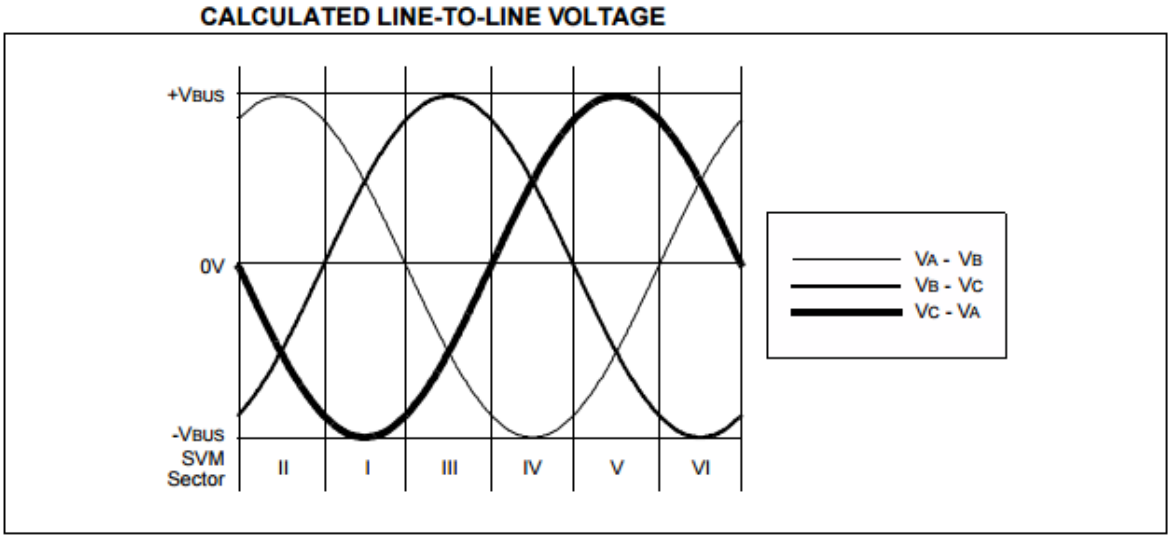

Figure 21: Line-to-Line Voltages Extracted from SVM Profile (Figure 20) [22].

Although the resulting line-to-line form for SVM is similar to sinusoidal commutation the advantages of SVM per references [18] and [19] include less harmonic distortion in the output voltages and motor windings and utilization of 15% more of the available bus voltage due to the floating neutral.

One means of generating the SVM profiles, as implemented by the AVR32710 Microcontroller [20], is the use of (4), (5), Table 4, and Figure 23. In this system the currents or voltages from the systems three phases are transformed into the q and d axis reference frame via the Park's and Clarke's transforms discussed in *Section 1.3.8.2.1: FOC Position Feedback Requirements*. This space is then divided into six sectors as dictated by the six possible non-zero switch combinations than can be achieved by the driver. Table 4 (using (4) and (5) and defining T as 100% duty cycle) then identifies the duty cycle associated with each of the three phases necessary in order to drive the motor in either the clockwise or counter-clockwise direction. An example of the PWM outputs that result from the calculation are shown in Figure 23 where T represents the total period of each cycle and T_a, T_b, and T_c are the periods associated with the a, b, and c phases respectively. The calculations generate the wave forms show in Figure 20. Further explanation associated with this technique is discussed in *Section 2.2: Employed Brushless Motor Circuit and Associated LabVIEW Script.*

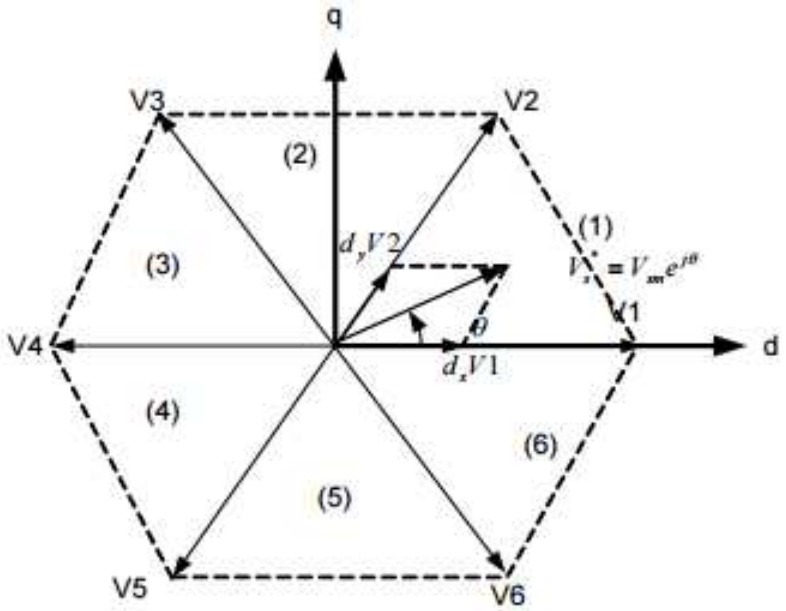

Figure 22: Basic Space Vectors [20].

$$dx = \sin\left(\frac{\pi}{3} - \theta\right) \tag{4}$$

$$dy = \sin(\theta) \tag{5}$$

Table 4: SVM Table from AVR32710 [20].

Sector Number	q	direction = CCW	direction = CW
1	$[0,\frac{\pi}{3}]$	PWM0 = (T - dx -dy)/2 PWM1 = (T + dx -dy)/2 PWM2 = (T + dx + dy)/2	PWM0 = (T + dx + dy) PWM1 =(T - dx - dy) PWM2 = (T - dx + dy)
2	$[\frac{\pi}{3},\frac{2\pi}{3}]$	PWM0 = (T - dx + dy)/2 PWM1 =(T - dx - dy)/2 PWM2 = (T + dx + dy)/2	PWM0 = (T + dx + dy)/2 PWM1 = (T + dx - dy)/2 PWM2 =(T - dx - dy)/2
3	$[\frac{2\pi}{3},\pi]$	PWM0 = (T + dx + dy)/2 PWM1 = (T - dx - dy)/2 PWM2 = (T + dx - dy)/2	PWM0 = (T - dx + dy)/2 PWM1 = (T + dx + dy)/2 PWM2 = (T - dx - dy)/2
4	$[\pi,\frac{4\pi}{3}]$	PWM0 = (T + dx + dy)/2 PWM1 = (T -dx + dy)/2 PWM2 = (T - dx + dy)/2	PWM0 = (T - dx -dy)/2 PWM1 = (T + dx + dy)/2 PWM2 = (T + dx - dy)/2
5	$[\frac{4\pi}{3},\frac{5\pi}{3}]$	PWM0 = (T + dx - dy)/2 PWM1 = (T + dx + dy)/2 PWM2 = (T - dx - dy)/2	PWM0 = (T - dx - dy)/2 PWM1 = (T - dx + dy)/2 PWM2 = (T + dx + dy)/2
6	$[\frac{5\pi}{3},2\pi]$	PWM0 = (T - dx - dy)/2 PWM1 = (T + dx + dy)/2 PWM2 = (T - dx + dy)/2	PWM0 =(T + dx -dy)/2 PWM1 = (T - dx -dy)/2 PWM2 = (T + dx + dy)/2

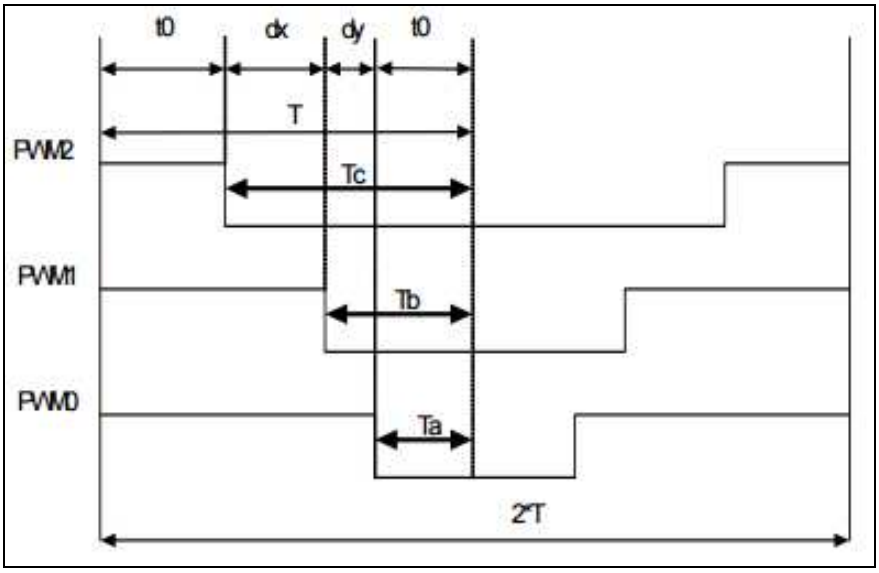

Figure 23: PWM Output Switching Pattern Example (Sector 1 in Table 4) [20].

1.3.8 Brushless Motor Control Theory

1.3.8.1 Desired Control Strategy

BLDC motors can be controlled in either an open-loop or closed-loop manner. Typically open-loop control is implemented when loads are relatively constant or performance is not paramount. An example of such a system would be a fan blowing air where the system is set up such that the circuit supplies a current or sequence of PWM signals (whose characteristics are set around an operating point).

However, in this thesis's haptic application, a high level of precision is required to accommodate both the position and force control conditions. A simple position controller would not be adequate as the system is dependent on force as opposed to geometric position. An example scenario might be where the hand is holding a heavy object with its palm down and the only thing holding it is simple friction contact between the object and the fingers. If position control were employed the fingers would have to deviate from the desired position set point in order for a torque signal to be sent to the motor, in which case the object may slightly deviate from the desired position and the lack of a large torque signal to compensate would allow the object to fall from the finger's grasp. With torque control applied the appropriate amount of force can be applied to the object to maintain the robotic hand's grip on the object.

Because of the application's intense need to control the motor torque, FOC appears to be a suitable technique to control the BLDC motors employed in this application and will be discussed below.

1.3.8.2 Field Oriented Control

Unlike brushed DC motors whose torque is directly proportional to the applied current (regardless of speed), the BLDC motor must transform the currents being delivered to each phase to a form identifying the stator field vectors. One of these (the q vector) is in the direction which produces maximum torque relative to rotor position. This allows one to control the motor torque directly, which is highly desirable in a haptic application. An example of FOC being implemented in LabVIEW is shown in Figure 24.

In the top left of Figure 24 the system inputs a speed set point and compares it to the measured speed in the PI controller. The control output is related to torque and is then compared with the i_q controller. This is the torque current value that is extracted from the Clarke (9-11) and Park's (12-13) transforms executed in the bottom left corner using the system's phase A and B currents and rotor angular position data. In addition to sending the i_q torque to the i_q controller the Park's transform also sends the i_d current to the i_d controller which compares it to a zero set point. The control output from the i_q and i_d controllers are processed back into voltages for the A, B, and C phases using the Inverse Park's (14-15) and Inverse Clarke (16-18) transforms. This data is then sent to the SVPWM block (which in this code was a lookup table) in order to determine the duty cycle associated with each phase.

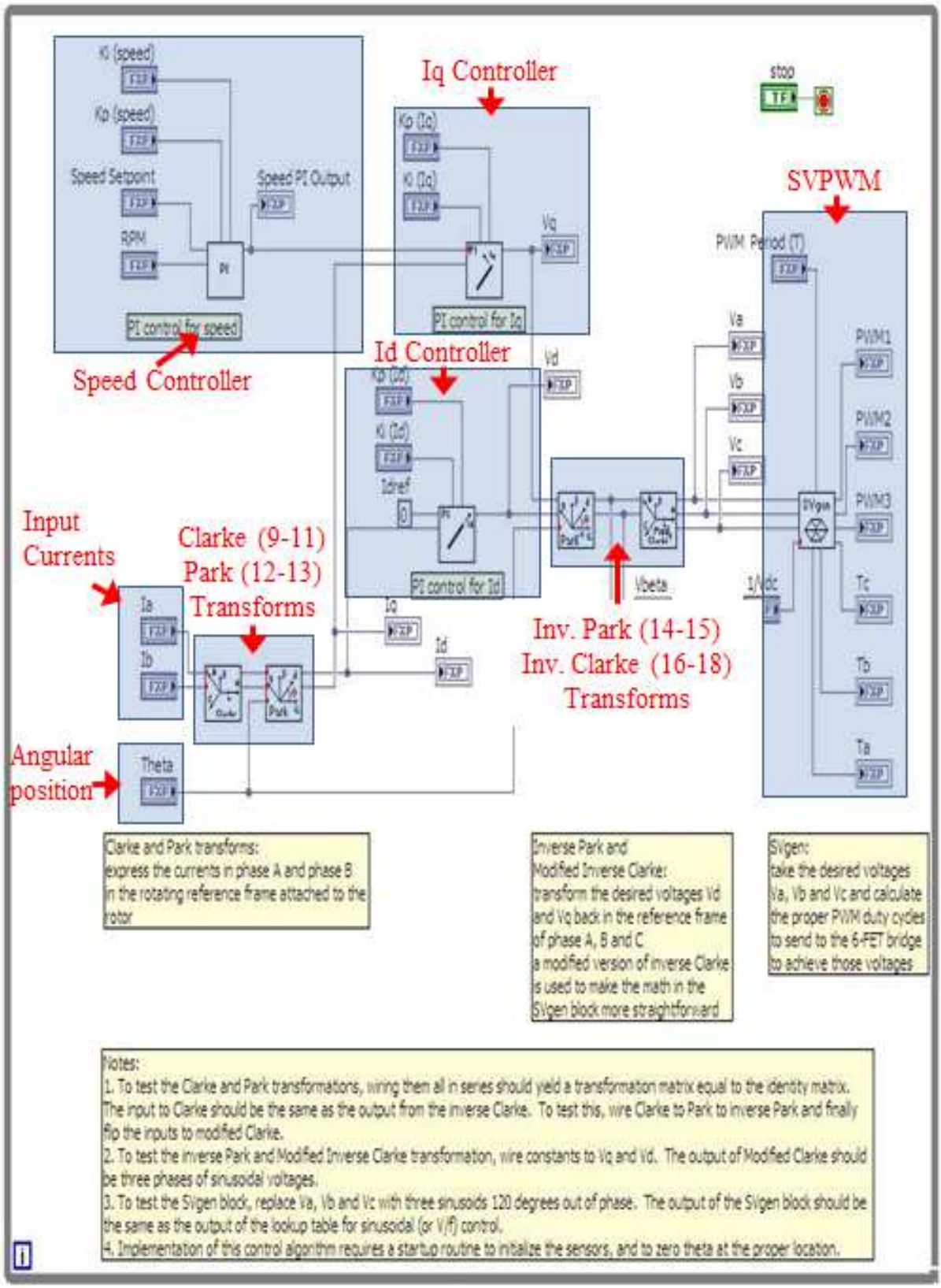

Figure 24: FOC Block Diagram Generated by Dr. Ben Black [16].

As shown in Figure 24, two of the phase currents are fed into a Clarke transform block. The processed data is then fed into the Park's transform block. The resulting d-q currents are fed into PI controllers which provide the desired torque set point for the i_q current and a zero set point for the i_d current. Only two currents versus three are provided to the Clarke transform as the sum of the three currents is always zero and this fact was implemented in the blocks as shown in Figure 24. The outputs from the control blocks are in the form of a voltage which, since they are in the q and d axes, are applied to the inverse Park's and inverse Clarke transforms in order to convert them back to the three phase form necessary to control the SVM. The equations for the Clarke and Park's transforms and inverse transforms are shown below as extracted from [21]:

Clarke Transform

$$i_\alpha = i_a \tag{6}$$

$$i_\beta = \frac{1}{\sqrt{3}} \cdot i_a + \frac{2}{\sqrt{3}} \cdot i_b \tag{7}$$

$$i_a + i_b + i_c = 0 \tag{8}$$

Park's

$$i_d = i_\alpha \cdot \cos(\theta) + i_\beta \cdot \sin(\theta) \tag{9}$$

$$i_q = -i_\alpha \cdot \sin(\theta) + i_\beta \cdot \cos(\theta) \tag{10}$$

Inverse Park's

$$V_\alpha = V_d \cdot \cos(\theta) - V_q \cdot \sin(\theta) \tag{11}$$

$$V_\beta = V_d \cdot \sin(\theta) + V_q \cdot \cos(\theta) \tag{12}$$

Inverse Clarke

$$V_a = V_\alpha \tag{13}$$

$$V_b = -\frac{1}{2} \cdot V_a + \frac{\sqrt{3}}{2} \cdot V_\beta \tag{14}$$

$$V_c = -\frac{1}{2} \cdot V_a - \frac{\sqrt{3}}{2} \cdot V_\beta \tag{15}$$

1.3.8.2.1 FOC Position Feedback Requirements

As discussed above, the resolver was selected as the means of monitoring the position control needed to accommodate the BLDC motor's three phases as well. The resolver position data is input as θ in Figure 24 and (12) – (15).

1.3.8.2.2 FOC Three Phase Current Feedback Requirements Using Bus Current

As discussed above the Clarke transformation within FOC requires current measurements from each phase of the three phase system. However, if there are a limited number of available wires to communicate with the FPGA software, a more elaborate strategy is required

in order to measure the current associated with each phase. One means to achieve this is to employ a single shunt resistor in the return bus line and employ an understanding of the current behavior through the resistor with respect to the overlap of the PWM signals (corresponding to the activation of each phase). A sample correlation between the bus current and the PWM signals for each phase is shown in Figure 25 extracted from reference [22].

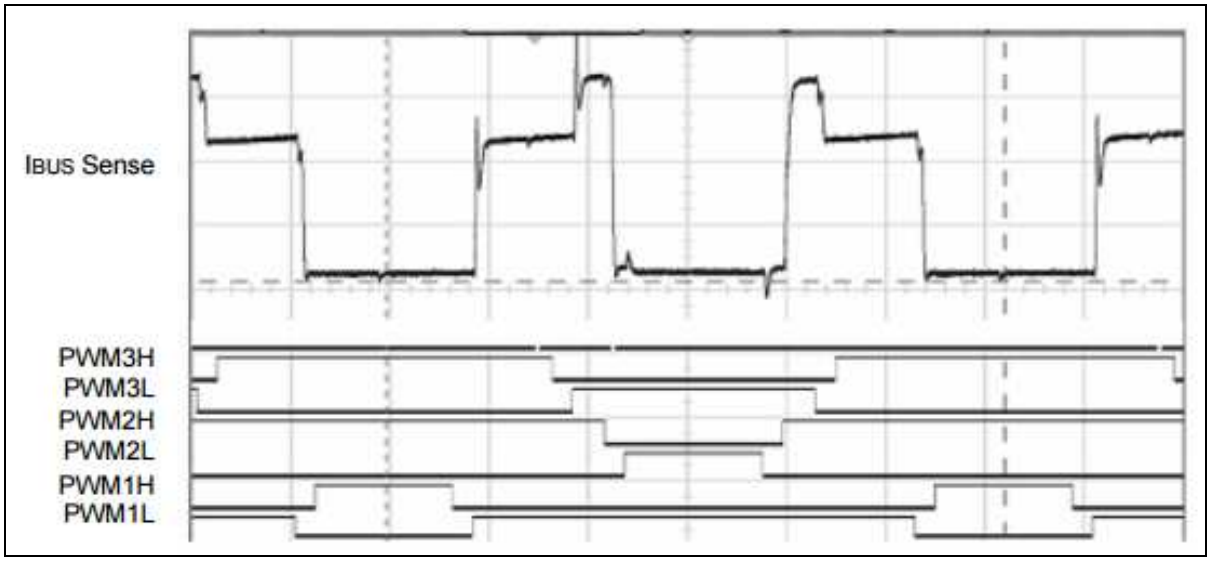

Figure 25: Bus Current Profile Which Can be Correlated to PWM Signals Associated with Each Phase [22].

To understand the technique's details one must first recognize the three different current levels in Figure 25. The zero current level corresponds to times when all the phases are either on or off. The highest level corresponds to times when two of the phases (in this case phase 1 and phase 3) are active. The middle level corresponds to times when only one phase is active (in this case phase 1). Two items of particular importance in Figure 25 includes the correlation between the PWM signals and the I_{BUS} signal as well as the observation that the

period of the PWM signal is sufficient to allow the current dynamics to settle out between transitions and take a sample of the current immediately before the next transition. It is anticipated that providing a sufficient PWM period which allows the current dynamics to properly settle out will be a key feature to consider when implementing this technique of extracting the three phase currents via a single bus current with the employed motor and FPGA platform.

1.3.9 Field-Programmable Gate Array Theory

FPGA technology provides more software process efficiency. This is especially important for real-time applications, such as the haptic systems that the associated brushless motors support, where delays can have highly adverse effects. Per the NI description [23] FPGAs operate by reprograming the physical chip itself rather than operating through a software program and its associated overhead operations which can lead to time lags when applied to motor drivE applications. Some of the advantages of FPGAs per [23] are*:*

- *Faster I/O response times and specialized functionality* (useful for haptics where communication frequency is critical and time lags are detrimental).

- *Exceeding the computing power of digital signal processors.*

- *Rapid prototyping and verification without the fabrication process of custom ASIC design* (because this is a research application, a lot of trial and error is employed and more rapid verification helps accommodate these actions).

- *Implementing custom functionality with the reliability of dedicated deterministic hardware* (reliance that the system will not be "interrupted" by other computer processes helps to avoid time lags that are detrimental to haptic operation).

- *Field-upgradable eliminating the expense of custom ASIC re-design and maintenance.*

Although FPGA systems have great capabilities, one critical disadvantage (as it applies to the hardware implemented in this research), is that space is limited. Thus, the number of operations that can be programed on the FPGA system can be limiting. If such limitations are encountered a unique program form and operations have to be employed.

1.4 Introduction Summary

The introduction presented the:

- Radiation environment effects on electrical equipment including circuit board structures and difficulty associated with maintenance activities that drive the need for more dependable equipment.
- Force-feedback theory as it applies to the robotic hand which will implement the brushless motor system described in this thesis.
- Brushless motor theory including a discussion associated with the three phase construction applicable to the employed motors.
- Resolver theory as it applies to conventional structure associated with employed device.
- Brushless motor driver circuitry theory
- Brushless motor commutation (trapezoidal, sinusoidal, space vector modulation)
- FOC theory

The following chapters discuss how these theories were implemented in the BLDC motor system used for this application.

CHAPTER 2: EMPLOYED HARDWARE AND SOFTWARE

The components implemented in this project include the brushless motor, resolver, developed circuit integrating the motor driver (APEX SA306) and resolver-to-digital converter (Analog Devices AD2S1210) as discussed in more detail in the following sections. The data sheets for these components are included in the appendices.

Additional support hardware and software necessary to operate the driver and converter, as shown in the overall system diagram (Figure 26), included the:

- National Instruments NI PXIe-8133 Embedded Controller LabVIEW software and Field-Programmable Gate Array (FPGA) module. Preliminary studies showed a serial CAN system was subject to delays on the order of 30ms which is inappropriate for haptic systems which require 1kHz (1ms) [8].

- NI PXI-6225 M Series Multifunction DAQ.

- SCB-68 M Series Devices Connector.

- 24V A24H1500M Acopian power supply.

- Array of brushless motor drivers and resolver to digital converter circuits.

Photos of these components are shown in Appendix I.

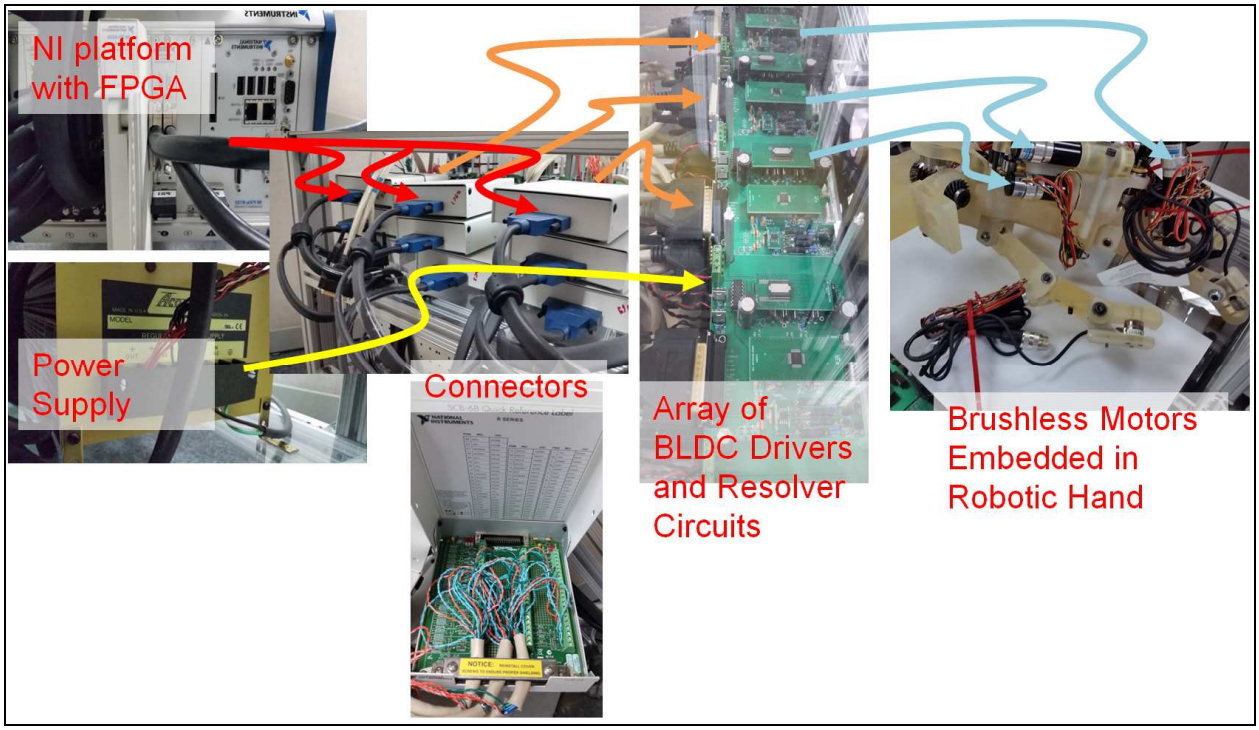

Figure 26: Overall Diagram of Brushless Motor Driver System.

2.1 Employed Brushless Motor

As stated in section 1.3.5: Brushless Motor Theory, BLDC motors are more appropriate for applications in a radiological environment than traditional DC motors. The employed motor was a Maxon EC 22 sensorless brushless 40W 48V (data sheet included in Appendix A and associated photo in Appendix I). The motor was sized in order to accommodate the force requirements at the end of the robotic finger. The requirements and associated calculations, including the gear ratios involved in the robotic finger transmission, are shown below. In these calculations the expected peak required torque is 27% of the stall torque, the peak expected speed is 93.5% of the specified limit, and the peak expected current is 5.5 Amps which is an important factor considered in the selection of the associated circuit driver.

Finger MCP Flexion Motor (new design with double transmissions)

$mN := 0.001N$ — mili-Newton to Newton conversion

Requirements

$RT := 50N \cdot 0.15m = 7.5 \cdot N \cdot m$ — Required torque at stall

$RS := \frac{\left(\frac{\pi}{2}\right)}{0.2sec} = 75 \cdot \frac{rev}{min}$ — Max no-load speed to clasp pip joint [visual verification]

$BGR := 4$ — Bevel gear connection gear ratio

$Rmg_T := \frac{RT}{BGR} = 1.875 \cdot N \cdot m$ — Required motor + gearhead torque (must use 22mm or higher gearhead to achieve required torque capacity)

Motor Specifications

$mT_{cont} := 20mN \cdot m$ — Continuous torque of motor 386659/63

$mT_{stall} := 221mN \cdot m$ — Stall torque of motor 386659/63

$m_S := 31600 \frac{rev}{min}$ — Speed limitation of motor 386659/63

$V_{nom} := 36V$ — Nominal voltage of motor 386659/63

$ST_{grad} := 144 \frac{rpm}{mN \cdot m}$ — Speed torque gradient of motor 386659/63

$T_{con} := 10.8 \frac{mN \cdot m}{A}$ — Torque constant of motor 386659/63

Gearhead Specifications

$GR := 53$ — Gear ratio of gearhead 370776

$Eff := 0.59$ — Efficiency of gearhead 370776

$T_{max} := 3.5N \cdot m$ — Maximum permissible torque of gearhead 370776

$g_S := 17000 \frac{rev}{min}$ — Speed limitation of gearhead 370776

Demand to Capacity Comparisons

$mg_S := \min(m_S, g_S) = 1.7 \times 10^4 \cdot \frac{rev}{min}$ Limiting speed of motor/gearhead

$R_{Tcont} := \frac{RT}{Eff \cdot GR \cdot BGR \cdot mT_{cont}} = 2.998$ Demand to capacity for nominal torque value (this compares max to cont which is intermittent and thus it is expected that this value will be over unity)

$R_{Tstall} := \frac{RT}{Eff \cdot GR \cdot BGR \cdot mT_{stall}} = 0.271$ Demand to capacity for stall torque value

$R_S := \frac{GR \cdot BGR \cdot RS}{mg_S} = 0.935$ Demand to capacity for motor speed

$R_{GH} := \frac{Rmg_T}{T_{max}} = 0.536$ Demand to capacity for gearhead torque

Voltage and Current Requirements

$Lmg_S := GR \cdot BGR \cdot RS = 1.59 \times 10^4 \cdot rpm$ Max motor speed under very light loading

$Rm_{T\_LL} := \frac{0.15 \cdot Rmg_T}{GR \cdot Eff} = 8.994 \cdot mN \cdot m$ Light loading motor torque to complement speed

$Rm_{T\_ML} := \frac{Rmg_T}{GR \cdot Eff} = 59.962 \cdot mN \cdot m$ Maximum loading motor torque

$V_{app} := \left(Lmg_S + Rm_{T\_LL} \cdot ST_{grad}\right) \cdot \frac{V_{nom}}{m_S} = 19.589\,V$ Applied voltage under light loading

$A_{app} := \frac{Rm_{T\_ML}}{T_{con}} = 5.552\,A$ Current required at maximum applied torque

2.2 Employed Brushless Motor Circuit and Associated LabVIEW Script

The means to drive the brushless motor was accomplished via the APEX SA-306 three phase switching amplifier (the sample drive circuit shown in Figure 27 was provided by the APEX data sheet as shown in Appendix F). The primary motivations to employ this amplifier included:

- Its ability to handle peak currents up to 15 amps (data sheet for employed motors reports a stall torque of 20 amps but as stated in the previous section the expected peak current under the expected haptic loads is approximately 5.5 Amps. However, this circuit may be implemented for larger motors in the future, and this aspect will have to be reconsidered for any alternate motor which this driver might be applied).

- Its ability to control the six FET inputs in order to achieve effective SVM and calculate the FOC parameters off the chip.

- It does not require any additional inputs such as Hall sensors.

- Its ability to provide low current signals for each of the phase currents that will be used in the FOC strategy to be employed.

- It has ports to communicate faults associated with temperature and short circuit conditions.

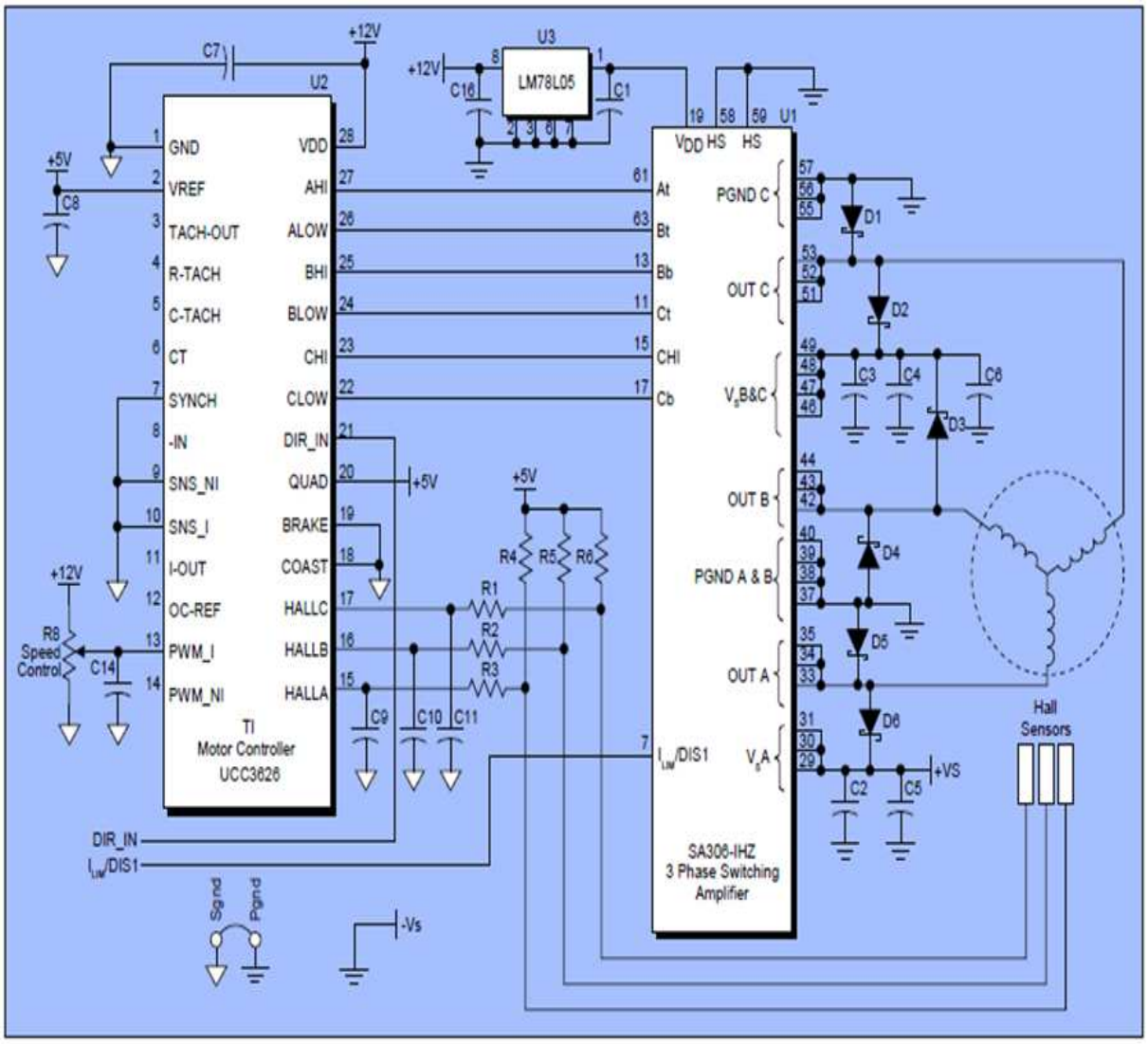

Figure 27: Sample Drive Circuit for the APEX SA-306 [14] Three Phase Switching Amplifier Provided in the Data Sheet in Appendix F.

A few issues associated with the proposed circuit in Figure 27 when applied to the target application were that the microcontroller (TI UCC3626) required Hall sensors and appeared to be more applicable to speed control rather than the desired FOC. Even if FOC was appropriate, an additional circuit would have to be employed to convert the resolver signal to a Hall sensor signal. As such, this project chose to control the driver via LabVIEW's FPGA software.

The actual circuit designed and fabricated in this research is shown in Figure 28 and Figure 29. Most of the components implemented in the circuit were soldered to the board except the actual driver chip which was plugged into a connector on the surface. This was done to allow it to be rapidly replaced if it failed.

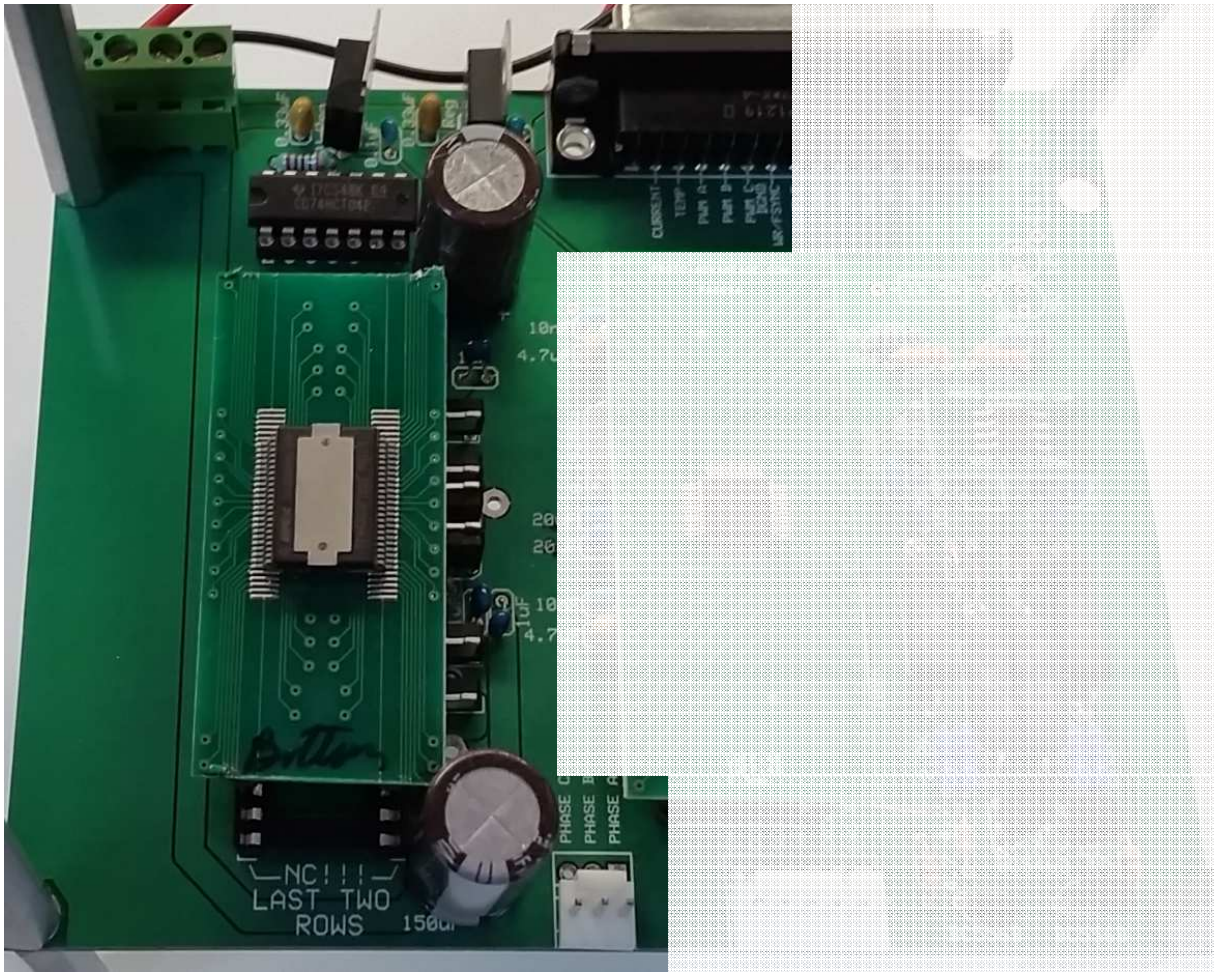

Figure 28: Portion of Developed Circuit Associated with Brushless Motor Driver as Interpreted from Schematic Shown in Figure 27.

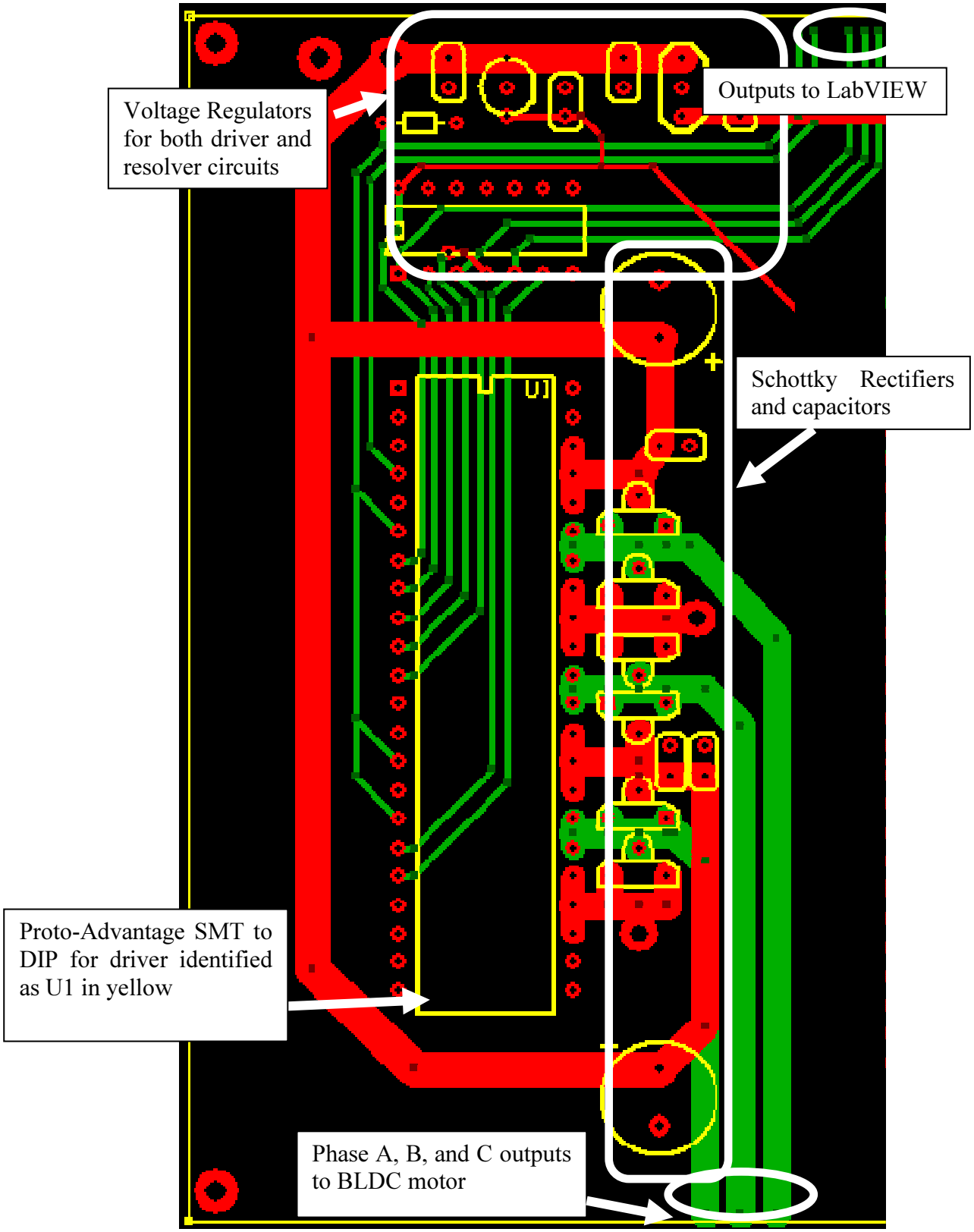

Figure 29: PCB Design Replicating Driver Schematic Represented in Figure 27 {Bottom (Green Lines), Top (Red Lines), and Top Components (Outlined in Yellow)}.

The following LabVIEW code was generated in order to apply SVM to the selected motor. Initially it was found that simple look-up tables (Figure 30) of 1024 points (associated with a 10 bit number) representing the SVM profiles for each phase would operate the motor when applied to the circuit above.

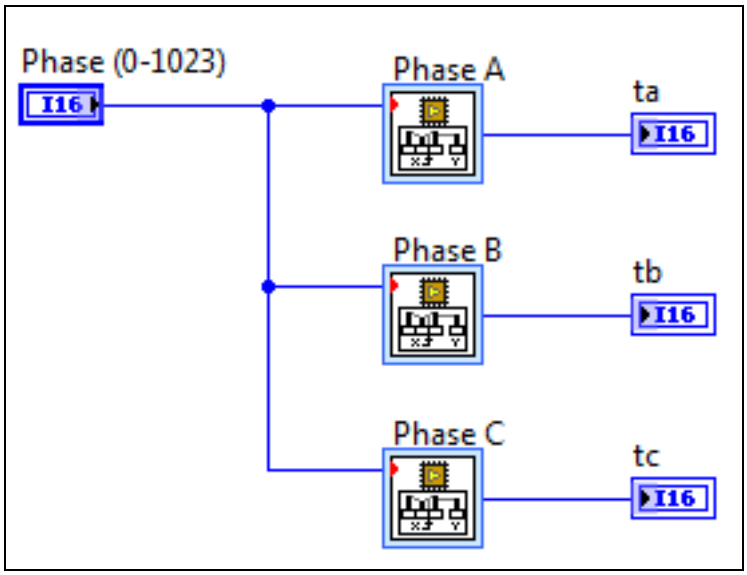

Figure 30: Look-up Table Method for Applying SVM to Motor [16].

However, when incorporated into the FPGA system it appeared that storing that much data was memory intensive (at least in the LabVIEW table structure) and consequently prevented all of the programing associated with this system from fitting on the FPGA system. As such, it was found that a series of switches and basic numerical operations (addition and multiplication) using 64-bit integers (rather than floating point numbers), use of the division operation, or trigonometric functions was able to fit on the chosen FPGA system's limited space to implement the SVM profile.

In order to represent the SVM profiles in terms of simple addition and multiplication operations, which require much less space on an FPGA system, a method implementing curve fits of the profile was developed. The method divided the profile into four distinct portions (curve up, curve down, linear increase, linear decrease) and then implemented switches to connect the appropriate portion to the appropriate phase as driven by the sector with which the motor operated. The SVM profile data necessary to apply the curve fit technique used the equations and table represented in section 1.3.7.3: Space Vector Modulation Theory to create the profiles shown in Figure 31 and Figure 32. Data associated with the four distinct sections of the profile were then scaled up by a factor of 2^{23} such that it could be presented with sufficient accuracy (maybe even more than sufficient) into the LabVIEW code without the need to use any floating point values as discussed above. By using a factor of two to a power allowed one to simply convert the number to a smaller bit size, which is essentially dividing the number by a factor of two to a power. These curve fits are shown in Figure 33 through Figure 36. The generated equations can be seen in the LabVIEW code blocks in Appendix D.

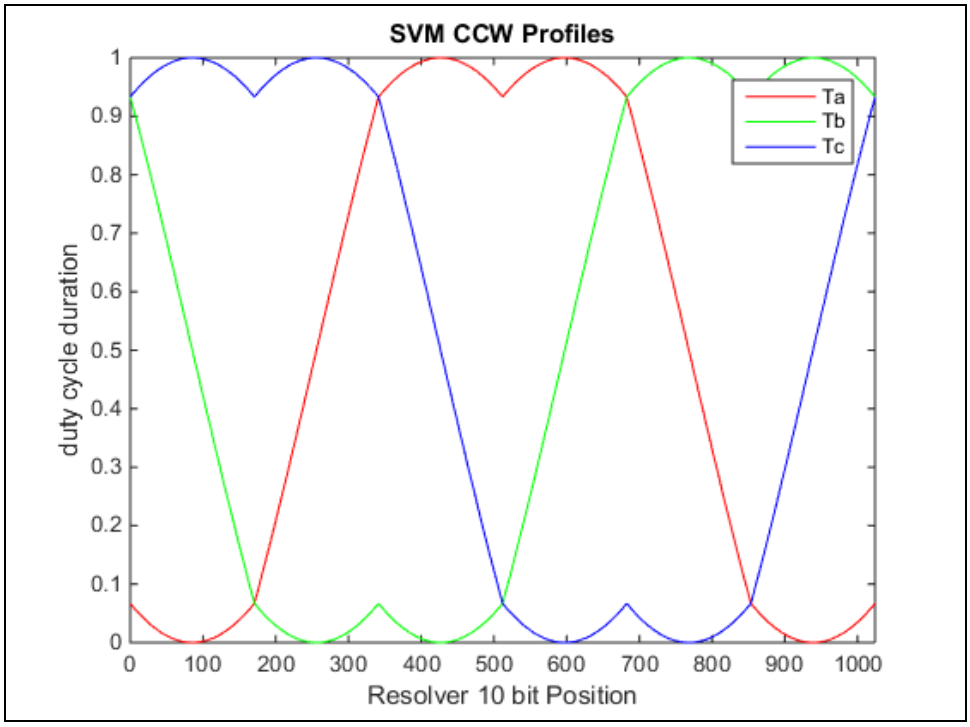

Figure 31: SVM Profile for Counter-Clockwise Motion Generated in Appendix C Using the Equations and Table Presented in *Section 1.3.7.3*.

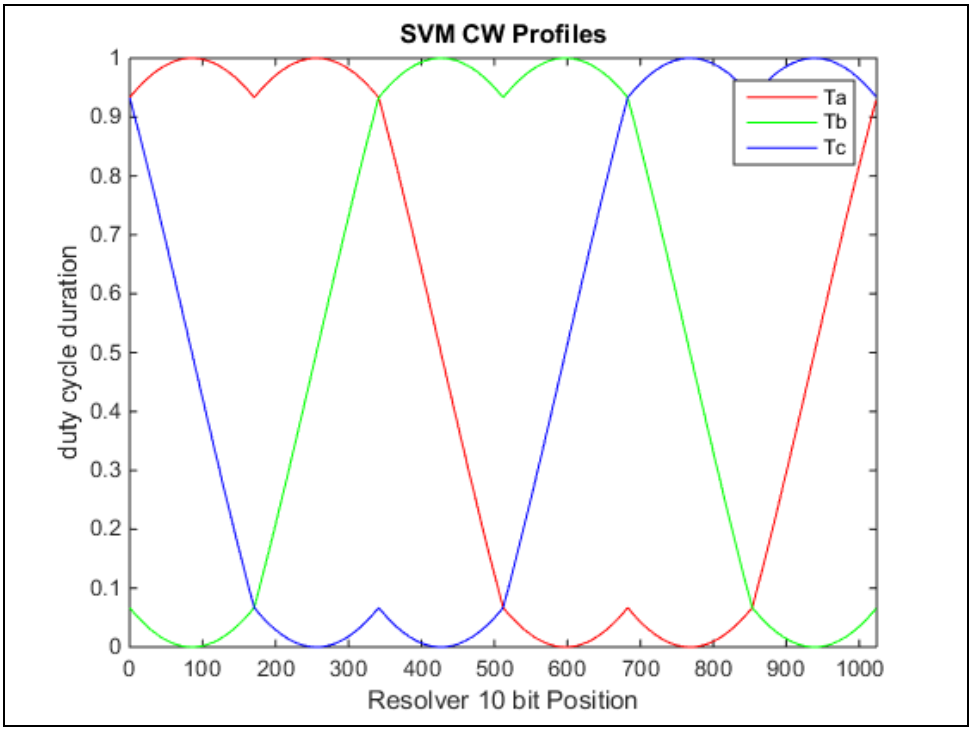

Figure 32: SVM Profile for Clockwise Motion Generated in Appendix C Using the Equations and Table Presented in *Section 1.3.7.3*.

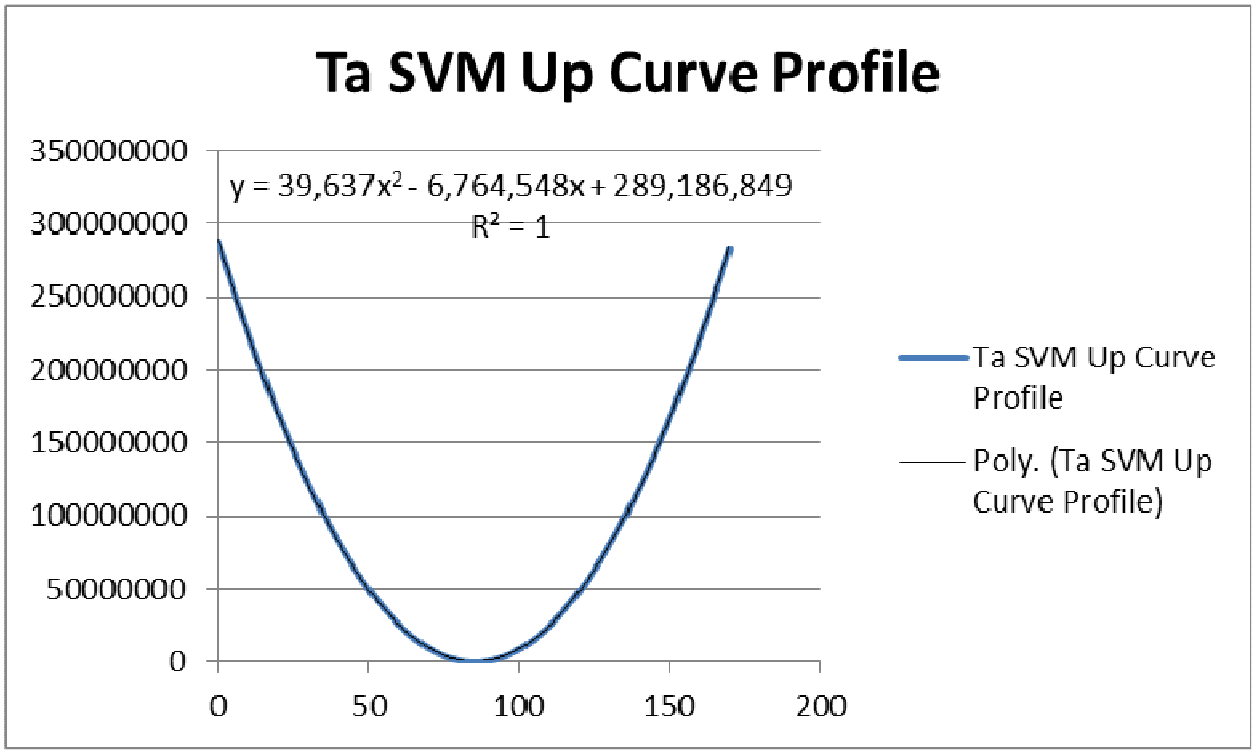

Figure 33: Curve Fit Associated with SVM Up Curve Profile.

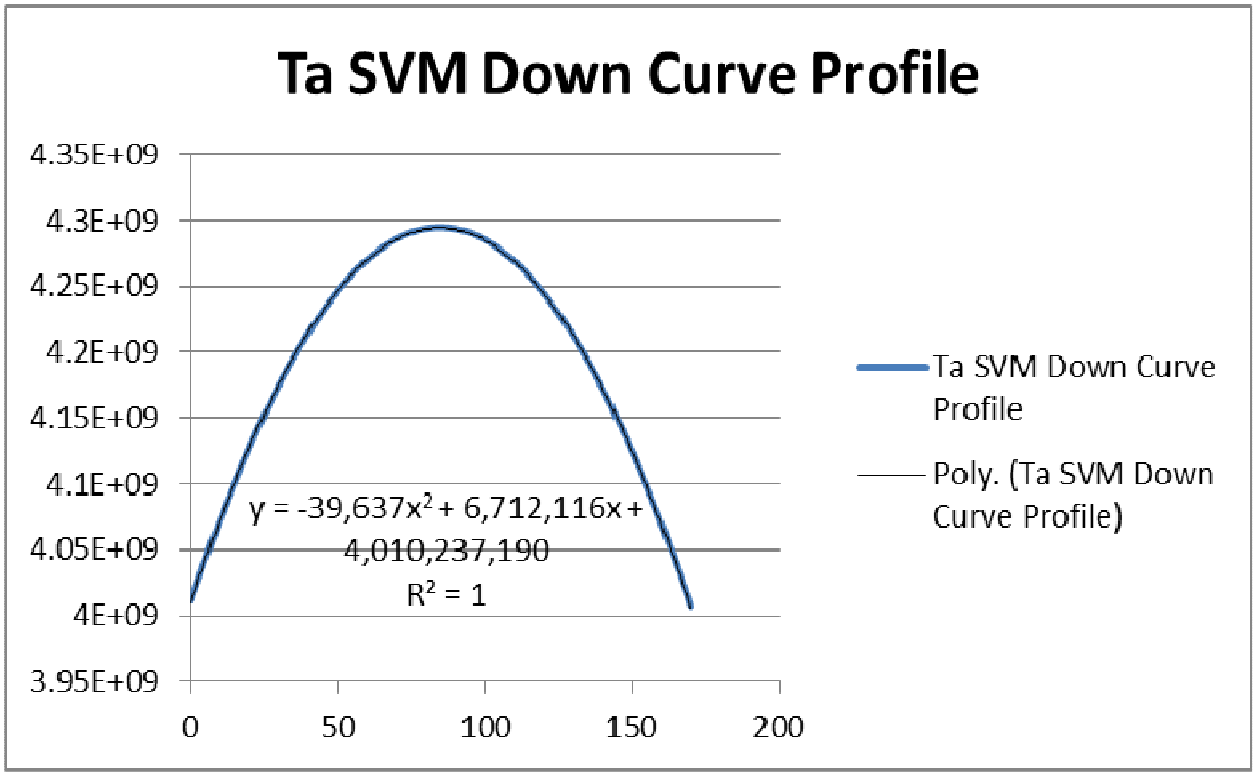

Figure 34: Curve fit Associated with SVM Down Curve Profile.

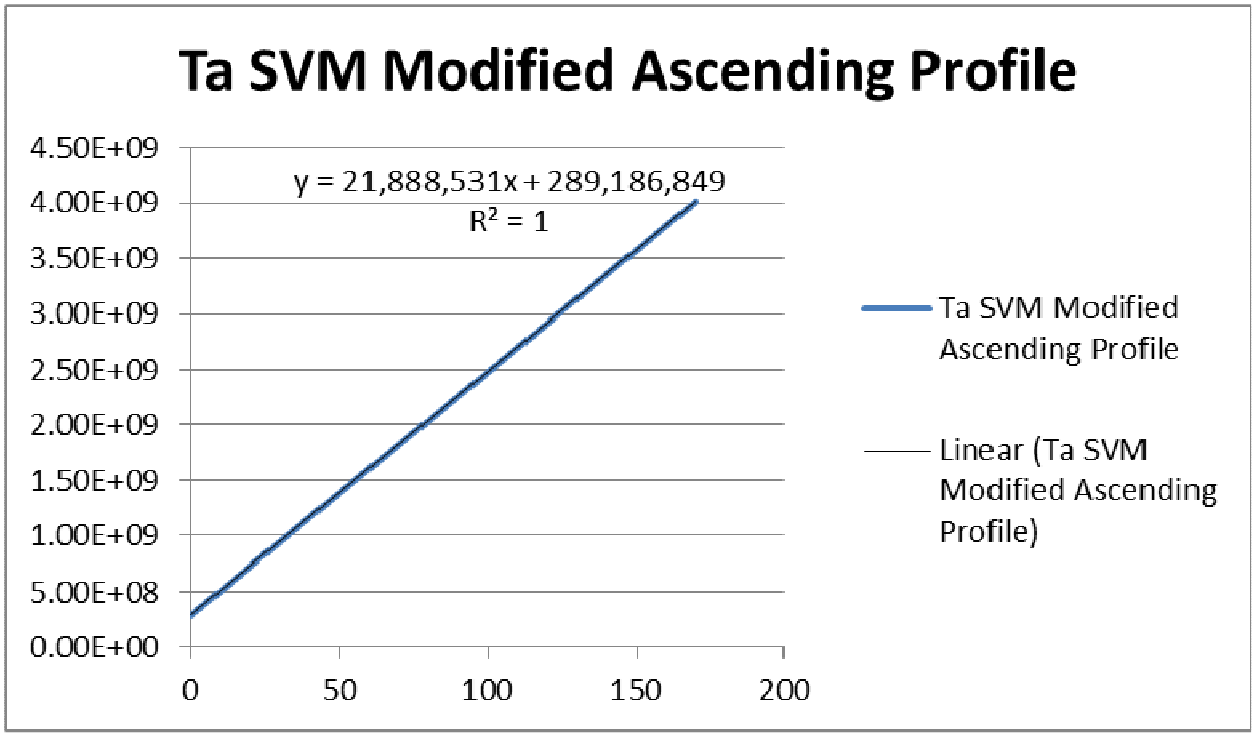

Figure 35: Curve Fit Associated with SWM Ascending Profile (Modified to Ensure Beginning and End Points Intersect with Other Profiles in LabVIEW Code)

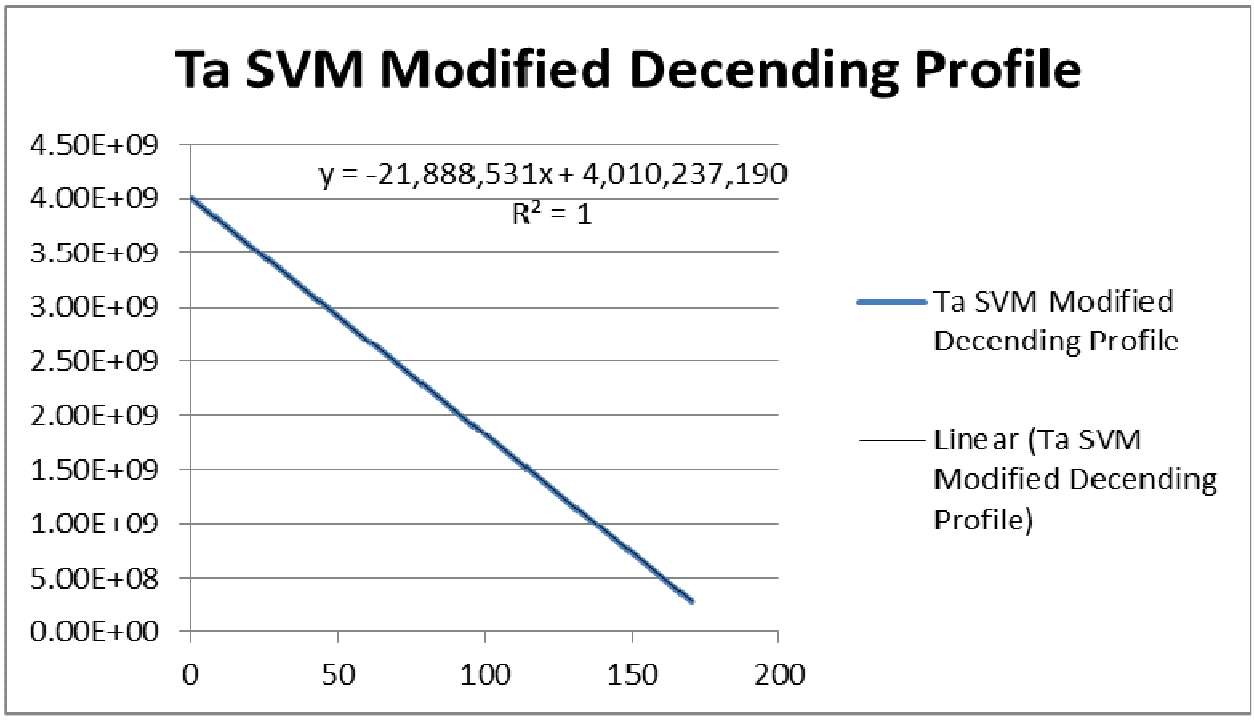

Figure 36: Curve Fit Associated with SWM Ascending Profile (Modified to Ensure Beginning and End Points Intersect with Other Profiles in LabVIEW Code)

The primary components associated with the SVM LabVIEW code are shown in Figure 37. The four primary portions of the figure are discussed in the following list with a numerical example following each description. This system proved to be very dependable and will allow the research to work with items such as the PWM duty cycle, if need be, in order to be cohesive with characteristics associated with the rest of the system (e.g. dynamics, digital chip sample rate requirements, etc.).

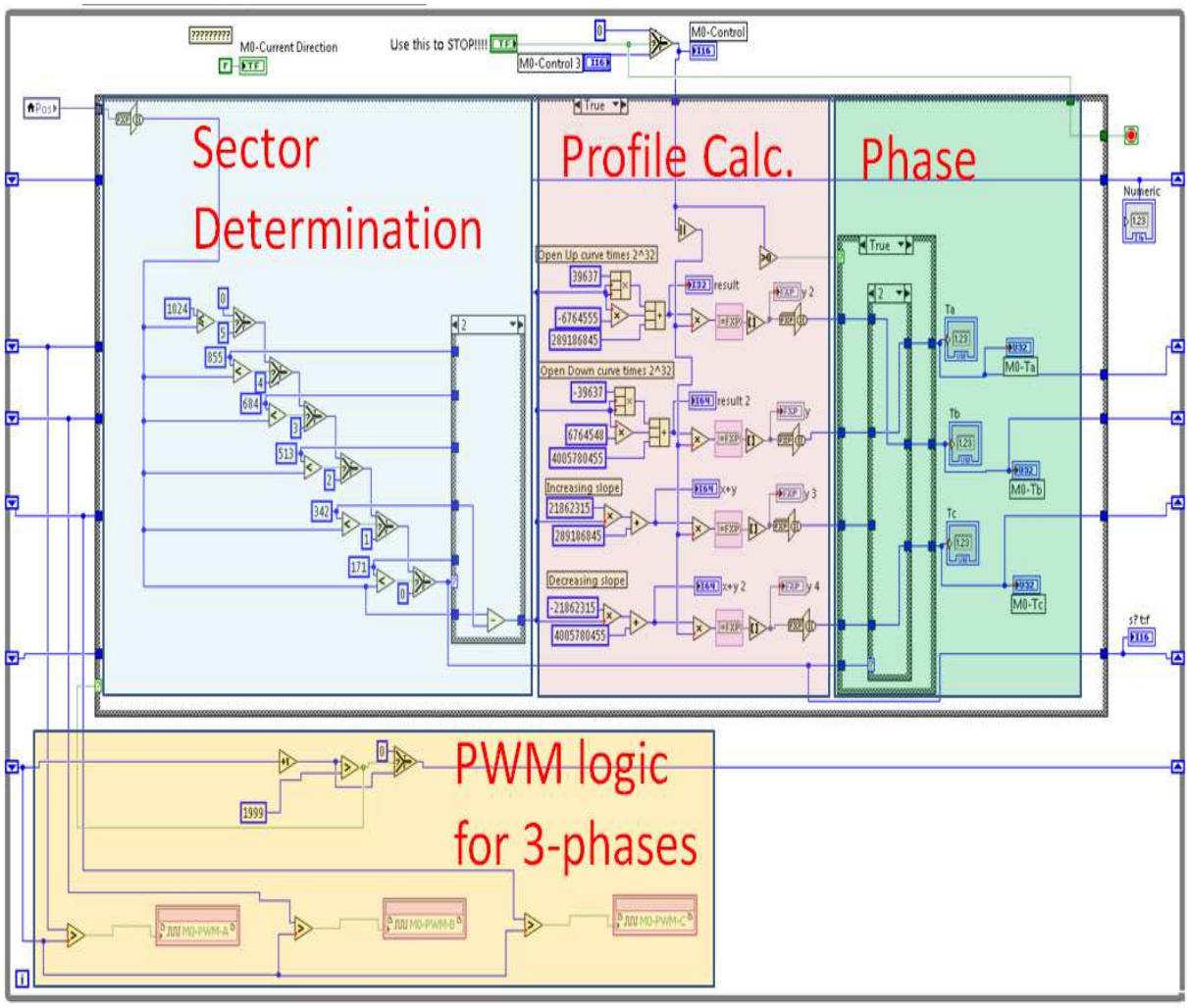

Figure 37: Primary Components of SVM LabVIEW Code.

Sector determination portion:

This portion takes the position signal calculated by the resolver, converted to a 10 bit number, and via a series of comparisons identifies which sector the rotor is in. The sector number data is fed into the case structure and the position value is subtracted from lowest position value belonging to the sector of interest. This is done because all the curve fits begin at zero degrees and this action shifts the data to operate in that sector. The modified position data is then sent to the profile calculation portion. *An example might be a position of 132 degrees represented as a 10 bit number 376 which when subject to the comparison block identifies it as belonging to sector 2 and the case structure subtracts 342 from 376 to get 34 which is fed into profile calculator block.*

Profile calculation portion:

This portion takes the modified position signal calculated in the sector determination block and applies it to all four of the curve fit equations. The results from the curve fit equations can be a number up to 43 bits due to the square operation applied to a 10 bit number times a 23 bit number. Rather than use the division function the bit size of the number is reduced back to a 10 bit number which is then sent to the phase block. *An example might be the 10 bit number 34 is input into the profile calculator block's curve up equation to generate a number of 105,012,347 which is then reduced to the 10 bit number 12 and then fed into the phase block.*

Phase portion:

This portion takes the sector information identified in the sector determination block as well as the clockwise/counter-clockwise determination to identify which curve fit value corresponds to which phase. *An example might be the identified sector is 2, the motor is rotating clockwise, and the input number from the curve up equation is 12 which is then routed to be the period that will be applied to phase b which is fed into the PWM logic for the three phase block.*

PWM logic for three phases portion:

This portion takes 10 bit periods calculated for each phase (represented as number of clock ticks) and compares them to the current number of ticks that have passed for this period (identified here as a maximum ticks of 2000). The 10 bit scale was chosen such that the pulse width modulation signals would never have a full hundred percent duty cycle. This was done because, in this application, the motor has to hold a position (stall), in which case, current would be highest and would be constantly flowing through the FET defined to have a full hundred percent duty cycle and rapidly cause overheating of both the driver and motor. Experience showed this to be true as indicated by one of the drivers catching fire during testing. The periods calculated in the portions discussed above are performed in a single iteration out of the 2000 in order to reduce the number of calculations and ensure real-time conditions such as rotor position are employed. *An example might be that for a phase b period of 12 the PWM signal only becomes active for values less than 12 and the remainder of the time is off until the next cycle.*

2.3 Employed Resolver

The resolver employed in this project was the Tamagawa Smartsyn TS2605N31E64 [9] as shown in Appendix I. The data sheet and the key geometric features of the component and the associated wiring diagram are included in Appendix B. Reference [9] describes this resolver as having:

Wide temperature range.

- *Operating temperature range: -55 + 155°C* (radiation environments can exist at either end of this spectrum).

Superior environment resistance.

- *Vibration: 196m/s^2{20G} at 10Hz .500Hz, for 2 hours to each of three axes.*
- *Shock: 981m/s^2{100G} for 6ms, 3 times to each of 6 axes, 18 times in total* (in a haptic hand application it is expected that the device will be subject to impact loads).
- *Humidity: 90% RH or above at 60°C.*

High speed rotation.

- *10,000min^{-1}{rpm} (Size 08: 40,000min^{-1}{rpm})* (not as critical for this application).

High reliability.

- *Extremely long life and high reliability are assured by the structure of mechanical parts and automated coil incorporation* (good for operating in a radiation environment).
- *Absolute position detection* (good for high precision operation).
- *Long-distance transmission robustness against noise enables long-distance transmission* (beneficial due to location of electronics being outside cell).

2.4 Employed Resolver Circuit and Associated LabVIEW Script

The means to read the resolver position and velocity could have been accomplished via analog means (reading the analog signal and extracting the position and velocity data in LabVIEW). However, the analog signals were not fed directly into LabVIEW because the National Instrument system employed had limited analog inputs that were already reserved to read the analog current feedback signal. As such, the Analog Devices AD2S1210 resolver to digital converter with reference oscillator was implemented.

This project implemented the circuit presented in the converter's associated data sheet (Figure 38 and Figure 39 extracted from Appendix G: Employed Resolver-to-Digital Converter (AD2S1210) Data Sheet). Figure 38 is a circuit which indicates how one is to connect the chip in order to send the resolver the proper excitation signal and read the corresponding signal and send it to the digital input. Figure 39 is the buffer signal indicated in Figure 38 which is used to filter out any noise that may adversely affect the data.

This circuit was designed into the printed circuit board shown (PCB) in Figure 40 and Figure 41. In Figure 40 the AD2S1210 chip is connected to a base board which is then plugged into the PCB. The details associated with the circuit shown in Figure 40 can be seen in more detail in Figure 41. The lower portion of Figure 41 shows the resolver connector that communicates the analog signals, the upper portion shows the FPGA connector which communicates the digital signals from the chip, and the intermediate portion shows the location of the chip and how all components is connected to replicate the schematics shown in Figure 40.

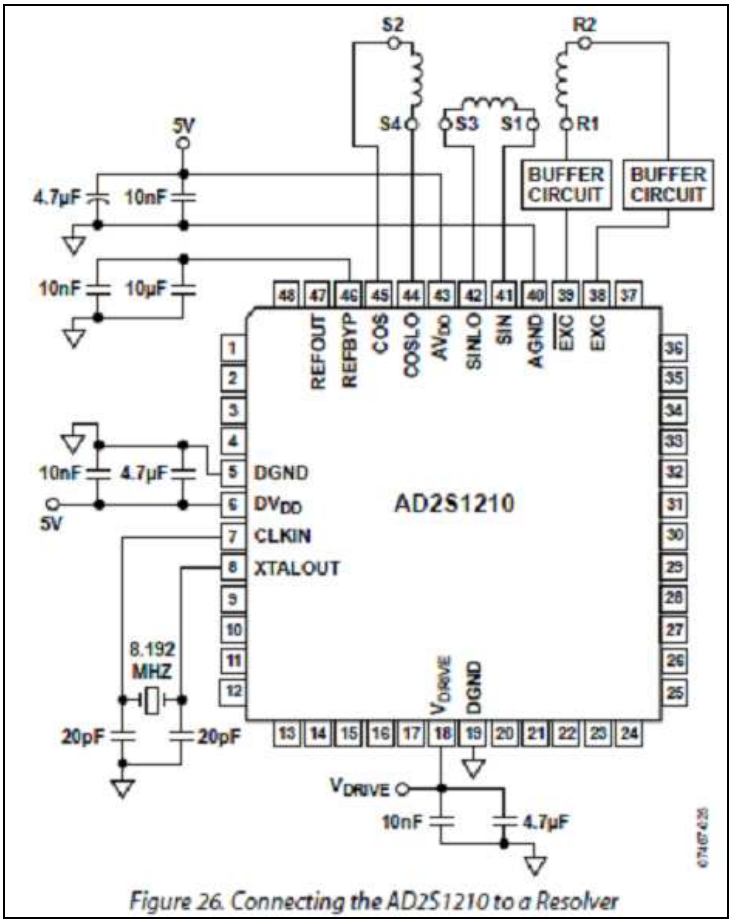

Figure 38: Circuit Identified by Analog Devices to Connect AD2S1210 to the Resolver [10].

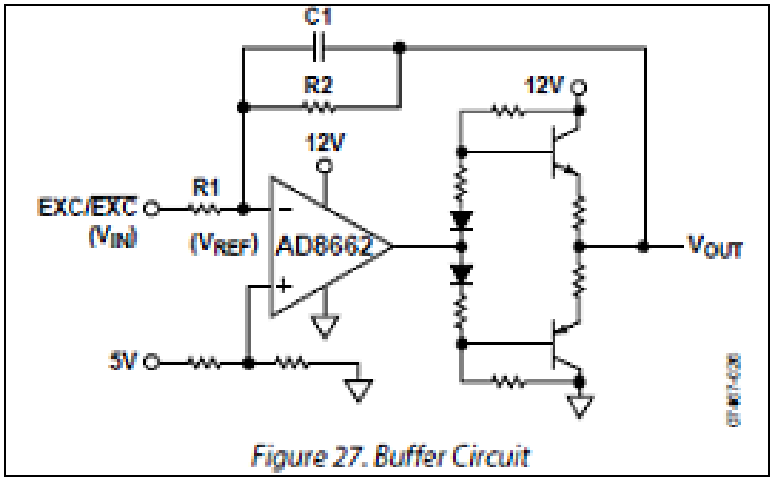

Figure 39: Buffer Circuit Referenced in Figure 38 [10].

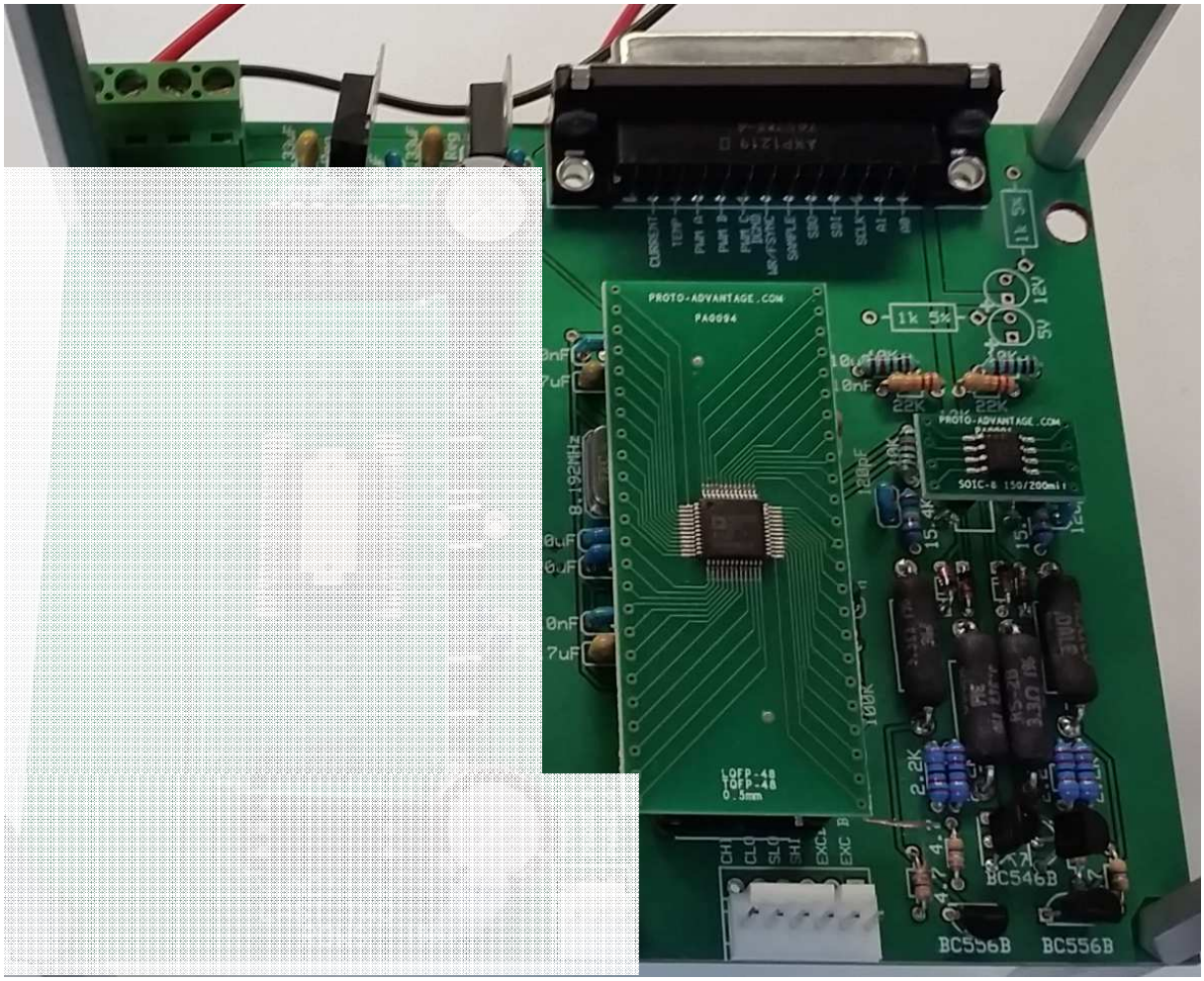

Figure 40: Resolver-to-Digital Converter Portion of Developed Circuit.

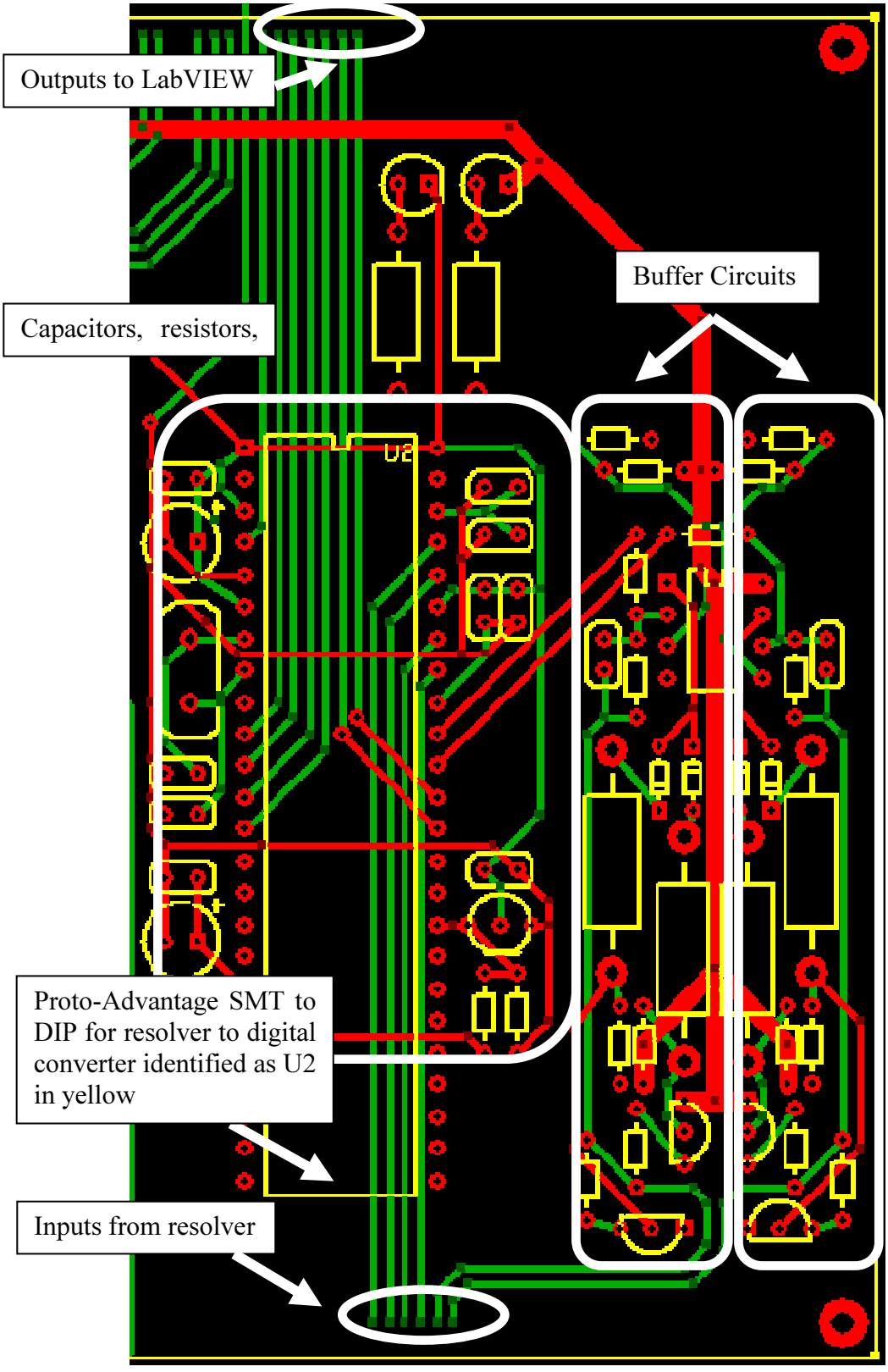

Figure 41: Bottom (Green Lines), Top (Red Lines), and Top Components (Outlined in Yellow) Used to Replicate Schematic Represented in Figure 38 and Figure 39.

The front panel for the LabVIEW program associated with the resolver is shown in Figure 42. The associated configuration mode setting table is shown in Table 5 indicating the values of A0 and A1 that are required to place the chip in position or velocity read modes.

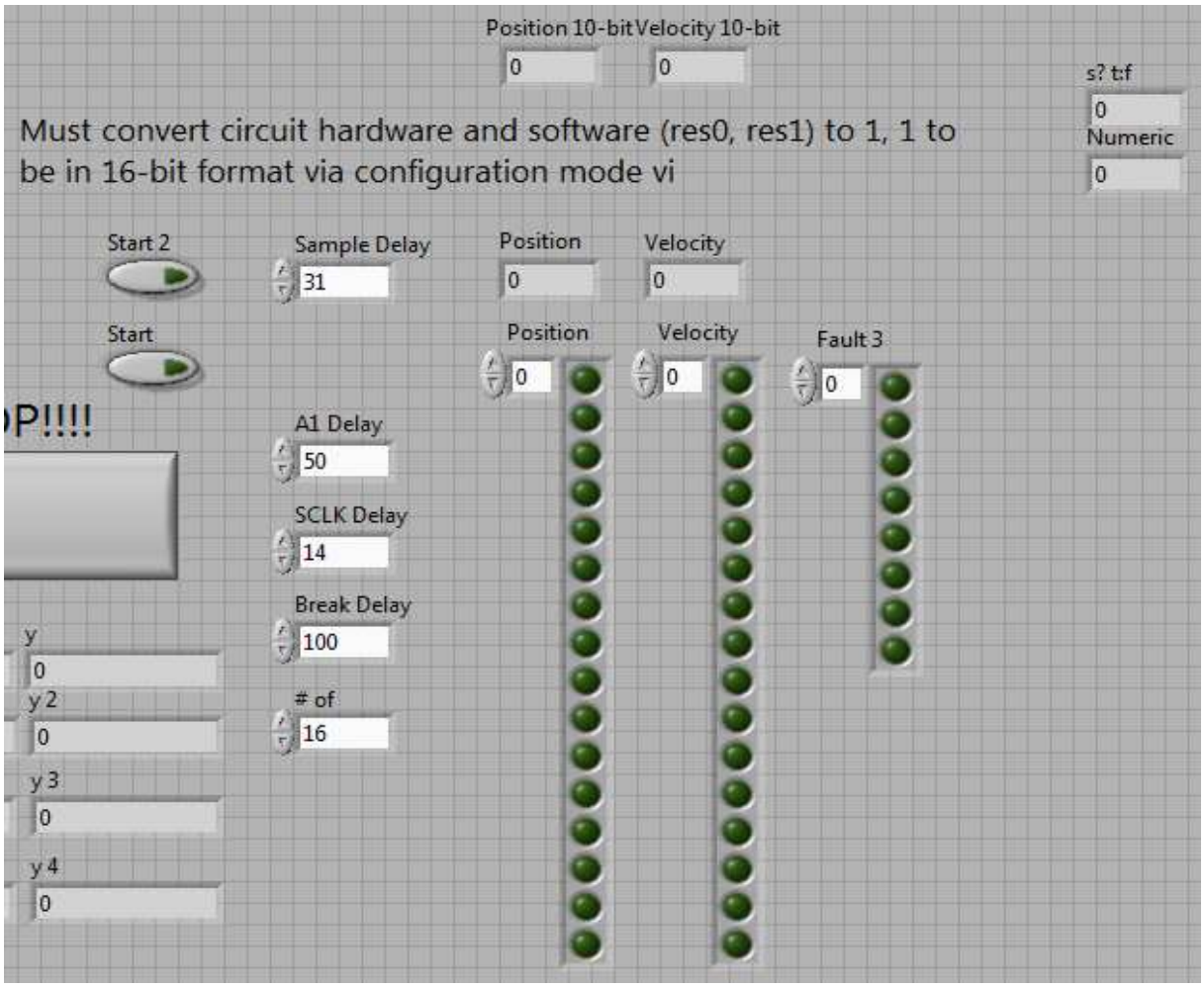

Figure 42: Front Panel of Inputs/Outputs Corresponding to Resolver Portion of Circuit.

Table 5: Configuration Mode Setting

Table 8. Configuration Mode Settings

A0	A1	Result
0	0	Normal mode—position output
0	1	Normal mode—velocity output
1	0	Reserved
1	1	Configuration mode

Figure 43 shows the steps required to read the digital resolver position and velocity data. Figure 44 shows a representative block from 10 possible blocks to demonstrate which of the input variables correspond to the steps associated with Figure 43 and the corresponding portion of the data profiles presented by the resolver-to-digital converter data sheet. As indicated in Figure 44:

- Step 1 and Step 2 are primarily driven by switching the variable "Sample delay" on and off to properly initiate the system.
- Step 3 is driven by the "A1 delay" input which determines if the chip is to read either position or velocity.
- Step 4 and 5 are initially driven by the "SCLK delay" input which determines how long between switching instances the system is required to wait in order to read each bit of the 16 bit output signal and 8 bit fault signal. The "A1 delay" then follows each reading in order to reset the A1 variable input in Step 3.
- Step 6 is driven by the "Break delay" to reset the circuit.

Appendix E extensively describes each of the 10 possible block conditions and their associated step from Figure 43. These figures embedded in the appendix are paired such that each LabVIEW block diagram can be correlated to the digital signal input/outputs received/supplied by the chip in order to communicate the appropriate data. Each figure pair is preceded by a description of the primary functionality of the presented blocks (formatting was single spaced in order to fit the description, LabVIEW block diagram, and resolver sequences onto one page.

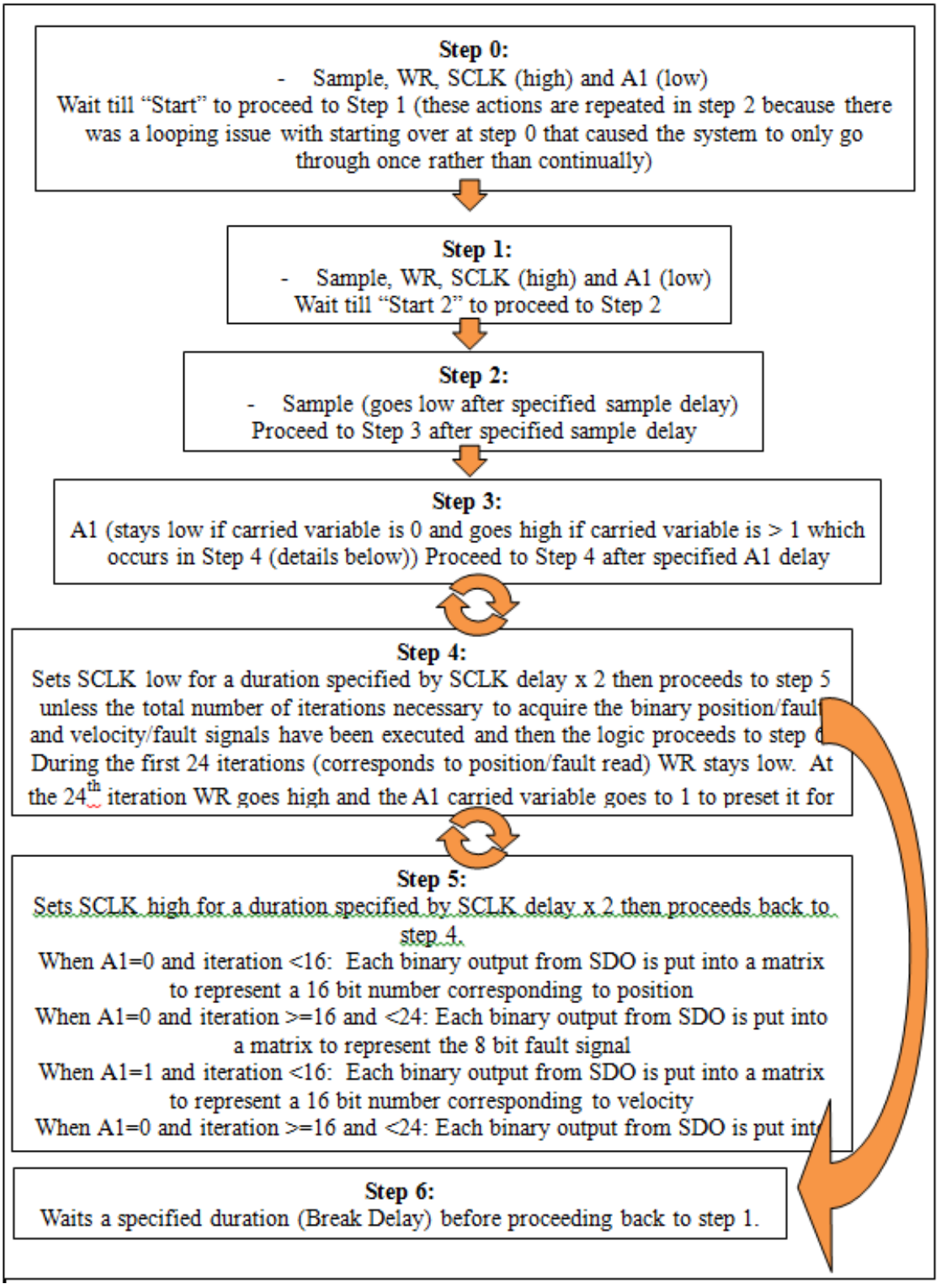

Figure 43: Steps Processed in Reading Resolver Data as Illustrated in Figure 44.

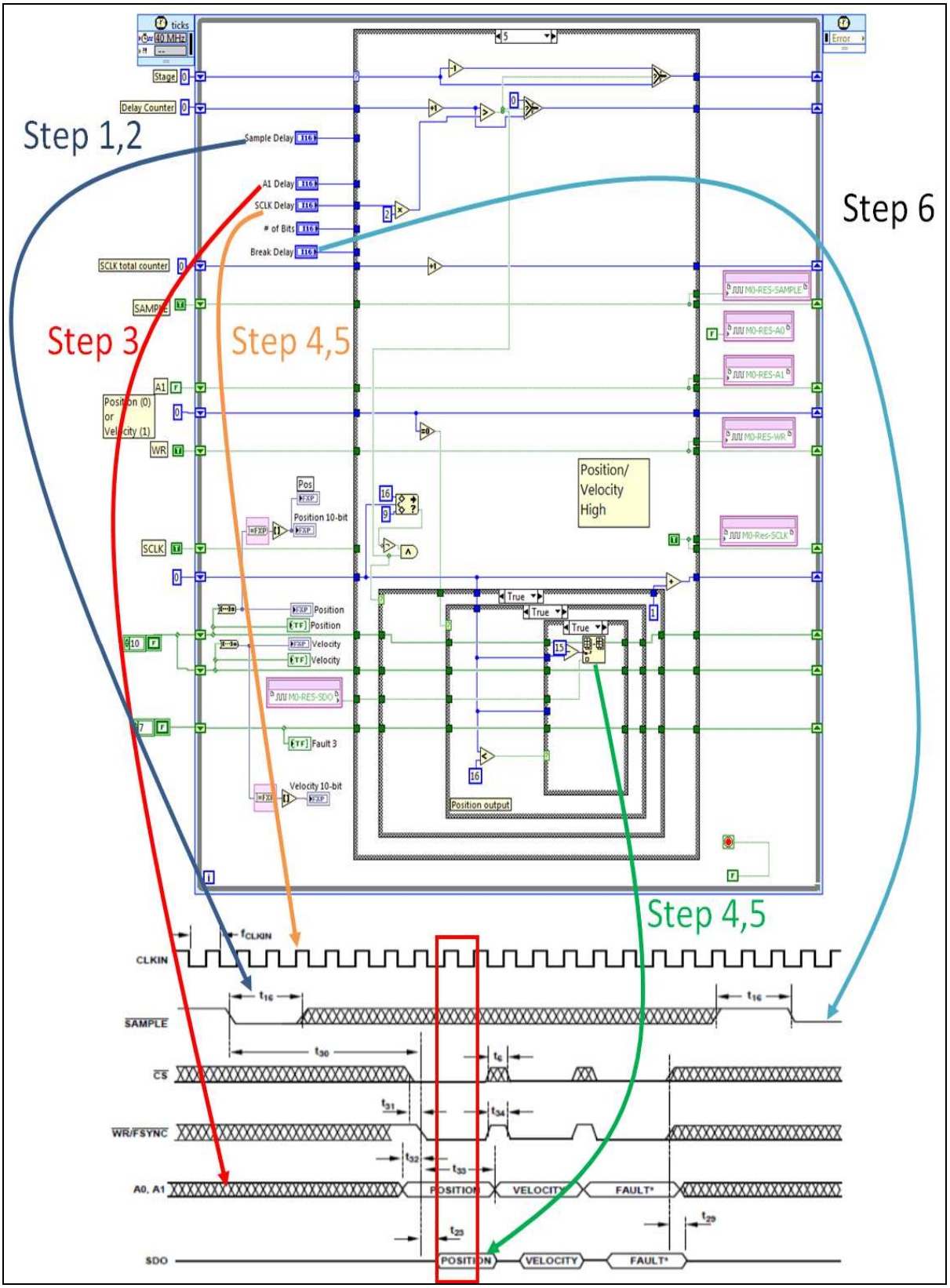

Figure 44: LabVIEW Block Diagram Which Corresponds to Steps in Figure 43.

2.5 Proposed Field Oriented Control

This project generated the above system such that it would be able to accommodate FOC. This project proposes to implement a modified version of Figure 24. The Park's and Clarke transformation aspects embedded in the approach presented in Figure 24 will remain the same. However, instead of a speed controller, the proposed system will control torque. Highlights associated with this modification are shown in the future work section.

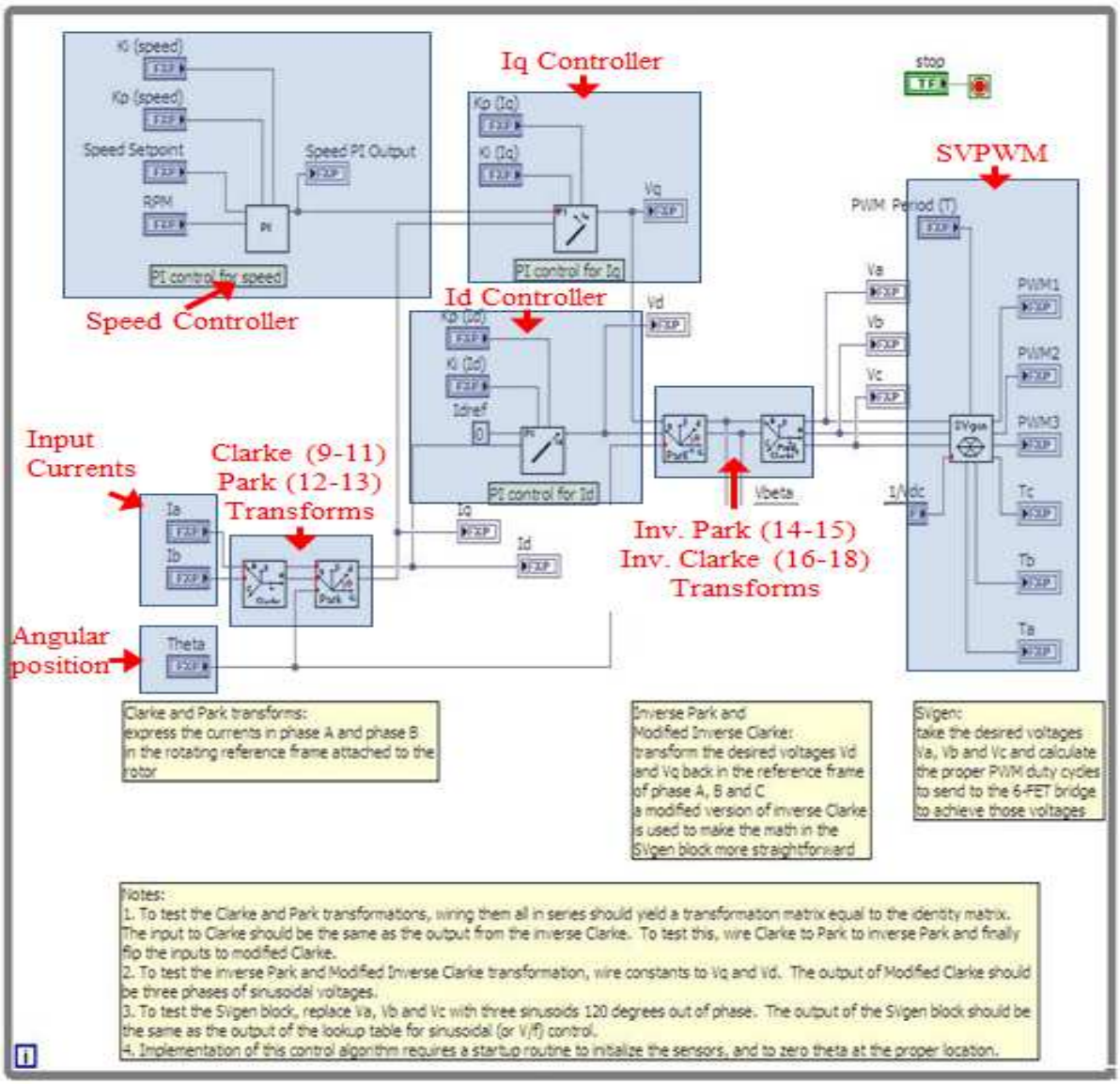

Figure 45: LabVIEW Block Diagram Associated with FOC [16].

2.6 Proposed Single Signal Three Phase Current Feedback/Sensing

FOC control requires both position/speed and current/torque feedback. Because there are a limited number of analog inputs available from the FPGA system, only a single current (generated by combining all three phase currents together) and time-based information will be implemented to identify the current associated with all three phases.

Interestingly enough the driver actually supplied outputs for all three of the current signals to the user which would have been valuable data if there had been a sufficient number of analog system inputs. These signals were combined by routing them into a single line and sending them to the FPGA system as shown in Figure 46. The resulting current signal will be run through a resistor to generate a voltage and its association with the PWM signal as well as the dynamics will be used to extract the current associated with each phase.

Data included in the results section will illustrate the preliminary results and demonstrate the correlation between the PWM signals and the current response. A more extensive description of the proposed techniques that will be employed to read the three phase currents will be discussed in the future work section.

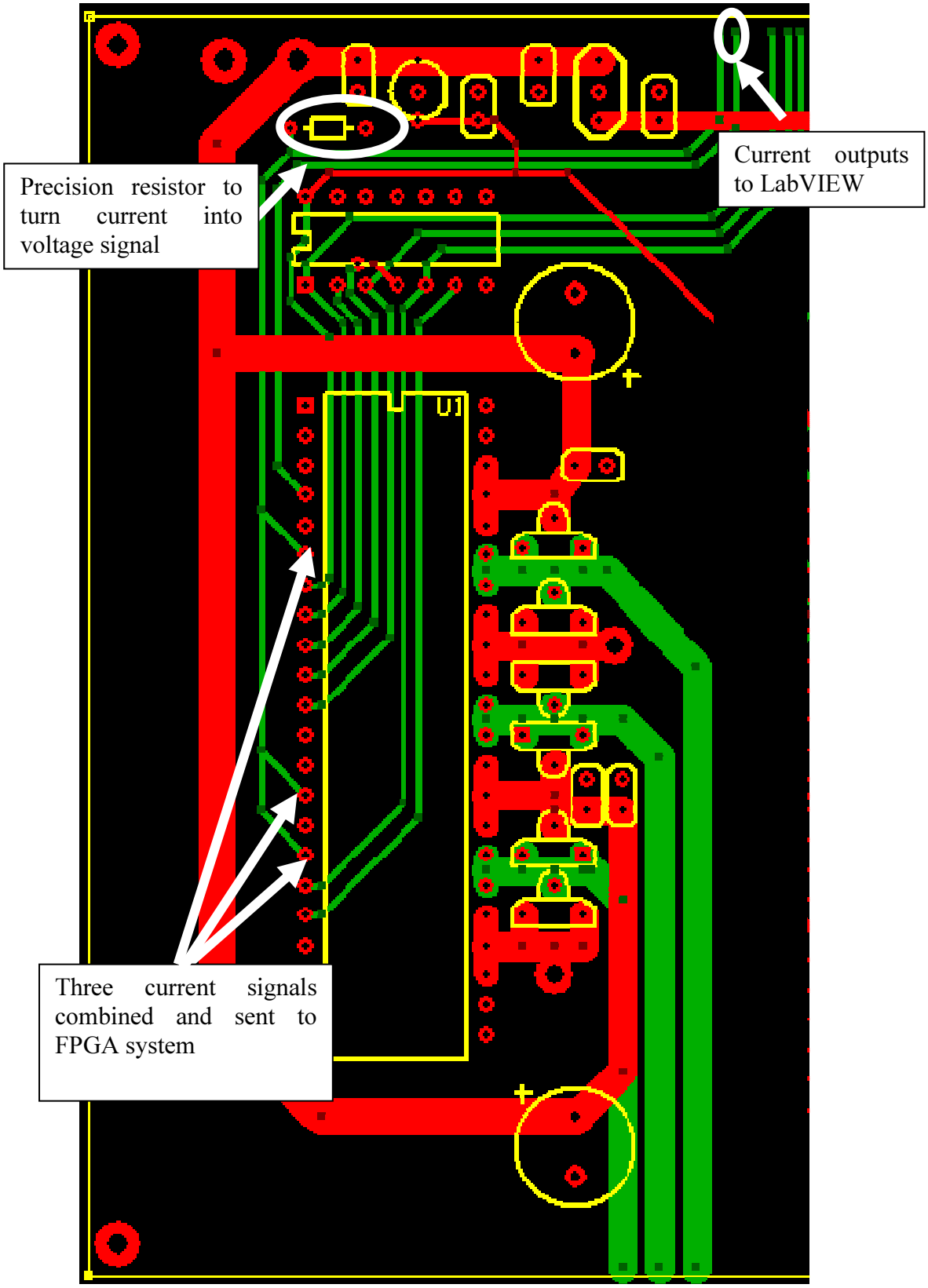

Figure 46: Three Output Current Signals Combined when Sent to FPGA.

2.7 Employed Hardware and Software Summary

The employed hardware and software section presented the following:

- The employed BLDC motor including the calculations validating its performance with regard to the haptic robotic hand application.
- The employed BLDC motor driver circuit including justification that its form (three half bridge circuit) and sizing (up to 15 Amp capacity) are sufficient to drive the selected BLDC motors.
- The employed resolver and justification for its use in this application.
- The employed resolver circuit including the resolver-to-digital aspects necessary to convert the analog signals to digital signals in order to complement the employed LabVIEW FPGA's lack of analog input/outputs and plethora of digital input/outputs.
- A sample LabVIEW program that may be modified in order to implement FOC to control the BLDC motor given torque commands as dictated by the haptic requirements.
- The developed aspects of the BLDC driver circuit necessary in order to implement three phase current acquisition from a single current signal and its correlation with the PWM pulses.

The following chapters demonstrate how this hardware and software were effectively implemented as well as a discussion of future work that will have to be realized in order to fully implement the BLDC motor system into the targeted haptic robotic hand application.

CHAPTER 3: RESULTS

Because the components associated with this research were repurposed prior to the BLDC motors being implemented in a haptic application, the results do not demonstrate the upper most level of haptic-feedback between the user interface and the robotic hand. However, the simple act of demonstrating smooth and reversible rotary motion via the employed hardware and software does demonstrate the implemented system's ability to accommodate the performance criteria imposed by the haptic and radiological constraints, including:

- The circuitry driving the motor was adequately sized to drive the motor.
- The three space vector modulated signals were all operating in their proper respective sectors in both directions.
- The curve fit approximations associated with the space vector modulated signals were sufficiently accurate.
- The resolver position signal properly identified the position of the rotor relative to the stator's three phases.
- The software and associated strategies (e.g. approximated curve fit associated with space vector modulated signals, switch) developed on the FPGA system operated properly within the associated memory space constraints.
- The selected time period associated with the PWM signals provided sufficient time needed to:
    - Extract the resolver position data every cycle such that the present position is constantly communicated to the device.

- Allow the dynamics of the current signal to die out in order to more accurately determine the current data associated with each phase as extracted from the single bus signal (platform for future development).

Results are also presented below related to the required future work necessary to fully realize this system's application in the proposed haptic application including:

- The modification of an acquired LabVIEW FOC program acquired from National Instruments to be applied for torque control rather than speed control.
- The measurement of the three phase currents from a single bus signal current profile via its correlation to the applied PWM signals and how the system dynamics need to be considered via adjustments in the PWM period.

3.1 General BLDC Motor Rotational Operation

Figure 47 shows the BLDC motor being operated. This was performed at full pulse width modulation potential (100% maximum duty cycle). The motor's operation was extremely smooth and reversible based on the sign of the input signal. This indicated that the coding, which controlled the space vector modulation program, works effectively in employing the position data extracted from the resolver-to-digital converter. Under this no load and no motion inhibition, the cycling of the phases was allowed to cool sufficiently during rotation and neither the driver nor the motor overheated.

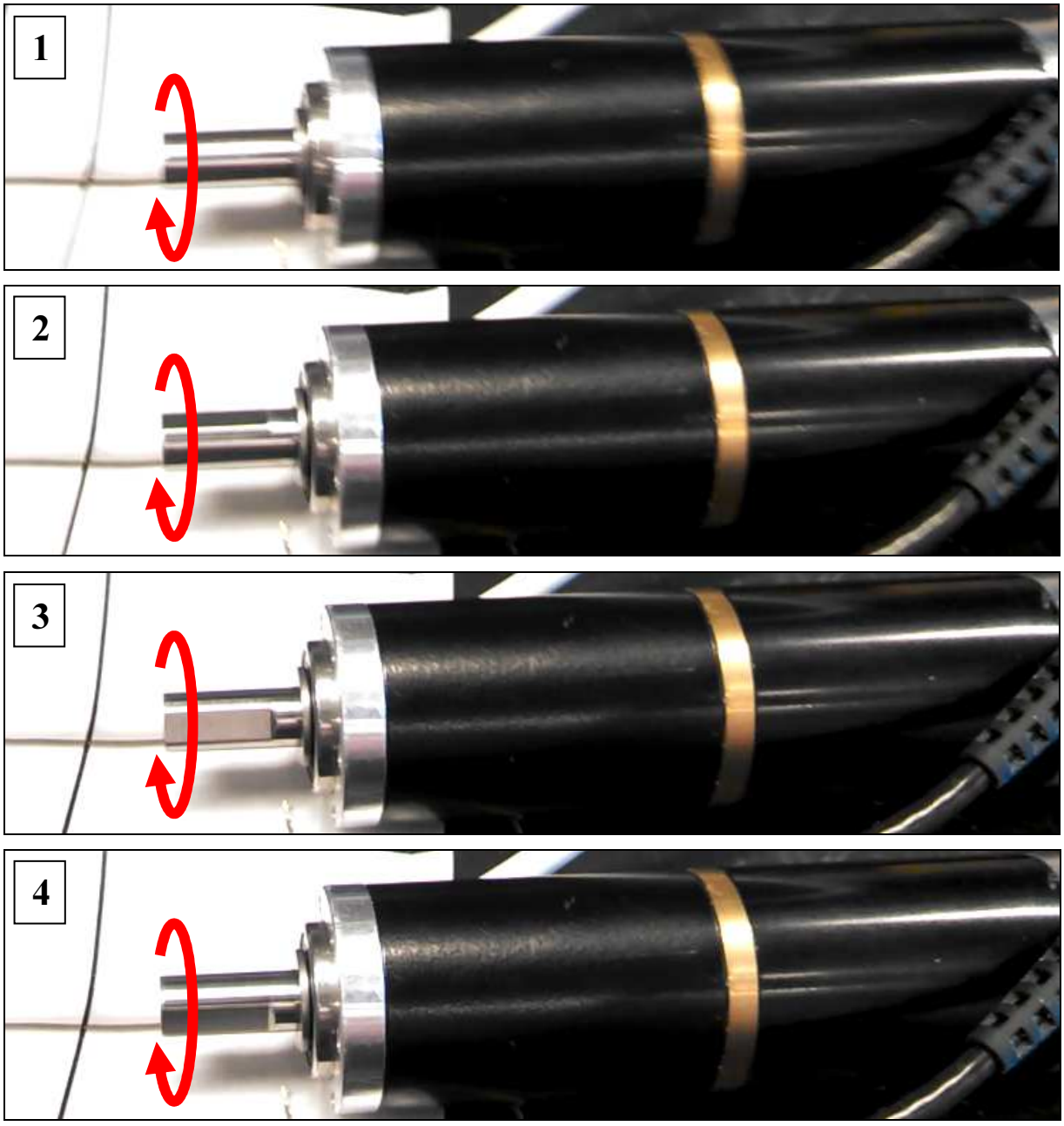

Figure 47: Smooth Motion Progression of Motor Shaft as Motor Turns.

3.2 General BLDC Motor Operation in a Haptic Related Scenario

Unlike the experiment above where the motor movement was uninhibited, haptic applications often require a mechanism to remain in a fixed position while still supplying a torque. This may be the case if the robotic hand is squeezing a compliant object such as a rubber block. This was tested by rigidly securing the shaft and applying a maximum control signal corresponding to a 100% maximum duty cycle potential by any of the phases. When this was applied, the SA 306 driver chip overheated, failed, and was destroyed. In order to prevent this in the future, this research implemented in the coding a maximum possible duty cycle output of less than 100%. A 52% duty cycle has been shown to be sufficiently low that overheating did not occur during the testing. Further testing will have to be conducted to validate that a 52% maximum duty cycle will be sufficient for this application, which is expected to be the case since the calculated demand to capacity ratio comparing the torques required to apply the expected loading (maximum desired fingertip force) to the related motor torque capacity calculated in Section 2.1 is less than this value (27.1%). However, this parameter may be further tuned based on its function when employed in the final device as is discussed in Section 3.3: Duty Cycle Related to Initial Performance.

Another experiment demonstrated the motor/resolver system employed in a single robotic finger. Figure 48 shows the finger both flexing and extending at maximum duty cycle of 0.1/24 = 0.4%. In the video corresponding to this figure it was shown that despite the extremely low duty cycle, the finger clasped at a rate commensurate with that of casual human hand movement. This is encouraging because it shows that the dead zone associated with these BLDC motors is relatively minimal. The dead zone corresponds to friction that

could have been an issue in this haptic application. This is because the hand motion requires the motors to constantly change direction and sometimes hold a position but still maintain a certain level of torque. If there is a dead zone that is rather large, the motors will tend to wind up with potential energy or an amplified torque signal while trying to overcome the dead zone. When they overcome the dead zone there is a sudden release leading to jerky motion. If the dead zone is small the wind up of potential energy when proceeding through the dead zone is less significant and leads to much smoother motion.

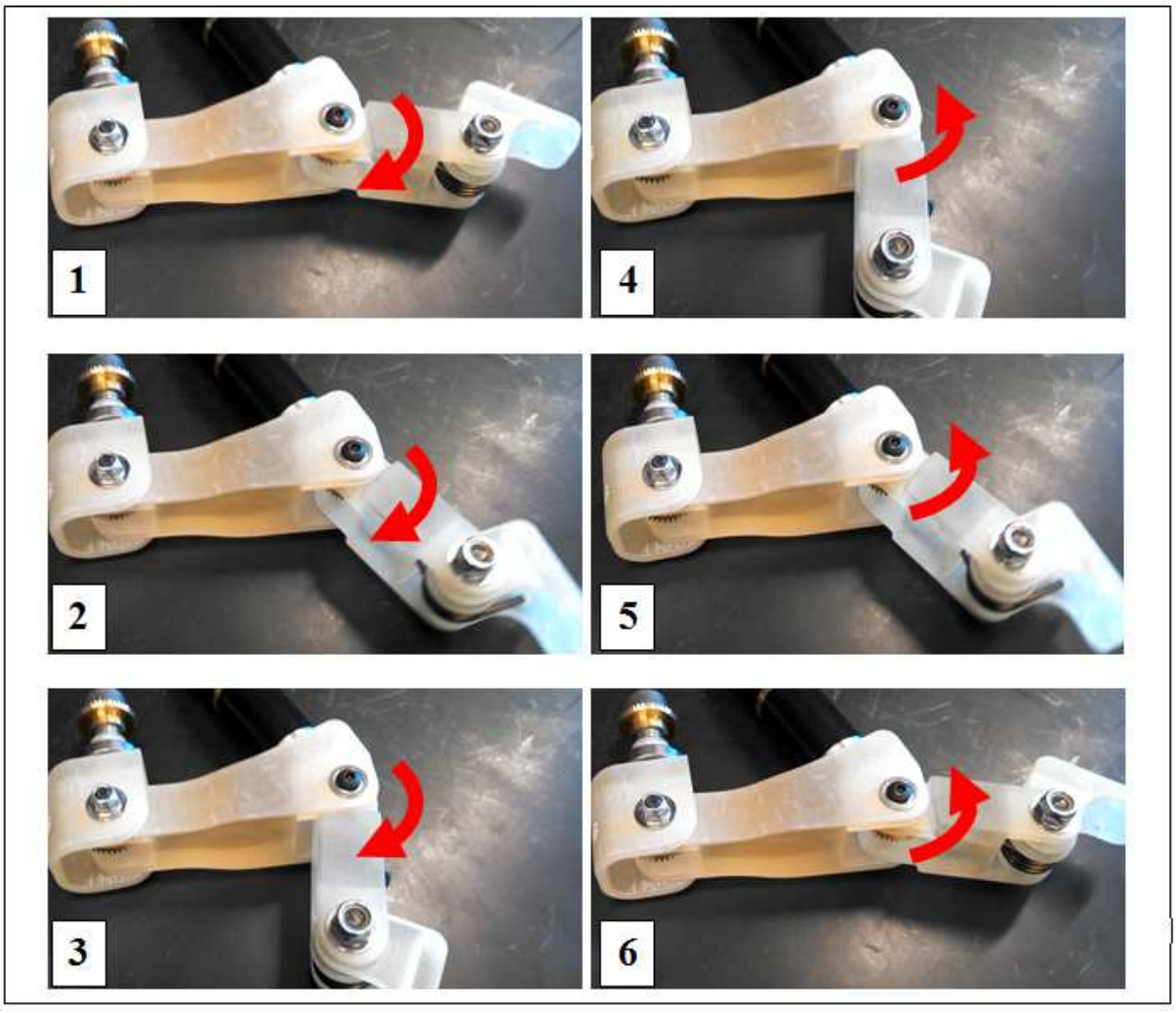

Figure 48: Smooth Motion Progression of Finger as it Closes (1-3) and Opens (4-6)

3.3 Duty Cycle Related to Initial Performance

Given the demonstrated smooth performance presented above it was shown that with a duty ratio allowed to perform up to 100% duty cycle at the peak of the SVM profile input, the system was able to operate smoothly under continuous motion. However, stall conditions are expected in the haptic finger application associated with this research which can produce a consistent current going through each phase resulting in overheating of both the driver circuit and motor. If the maximum allowable duty cycle is not too high the motor gets repeated relief and overheating is mitigated even in a stall condition. As such, the current program employs a 52% maximum duty cycle which may be modified depending on future performance studies as discussed in *Section 4.2: Tuning the Duty Cycle*.

The above discussion applies to the duty cycle as it applies to the motor and driver which is based on the fact that the software in its current configuration sends the PWM signals a 10 bit number (maximum 1024) to represent the maximum number of clock ticks associated with a PWM signal compared to the current period of 2000 clock ticks (thus the maximum 1024/2000 = 52% duty cycle mentioned above). However, this only considered the driver itself and not that of the resolver circuit.

In the resolver circuit the software had to implement the appropriate timing and delays to communicate with the associated digital resolver-to-digital circuit. Some delays implemented in the initial programming attempts were not sufficient and erratic position measurements ensued. This was believed to be a consequence of the dynamics within the system not being allowed to die out prior to sampling of the signal and thus producing improper data. As a result these delays were extended in order to allow the dynamics to die out. However, the

project desired to supply the driver with current position data every cycle and consequently targeted for the position acquisition cycle to be shorter than the period applied to the driver (2000 ticks). The current period for the resolver position and velocity acquisition is 1,575 ticks using conservative delays.

3.4 Reading the Three Phase Current Signals from a Single Analog Line

As discussed, the limited number of available analog inputs prevents this project from acquiring the currents associated with all three phases. As such, this research employed a technique of measuring the three phase currents outputs from the driver, which are combined into a single signal, and correlate them with the pulse width modulated signals associated with each phase.

This combined current signal could have also been acquired from the driver bus current. However, because the SA306 circuit provided these currents independently, the output from nodes were all combined into one line which generated a voltage across a small shunt resistor and was read into the NI system. The circuit nodes that were combined to create this unified current signal are shown in Figure 49.

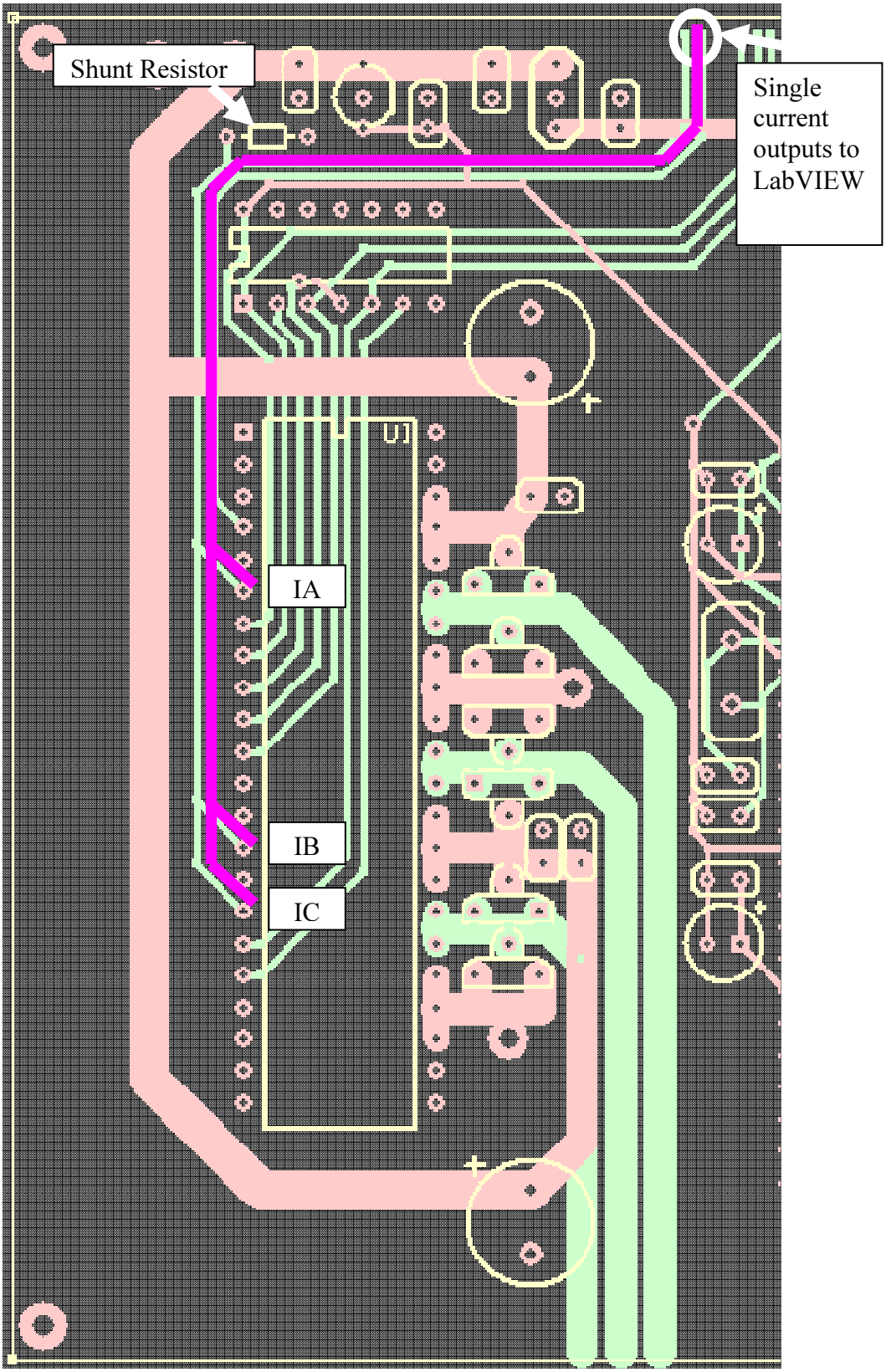

Figure 49: Independent Phase Currents Combined and Delivered to FPGA System.

As discussed in *Section 1.3.8.2.2: FOC Three Phase Current Feedback Requirements Using Bus Current* the PWM signal correlates will with the transitions seen in the bus current signal. This is shown in Figure 50 through Figure 52.

The results in Figure 50 through Figure 52 correspond to a PWM period of 2000 ticks (50 µs) and show that the current dynamics do not appear to settle out between transitions. In the results shown in Figure 53 and Figure 54 the PWM period was increased to 40,000 ticks (1.25 ms). These figures show that the dynamics have had time to settle out after the first initial first order response, which would produce more reliable current data measurements. The 40,000 ticks (1.25 ms) which results in a frequency (800 Hz) is lower than the 1kHz necessary for effective haptic operation. To get the appropriate 1kHz (1ms) period, the PWM period would have had to be adjusted down to 32,000 ticks.

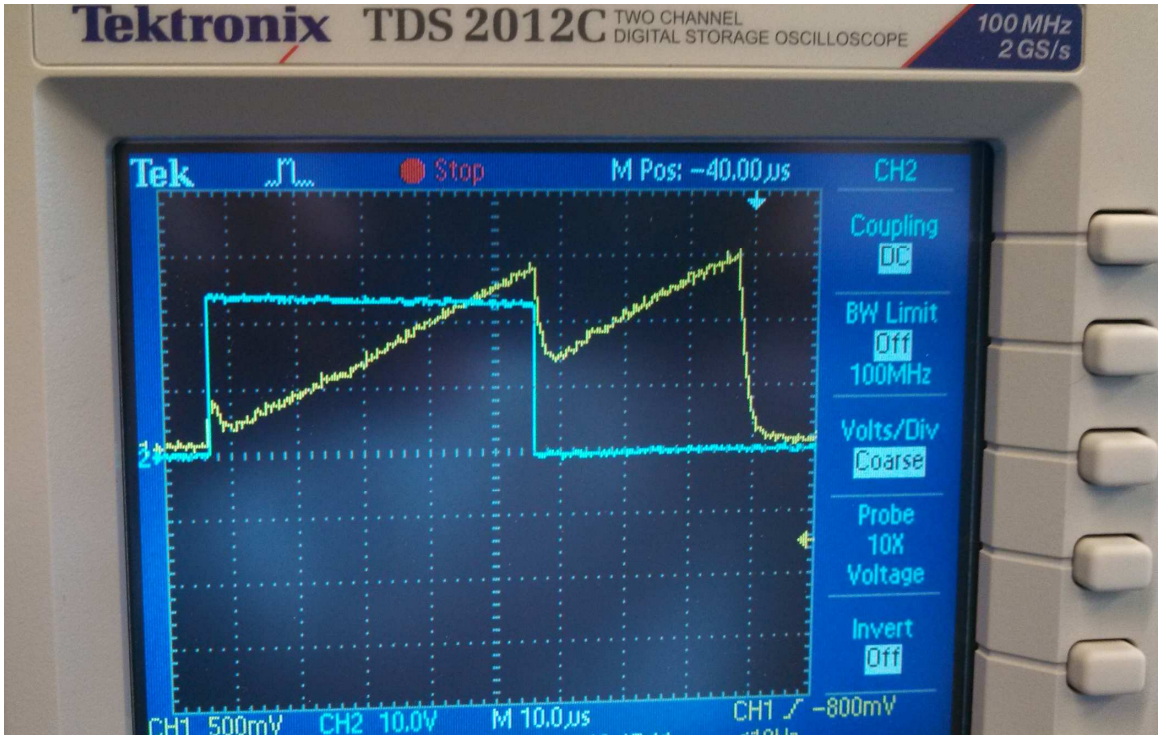

Figure 50: Combined Phase Currents Over the Course of the Mid-Sized PWM Signal.

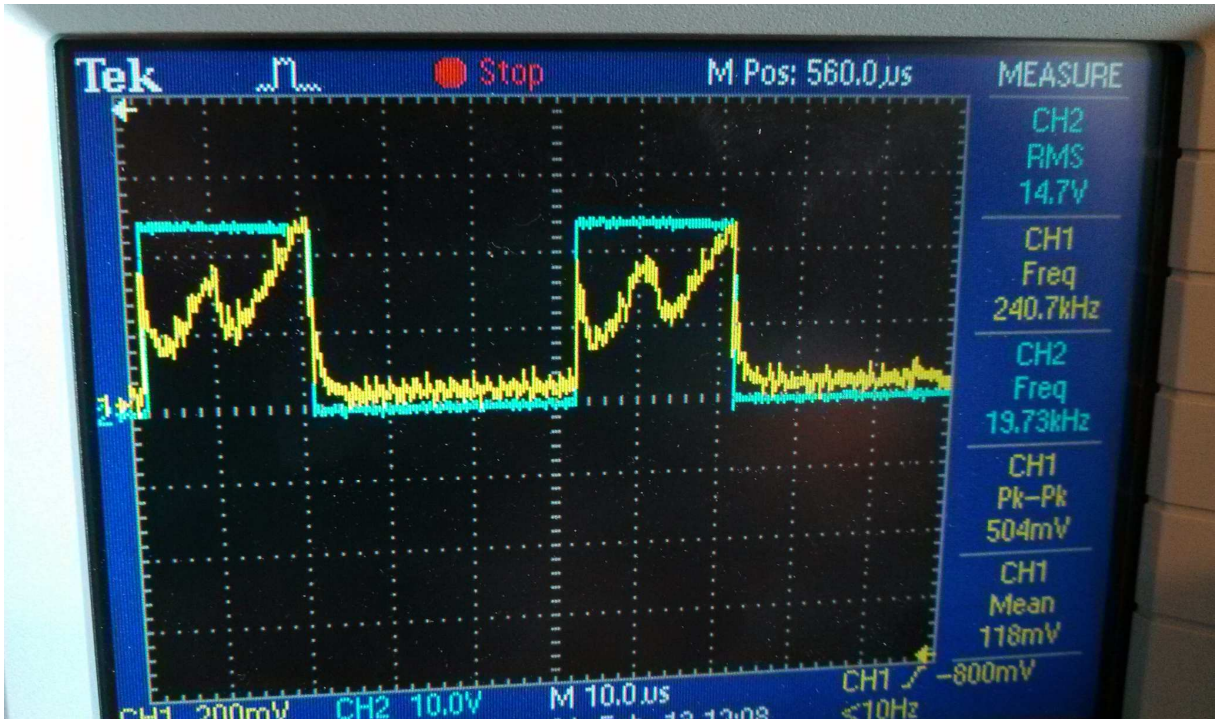

Figure 51: Combined Phase Currents Over the Course of the Largest PWM Signal.

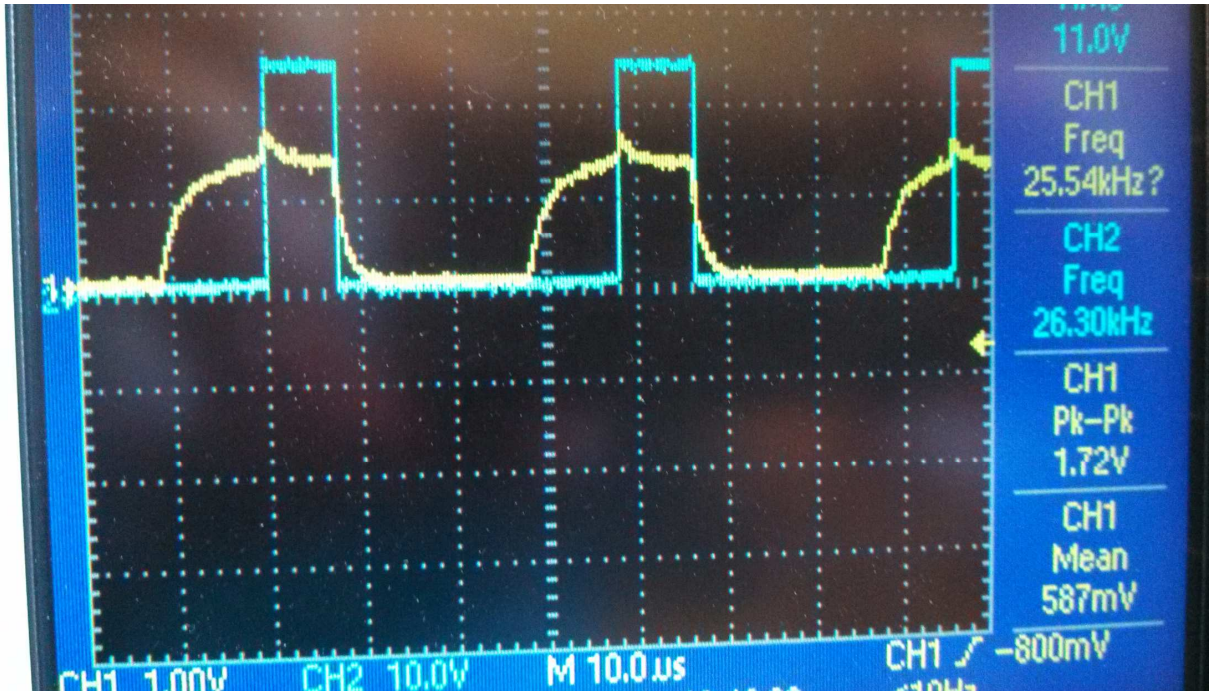

Figure 52: Combined Phase Currents Over the Course of the Mid-Sized PWM Signal.

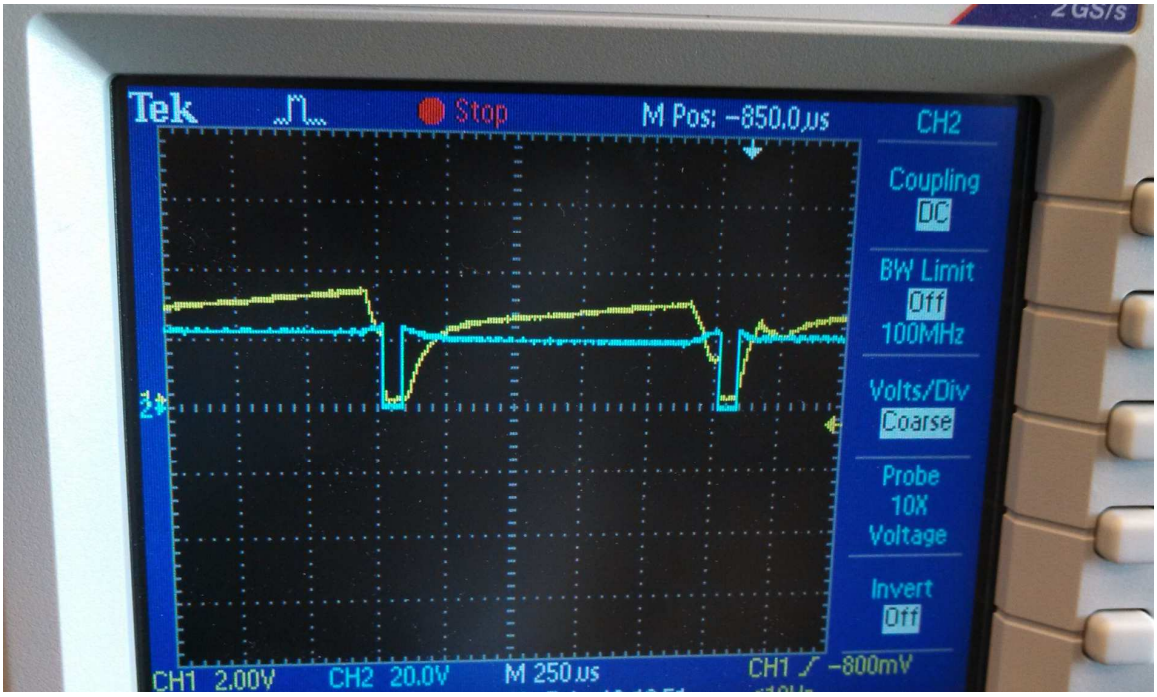

Figure 53: Combined Phase Currents Over the Course of the Largest PWM Signal.

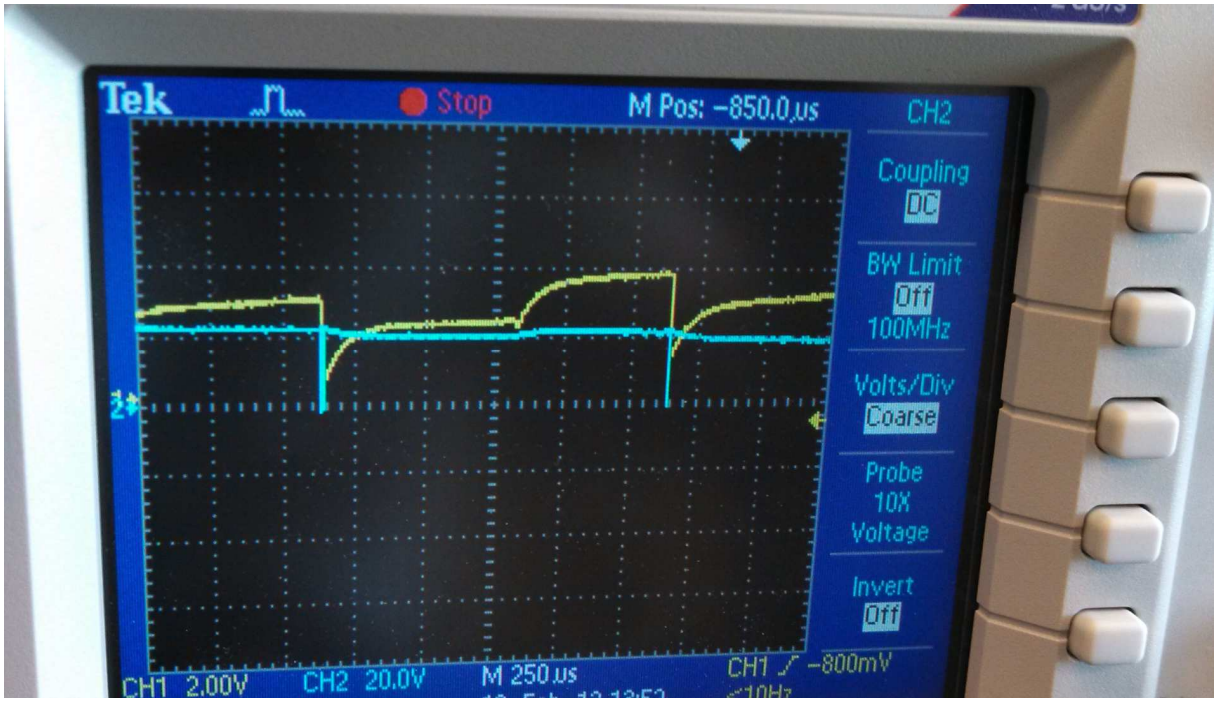

Figure 54: Combined Phase Currents Over the Course of the Largest PWM Signal.

3.5 Results Summary

The results section presented data necessary to validate that the employed hardware, software, and techniques have sufficient promise to enable effective haptic hand operation in a radiological environment. The presented data includes:

- An experiment demonstrating smooth continuous rotational motion employing a maximum duty cycle of 100%.
- An experiment demonstrating the BLDC system's ability to smoothly operate the haptic finger in flexion/extension with adequate speed for manipulation.
- Validation that the currently employed duty cycle (52%) provides promise with regard to generating the necessary torque for this application while providing sufficient breaks in a stall condition such that the motor or driver circuit will not be overloaded and potentially overheat.
- Validation that the correlation between the three phase PWM signals and the single current measurement generated from all three phase signals combined into one has a form suitable to determine the currents experienced by each independent phase.
- Validation that all the software techniques were intelligently structured using switches and operations that were simple enough that they did not require more memory space than the employed FPGA system could provide.

The future work chapter will discuss what work is needed to fully realize the implementation of these BLDC motors into the haptic robotic hand application.

CHAPTER 4: FUTURE WORK

4.1 Haptic Related Testing

In order for the developed BLDC system to be fully qualified for use in a haptic hand application within a radiological environment it will have to demonstrate:

- Speed commensurate to the rotary motion of the human hand joints.
- Torque commensurate to that of the human hand joints to get a desired fingertip force.
- Ability to reliably communicate signals from the BLDC system within a radiological cell to outside the cell with limited distortion.

Experiments to validate these requirements will include manipulation and grasping tasks. Quantitative experiments that will be applied to the device will be similar in nature to those devised by the author and presented in [6] and [7]. The first of these experiments was grasping a virtual cup being filled with a fluid and the second was to use the finger to trace a circle as quickly and accurately as possible. Both experiments were performed while requiring that the user operated within a particular force range. The force range requirement implemented in the virtual cup grasping task simulated a fragile cup that may be crushed if held too tightly or slip out of the hand if held too loosely. The force range requirement implemented in the circle trace application simulated a manipulation task that requires dexterity but applying too much force may cause the object being handled to be broken or flip out of the relatively awkward postures often implemented during manipulation tasks.

Rather than a virtual cup or surface the robotic hand will need to be tested by performing an array of tasks including grasping of a cup being filled with a fluid, tracing a circle on a

surface, operating a screw driver, and screwing in a light bulb, to name a few. Because the robotic finger has its own force sensors it will be able to report quantitative data to qualify and enhance its performance to execute these tasks.

4.2 Tuning the Duty Cycle

Future work will also be performed in order to determine if the haptic performance (as specified in the previous section) can be enhanced by altering the BLDC system's current duty cycle from 52% to an elevated level and the implication this may have on any overloading considerations. Simply changing the duty cycle to a fixed value may present an acceptable intermediate operating point.

More advanced strategies to limit the compromise between stall heat overloading and maximum torque/speed capability may be achieved by also implementing motor velocity measurements. It is proposed that during faster velocities, the motor phases oscillates between high and low current loads and thus allows for breaks which help prevent overheating. During stall, when velocities are near zero, one phase may experience a high current command for an extended period of time and be more prone to overloading. Consequently, it may be of interest to correlate the maximum allowable current with the experienced velocity (e.g. at maximum expected velocity the maximum allowable duty cycle is 100% and at zero velocity the maximum allowable duty cycle is 52%). Experiments may be required to identify optimal values for these two end points and possible linear or nonlinear profiles to link them. The total period is also an intertwined aspect which may need to be adjusted to allow the dynamics to settle out of the current applied to each phase in order to get its full potential without overloading the motor.

Adjusting the period has implications on the resolver-to-digital signal as well and any adjustment will have to provide sufficient time for the inherent dynamics to die out and the circuitry to provide reliable digital outputs.

4.3 Reading the Three Phase Current Signals from a Single Analog Line

Future work will also have to be performed to determine the proper technique to extract the current data. The current period (2000 ticks) shown in Figure 50 through Figure 52 indicates that the current may not have reached its full potential prior to being switched to another phase. The results in Figure 53 and Figure 54 show the result had the PWM period been increased to 40,000 ticks (1.25 ms) and show that the dynamics have settled out and would produce more reliable current data measurements. However, an adverse consequence of increasing the period is that it may cause excessive heating without relief within the driver or motor if the motor is in a stall state. It is postulated that measuring the current immediately before the switch operation will produce the best results. This will have to be validated.

4.4 Adapting NI's FOC Program from Speed to Haptic Torque Control

In order to utilize the FOC control presented in Figure 45 this research intends to modify the PI controller to utilize the torque input as determined in haptic finger serial link torque calculations, which were not discussed in this thesis. The motor torque will be extracted from the measured phase currents. The SVPWM block will be replaced with the SVPWM LabVIEW code developed in *Section1.3.8.2: Field Oriented Control*. These modifications are shown in Figure 55.

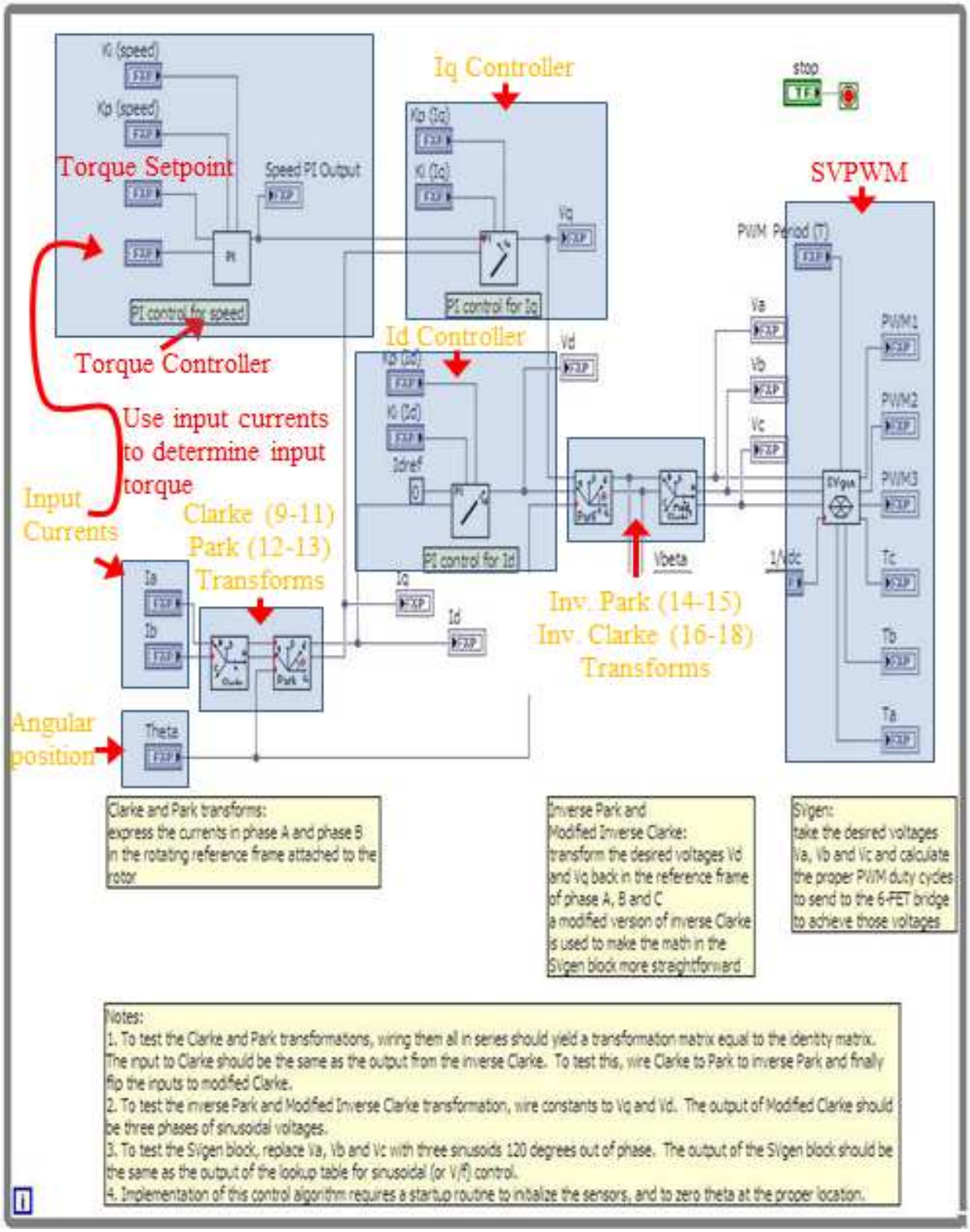

Figure 55: Modified LabView Block Diagram Associated with FOC [16].

4.5 Adapting LabVIEW Code to Simultaneously Operate Multiple Motors

Future work is also required in order to adapt the LabVIEW programs such that they are able to simultaneously operate up to 21 motors. It is anticipated that relatively simple programing would be required to adapt both the driver and resolver-to-digital converter programs.

It is proposed that the BLDC motor driver code presented in *Section 2.2: Employed Brushless Motor Circuit and Associated LabVIEW Script* would require a simple switch that routes the position and control data associated with each motor to the curve fit equations and then to their corresponding PWM period data carrying wire (the data carry wires for all the additional motors would also have to be implemented). This is possible because the current program identifies the required PWM period for each phase only during the first iteration of the cycle. The switch would progress through the motors such that the PWM periods for the first motor are calculated in the first iteration, for the second motor in the second iteration, and so forth. Inputs for each motor's position and outputs sending the PWM data to the driver would also be required.

The resolver read code presented in *Section 2.4: Employed Resolver Circuit and Associated LabVIEW Script* would also have to add additional data carry wires but just for the position, velocity, and fault data associated with each motor. Either additional matrix write blocks or a switch to rotate which motor data is updated could be implemented. Because the delay associated with writing this data in the current program (SCLK delay = 14) is relatively short compared to the number of motors for an entire robotic hand/arm system some adaptation may be required (extending SCLK during the reading portion) if the switch technique using just one FPGA card for all motors is pursued. Additionally, because all of the resolver

circuits require the same input activation signals, they can all be output from the system and connected in parallel to all of the resolver-to-digital converter chips which frees up space on the FPGA system and required digital outputs.

4.6 Future Work Summary

The future work section presented the techniques and experiments that will be pursued in order to fully realize the implementation of these BLDC motors into the haptic robotic hand application. The techniques include:

- Tuning the overall period and duty cycle necessary in order to achieve sufficient 1kHz feedback rate necessary for haptic applications, smooth motion, reliable current data acquisition, and reliable reading of the resolver-to-digital chip without overheating, especially during stall conditions.
- Applying grasping and manipulation experiments (e.g. holding a collapsible cup being filled with fluid, screwing in a light bulb, etc.) to validate that the BLDC motor system can operate sufficiently in a variety of conditions.
- Develop a strategy to read the currents of each phase from a single signal.
- Adapt a LabVIEW FOC program to accept haptic torque set points to be used in control.
- Adapting the LabVIEW SVM and resolver read programs to control/read 21 motors that will be employed in the final haptic hand/arm system.

CHAPTER 5: CONCLUSIONS

This thesis presented a BLDC motor and resolver system driven by SVM commutation capable of controlling a haptic robotic hand in a radiological environment. The employed BLDC motor and resolver technologies have been identified as capable of operating in radiological environments up to and including category D environments (<10,000 Gγ per hour, 1 MGγ total dose). The torque, speed, current, and voltage requirements associated with the BLDC motor were also shown to accommodate the specified haptic force requirements deemed appropriate for targeted in-cell tasks.

The additional hardware capable of supporting the motor's voltage and current needs was also identified. This included the LabVIEW FPGA system and its associated support hardware capable of achieving at least a 1kHz communication rate (without delays) as required for effective haptic operation. The most involved components of the system supporting the motor and resolver were the BLDC driver and resolver-to-digital converter and the supporting software programs.

The driver circuit implemented components capable of handling up to 15 Amps compared to the expected 5.5 Amps calculated for the motor when executing expected tele-operation tasks. The associated LabVIEW software program implemented a unique SVM technique in order to fit within the limited space of the implemented FPGA system. The technique implemented a switching form and curve fits to represent the four primary portions of the SVM form. This technique implemented switching/comparison logic and simple operations such as addition, multiplication, and bit number truncation (replaces division operation) to execute operations

traditionally performed via floating point numbers/operations, trigonometric functions, and division which take up a lot more space on an FPGA system as implemented.

The resolver-to-digital circuit was implemented with adequate timing and lag periods to effectively read the resolver's position, velocity, and fault data. This action was achievable for every cycle performed by the driver circuit thus ensuring that the driver was operating with an appropriate level of real-time data. Like the driver code, the sequence of switchings was sufficiently small in terms of its FPGA footprint to fit on the implemented FPGA system.

Smooth rotary motion of the motor to open and close the haptic finger demonstrated that the mentioned curve fit approximations associated with the space vector modulated signals were sufficiently accurate and properly referenced with respect to the motor phases, and the resolver was sufficiently prompt and accurate to direct the SVM coding.

Proposed future work will include the development of the three phase current measurement system via a single bus current signal and studying the implications that the selected PWM periods may have in achieving this end. Once the current measurement technique is established the project will implement a modified version of the LabVIEW FOC program acquired from National Instruments to be applied for torque control rather than speed control. Only relatively minor adaptations to the driver and resolver-to-digital codes, primarily consisting of straight forward switching structures, are anticipated to convert the system from a single motor to the 21 motors that will be embedded in the proposed haptic robotic hand and arm.

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APPENDIX A: EMPLOYED BRUSHLESS MOTOR DATA SHEET

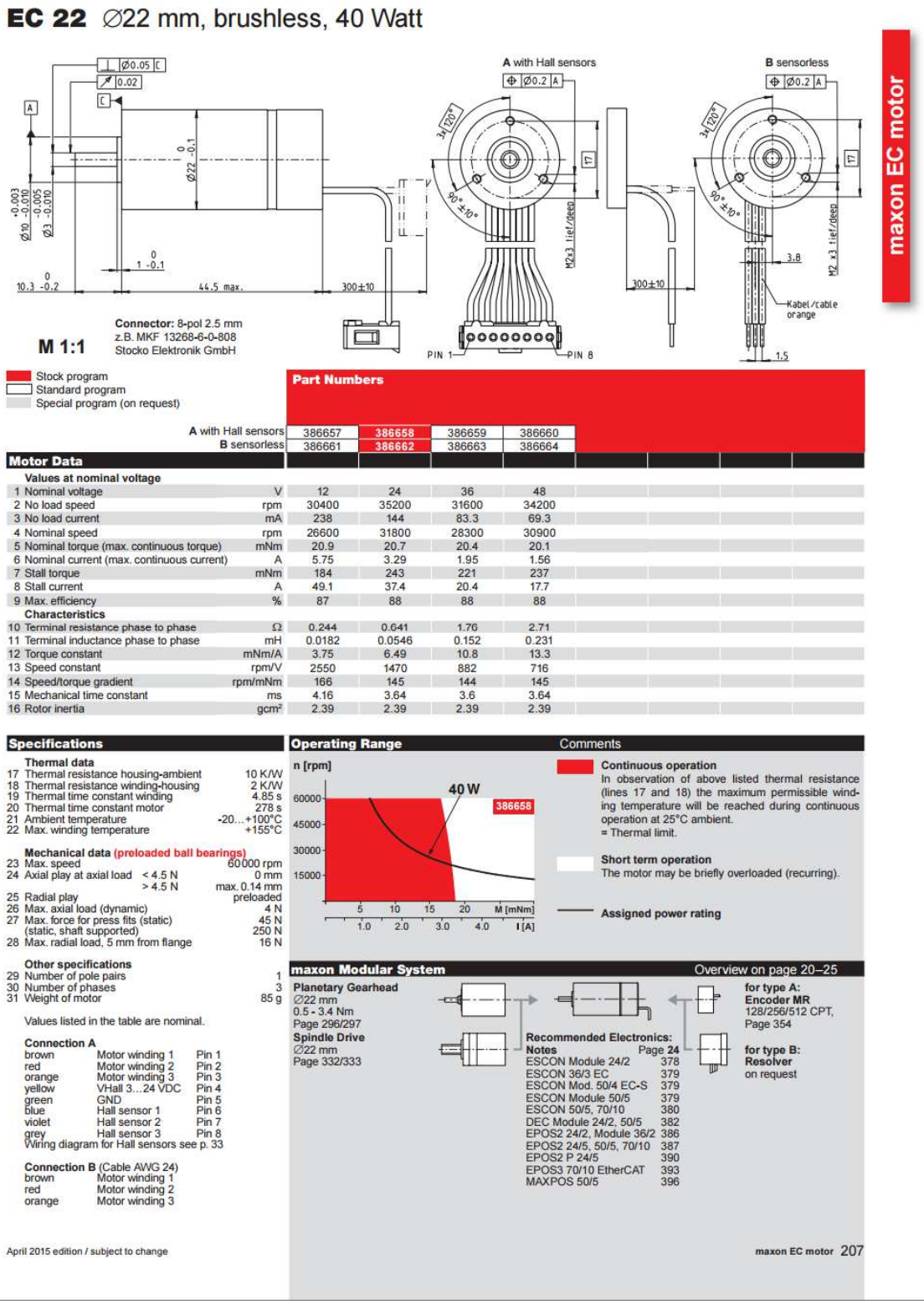
The following Figures indicated which motors where applied in this research as extracted from reference [13].

Combination data		
Nominal voltage	V	48
No load speed	min-¹	646
Max. continuous torque	Nm	1.2
Stall torque	mNm	1.9
Motor data		
Article No.	386664	
Program	EC 22 Ø22 mm, brushless, 40 Watt, sensorless	
Assigned power rating	W	40
Nominal voltage	V	48
No load speed	min-¹	34200
Stall torque	mNm	237
Max. continuous torque	mNm	19.8
Speed / torque gradient	min-¹ / mNm-¹	145
No load current	mA	79.4
Starting current	A	17.7
Terminal resistance	Ohm	2.71
Max. permissible speed	min-¹	60000
Nominal current (max. continuous current)	A	1.54
Max. efficiency	%	87.2
Torque constant	mNm / A-¹	13.3
Speed constant	min-¹ / V-¹	716
Mechanical time constant	ms	3.64
Rotor inertia	gcm²	2.39
Terminal inductance	mH	231
Thermal resistance housing-ambient	KW-¹	10
Thermal resistance winding-housing	KW-¹	2
Thermal time constant winding	s	5.07
Motor lenght	mm	44.5
Motor lenght	mm	44.5
Weight	g	85
Gear data		
Article No.	143980	
Program	Planetary Gearhead GP 22 C Ø22 mm, 0.5 - 2.0 Nm, Ceramic Version	
Reduction		53:1
No. of stages		3
Max. continuous torque	Nm	1.2
Intermittently permissible torque at gear output	Nm	1.9
Sense of rotation, drive to output		=
Max. efficiency	%	59
Average backlash no load	°	1.6
Mass inertia	gcm²	0.4
Gearhead length L1	mm	39
Weight	g	68
Max. motor shaft diameter	mm	4

Figure A 1: Brushless Motor Employed in Research.

Combination data		
Nominal voltage	V	48
No load speed	min-¹	329
Max. continuous torque	Nm	3
Stall torque	mNm	3.5
Gear data		
Article No.	370783	
Program	Planetary Gearhead GP 22 HP Ø22 mm, 2.0 - 3.4 Nm, High Power	
Reduction		104:1
No. of stages		3
Max. continuous torque	Nm	3
Intermittently permissible torque at gear output	Nm	3.5
Sense of rotation, drive to output		=
Max. efficiency	%	59
Average backlash no load	°	1.6
Mass inertia	gcm²	0.4
Gearhead length L1	mm	36
Weight	g	78
Max. motor shaft diameter	mm	3.2
Motor data		
Article No.	386664	
Program	EC 22 Ø22 mm, brushless, 40 Watt, sensorless	
Assigned power rating	W	40
Nominal voltage	V	48
No load speed	min-¹	34200
Stall torque	mNm	237
Max. continuous torque	mNm	19.8
Speed / torque gradient	min-¹ / mNm-¹	145
No load current	mA	79.4
Starting current	A	17.7
Terminal resistance	Ohm	2.71
Max. permissible speed	min-¹	60000
Nominal current (max. continuous current)	A	1.54
Max. efficiency	%	87.2
Torque constant	mNm / A-¹	13.3
Speed constant	min-¹ / V-¹	716
Mechanical time constant	ms	3.64
Rotor inertia	gcm²	2.39
Terminal inductance	mH	231
Thermal resistance housing-ambient	KW-¹	10
Thermal resistance winding-housing	KW-¹	2
Thermal time constant winding	s	5.07
Motor lenght	mm	44.5
Motor lenght	mm	44.5
Weight	g	85

Figure A 2: Brushless Motor Employed in Research.



EC 22 ∅22 mm, brushless, 40 Watt

maxon EC motor

A with Hall sensors

B sensorless

M 1:1

Connector: 8-pol 2.5 mm
z.B. MKF 13268-6-0-808
Stocko Elektronik GmbH

PIN 1 PIN 8

Kabel/cable orange

Stock program
Standard program
Special program (on request)

Part Numbers

A with Hall sensors	386657	386658	386659	386660
B sensorless	386661	386662	386663	386664

Motor Data

	Values at nominal voltage				
1	Nominal voltage	V	12	24	36	48
2	No load speed	rpm	30400	35200	31600	34200
3	No load current	mA	238	144	83.3	69.3
4	Nominal speed	rpm	26600	31800	28300	30900
5	Nominal torque (max. continuous torque)	mNm	20.9	20.7	20.4	20.1
6	Nominal current (max. continuous current)	A	5.75	3.29	1.95	1.56
7	Stall torque	mNm	184	243	221	237
8	Stall current	A	49.1	37.4	20.4	17.7
9	Max. efficiency	%	87	88	88	88
	Characteristics					
10	Terminal resistance phase to phase	Ω	0.244	0.641	1.76	2.71
11	Terminal inductance phase to phase	mH	0.0182	0.0546	0.152	0.231
12	Torque constant	mNm/A	3.75	6.49	10.8	13.3
13	Speed constant	rpm/V	2550	1470	882	716
14	Speed/torque gradient	rpm/mNm	166	145	144	145
15	Mechanical time constant	ms	4.16	3.64	3.6	3.64
16	Rotor inertia	gcm²	2.39	2.39	2.39	2.39

Specifications

Thermal data

17	Thermal resistance housing-ambient	10 K/W
18	Thermal resistance winding-housing	2 K/W
19	Thermal time constant winding	4.85 s
20	Thermal time constant motor	278 s
21	Ambient temperature	-20...+100°C
22	Max. winding temperature	+155°C

Mechanical data (preloaded ball bearings)

23	Max. speed		60000 rpm
24	Axial play at axial load	< 4.5 N	0 mm
		> 4.5 N	max. 0.14 mm
25	Radial play		preloaded
26	Max. axial load (dynamic)		4 N
27	Max. force for press fits (static)		45 N
	(static, shaft supported)		250 N
28	Max. radial load, 5 mm from flange		16 N

Other specifications

29	Number of pole pairs	1
30	Number of phases	3
31	Weight of motor	85 g

Values listed in the table are nominal.

Connection A

brown	Motor winding 1	Pin 1
red	Motor winding 2	Pin 2
orange	Motor winding 3	Pin 3
yellow	VHall 3...24 VDC	Pin 4
green	GND	Pin 5
blue	Hall sensor 1	Pin 6
violet	Hall sensor 2	Pin 7
grey	Hall sensor 3	Pin 8

Wiring diagram for Hall sensors see p. 33

Connection B (Cable AWG 24)

brown	Motor winding 1
red	Motor winding 2
orange	Motor winding 3

Operating Range

n [rpm]

40 W

386658

M [mNm]

I [A]

Comments

Continuous operation
In observation of above listed thermal resistance (lines 17 and 18) the maximum permissible winding temperature will be reached during continuous operation at 25°C ambient.
= Thermal limit.

Short term operation
The motor may be briefly overloaded (recurring).

Assigned power rating

maxon Modular System Overview on page 20–25

Planetary Gearhead
∅22 mm
0.5 - 3.4 Nm
Page 296/297

Spindle Drive
∅22 mm
Page 332/333

Recommended Electronics:

Notes	Page 24
ESCON Module 24/2	378
ESCON 36/3 EC	379
ESCON Mod. 50/4 EC-S	379
ESCON Module 50/5	379
ESCON 50/5, 70/10	380
DEC Module 24/2, 50/5	382
EPOS2 24/2, Module 36/2	386
EPOS2 24/5, 50/5, 70/10	387
EPOS2 P 24/5	390
EPOS3 70/10 EtherCAT	393
MAXPOS 50/5	396

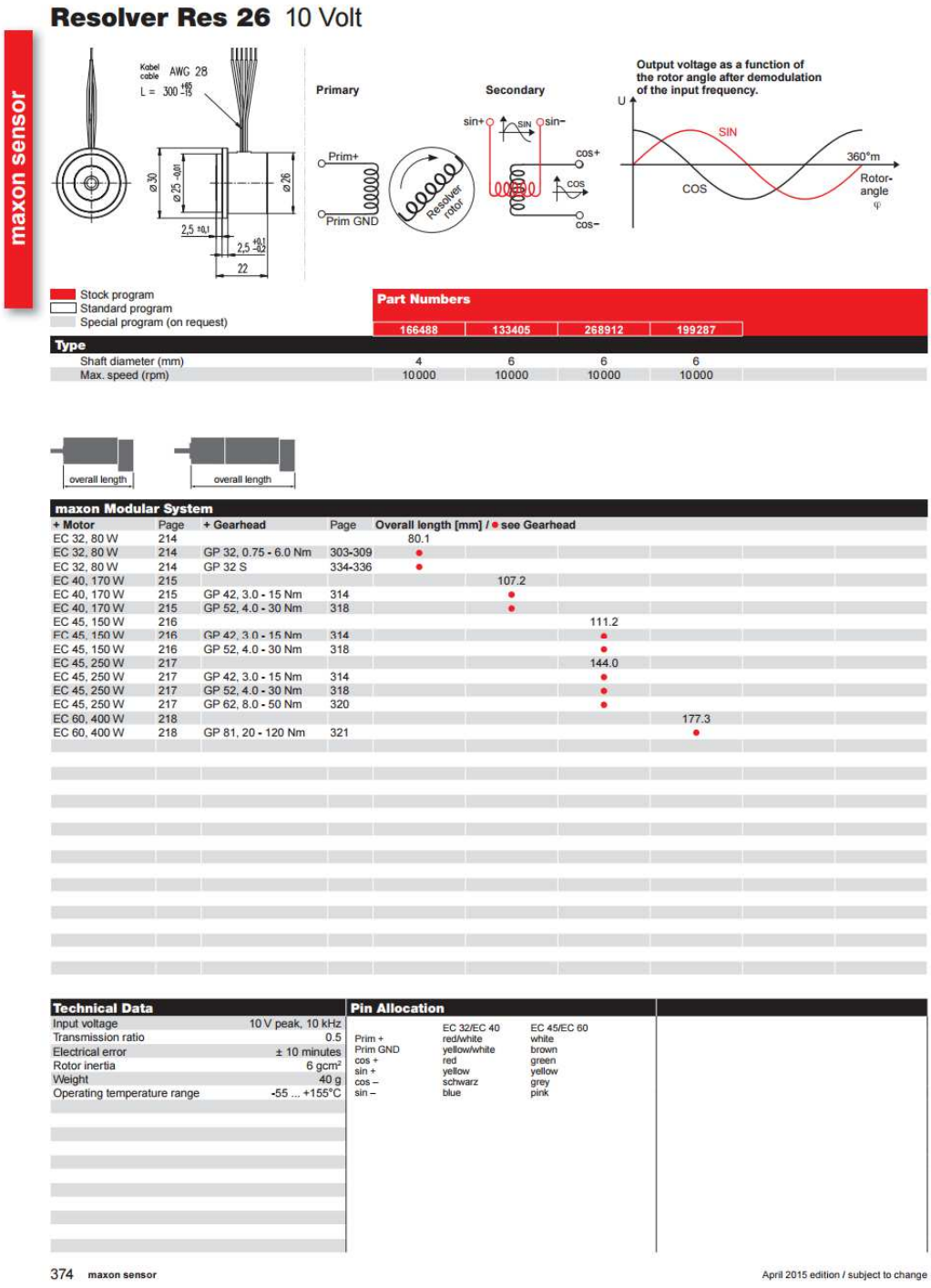
for type A:
Encoder MR
128/256/512 CPT,
Page 354

for type B:
Resolver
on request

Figure A 3: Brushless Motor Employed in Research.

APPENDIX B: EMPLOYED RESOLVER DATA SHEET

Although Maxon Motors did not have a resolver in their catalog that would fit the selected EC 22 motor they did identify the tamagawa TS2640N321E64 resolver would fit the application.



maxon sensor

Resolver Res 26 10 Volt

Kabel cable AWG 28
L = 300 +65 -15

Primary
Prim+
Prim GND
Resolver rotor
Secondary
sin+ sin− cos+ cos cos−
Output voltage as a function of the rotor angle after demodulation of the input frequency.
U
SIN
COS
360°m
Rotor-angle φ

Stock program
Standard program
Special program (on request)

Part Numbers	166488	133405	268912	199287
Type				
Shaft diameter (mm)	4	6	6	6
Max. speed (rpm)	10000	10000	10000	10000

overall length
overall length

maxon Modular System

+ Motor	Page	+ Gearhead	Page	Overall length [mm] / ● see Gearhead			
EC 32, 80 W	214			80.1			
EC 32, 80 W	214	GP 32, 0.75 - 6.0 Nm	303-309	●			
EC 32, 80 W	214	GP 32 S	334-336	●			
EC 40, 170 W	215				107.2		
EC 40, 170 W	215	GP 42, 3.0 - 15 Nm	314		●		
EC 40, 170 W	215	GP 52, 4.0 - 30 Nm	318		●		
EC 45, 150 W	216					111.2	
EC 45, 150 W	216	GP 42, 3.0 - 15 Nm	314			●	
EC 45, 150 W	216	GP 52, 4.0 - 30 Nm	318			●	
EC 45, 250 W	217					144.0	
EC 45, 250 W	217	GP 42, 3.0 - 15 Nm	314			●	
EC 45, 250 W	217	GP 52, 4.0 - 30 Nm	318			●	
EC 45, 250 W	217	GP 62, 8.0 - 50 Nm	320			●	
EC 60, 400 W	218						177.3
EC 60, 400 W	218	GP 81, 20 - 120 Nm	321				●

Technical Data	
Input voltage	10 V peak, 10 kHz
Transmission ratio	0.5
Electrical error	± 10 minutes
Rotor inertia	6 gcm²
Weight	40 g
Operating temperature range	-55 ... +155°C

Pin Allocation	EC 32/EC 40	EC 45/EC 60
Prim +	red/white	white
Prim GND	yellow/white	brown
cos +	red	green
sin +	yellow	yellow
cos –	schwarz	grey
sin –	blue	pink

374 maxon sensor

April 2015 edition / subject to change

Figure B 1: Data Sheet for Maxon Resolver [13].

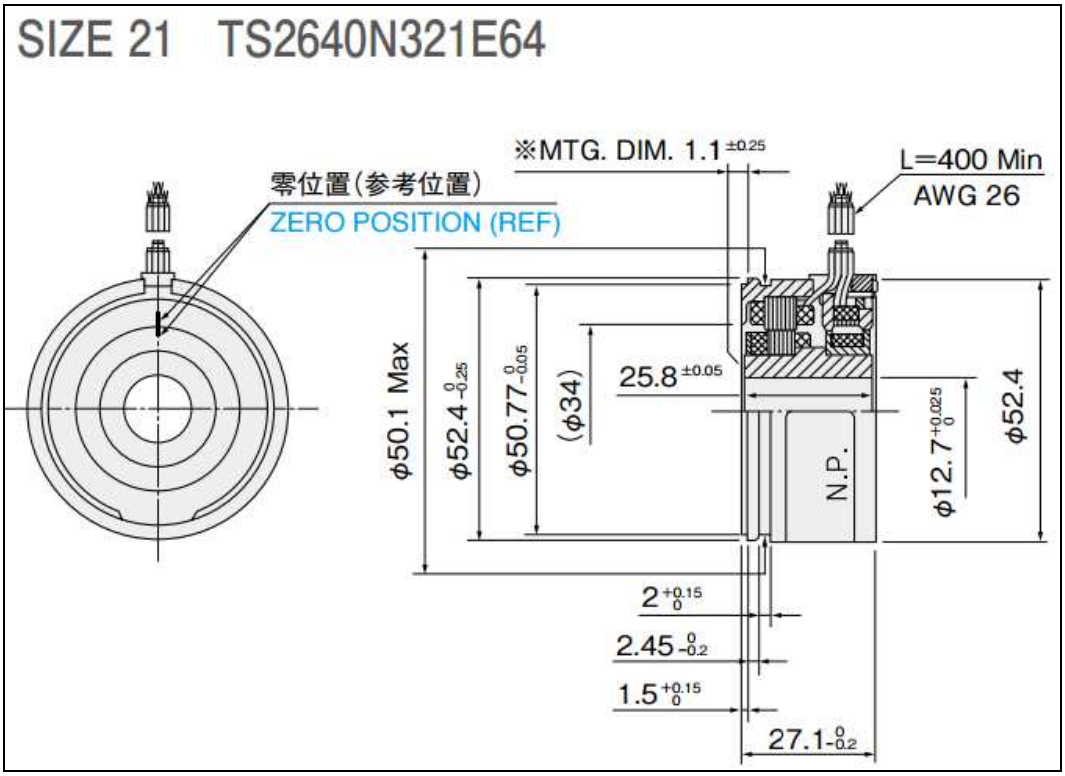


Figure B 2: Geometric Dimensions Associated with Tamagawa Smartsyn TS2605N31E64 Resolver [9].

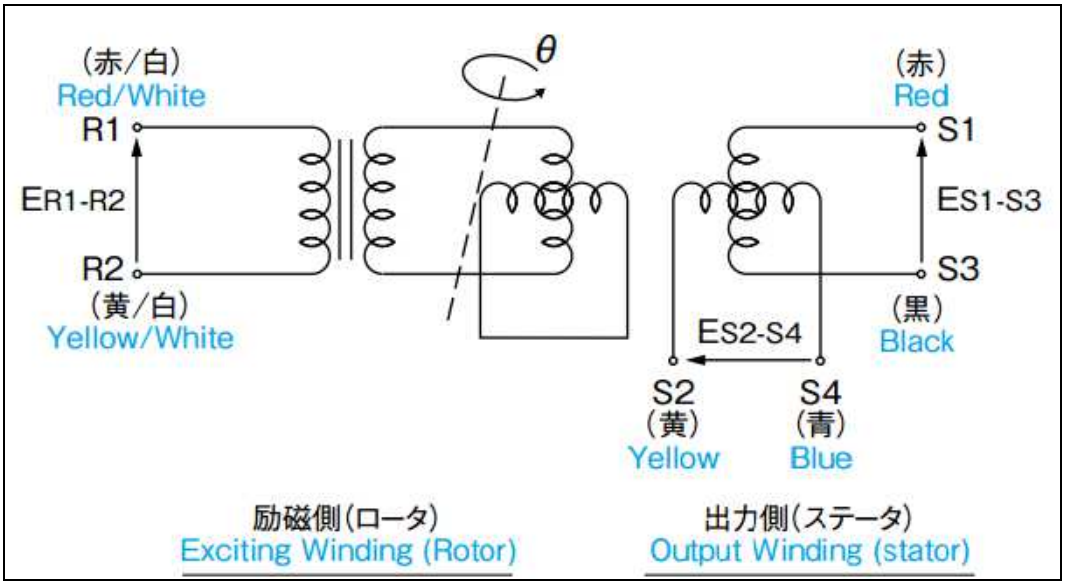


Figure B 3 Wiring Diagram Associated with Tamagawa Smartsyn TS2605N31E64 Resolver as Identified on Top of Circuit Board Shown in Figure 40 [9].

Table B 1: Properties Associated with Tamagawa Smartsyn TS2605N31E64 Resolver [9].

Size		21
Model		TS2640N321E64
Type		1x-BRX
Primary		R1-R2(Rotor)
Input voltage		AC7Vrms 10kHz
Transformation ratio [K]		0.5±5%
Electrical error (Accuracy)		±10'Max
Residual voltage		20mVrms Max
Phase shift		+1°Nom
Input impedance	Z_{ro}	100+j140Ω±15%
Output impedance	Z_{so}	140+j270Ω±15%
	Z_{ss}	120+j240Ω±15%
Allowable rotation speed		10000min^{-1}{rpm}
Operating temperature range		-55°C~+150°C
Dielectric strength		500V AC rms for one minute
Insulation resistance		100MΩMin
Mass		0.28kg Nom

APPENDIX C: MATLAB SCRIPT CALCULATING SVM PROFILE

```
 %This script calculates the SVM signal that should go to the brushless DC
%motor.  The coding followed the values provided by the ATMEL 32-bit AVR
%Microcontroller application note (32094B-AVR32-05/09)Table 6-1.  However,
%when plotting the data it was apparent that there were some
%inconsistencies that made the profiles discontinuous (primarily with the
%linear like region where descending and ascending slopes were switched) as
%such this code modified those inputs from the values provided in the table
step=pi/512;
i=0:step:2*pi;
Ts=1024;
Ts=1;
for k=1:length(i)
    if i(k)<=pi/3
        dk(k)=sin(pi/3-i(k));
        dkp1(k)=sin(i(k));
        Ta(k)=Ts*(1-dk(k)-dkp1(k))/2;
        Tb(k)=Ts*(1+dk(k)-dkp1(k))/2;
        Tc(k)=Ts*(1+dk(k)+dkp1(k))/2;
    end
    if i(k)>pi/3 && i(k)<=2*pi/3
        dk(k)=sin(pi/3+i(k));
        dkp1(k)=sin(5*pi/3+i(k));
        Ta(k)=Ts*(1-dk(k)+dkp1(k))/2;
        Tb(k)=Ts*(1-dk(k)-dkp1(k))/2;
        Tc(k)=Ts*(1+dk(k)+dkp1(k))/2;
        m=k
    end
```

```
if i(k)>2*pi/3 && i(k)<=pi
    dk(k)=sin(i(k));
    dkp1(k)=sin(4*pi/3+i(k));
    Ta(k)=Ts*(1+dk(k)+dkp1(k))/2;
    Tb(k)=Ts*(1-dk(k)-dkp1(k))/2;
    Tc(k)=Ts*(1+dk(k)-dkp1(k))/2;
end
if i(k)>pi && i(k)<=4*pi/3
    dk(k)=sin(5*pi/3+i(k));
    dkp1(k)=sin(6*pi/3-i(k));
    Ta(k)=Ts*(1+dk(k)+dkp1(k))/2;
    Tb(k)=Ts*(1-dk(k)+dkp1(k))/2;
    Tc(k)=Ts*(1-dk(k)-dkp1(k))/2;%Modified from Ts*(1-dk(k)+dkp1(k))/2
    M=k
end
if i(k)>4*pi/3 && i(k)<=5*pi/3
    dk(k)=sin(4*pi/3+i(k));
    dkp1(k)=sin(1*pi/3-i(k));
    Ta(k)=Ts*(1+dk(k)-dkp1(k))/2;
    Tb(k)=Ts*(1+dk(k)+dkp1(k))/2;
    Tc(k)=Ts*(1-dk(k)-dkp1(k))/2;
end
if i(k)>5*pi/3 && i(k)<=6*pi/3
    dk(k)=sin(6*pi/3-i(k));
    dkp1(k)=sin(1*pi/3+i(k));
    Ta(k)=Ts*(1-dk(k)-dkp1(k))/2;
    Tb(k)=Ts*(1+dk(k)+dkp1(k))/2;
    Tc(k)=Ts*(1-dk(k)+dkp1(k))/2;
```

```
    end
end

I=0:length(i)-1
Figure(1)
plot(I,Ta,'r',I,Tb,'g',I,Tc,'b')
title('SVM CCW Profiles')
ylabel('duty cycle duration')
xlabel('Resolver 10 bit Position')
axis([0 1024 0 1])
legend('Ta','Tb','Tc')

n=1:length(i);
MTa(:,1)=n;     MTa(:,2)=Ta;
fileIDa     =     fopen('Ta.txt','w+');     fprintf(fileIDa,'%12.8f\r\n',Ta);
fclose(fileIDa)

MTb(:,1)=n;     MTb(:,2)=Tb;
fileIDb     =     fopen('Tb.txt','w+');     fprintf(fileIDb,'%12.8f\r\n',Tb);
fclose(fileIDb);

MTc(:,1)=n;     MTc(:,2)=Tc;
fileIDc     =     fopen('Tc.txt','w+');     fprintf(fileIDc,'%12.8f\r\n',Tc);
fclose(fileIDc);

clear
step=pi/512;
```

```
i=0:step:2*pi-step;
Ts=1;
for k=1:length(i)
    if i(k)<=pi/3
        dk(k)=sin(pi/3-i(k));
        dkp1(k)=sin(i(k));
        Ta(k)=Ts*(1+dk(k)+dkp1(k))/2;
        Tb(k)=Ts*(1-dk(k)-dkp1(k))/2;
        Tc(k)=Ts*(1+dk(k)-dkp1(k))/2;%Modified from Ts*(1-dk(k)+dkp1(k))/2;
    end
    if i(k)>pi/3 && i(k)<=2*pi/3
        dk(k)=sin(pi/3+i(k));
        dkp1(k)=sin(5*pi/3+i(k));
        Ta(k)=Ts*(1+dk(k)+dkp1(k))/2;
        Tb(k)=Ts*(1-dk(k)+dkp1(k))/2;%Modified from Ts*(1+dk(k)-dkp1(k))/2;
        Tc(k)=Ts*(1-dk(k)-dkp1(k))/2;
        m=k
    end
    if i(k)>2*pi/3 && i(k)<=pi
        dk(k)=sin(i(k));
        dkp1(k)=sin(4*pi/3+i(k));
        Ta(k)=Ts*(1+dk(k)-dkp1(k))/2;%Modified from Ts*(1-dk(k)+dkp1(k))/2;
        Tb(k)=Ts*(1+dk(k)+dkp1(k))/2;
        Tc(k)=Ts*(1-dk(k)-dkp1(k))/2;
    end
    if i(k)>pi && i(k)<=4*pi/3
        dk(k)=sin(5*pi/3+i(k));
        dkp1(k)=sin(6*pi/3-i(k));
```

```
        Ta(k)=Ts*(1-dk(k)-dkp1(k))/2;
        Tb(k)=Ts*(1+dk(k)+dkp1(k))/2;
        Tc(k)=Ts*(1-dk(k)+dkp1(k))/2;%Modified from Ts*(1+dk(k)-dkp1(k))/2;
        M=k
    end
    if i(k)>4*pi/3 && i(k)<=5*pi/3
        dk(k)=sin(4*pi/3+i(k));
        dkp1(k)=sin(1*pi/3-i(k));
        Ta(k)=Ts*(1-dk(k)-dkp1(k))/2;
        Tb(k)=Ts*(1+dk(k)-dkp1(k))/2;%Modified from Ts*(1-dk(k)+dkp1(k))/2;
        Tc(k)=Ts*(1+dk(k)+dkp1(k))/2;
    end
    if i(k)>5*pi/3 && i(k)<=6*pi/3
        dk(k)=sin(6*pi/3-i(k));
        dkp1(k)=sin(1*pi/3+i(k));
        Ta(k)=Ts*(1-dk(k)+dkp1(k))/2;%Modified from Ts*(1+dk(k)-dkp1(k))/2;
        Tb(k)=Ts*(1-dk(k)-dkp1(k))/2;
        Tc(k)=Ts*(1+dk(k)+dkp1(k))/2;
    end
end
I=0:length(i)-1
Figure(2)
plot(I,Ta,'r',I,Tb,'g',I,Tc,'b')
title('SVM CW Profiles')
ylabel('duty cycle duration')
xlabel('Resolver 10 bit Position')
axis([0 1024 0 1])
legend('Ta','Tb','Tc')
```

APPENDIX D: BRUSHLESS MOTOR LABVIEW PROGRAM

The figures in this appendix demonstrate all possible conditions that might arise in order to realize full SVM using the curve fit technique.

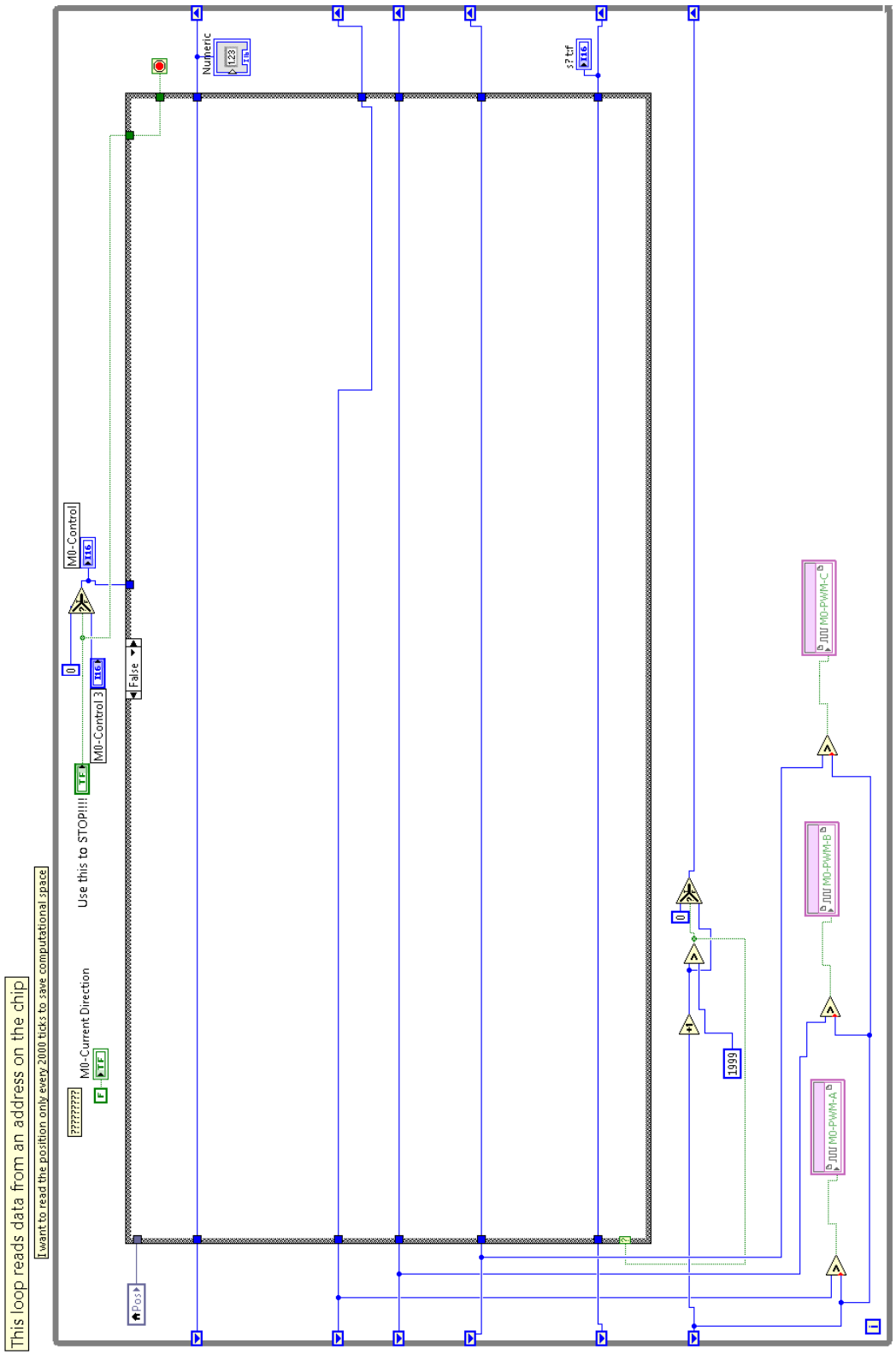


Figure D 1: False condition that occurs during the majority of the time forcing the calculated control signal to only be read once every 2000 ticks of the clock.

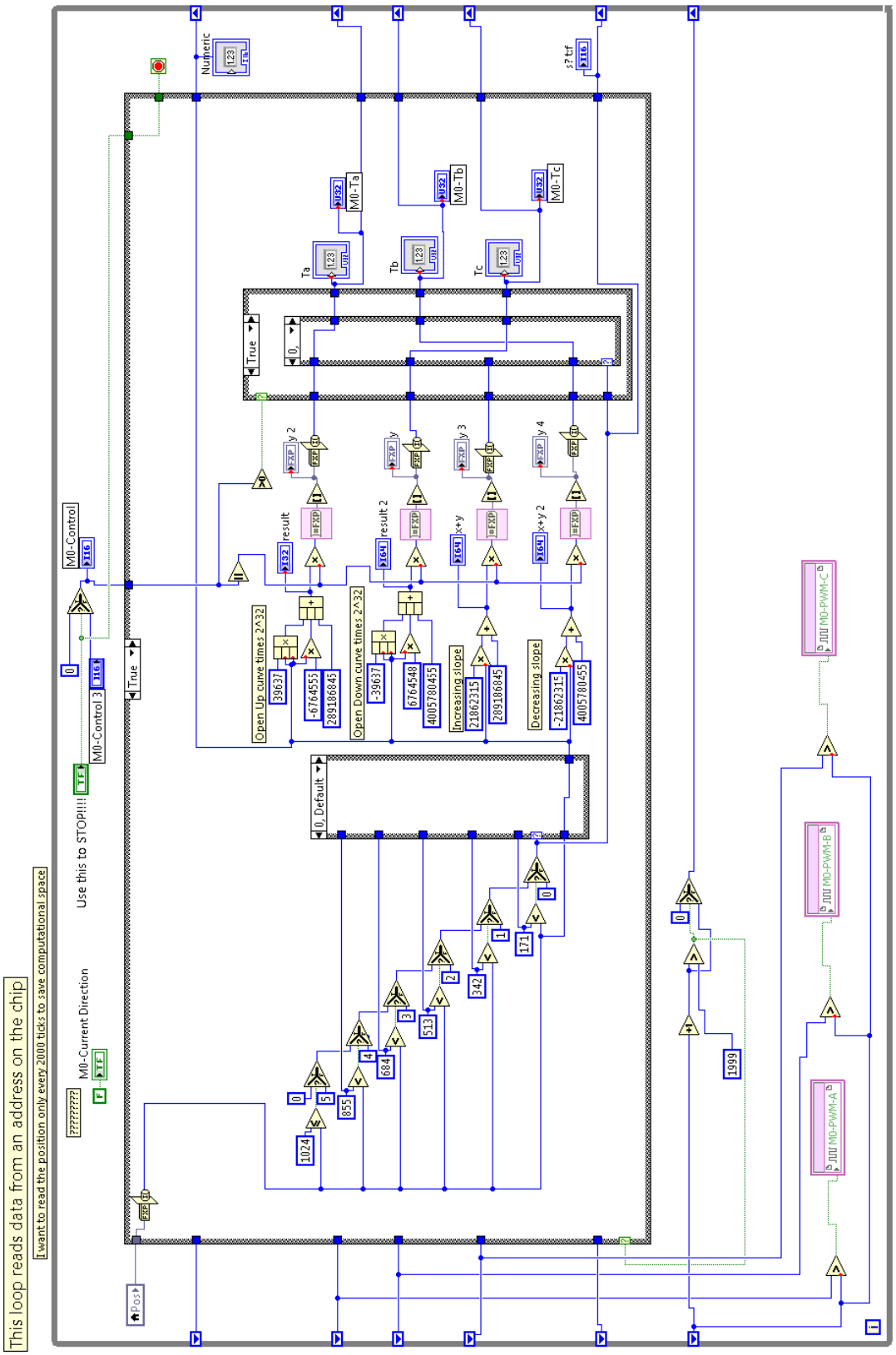


Figure D 2: True condition phase 1 clockwise SVM operation.

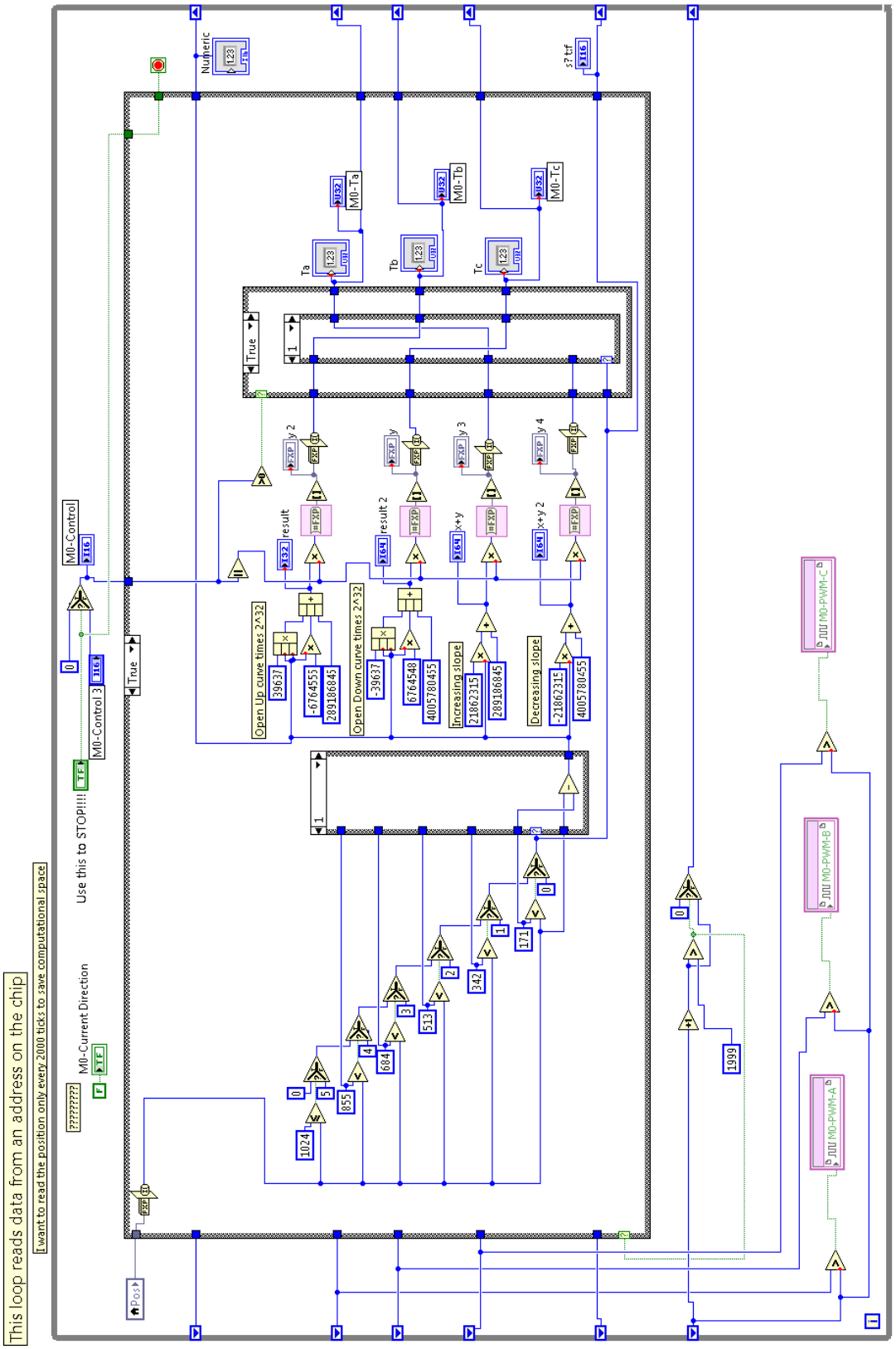


Figure D 3: True condition phase 2 clockwise SVM operation.

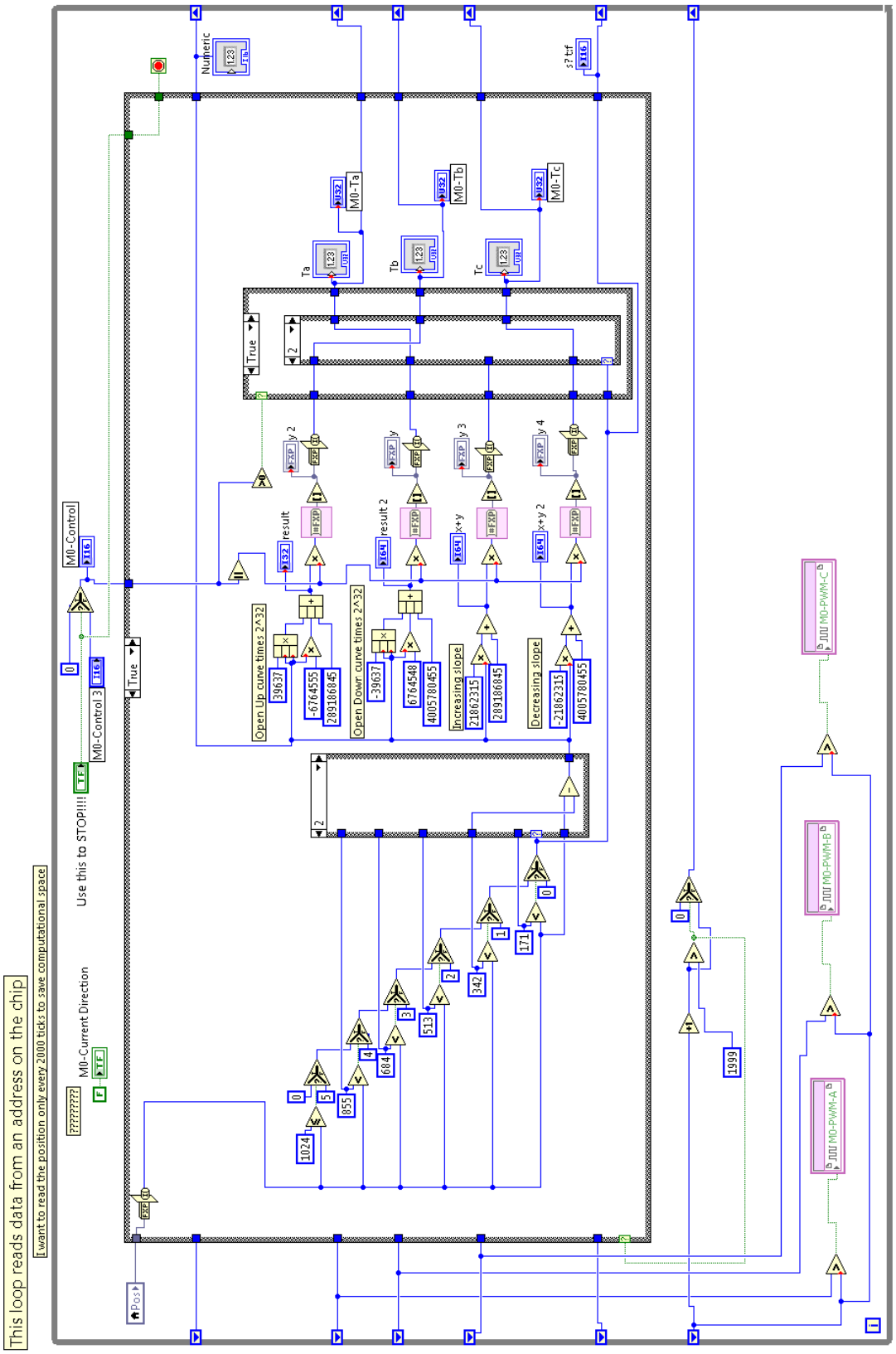


Figure D 4: True condition phase 3 clockwise SVM operation.

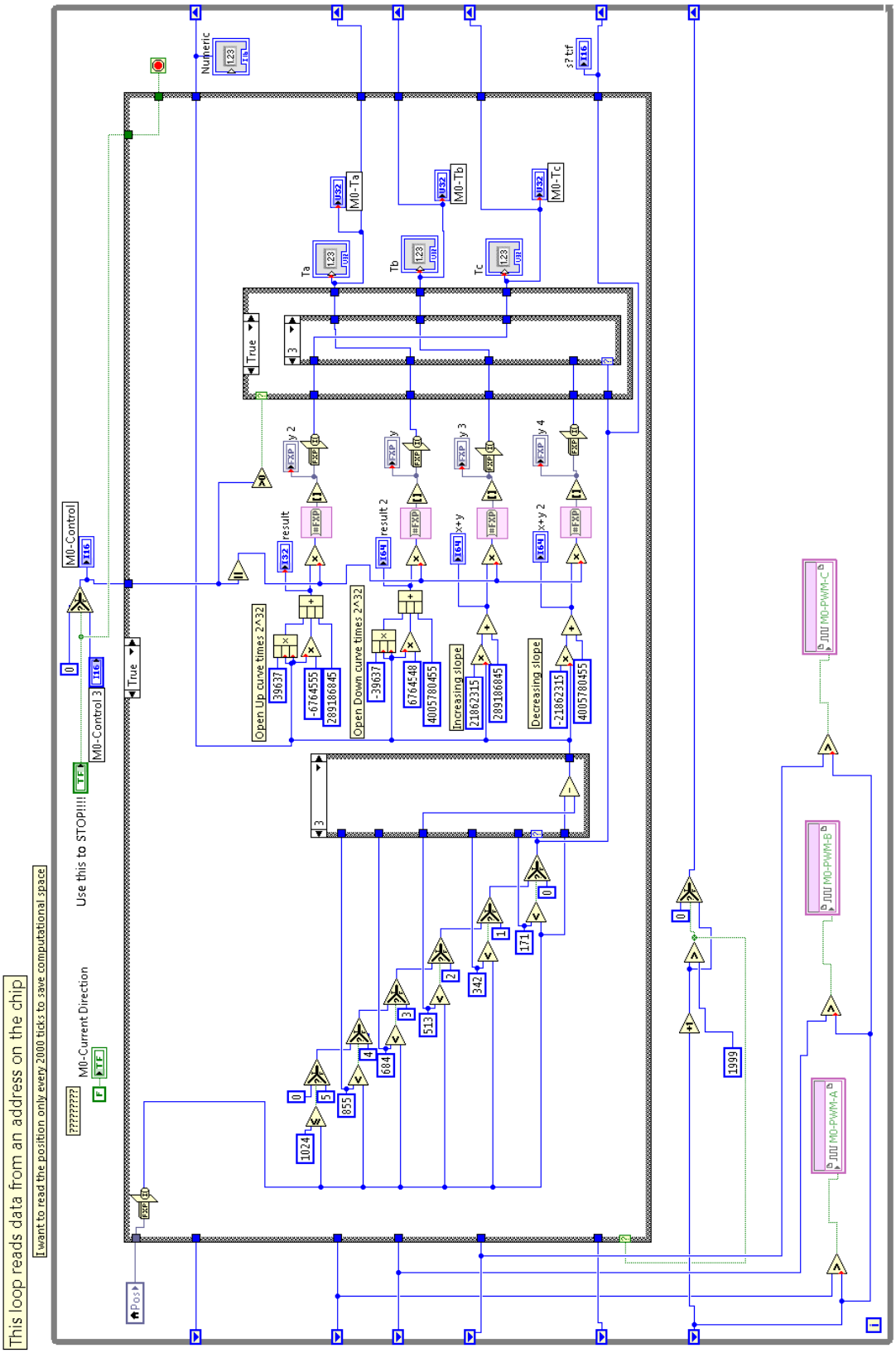


Figure D 5: True condition phase 4 clockwise SVM operation.

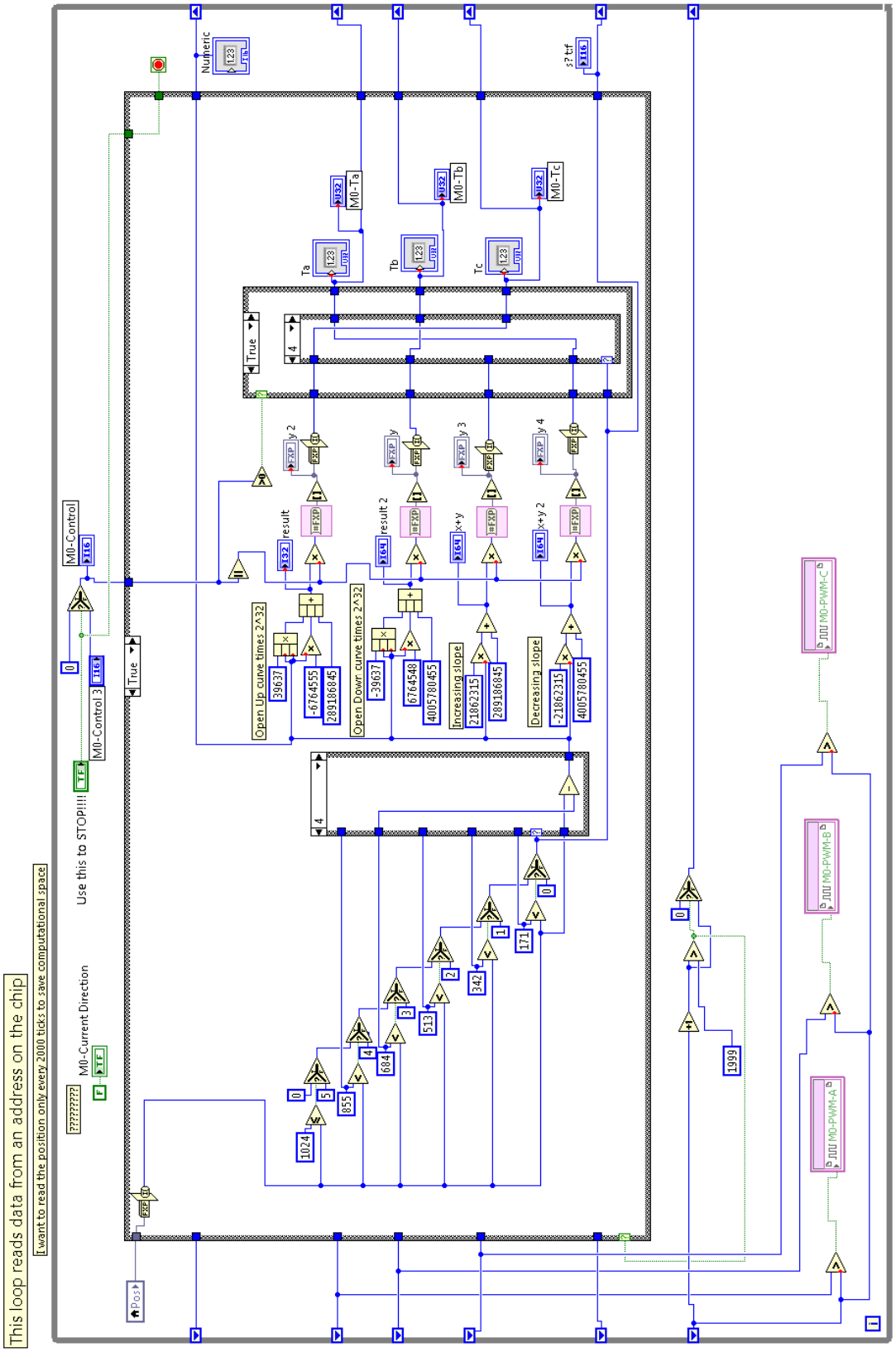


Figure D 6: True condition phase 5 clockwise SVM operation.

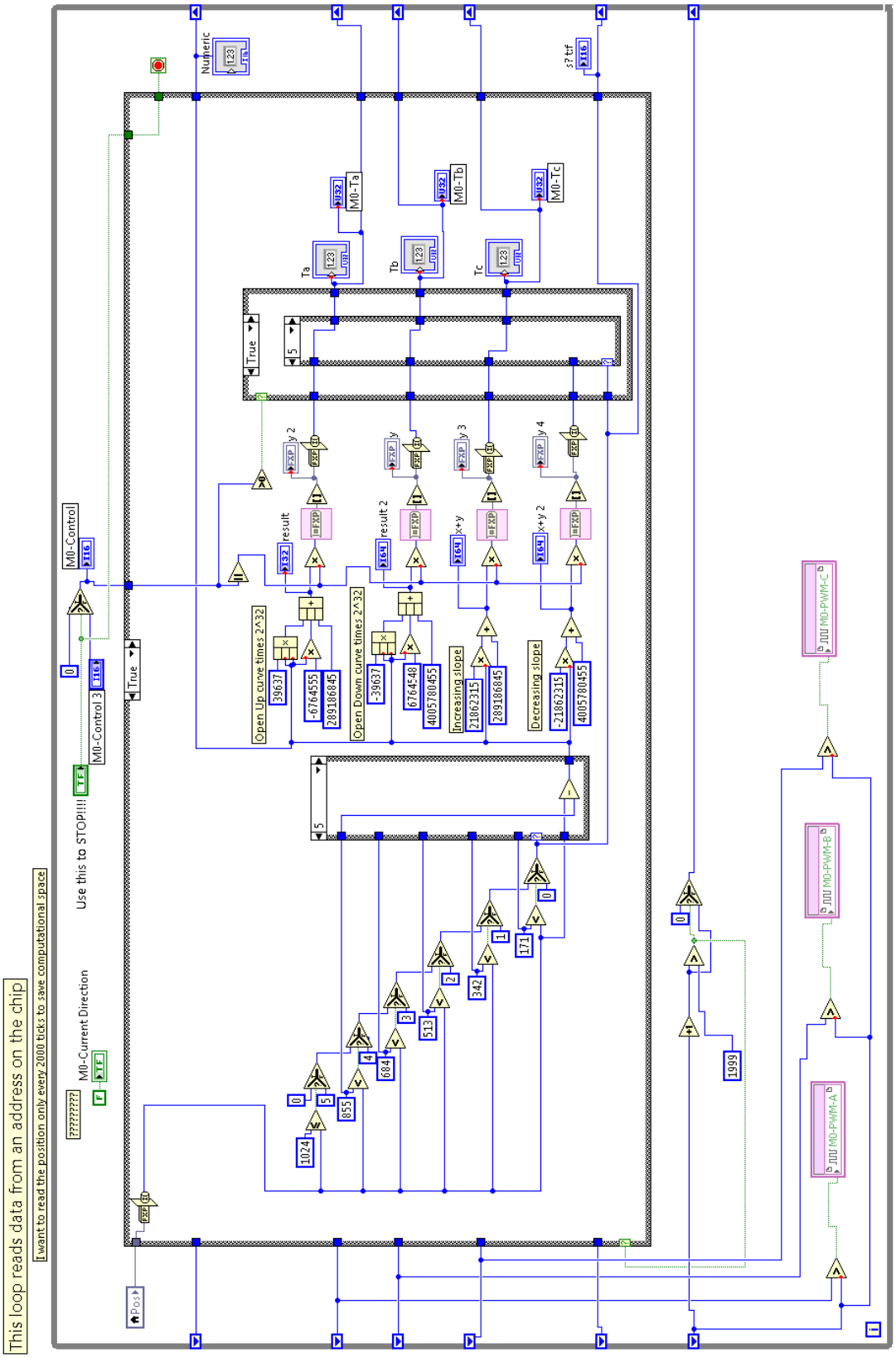


Figure D 7: True condition phase 6 clockwise SVM operation.

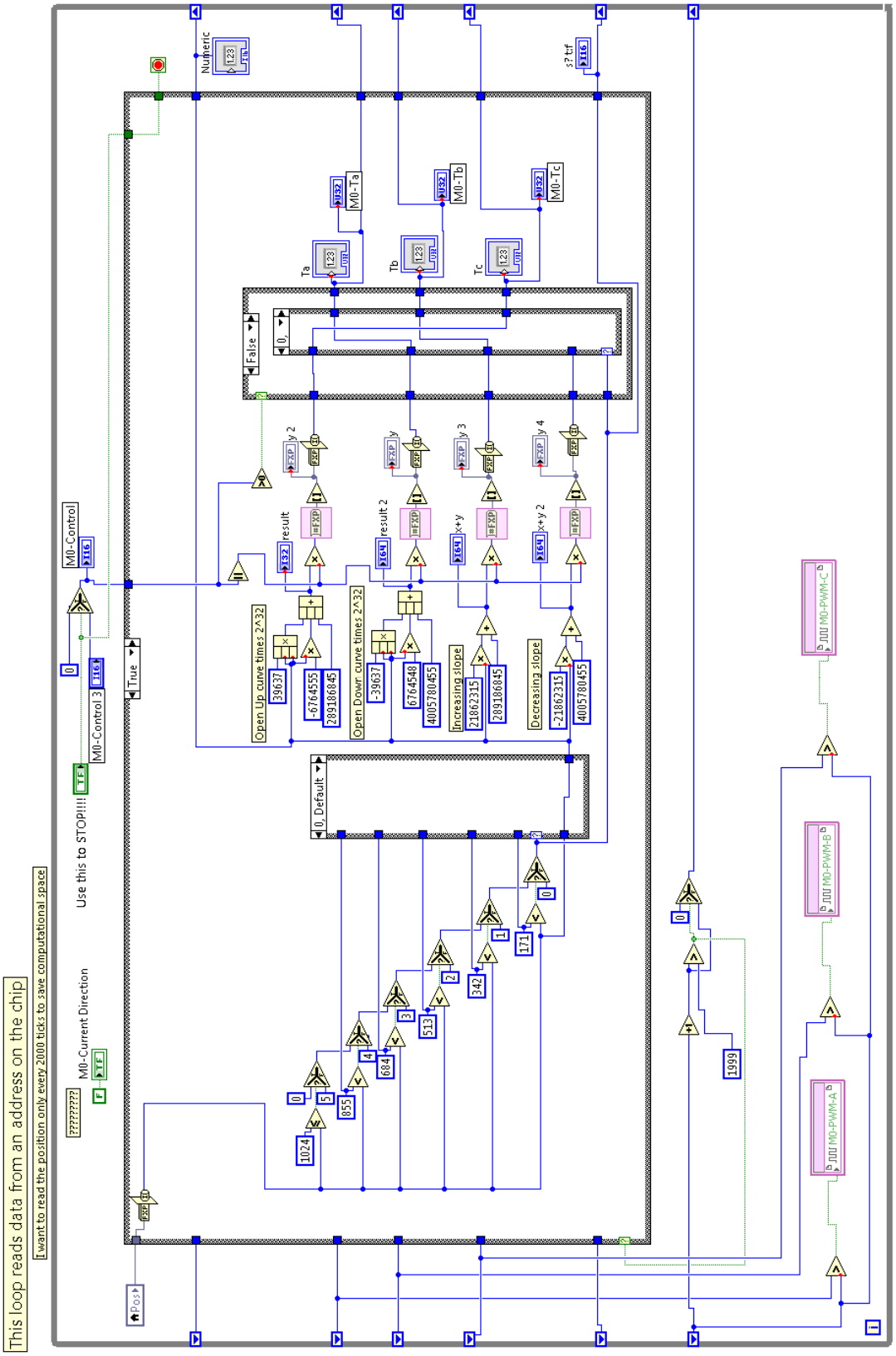


Figure D 8: True condition phase 1 counter-clockwise SVM operation.

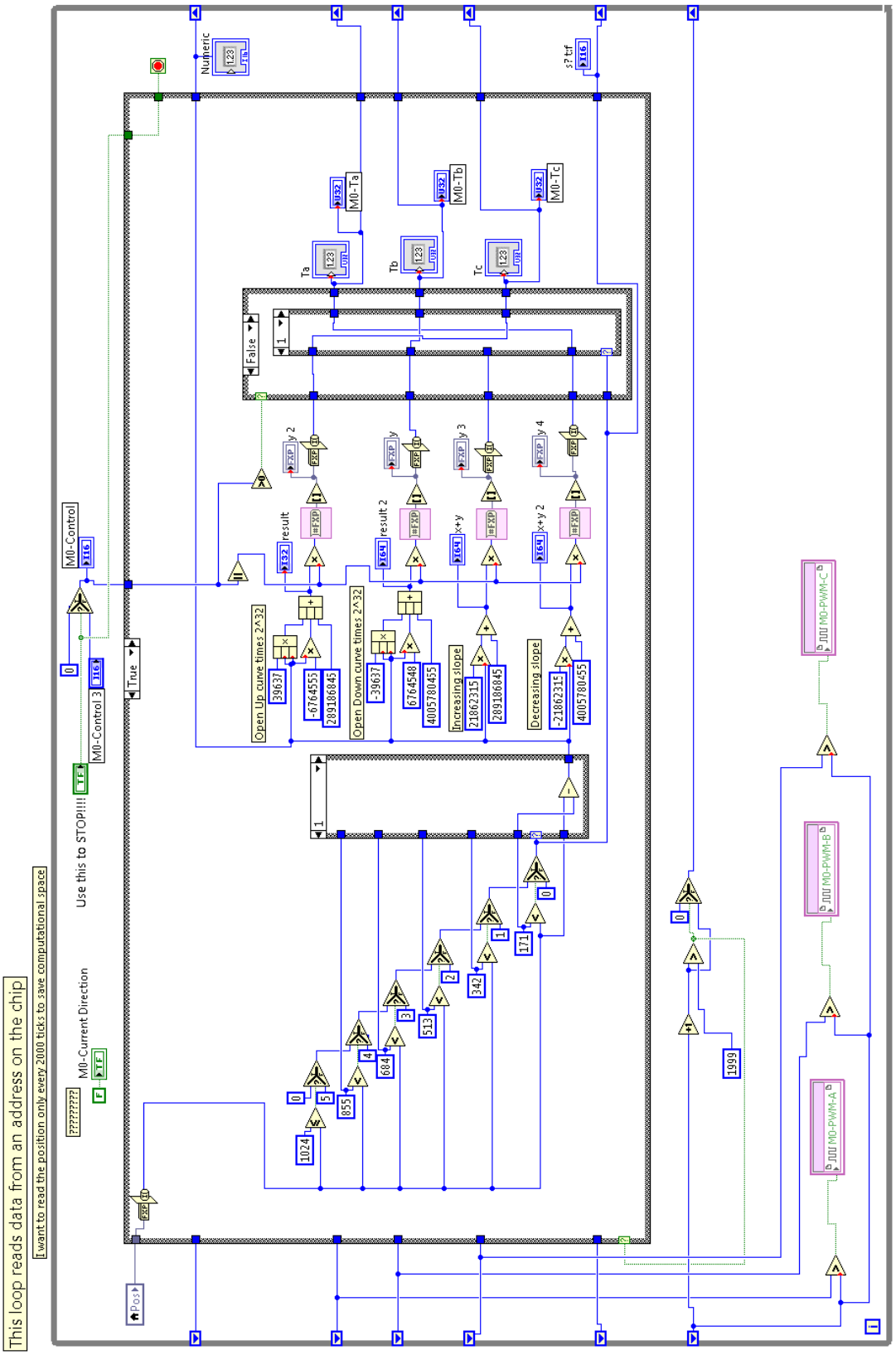


Figure D 9: True condition phase 2 counter-clockwise SVM operation.

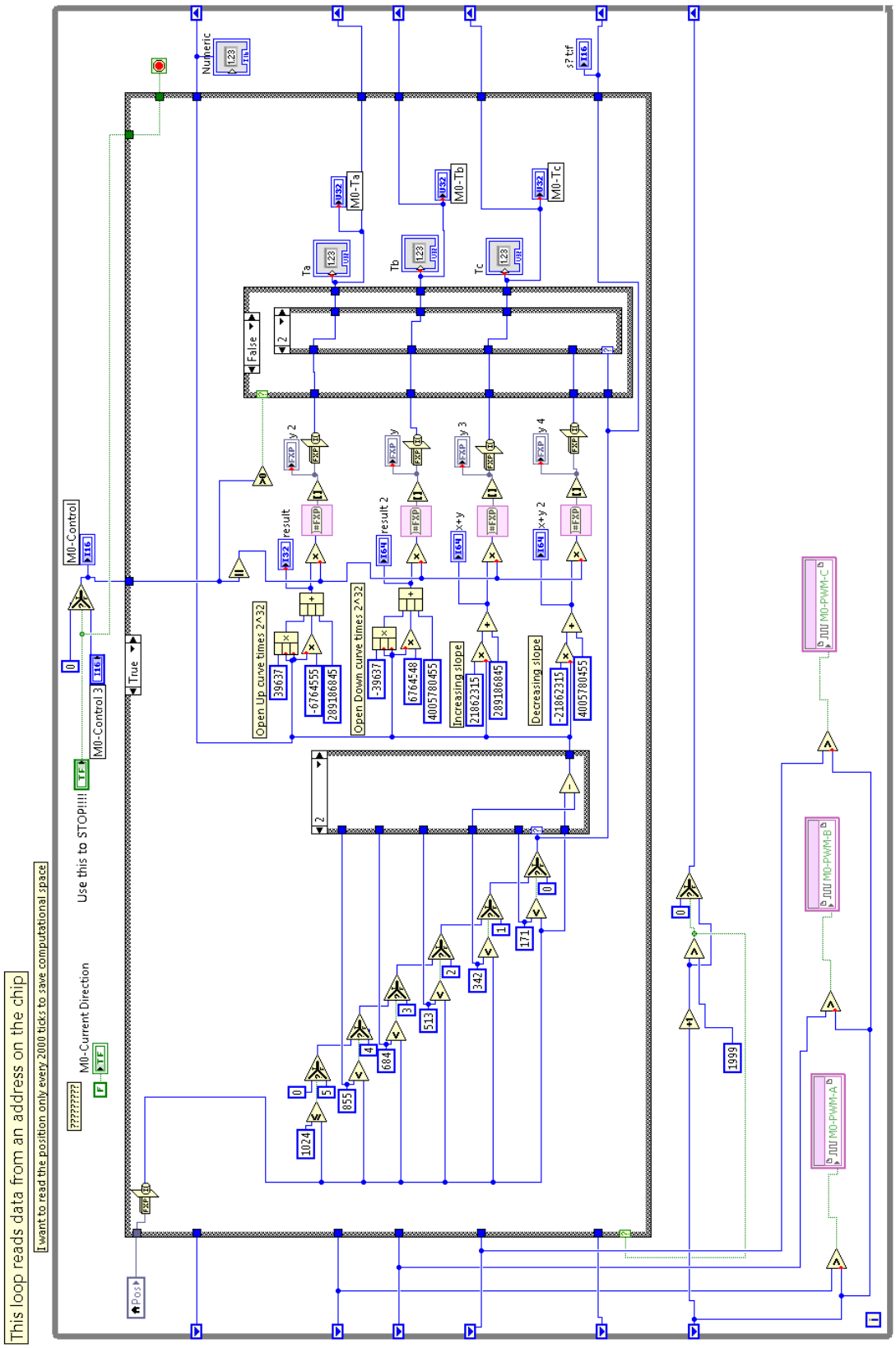


Figure D 10: True condition phase 3counter-clockwise SVM operation.

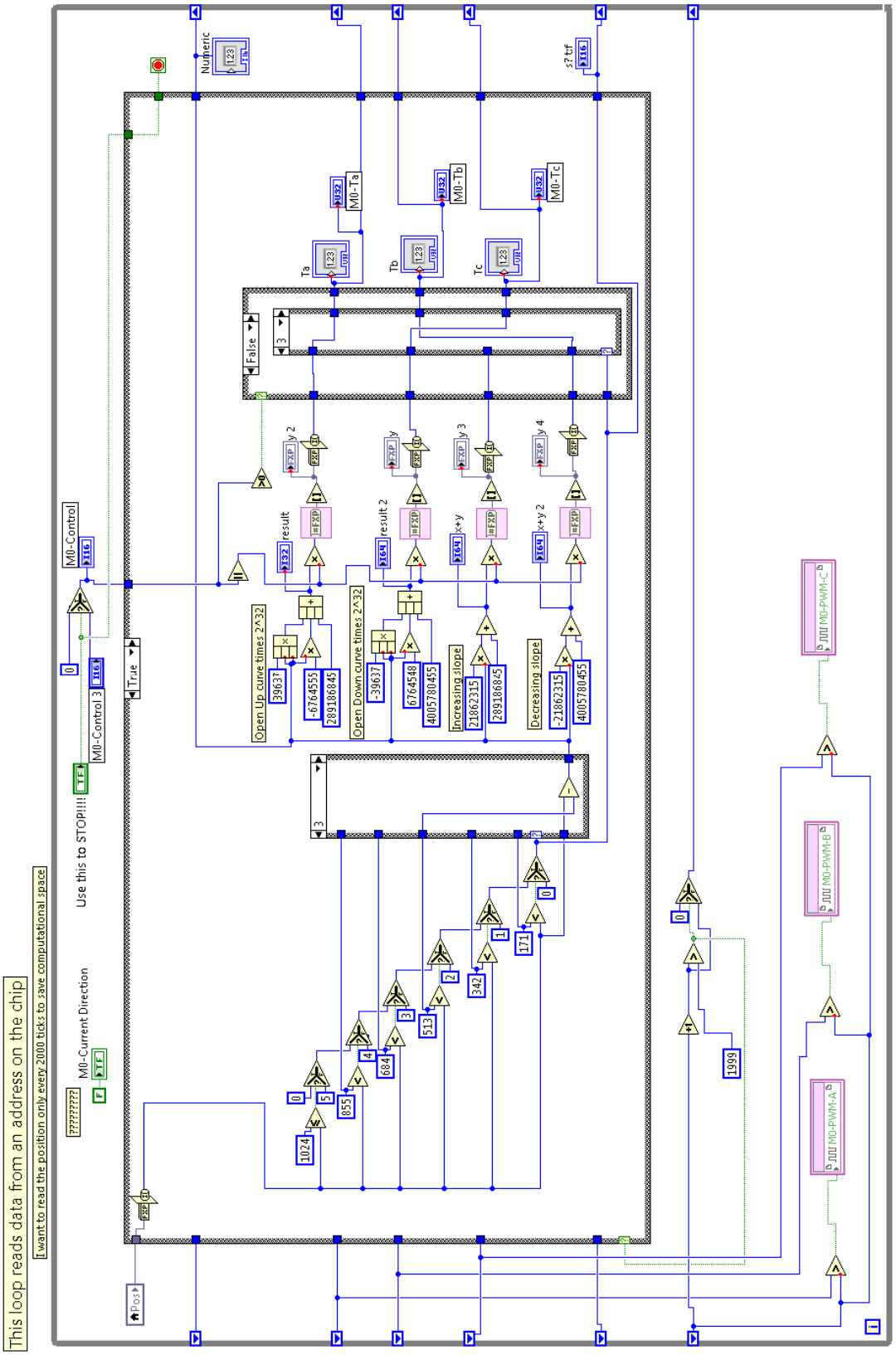


Figure D 11: True condition phase 4 counter-clockwise SVM operation.

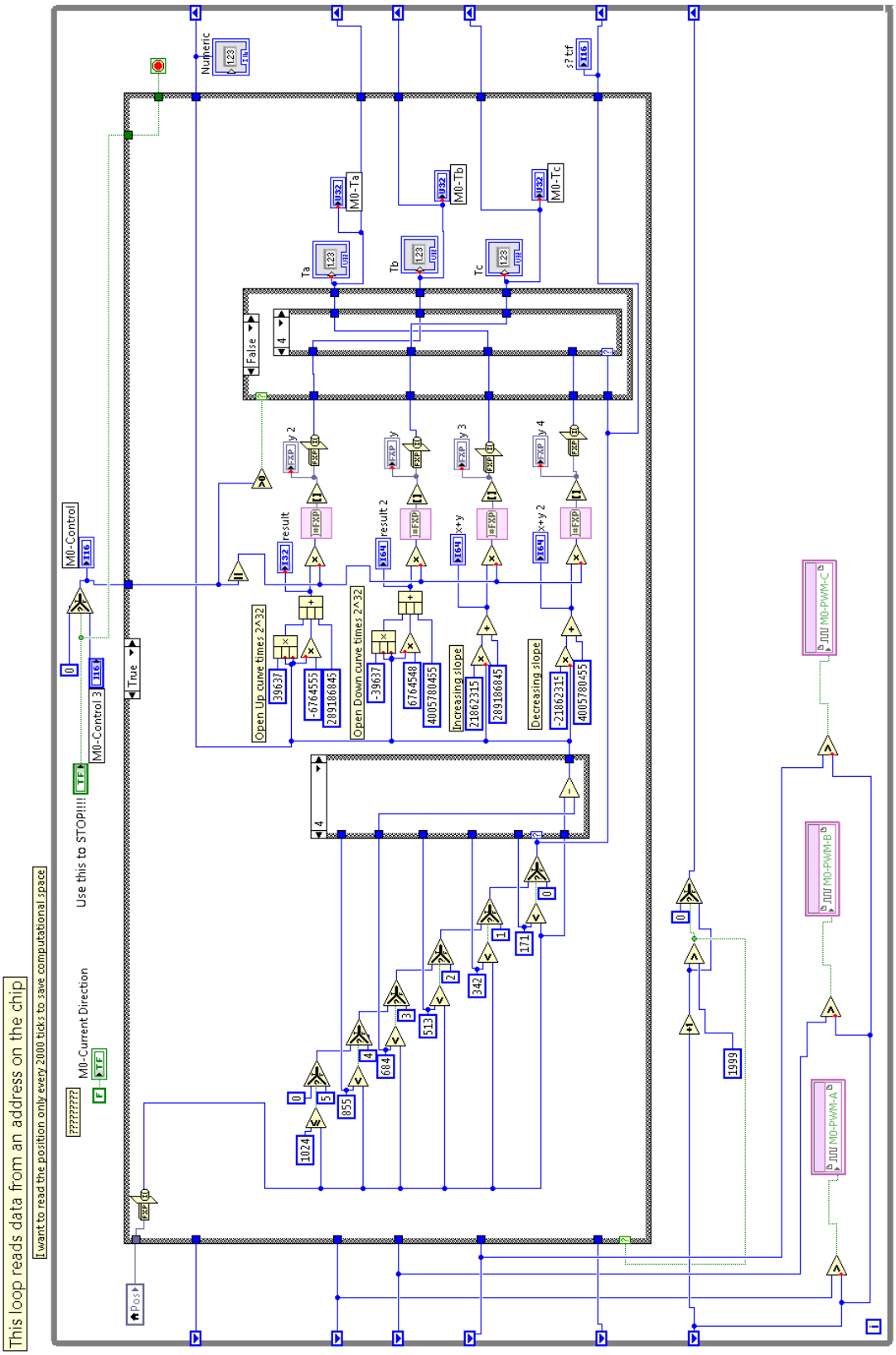


Figure D 12: True condition phase 5 counter-clockwise SVM operation.

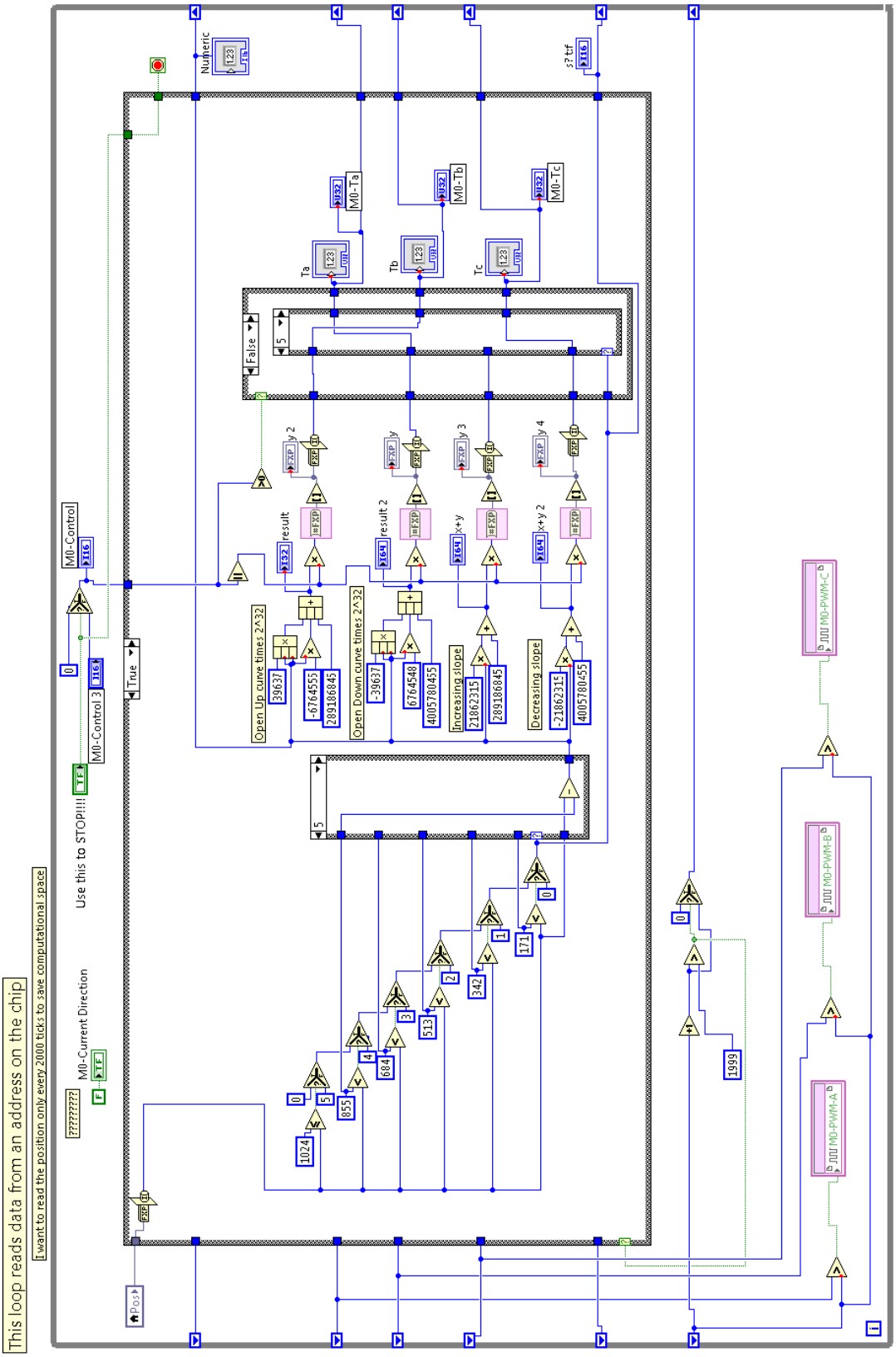


Figure D 13: True condition phase 6 counter-clockwise SVM operation.

APPENDIX E: RESOLVER READ LABVIEW PROGRAM

Figure E 1 to Figure E 20 represents the LabVIEW programing necessary to acquire the resolver position and velocity signals. These Figures are paired such that each LabVIEW block diagram can be correlated to the digital signal input/outputs received/supplied by the chip in order to communicate the appropriate data. Each Figure pair is preceded by a description of the primary functionality of the presented blocks (formatting was single spaced in order to fit the description, LabVIEW block diagram, and resolver sequences onto one page.

Step 1 (Figure E 1 and Figure E 2) baselines Sample, WR, and SCLK high and A1 low and waits until “Start 2” is pressed before proceeding.

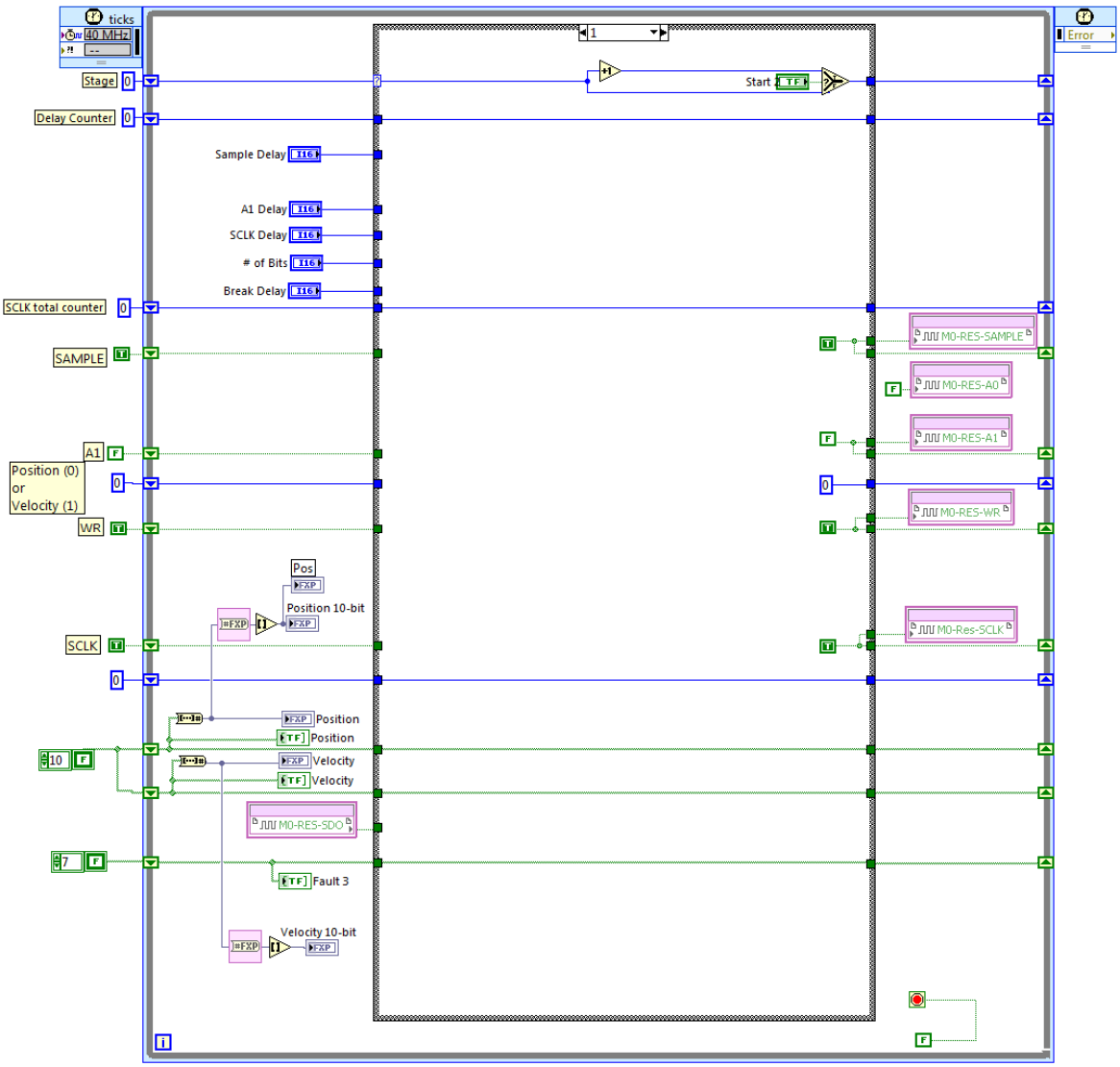


Figure E 1: Step 1

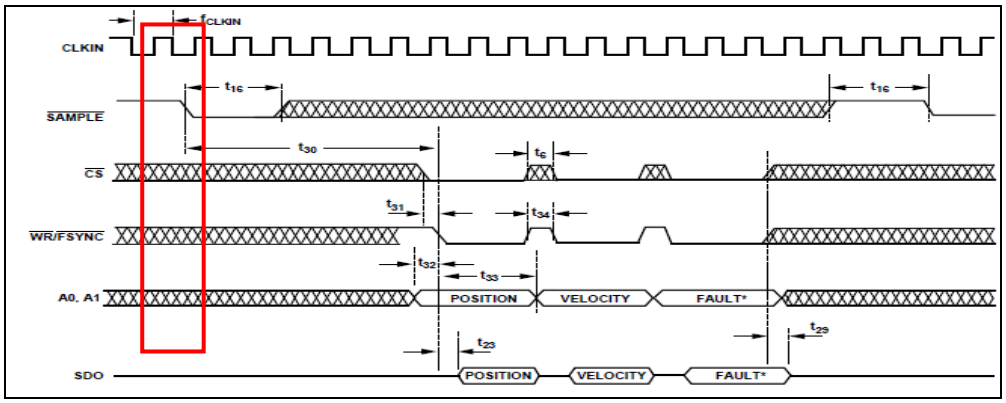


Figure E 2: Portion of serial interface read timing corresponding to step 1(Figure E 1).

Step 2 (Figure E 3 and Figure E 4) sets sample high once it has proceeded past the specified sample delay (a minimum of 16 ticks as specified in Figure E 4) .

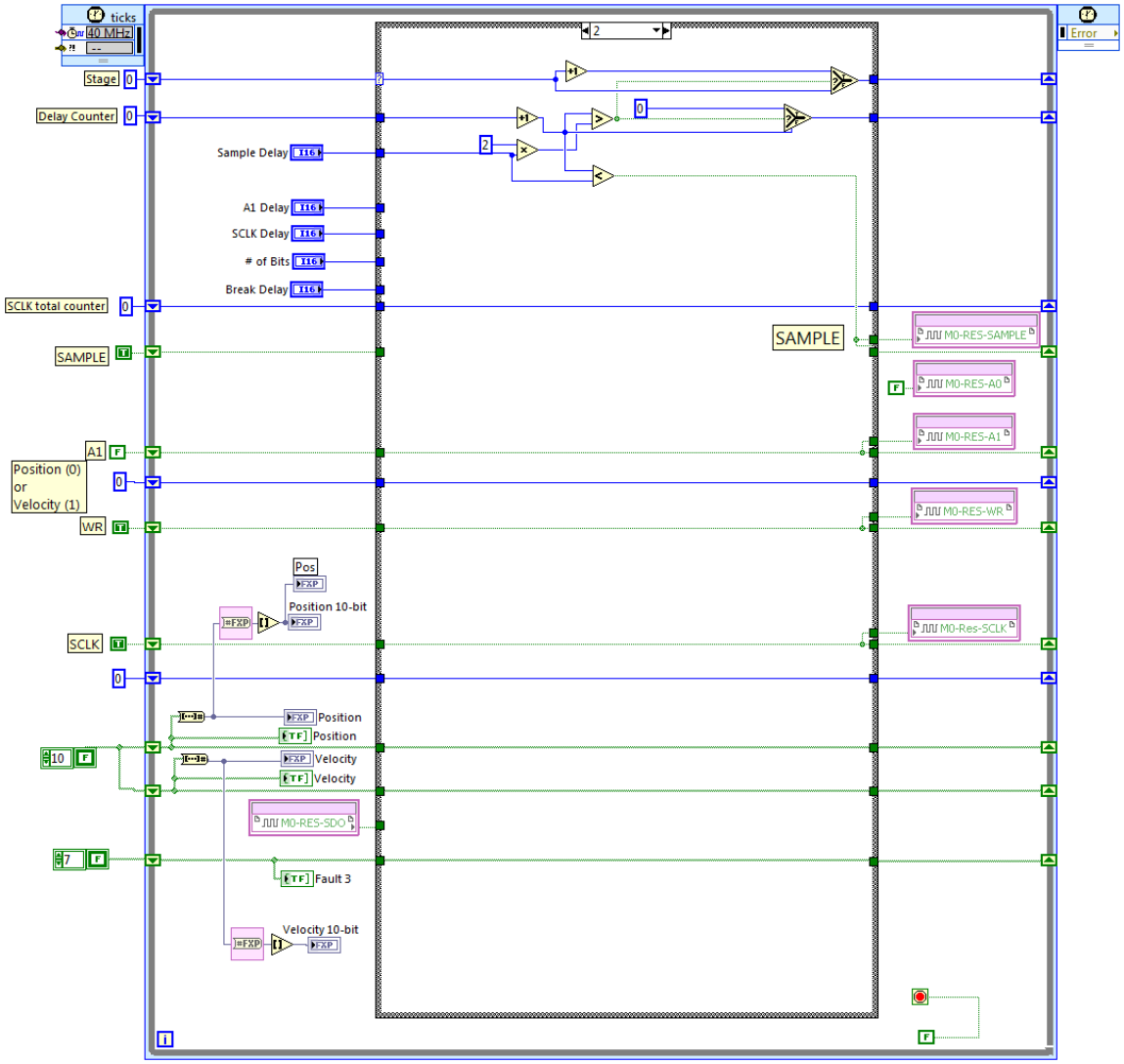


Figure E 3: Step 2.

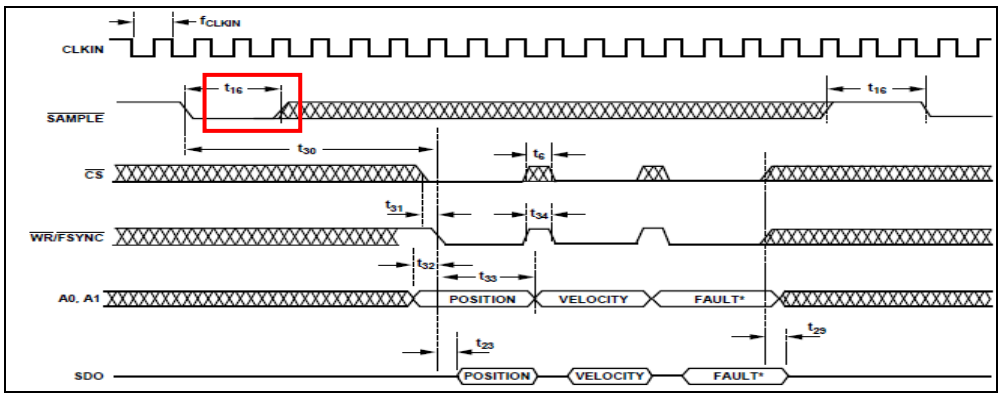


Figure E 4: Portion of serial interface read timing corresponding to step 2 (Figure E 3).

Step 3 (Figure E 5 and Figure E 6) sets A1 to either 0 or 1 depending if the blue wire carrying the variable for A1 has been altered from its initial value of 0 to 1 which will occur in step 4. A1=0 corresponds to position output and A1=1 corresponds to velocity output.

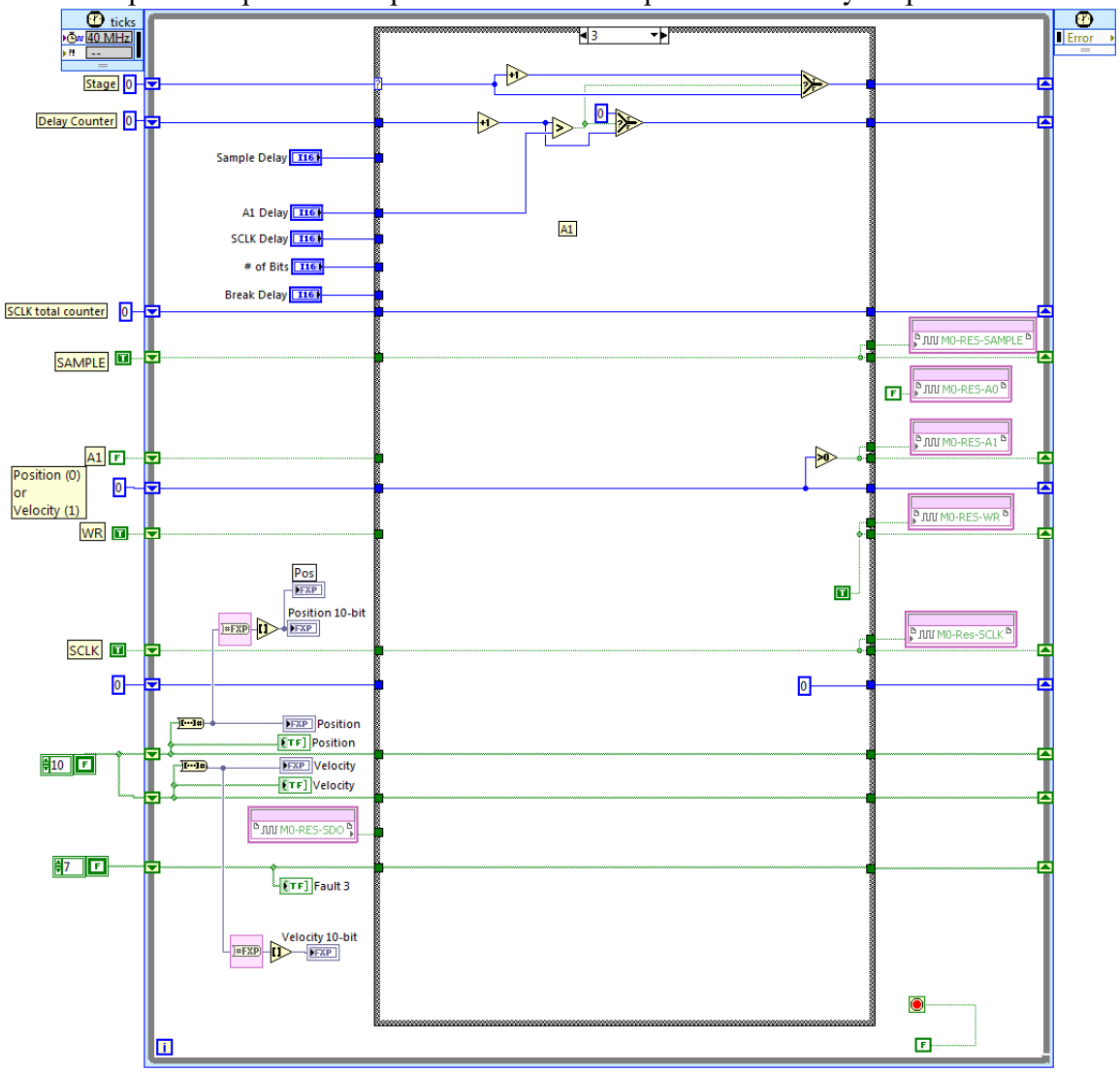


Figure E 5: Step 3.

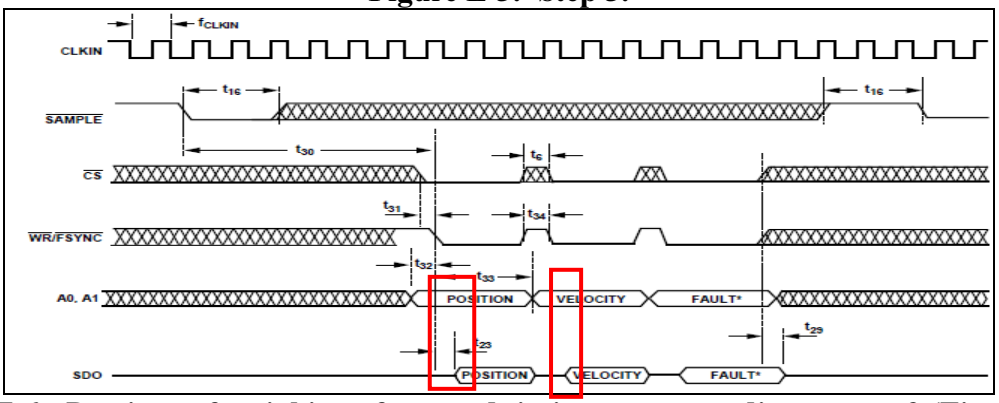


Figure E 6: Portions of serial interface read timing corresponding to step 3 (Figure E 5).

Step 4 (Figure E 7 and Figure E 8) sets SCLK low and WR to be low while the number of bits desired by user plus the 8 bits associated with the fault signal which is tacked onto the end of the position and velocity signals. WR goes high in between these output signals which indicates to the resolver-to-digital converter to change states. The duration of this stage is dictated by SCLK delay in order to ensure that the chip dynamics settled out prior to switching to the next stage. Once the fault signal is fully read the SCLK total counter exceeds its limit and the variable controlling A1 is adjusted to 1 and the process is repeated for velocity. Once velocity and its fault signal are read the system jumps to step 6.

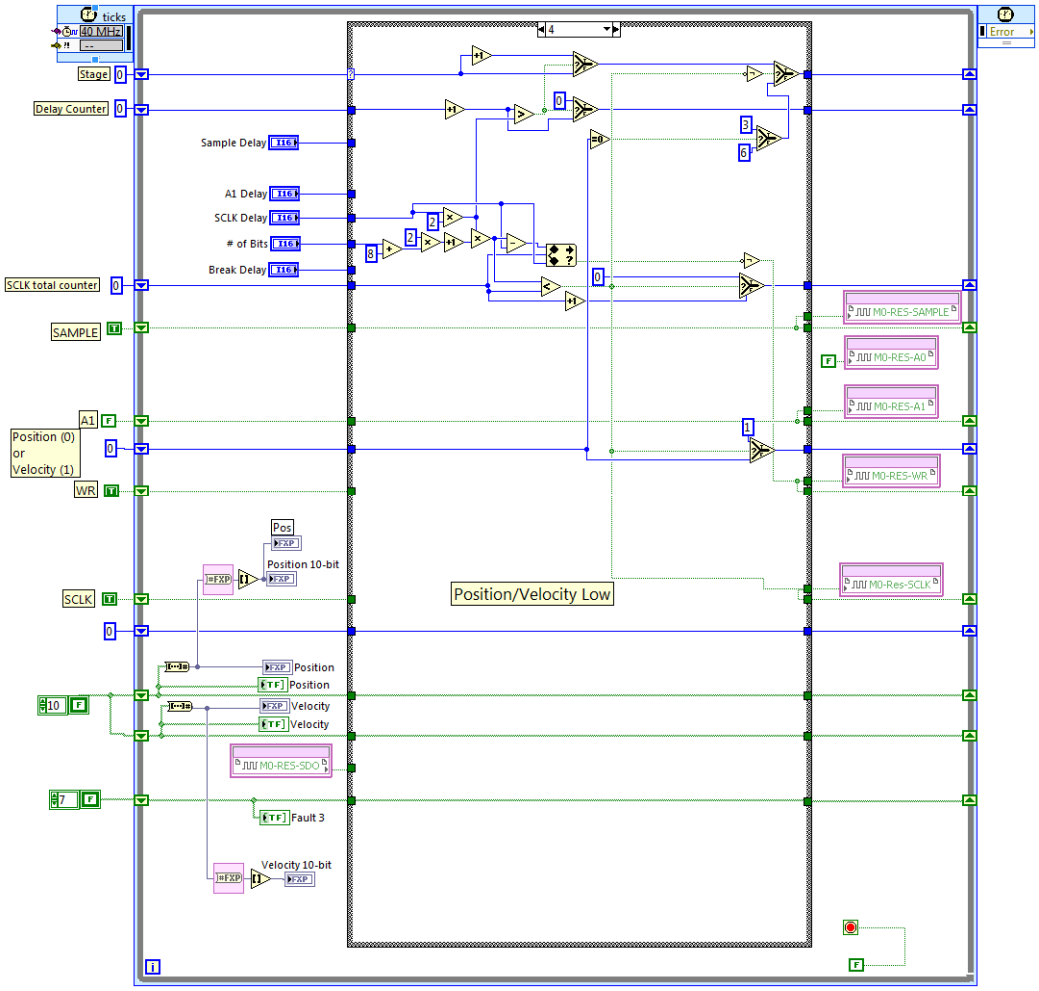


Figure E 7: Step 4.

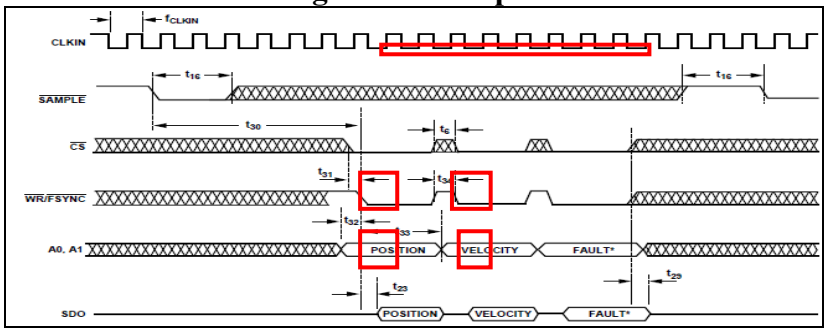


Figure E 8: Portion of serial interface read timing corresponding to step 4 (Figure E 7).

Step 5 (Figure E 9 and Figure E 10) when A1=0 and the number of iterations is less than 16 reads SDO output from the resolver-to-digital converter for each of the binary numbers associated with the 16 bit signal desired/defined by the user and reads it into the position matrix. This binary position value is converted to a number from the 16 bit signal and truncated to a 10 bit signal and then read again in order to determine how significant the number of bits was with respect to this application (had little difference). The duration of this stage is dictated by SCLK delay to ensure that the chip dynamics settle out prior to switching to step 4.

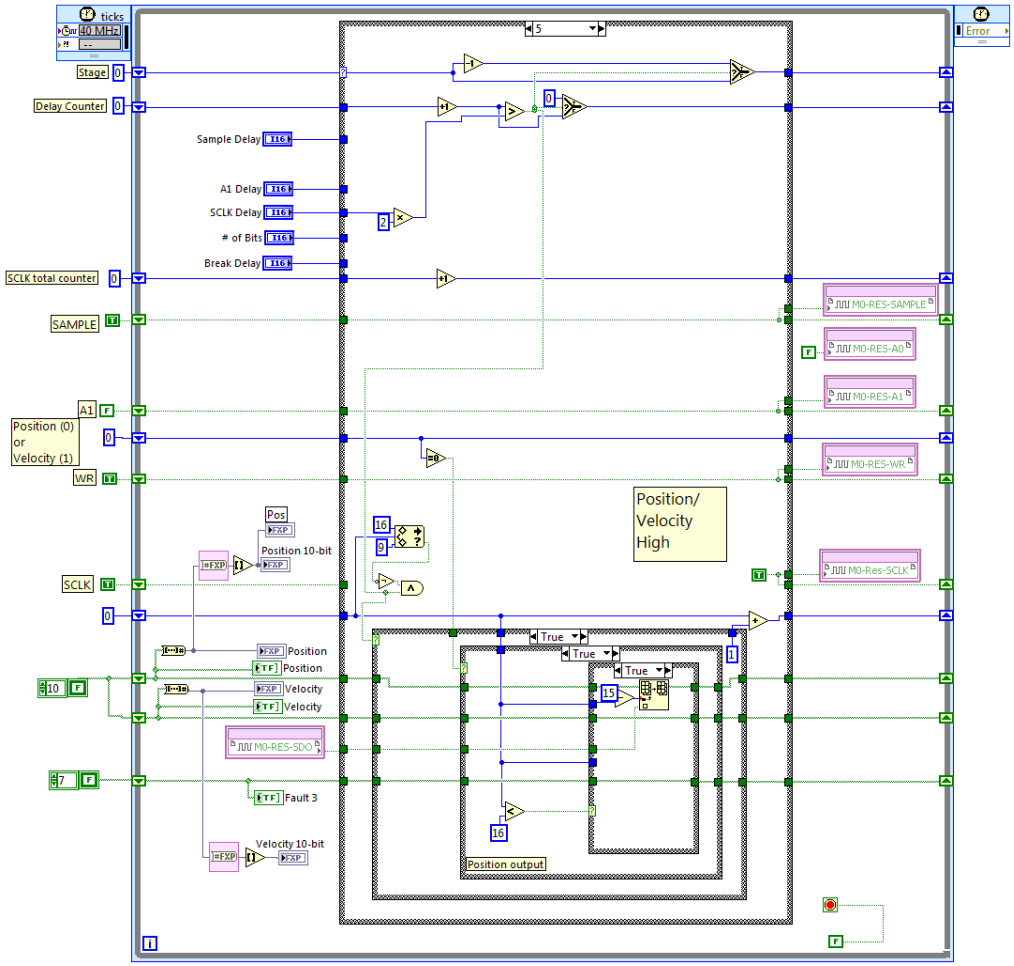


Figure E 9: Step 5 when A1=0 and the number of iterations is less than 16 reads.

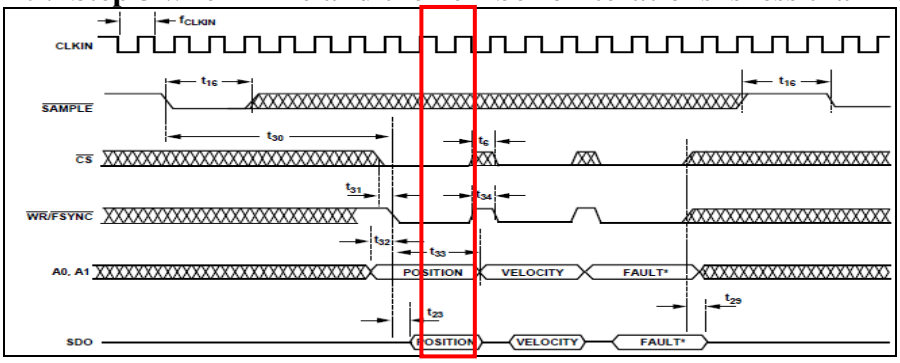


Figure E 10: Portion of serial interface read timing corresponding to step 5 (Figure E 9).

Step 5 (Figure E 11 and Figure E 12) when A1=0 and the number of iterations is between 16 and 24 reads SDO output from the resolver-to-digital converter for each of the binary numbers associated with the 8 bit binary signal corresponding to any fault condition and puts it into a matrix. The duration of this stage is dictated by SCLK delay in order to ensure that the chip dynamics settled out prior to switching back to step 4.

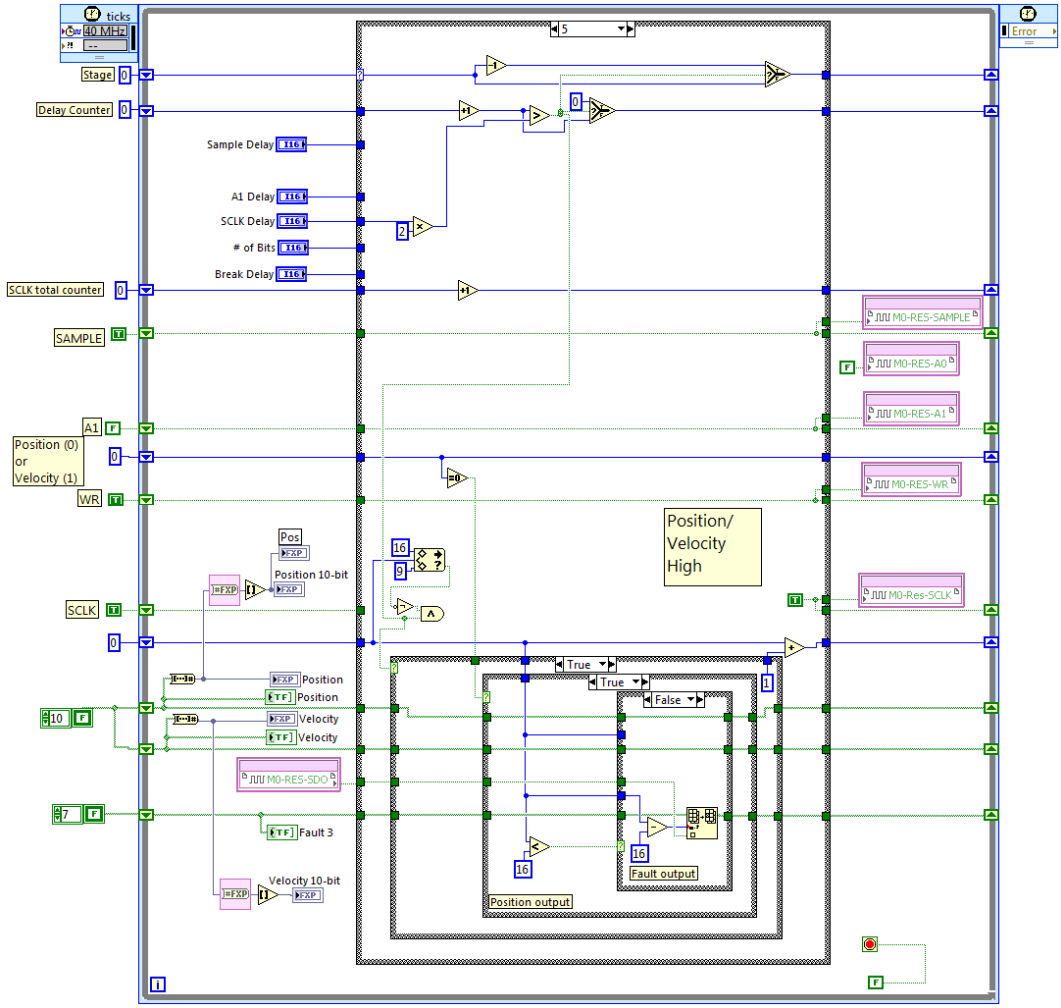


Figure E 11: Step 5 when A1=0 and the number of iterations is between 16 and 24.

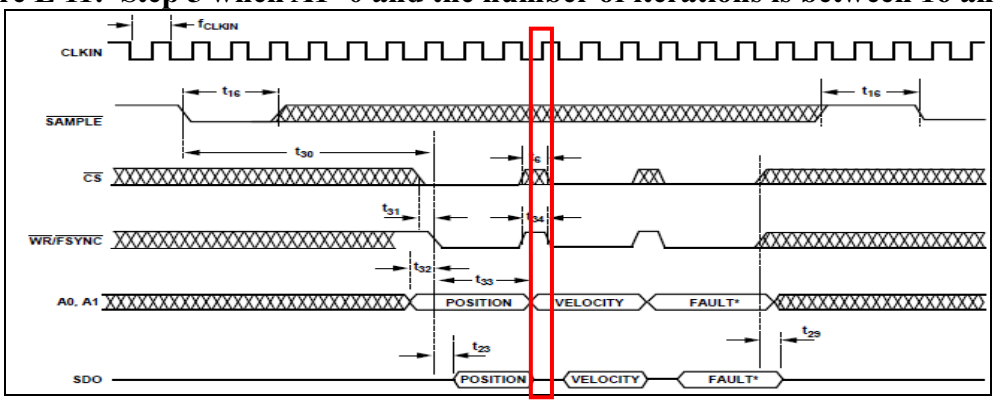


Figure E 12: Portion of serial interface read timing corresponding to step 5 (Figure E 11).

Step 5 (Figure E 13) when A1=1 and the number of iterations is less than 16 reads SDO output from the resolver-to-digital converter for each of the binary numbers associated with the 16 bit signal desired/defined by the user and reads it into the velocity matrix. This binary position value is converted to a number based on the 16 bit signal and was truncated to a 10 bit signal and then read again in order to determine how significant the number of bits was with respect to this application (had little difference). The duration of this stage is dictated by SCLK delay in order to ensure that the chip dynamics settled out prior to switching to step 4.

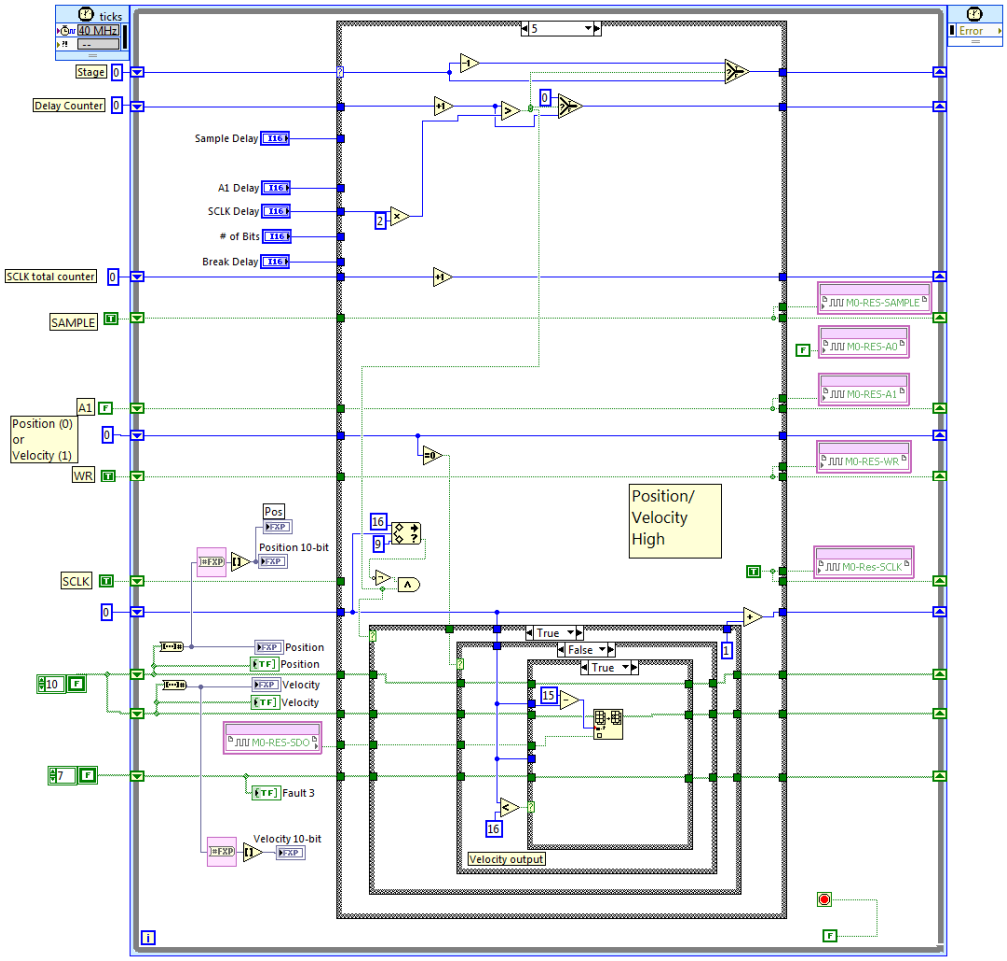


Figure E 13: Step 5 when A1=1 and the number of iterations is less than 16.

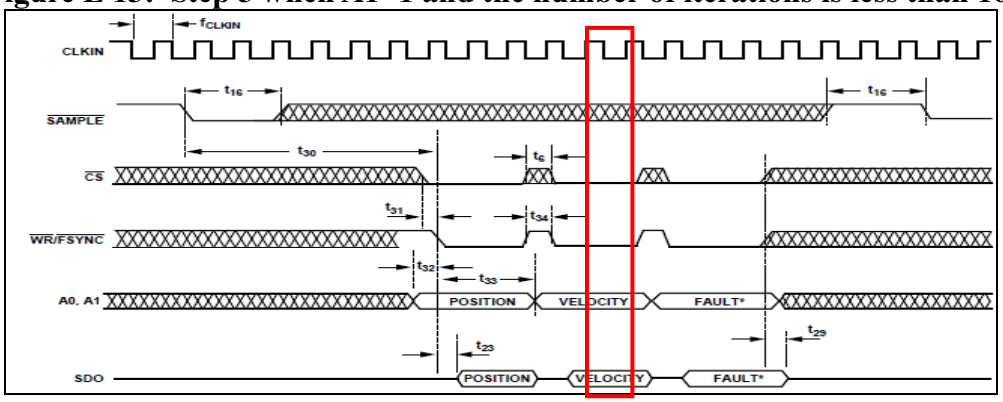


Figure E 14: Portion of serial interface read timing corresponding to step 5 (Figure E13).

Step 5 (Figure E 15) when A1=1 and the number of iterations is between 16 and 24 reads SDO output from the resolver-to-digital converter for each of the binary numbers associated with the 8 bit binary signal corresponding to any fault condition and puts it into a matrix. The duration of this stage is dictated by SCLK delay in order to ensure that the chip dynamics settled out prior to switching back to step 4.

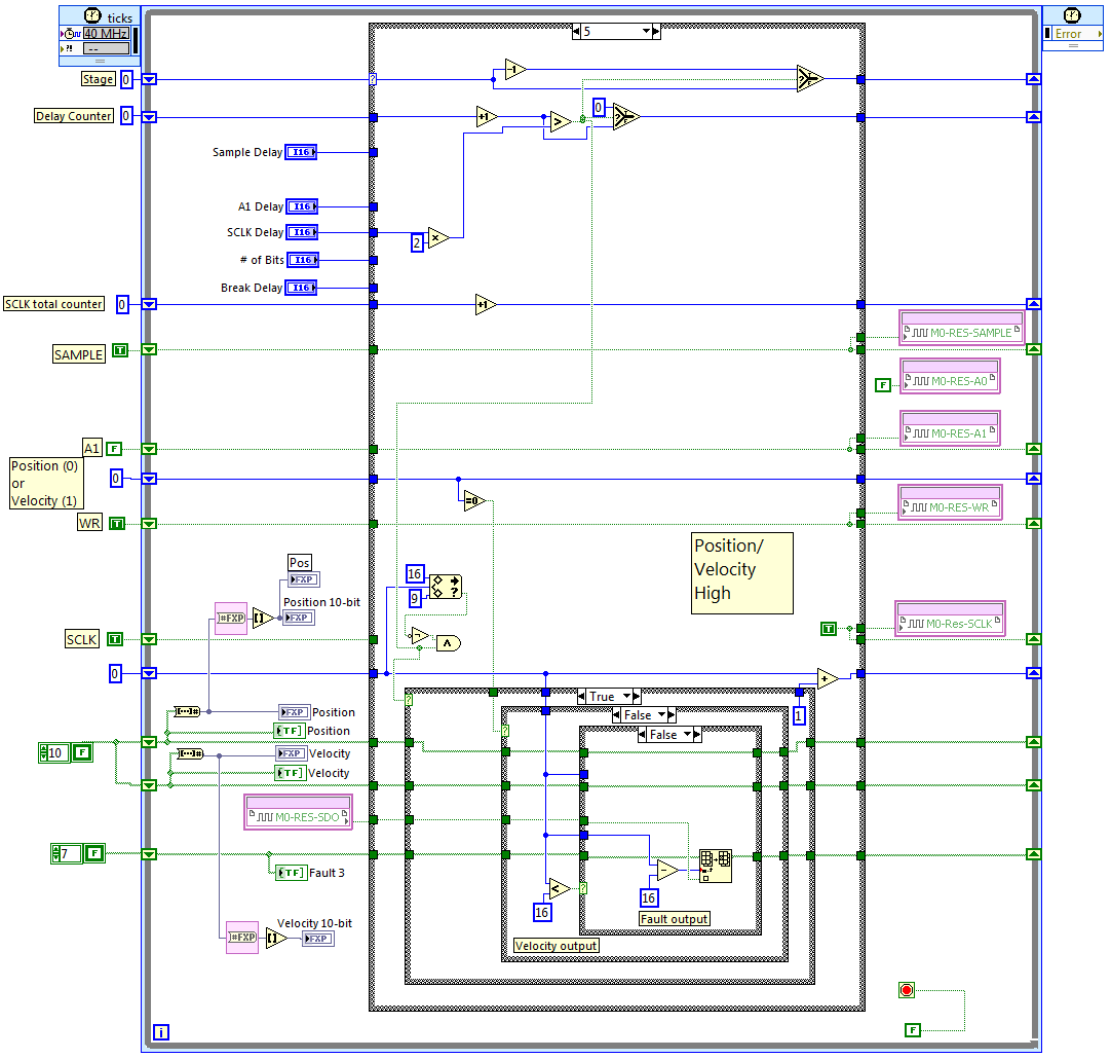


Figure E 15: Step 5 when A1=1 and the number of iterations is between 16 and 24.

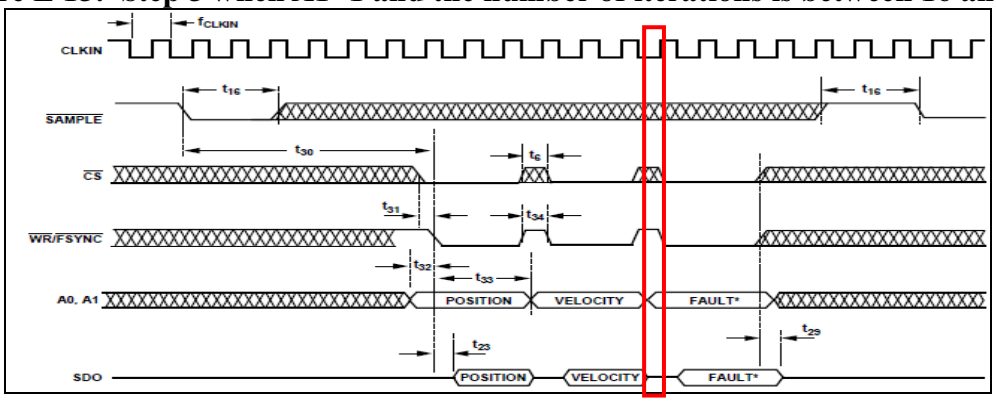


Figure E 16: Portion of serial interface read timing corresponding to step 5 (Figure E 15).

Step 5 (Figure E 17) when lower condition block is false because SCLK Delay value x 2 is greater than Delay Counter. This forces the position, velocity, and fault data to only be read at one point in time at the end of the iteration when it is known that the system dynamics have settled.

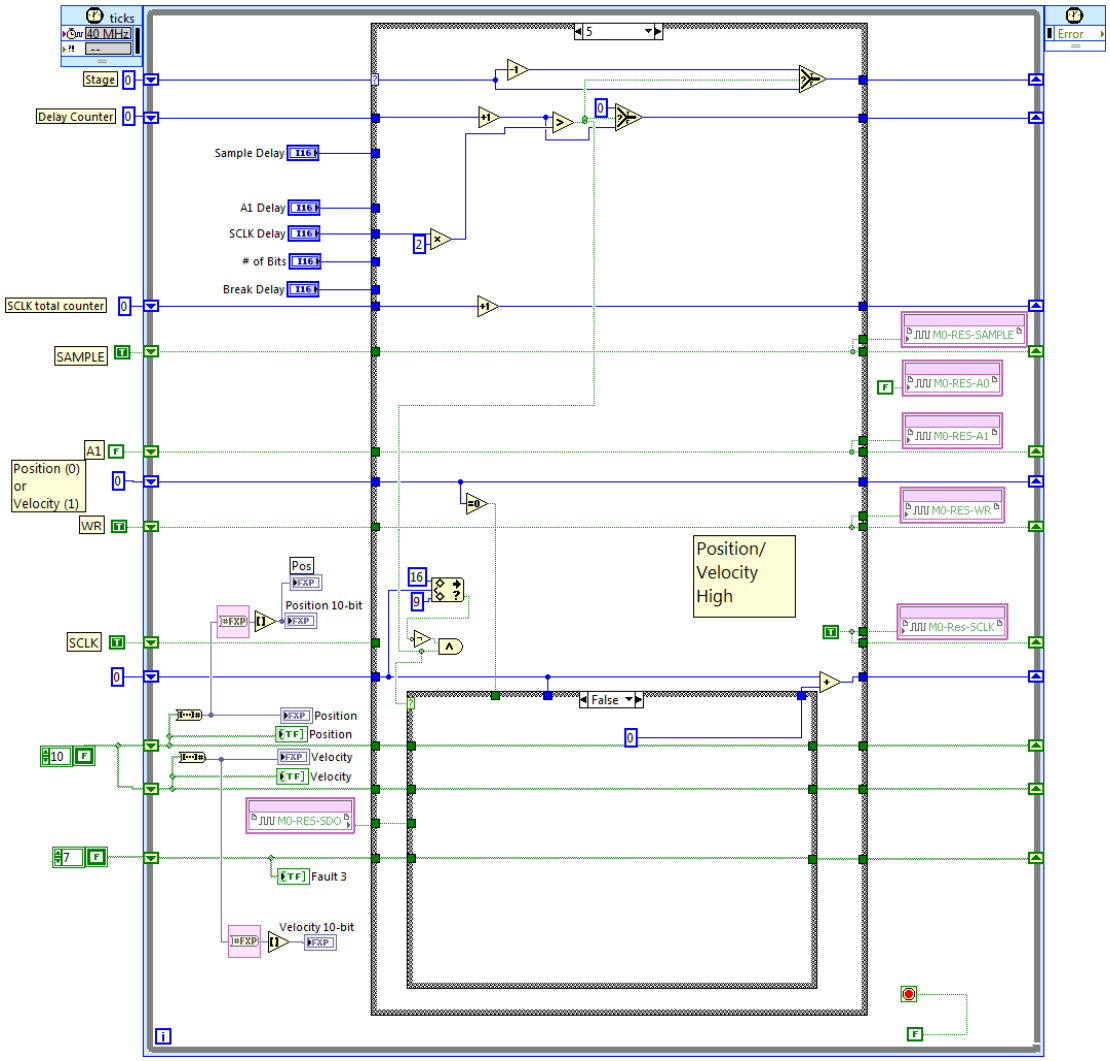


Figure E 17: Step 5 when lower condition block is false because SCLK Delay value x 2 is greater than Delay Counter.

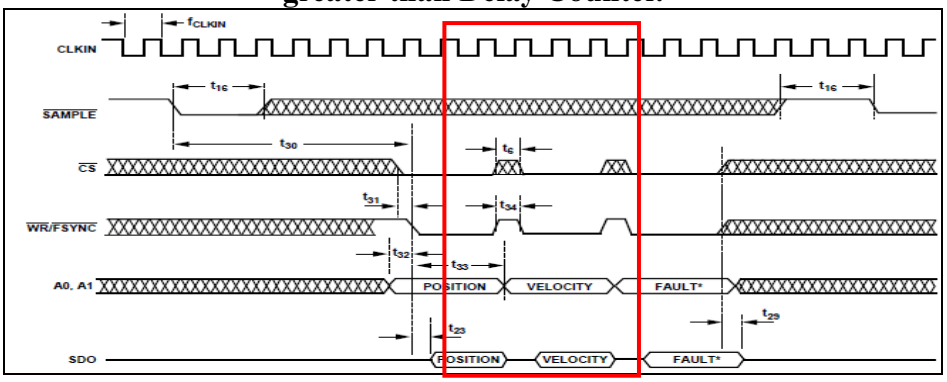


Figure E 18: Portion of serial interface read timing corresponding to step 5 (Figure E 17).

Step 6 (Figure E 19) delays the length of the defined “Break Delay” variable before repeating the process beginning with step 1 to read the data from the circuit.

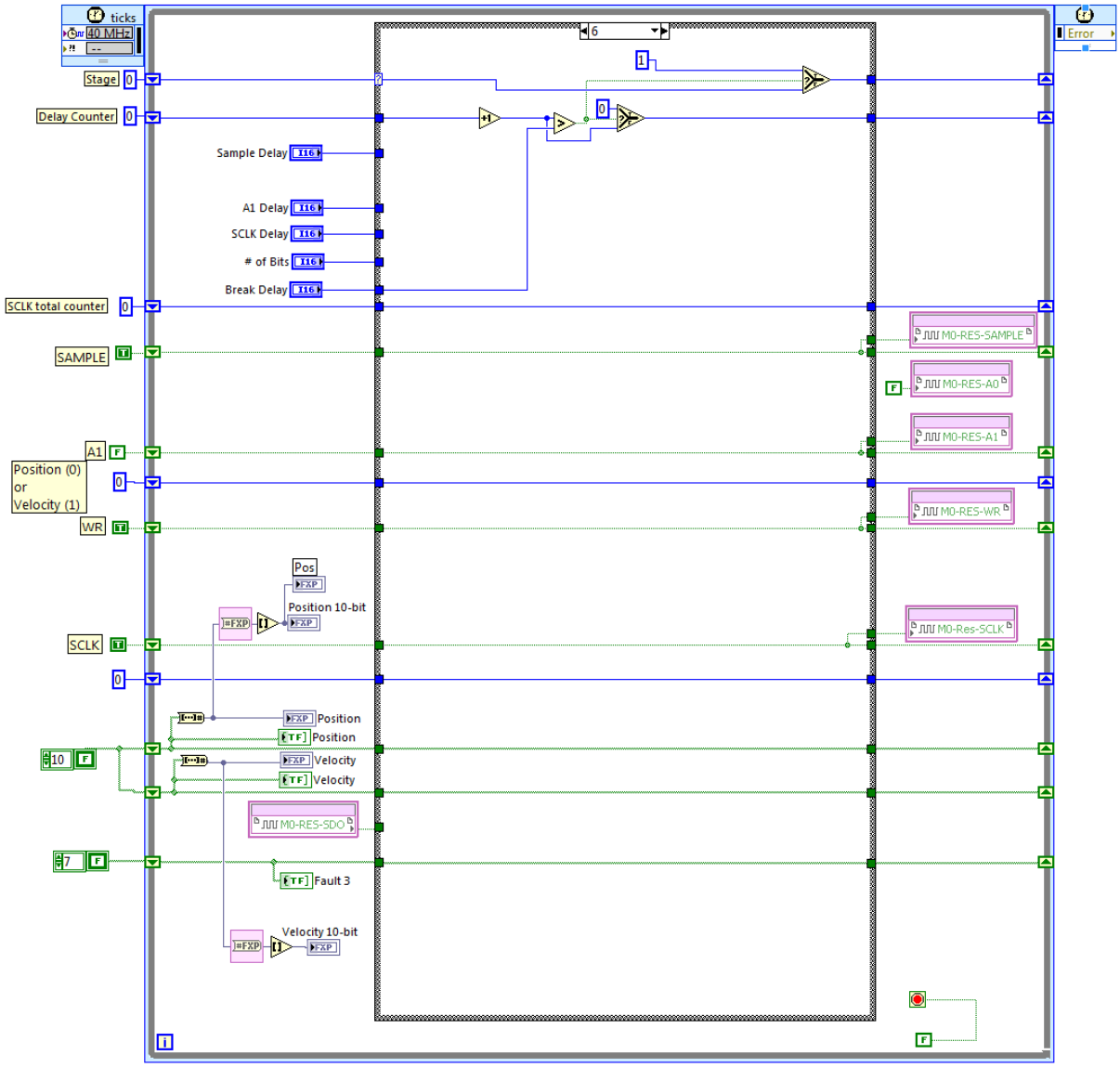


Figure E 19: Step 6 delays the length of the defined “Break Delay” variable before repeating the process beginning with step 1 to read the data from the circuit.

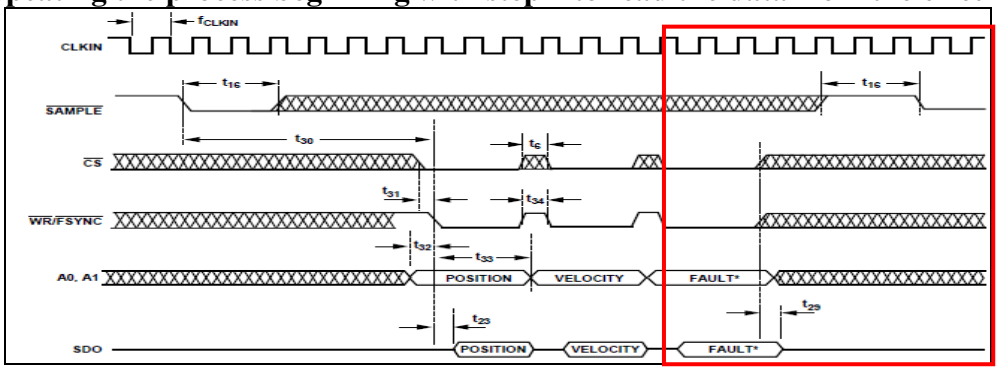


Figure E 20: Portion of serial interface read timing corresponding to step 6 (Figure E 19).

APPENDIX F: EMPLOYED BRUSHLESS MOTOR DRIVER (SA306) DATA SHEET

APEX PRECISION POWER Product Innovation From CIRRUS LOGIC

APEX – AN46

3-Phase Switching Amplifier - SA306-IHZ

INTRODUCTION

The SA306-IHZ is a fully-integrated switching amplifier designed primarily to drive three-phase brushless DC (BLDC) motors. Three independent half bridges, each comprising a P-FET and a N-FET in a configuration, provide more than 15 A of PEAK output current under digital control. Thermal and short circuit monitoring is provided, which generates fault signals for the microcontroller to take appropriate action. A block diagram of this IC is provided in Figure 1.

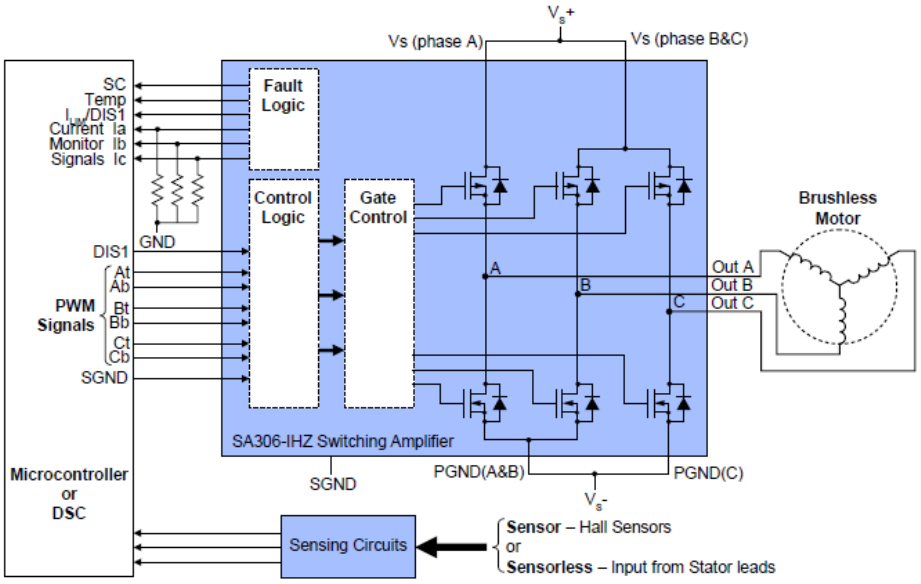


Figure 1. Polarity is Easily Switched – DC-to-DC converter, three terminal module can be switched from a positive to a negative converter by simply interchanging the jumpers identified by Note 2.

DRIVING BRUSHLESS MOTORS

Brushless motors of the same horsepower as their brush counterparts are smaller and lighter. What is absent in the former is the familiar brush–commutator arrangement that has been at the heart of single-phase DC brush motors for more than a century. Because they lack this brush-commutator interface, brushless motors exhibit lower acoustic noise; are virtually maintenance free; and a brushless motor will exhibit a longer life cycle. As recently as 2004, brushless motors were considered to be significantly more expensive than brush motors. At the time of this writing in 2008, brushless motors have benefited from a decrease in cost so that today the price differential is as little as a 10% when shopped against an equivalent brush motor.

CYCLE-BY-CYCLE CURRENT LIMIT – THE BENEFITS

Traditionally, in applications where the current flow to a brushless motor is not otherwise directly controlled, the inrush current had to be considered when selecting a proper driver amplifier. This is in addition to the average current that will flow. As an example, a 1 A continuous motor might require a drive that can deliver well over 10 A PEAK in order to deliver the initial inrush current that flows during startup. Many discrete motor drives use over-sized FETs to withstand startup conditions which results in higher system costs and larger package sizes.

However with the unique and robust cycle-by-cycle current limit scheme designed into the SA306-IHZ, the inrush current requirements of the motor are no longer an issue when selecting the drive. Current limit schemes inherently reduce acceleration of the motor; however, the average current delivered by the SA306-IHZ during start up is higher

than would be delivered by other current limit schemes. By using the SA306-IHZ, the motor will reach its operating RPM faster. Thus the SA306-IHZ is able to safely and easily drive virtually any brushless motor which requires 5 A continuously or less, through its startup interval — without regard to what its in-rush requirements are. (Up to 8 A continuously in the case of the SA306A-FHZ).

SA306-IHZ APPLICATIONS

The SA306-IHZ is designed primarily to drive three-phase motors. However, it can be used for any application requiring three high current outputs. The signal set of the SA306-IHZ is designed specifically to interface with a DSP or microcontroller. A typical system block diagram is shown in Figure 1. As explained below, over-temperature, short-circuit and current limit fault signals provide important feedback to the system controller that can safely disable the output drivers in the presence of a fault condition. High-side current sensors monitor the output current of all three phases, providing performance information that can be used to regulate or limit torque.

A SYSTEM OVERVIEW OF THE SA306-IHZ

With the introduction of the SA306-IHZ, designers now have an off-the-shelf solution for driving BLDC motors versus developing driver circuits by configuring three discrete gate drivers and six FETs. The performance specifications for the SA306-IHZ are unusual in that it can deliver over 15 A PEAK with up to 60 V applied to its FETs[1].

Imparting Rotation – Three independent DMOS FET half bridges pro¬vide the output current. In operation, as the motor rotor revolves, the controller causes one motor terminal to be driven HIGH, a second LOW and the third to FLOAT in a high impedance state, as depicted in Figure 2. This causes the magnetic field to rotate in six steps per electrical revolution in the simplest case, imparting rotation to the permanent magnets in the rotor. Proper synchronization of this sequence is assured by the feedback from either Hall sensors or a sensorless control system that keeps the microcontroller continuously informed of the position of the rotor with regard to the stator windings.

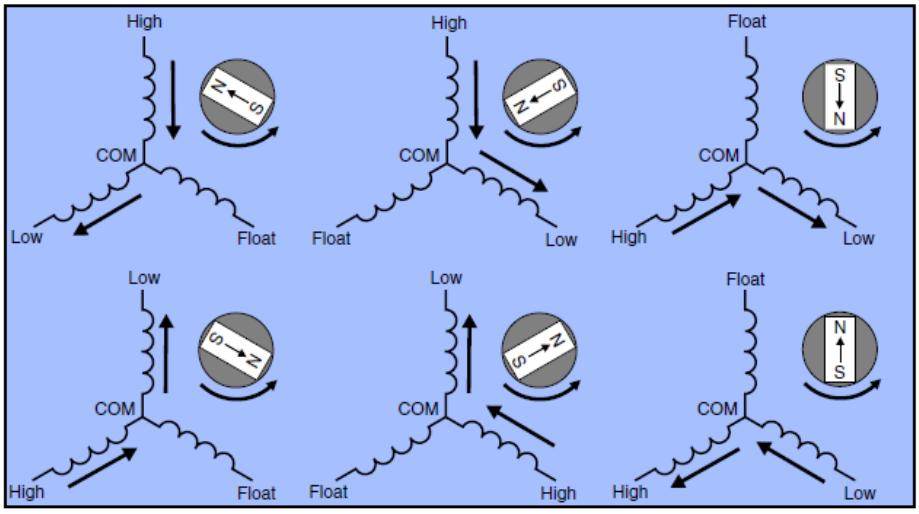


Figure 2. Imparting Rotation – By monitoring the Hall sensors – or by monitoring Back EMF in a sensorless configuration – the stator winding fields can be made to rotate so that the resultant field of the two energized stator windings and the pole of the permanent magnet rotor remain at right angles, thereby maximizing the instantaneous torque.

Shoot-Through Protection – The shoot-through protection feature of this IC identifies the state in which both the upper and lower portions of a half bridge are ON at the same time. Shoot through must be avoided, for if it were to occur, it would short the supply to ground, overload the circuit and destroy the FETs. Consequently, a 'dead time' is programmed to allow a FET to turn fully off before its companion FET is turned on. During dead time, inductive winding currents continue to flow, or commutate, through internal or external reverse biased diodes. Fault status

indication and current level monitors are provided directly to the controller. Output currents are measured using an innovative low-loss technique discussed in a later section. The SA306-IHZ also offers superior thermal performance with a flexible footprint.

Controlling Brushless Motor Drivers – Most brushless motor drivers are controlled by microcontrollers or some other intelligent system. A number of manufacturers including Analog Devices, Freescale, Microchip and Texas Instruments market microcontrollers for motion control – and more specifically for driving brushless motors.

Choosing a Brushless Motor – Although there are a number of sources for assistance in choosing a motor, brushless or otherwise, a good starting point is Reference 2. As the author points out, choosing a motor requires looking at a whole list of issues including efficiency, torque, power reliability and cost.

What can be said categorically is that a brushless permanent magnet motor is the highest performing motor in terms of torque versus efficiency. Also all three stator windings can be controlled which is not the case in a traditional DC motor where commutation relies on brushes.

SENSOR VERSUS SENSORLESS COMMUTATION

Hall Sensors are not required in sensorless commutation. Instead the instantaneous position of the rotor relative to the stator is determined by the Back EMF (BEMF) developed in the stator windings. The absence of both the Hall Sensors and the attendant wiring lowers the motor's cost and increases reliability, though deriving the lost information from the BEMF requires somewhat more complex control. This approach is attractive in applications such as refrigeration or HVAC systems which generate heat that could accelerate failures of the Hall Sensors.

On the other hand, starting presents a problem in sensorless commutation simply because there is no BEMF when the motor is at rest. Secondly, abrupt changes in the motor load can cause a BEMF drive loop to go out of synchronization. Central to both sensorless- and sensor-based control systems is the presence of pulse width modulation (PWM) which is discussed in the Appendix.

CYCLE BY CYCLE CURRENT LIMITING – THE FUNDAMENTALS

In applications where the current in the motor is not directly controlled, both the average current rating of the motor and the in-rush current must be considered when selecting a proper drive. For example, a motor that requires 1 A when running at constant speed, might require a drive that can deliver well over 10 A PEAK in order to survive the inrush condition at startup. But as this discussion will make clear, this is not the case when using the SA306-IHZ.

Depicted in Figure 3a is the behavior in a traditional motor where there is no cycle-by-cycle current limit. (This is discussed in more detail in the Appendix)

In this case, when the rotor is not turning (no BEMF), the current is limited only by the resistance of the rotor of the motor plus any series resistance that may be present. As the motor accelerates, the back EMF builds up, gradually reducing the current so that it diminishes to the steady-state current.

Figure 3 illustrates motor behavior when cycle-by-cycle current limit is applied at start-up. In this case, the current is limited by circuitry within the SA306-IHZ – not by the impedance of the rotor. As the motor reaches its steady-state speed, the current tails off.

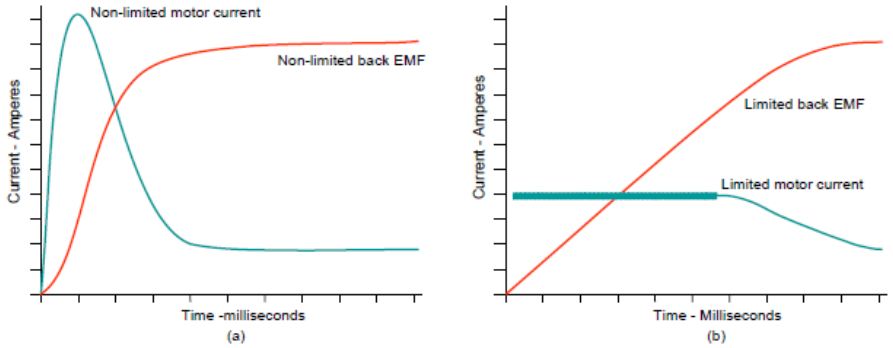


Figure 3. Motor Current Behavior at Startup – (a) Without cycle-by-cycle current limit. (b) With cycle-by-cycle current limit.

CYCLE-BY-CYCLE CURRENT LIMIT BEHAVIOR

Shown along the top of Figure 4 is the cycle-by-cycle behavior of the PWM pulse train applied to the SA306-IHZ by the microcontroller. The motor current is shown in blue at the bottom of the illustration. Outlined in red, and superimposed over the current waveform, is the actual PWM pulse train ('PWM output') delivered by the FETs which has, in effect, been modulated by the current flow. It shuts off the output pulse should the current exceed the 'current limit' set externally by the user.

1st Pulse – In the case of the 1st PWM pulse, no current limiting occurs because the pulse ends before the rising current reaches the current limit threshold. At the end of the 1st pulse there is a short decay before the PWM pulse turns on once more and the current resumes its rise. Note that because current cannot change instantaneously in an inductive reactance, which is, in fact, what the rotor of the brushless motor is, the current value, unlike the PWM voltage, is always continuous.

2nd Pulse – In the case of the second PWM pulse, the current reaches the limit value before the PWM input pulse ends. Consequently, the PWM output pulse is shut off early in its cycle. Then the motor current decays until the third pulse is applied which once again causes the current to rise.

Subsequent pulses – The behavior just described continues until the back EMF rises to the point where the current falls below the current limit threshold. This occurs as the motor approaches its operating speed and the current descends to its steady state value, as depicted in Figure 3b. The ratio of the peak-to-average motor current depends on the inductance of the motor winding, the back EMF developed in the motor, mechanical loading of the systems and the width of the pulse.

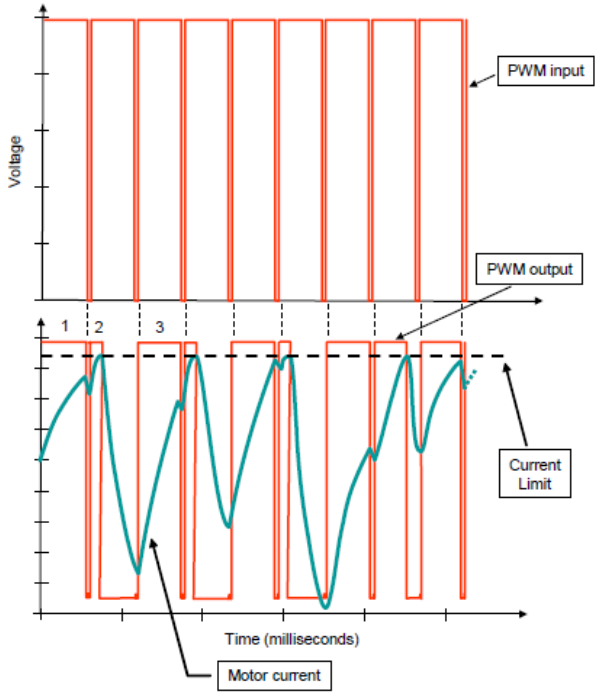


Figure 4. Cycle by Cycle Current Limit

CONTROL AND SENSE ARCHITECTURE

As depicted in Figure 5, the output current of the upper output FET U14 for OUT A is continually measured, (The same occurs for the corresponding output FETs for OUT B and OUT C). The output of the current sense circuit is applied to a current mirror comprising U1, U2 and U3 which develops a voltage across the external current limit resistor. This voltage is compared with the current limit threshold by Comparator U6.

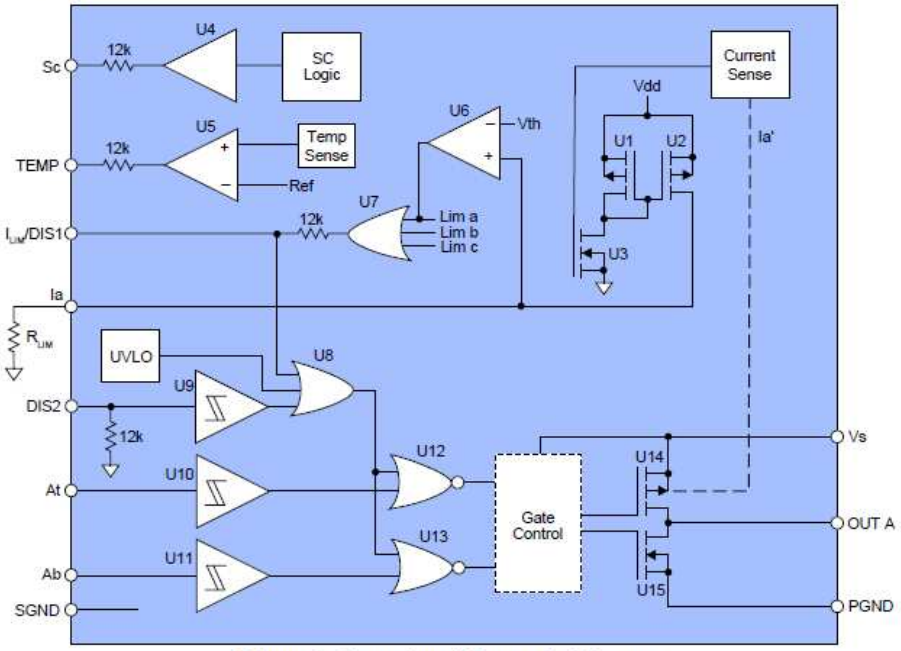


Figure 5. Control and Sense Architecture

Disabling Circuitry – If the voltage applied to the plus terminal of comparator U6 exceeds the current limit threshold voltage (Vth), all three outputs OUT A, OUT B and OUT C are disabled. The disabling path is via gates U7 and U8 and gates U12 and U13. Once the voltage applied to Comparator U6 falls below the Vth threshold voltage, and the disabled top side input to the gate control goes low, the output stage will return to an active state on the rising edge of any top side input command signal (At, Bt, or Ct). Note that the corresponding disable signals from phases B and C are also applied via gate U7 and their behavior is exactly the same as is the case for OUT A. Also the ILIM/DIS1 goes HIGH when any of the three current sense circuits detects an overcurrent situation. The cycle-by-cycle current limit feature of the SA306-IHZ will reset each PWM cycle. Thus the PEAK current is limited in each phase during each PWM cycle, as illustrated in Figure 4. Notice also that the moment at which the current sense signal exceeds the Vth threshold is asynchronous with respect to the input PWM signal because this event is governed by the inter-section of the rising current with the current limit – not the PWM duty cycle. The difference between the PWM period and the motor winding L/R time constant will often result in an audible beat frequency sometimes called a 'sub-cycle oscillation'. This oscillation can be viewed with an oscilloscope by applying a probe to pin 7, I_{LIM}/DIS1.

Undervoltage Lockout – See Table 1 and Page 7.

Limitations at High and Low Speeds – Input signals applied to the PWM and commanding a 0%- or a 100%-duty cycle, may be incompatible with the current limit feature due to the absence of rising edges of At, Bt, and Ct – except at instances when the rotation of the motor requires the output FETs to change states. At high motor speeds, this may result in poor performance and significantly increased torque ripple. Whereas at low motor speeds the motor may stall if the current limit trips and the motor current reaches zero without a commutation edge that would change the state of the output FETs and normally reset the current limit latch.

Disabling Cycle-by-Cycle Current Limit – The current limit feature may be disabled by pulling the I_{LIM}/DIS1 pin to GND. The current sense circuitry identified in Figure 5, will continue to provide top FET output current information.
External Current Control Options – Typically the current sense pins source current into grounded resistors which provide voltages to the current limit comparators, as shown in Figure 1. If instead the current limit resistors are connected to a voltage output DAC, the current limit can be controlled dynamically by the system controller. This technique essentially reduces the current limit threshold voltage to (Vth-VDAC). During expected conditions of high torque demand, such as start-up or reversal, the DAC can adjust the current limit dynamically to allow periods of high current. In normal operation when a low current is expected, the DAC output voltage can increase, reducing the current limit setting to provide more conservative fault protection. This is discussed in detail under 'Current Sense – An Advantage'.
Three Degrees of Freedom – The applied voltage, the switching frequency and the PWM duty cycle are three crucial parameters that can be programmed independently. How these variables are selected will affect the behavior of the motor with regard to how fast it will accelerate, and consequently how fast its speed and torque will rise.

CONTROL AND SENSE PINS

A summary of the control and sense pins, and their functions, is supplied in Table 1.

Table 1. Control and Sense Features

Nomenclature	Pin #	Function	Description	Remarks
DIS2	23	Control	When a HIGH is applied to this Schmitt triggered logic level, it places OUT A, OUT B, and OUT C in a high impedance state.	Pin DIS2 (23) has an internal 12kΩ pull-down resistor connected to ground and therefore may be left unconnected. (See Figure 5.)
I_{LIM}/DIS1	7	Control/Sense	Control: Pulling this pin to logic HIGH places OUT A, OUT B, and OUT C in a high impedance state. Pulling this pin to a logic LOW effectively disables the cycle-by-cycle current limit feature. Sense: This pin is also connected internally to the output of the current limit latch through a 12kΩ resistor and can be monitored to observe the function of the cycle-by-cycle current limit feature.	
SC	3	Sense	Goes HIGH if a short circuit is detected or an output occurs that is not in accordance with the input commands,	The SC signal is blanked for approximately 200 ns during switching transitions but in high current applications, short glitches may appear on the SC pin. A high state on the SC output will not automatically disable the device. The SC pin includes an internal 12kΩ series resistor, as shown in Figure 5.
TEMP	25	Sense	Goes HIGH if the SA306 die temperature reaches approximately 135ºC.	This pin WILL NOT automatically disable the device. The TEMP pin includes a 12kΩ series resistor. See Figure 5.

Nomenclature	Pin #	Function	Description	Remarks
UVLO (Under-voltage Lock Out)	None	Control/Sense	Disables all output FETs until V_S is above the UVLO threshold voltage which is typically 8.3 V.	See discussion in Section 3.4.
Vth	None	Control	If the voltage of any of the three current sense pins exceeds the current limit threshold voltage (Vth),which is typically 3.75 volts, all outputs are disabled. After all current sense pins fall below the Vth threshold voltage and the offending phase's top side input goes low, the output stage will return to an active state on the rising edge of ANY top side input command signal (At, Bt, or Ct).	

FAULT INDICATIONS

In the case of either an over-temperature or short-circuit fault, the SA306-IHZ will take no action to disable the outputs. However, the SC and TEMP signals can be fed to an external controller, as depicted in Figure 6, where a determination can be made regarding the appropriate course of action. In most cases, the SC pin would be connected to a FAULT input on the processor, which would immediately disable its PWM outputs. The TEMP fault does not require such an immediate response, and would typically be connected to a GPIO, or Keyboard Interrupt pin of the processor. In this case, the processor would recognize the condition as an external interrupt, which could be processed in software via an Interrupt Service Routine. The processor could optionally bring all inputs low, or assert a high level to either of the disable inputs on the SA306-IHZ. Figure 6 depicts an external SR flip-flop which provides a hard wired shutdown of all outputs in response to a fault indication. An SC or TEMP fault sets the latch, pulling the DIS2 pin HIGH. The processor clears the latched condition with a GPIO. This circuit can be used in safety critical applications to remove software from the fault-shutdown loop, or simply to reduce processor overhead. In applications which may not have available GPIO, the TEMP pin may be externally connected to the adjacent I_{LIM}/DIS1 pin. If the device temperature reaches ~135ºC all outputs will be disabled, de-energizing the motor. The SA306-IHZ will re-energize the motor when the device temperature falls below approximately 95ºC. The TEMP pin hysteresis is wide to reduce the likelihood of thermal oscillations that can greatly reduce the life of the device.

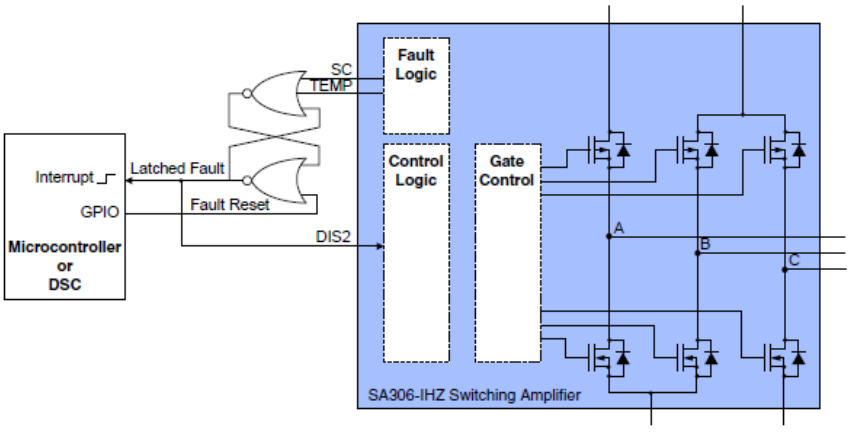


Figure 6. External Latch Circuit

UNDER-VOLTAGE LOCKOUT

Without sufficient supply voltage, the SA306-IHZ control circuit cannot sufficiently drive the gates of the output FETs. The undervoltage lockout condition results in the SA306-IHZ unilaterally disabling all output FETs until V_S is above the UVLO threshold indicated in the specification table in the Data Sheet[1]. There is no external signal indicating that an undervoltage lock-out condition is in progress. The SA306-IHZ has two V_S connections: one for phase A, and another for phases B & C. The supply voltages on these pins need not be the same, but the UVLO will engage if either is below the threshold. Hysteresis on the UVLO circuit prevents oscillations with typical power supply variations.

CURRENT SENSE — AN ALTERNATIVE

External power shunt resistors are not required with the SA306-IHZ. Forward current in each top, P-channel output FET is measured and mirrored to the respective current sense output pin, Ia, Ib and Ic, as depicted in Figures 1 and 5. By connecting a resistor between each current sense pin and a reference, such as ground, a voltage develops across the resistor that is proportional to the output current for that phase. As an alternative the currents Ia, Ib, and Ic can be fed to a single resistor and the voltage developed monitored by a high-impedance A/D converter, as shown in Figure 7.

As depicted in the 'Current Sense' plot on page 4 of the SA306-IHZ product data sheet, the maximum current per phase is slightly less than 2 milliamperes. Consequently, choose a resistor that will develop the voltage appropriate for the A/D Converter chosen. The full scale voltage will be the voltage developed across the resistor by the sum of the three currents — 6 milliamperes. Also allow a headroom of approximately 0.5 V.

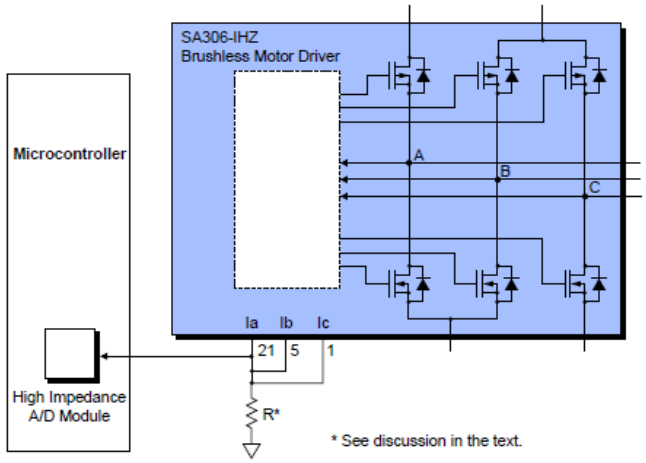


Figure 7. Current Monitoring Circuit

EXTERNAL FLYBACK DIODES

External fly-back diodes (D1 through D6), depicted in Figure 8, will offer superior reverse recovery characteristics and lower forward voltage drop than the internal back-body diodes. In high current applications, external flyback diodes can reduce power dissipation and heating during commutation of the motor current. Reverse recovery time and capacitance are the most important parameters to consider when selecting these diodes. Ultra-fast rectifiers offer better reverse recovery time and Schottky diodes typically have low capacitance. Individual application requirements will be the guide when determining the need for these diodes and for selecting the component which is most suitable.

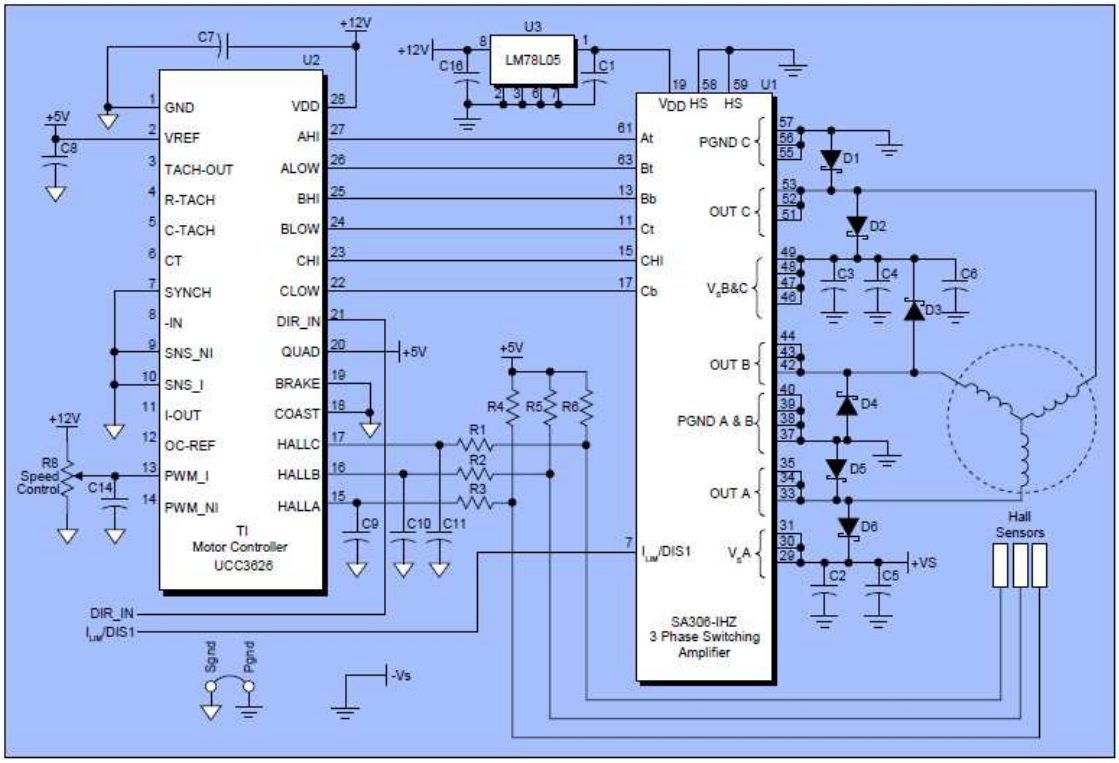


Figure 8. Three-Phase Motor Drive Circuit

A SPECIFIC EXAMPLE

Begin by choosing a motor that will exhibit the mechanical performance required — which is to say the torque, the efficiency, and other issues that will fulfill the motor drive requirements of your system. We have chosen as our example a low-inertia, brushless motor that delivers 557 mNm of torque at 2000 rpm. We selected a Maxon EC Flat motor www.maxonmotor.com. The characteristics of the windings of this motor are that any stator-winding pair exhibits a resistance (Rm) of 2.3 ohms and an inductance (Lm) of 2.5 millihenries. The torque constant (Kt) of the motor is 217 mMm oz-in/A.

DEMONSTRATION BOARD FOR THE SA306-IHZ

It is recommended that the designer acquire the DB64 Demonstration Board[3] and assemble a prototype. In the DB64 the SA306-IHZ input PWM control is achieved by means of a Texas Instrument on-board UCC3626 PW microcontroller[4]. The DB64 is designed to demonstrate the capabilities of the SA306-IHZ as a 3-phase brushless DC motor driver IC. From there one can easily convert the circuit developed with the DB64 Demonstration Board into a circuit similar to the one shown in Figure 8 which can serve as the base circuit for a production version.

LAYOUT CONSIDERATIONS

A simple two-layer printed circuit board construction is sufficient because of the convenient pinout of the SA306-IHZ PowerQuad package. Input signals are routed into one side of the SA306-IHZ package and high-power output signals are routed from the other side in 2 ounce copper. This eliminates the need to route control signals near motor connections where noise might corrupt the signals. Filling top and bottom layers with copper reduces inductive coupling from the high current outputs. Use 1 nF capacitors with excellent high frequency characteristics to bypass the V_S motor supplies at each phase as well as switching grade electrolytic capacitors. The six 100 V Schottky diodes (D1 – D6) conduct the commutation current via low forward voltage paths which reduces the power dissipation in the SA306-IHZ. These diodes are rated for 5 A continuous. Mount them close to the SA306-IHZ to reduce inductance in the commutating current loop. For applications with continuous currents less than 5 A, the Schottky diodes may not be necessary, but one must consider the higher forward voltage internal body diodes and the associated power dissipation that results.

Output Traces – Output traces carry signals with very high dV/dt and dI/dt. Proper routing and adequate power supply bypassing ensures normal operation. Poor routing and bypassing can cause erratic and low efficiency operation as well as ringing at the outputs.

Bypassing – The V_S supply should be bypassed with a surface mount ceramic capacitor mounted as close as possible to the V_S pins. Total inductance of the routing from the capacitor to the V_S and GND pins must be kept to a minimum to prevent noise from contaminating the logic control signals. A low ESR capacitor of at least 25 µF per ampere of output current should be placed near the SA306-IHZ as well. Capacitor types rated for switching applications are the only types that should be considered. Note that phases B & C share a V_S connection and the bypass recommendation should reflect the sum of B & C phase current. The bypassing requirements of the V_{DD} supply are less stringent, but still necessary. A 0.1 µF to 0.47 µF surface mount ceramic capacitor (X7R or NPO) connected directly to the V_{DD} pin is sufficient.

Ground Connections and Ground Planes – S_{GND} and P_{GND} pins are connected internally. However, these pins must be connected externally in such a way that there is no motor current flowing in the logic and signal ground traces as parasitic resistances in the small signal routing can develop sufficient voltage drops to erroneously trigger input transitions. Alternatively, a ground plane may be separated into power and logic sections connected by a pair of back-to-back Schottky diodes. This isolates noise between signal and power ground traces and prevents high currents from passing between the plane sections. Unused area on the top and bottom PCB planes should be filled with solid or hatched copper to minimize inductive coupling between signals. The copper fill may be left unconnected, although a ground plane is recommended.

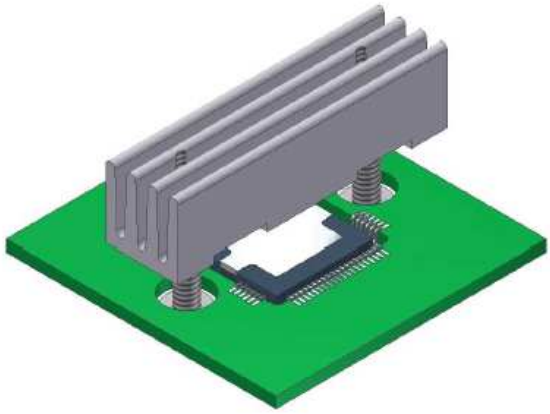
Table 2. Parts List for Figure 7

Reference Designation	Description
R1, R2, R3	470 Ω
R4, R5, R6	1 kΩ
R8	20 kΩ potentiometer (to control the PWM duty cycle)
R9, R10, R14, R15, R16, R17	5 kΩ
C1, C7, C8	1 µF
C2, C3, C4, C5, C6	1 nF
C9, C10, C11	2.2 nF
C14, C16	0.1 µF
D1, D2, D3, D4, D5, D6	PDS5100
U1	Apex Microtechnology SA306-IHZ or SA306A-FHZ
U2	Texas Instrument UCC3626
U3	LM78L05

POWER DISSIPATION

The thermally-enhanced package of the SA306-IHZ allows for several options for managing the power dissipated in the three output stages. Power dissipation in traditional PWM applications is a combination of output power dissipation and switching losses. Output power dissipation depends on the quadrant of operation and whether external flyback diodes are used to carry the reverse or commutating currents.

Switching losses are dependent on the frequency of the PWM cycle as described in the typical performance graphs. The size and orientation of the heatsink must be selected to manage the average power dissipation of the SA306-IHZ. Applications vary widely and various thermal techniques are available to match the required performance. The patent pending mounting technique shown in Figure 9, with the SA306-IHZ inverted and suspended through a cutout in the PCB, is adequate for power dissipation up to 17 W with the HS33 (a 1.5-inch long aluminum extrusion with four fins). In free air, mounting the PCB perpendicular to the ground, so that the heated air flows upward along the channels of the fins can provide a total θ_{J-A} of less than 14º C/W (9 W max average PD). Mounting the PCB parallel to the ground impedes the flow of heated air and provides a θ_{J-A} of 16.66º C/W (7.5 W max average PD). For applications in which higher power dissipation is expected or lower junction or case temperatures are required, a larger heatsink or circulated air can significantly improve the performance. Also see References 5 and 6.



Patent Pending

Figure 9. HS33 Heatsink

Appendix

A Brief Overview of PWM

The first pulse width modulation (PWM) ICs appeared on the market some 40 years ago. So the concept of PWM is at least as old. Though the earliest applications were in switching power supplies, it was not much later that the technique was first employed to drive brushless motors. The principal benefit of PWM as a control technique becomes clear by examining Figure A1. The traditional linear power delivery technique for limiting power simply employs a variable resistance as depicted in Figure A1(a). When maximum output is commanded, the driver reduces resistance of the pass element to a minimum. At this output level, losses in the linear circuit are relatively low. When zero output is commanded the pass element resistance again approaches infinity and losses again approach zero. However, the disadvantage of the linear circuit becomes clear in the midrange when the output level is in the vicinity of 50%. At these levels the resistance of the pass element is equal to the load resistance which means the heat generated in the amplifier is equal to the power delivered to the load! In other words, a linear control circuit exhibits a worst case efficiency of 50% when driving resistive loads at midrange power levels. What's more, when the load is reactive, this efficiency drops even further.

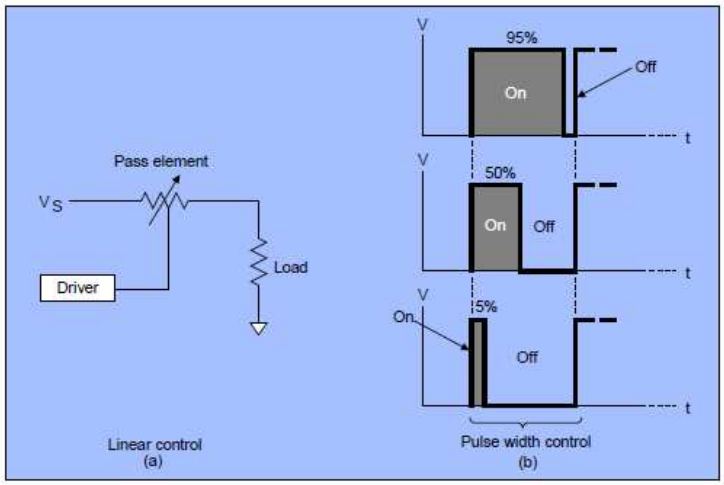


Figure A1. PWM versus Linear Control – PWM control in (b) exhibits far lower losses than the traditional linear control technique in (a)

Now consider PWM operation as depicted in figure A1(b). In a PWM control system an analog input level is converted into a variable-duty-cycle switch drive signal, The process of switching from one electrical state to another, which in this case is simply between OFF and ON, is called 'modulation', which accounts for why this technique is called 'pulse width modulation'. Beginning at zero duty cycle, which is to say OFF all the time, the duty cycle is often advanced as the motor begins to rotate, until it is running at the speed and/or the torque required by the application. In the case of a PWM control circuit, the rather negligible losses are primarily due to the ON resistance of the switching FET and the flyback diode which is why efficiencies as high as 80% to 95% are routine. However, at high switching frequencies the energy required to turn the FETs on and off can become significant.

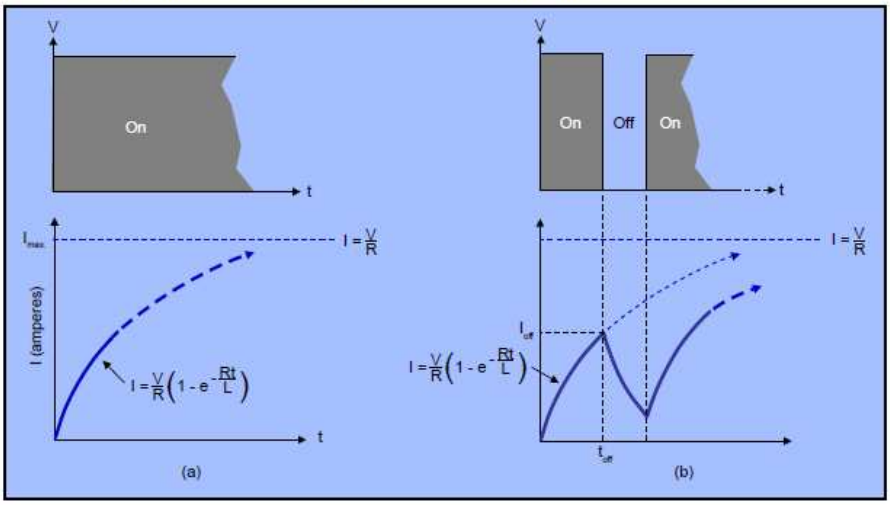


Figure A2. Linear versus PWM — Current behavior with a steady-state excitation in (a); Current behavior with PWM excitation in (b)

In addition to enhanced efficiency, PWM can play additional roles which include limiting the start-up current, controlling speed and controlling torque. The optimum switching frequency will depend on inertia and inductance of the brushless motor chosen and the application. The choice of the switching frequency affects both losses and the magnitude of the ripple current. A good rule of thumb is that raising the switching frequency increases the PWM losses. On the other hand, lowering the switching frequency limits the bandwidth of the system and can raise the heights of the ripple current pulses to the point that they become destructive or shut down the brushless motor driver IC. The ripple current pulses are depicted in Figure A2(a) and are discussed below.

BRUSHLESS MOTOR BEHAVIOR – AN OVERVIEW

One of the most critical moments with regard to a brushless motor – also true for a motor with brushes – is when power is first applied while the motor is at rest. At this time the rotor is stationary and is delivering no 'back EMF' (V_{BEMF}). V_{BEMF} can be expressed as:

$$V_{BEMF} = (K_b)(\text{Speed}) \qquad \text{(Equation1)}$$

Where: K_b = voltage constant (volts/1000 RPM)
Speed = revolutions per minute (expressed in thousands)

Once a voltage is applied to the motor, the rotor begins turning, generating a V_{BEMF} governed by (Equation 1). Ignore for the moment that the plan is to drive the motor with a PWM source, and assume the motor is driven by a steady-state voltage, then we can express the current by this equation:

$$I = [(V-V_{BEMF})/R_m][1-e^{-Rmt/Lm}] \qquad \text{(Equation 2)}$$

Where: V = the applied voltage
V_{BEMF} = back EMF
R_m = stator resistance (winding pair)
L_m = stator inductance (winding pair)

Note that in (Equation 2), the current (I) at any moment is a function of both the back EMF (V_{EMF}) and the time (t). The current when the motor is stopped ($V_{BEMF} = 0$) is illustrated in Figure A2(a) and is a familiar waveform for characterizing the current in any L-R circuit with its rise time governed by the time constant L/R.
Now let's exchange the steady-state excitation voltage for a PWM source, as shown in Figure A2(b). The current rises until the first ON pulse ends; when the voltage abruptly falls to zero at the end of the first applied voltage pulse, the current begins to decay towards zero. However, the next pulse will again drive the current upwards, and so forth, so that the current continues to rise. As the motor accelerates, the current waveform will exhibit a sawtooth profile. This sawtooth characteristic is also known as ripple. Because torque is directly proportional to current, the sequence of rising current pulses drive the motor, which develops a corresponding torque that accelerates the motor. But this is not so in the case of cycle-by-cycle current limit. Because in this case the current rise ceases immediately if the current reaches the limit value during any PWM pulse interval.

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4. *UCC2626, UCC3626 Brushless DC Motor Controller*, www.ti.com
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APPENDIX G: EMPLOYED RESOLVER-TO-DIGITAL CONVERTER (AD2S1210) DATA SHEET

Variable Resolution, 10-Bit to 16-Bit R/D Converter with Reference Oscillator

AD2S1210

FEATURES

Complete monolithic resolver-to-digital converter
3125 rps maximum tracking rate (10-bit resolution)
±2.5 arc minutes of accuracy
10-/12-/14-/16-bit resolution, set by user
Parallel and serial 10-bit to 16-bit data ports
Absolute position and velocity outputs
System fault detection
Programmable fault detection thresholds
Differential inputs
Incremental encoder emulation
Programmable sinusoidal oscillator on-board
Compatible with DSP and SPI interface standards
5 V supply with 2.3 V to 5 V logic interface
−40°C to +125°C temperature rating

APPLICATIONS

DC and ac servo motor control
Encoder emulation
Electric power steering
Electric vehicles
Integrated starter generators/alternators
Automotive motion sensing and control

GENERAL DESCRIPTION

The AD2S1210 is a complete 10-bit to 16-bit resolution tracking resolver-to-digital converter, integrating an on-board programmable sinusoidal oscillator that provides sine wave excitation for resolvers.

The converter accepts 3.15 V p-p ± 27% input signals, in the range of 2 kHz to 20 kHz on the sine and cosine inputs. A Type II servo loop is employed to track the inputs and convert the input sine and cosine information into a digital representation of the input angle and velocity. The maximum tracking rate is 3125 rps.

FUNCTIONAL BLOCK DIAGRAM

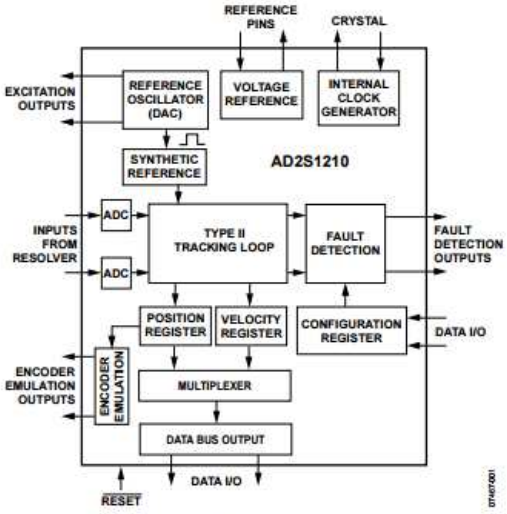

Figure 1.

PRODUCT HIGHLIGHTS

1. Ratiometric tracking conversion. The Type II tracking loop provides continuous output position data without conversion delay. It also provides noise immunity and tolerance of harmonic distortion on the reference and input signals.
2. System fault detection. A fault detection circuit can sense loss of resolver signals, out-of-range input signals, input signal mismatch, or loss of position tracking. The fault detection threshold levels can be individually programmed by the user for optimization within a particular application.
3. Input signal range. The sine and cosine inputs can accept differential input voltages of 3.15 V p-p ± 27%.
4. Programmable excitation frequency. Excitation frequency is easily programmable to a number of standard frequencies between 2 kHz and 20 kHz.
5. Triple format position data. Absolute 10-bit to 16-bit angular position data is accessed via either a 16-bit parallel port or a 4-wire serial interface. Incremental encoder emulation is in standard A-quad-B format with direction output available.
6. Digital velocity output. 10-bit to 16-bit signed digital velocity accessed via either a 16-bit parallel port or a 4-wire serial interface.

Rev. A

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REVISION HISTORY

2/10—Rev. 0 to Rev. A

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Changes to Ordering Guide ... 34

8/08—Revision 0: Initial Version

SPECIFICATIONS

AV_{DD} = DV_{DD} = 5.0 V ± 5%, CLKIN = 8.192 MHz ± 25%, EXC, $\overline{EXC}$ frequency = 10 kHz to 20 kHz (10-bit); 6 kHz to 20 kHz (12-bit); 3 kHz to 12 kHz (14-bit); 2 kHz to 10 kHz (16-bit); T_A = T_{MIN} to T_{MAX}; unless otherwise noted.[1]

Table 1.

Parameter	Min	Typ	Max	Unit	Conditions/Comments
SINE, COSINE INPUTS[2]					
Voltage Amplitude	2.3	3.15	4.0	V p-p	Sinusoidal waveforms, differential SIN to SINLO, COS to COSLO
Input Bias Current			8.25	µA	V_{IN} = 4.0 V p-p, CLKIN = 8.192 MHz
Input Impedance	485			kΩ	V_{IN} = 4.0 V p-p, CLKIN = 8.192 MHz
Phase Lock Range	−44		+44	Degrees	Sine/cosine vs. EXC output, Control Register D3 = 0
Common-Mode Rejection		±20		arc sec/V	10 Hz to 1 MHz, Control Register D4 = 0
ANGULAR ACCURACY[3]					
Angular Accuracy		±2.5 + 1 LSB	±5 + 1 LSB	arc min	B, D grades
		±5 + 1 LSB	±10 + 1 LSB	arc min	A, C grades
Resolution		10, 12, 14, 16		Bits	No missing codes
Linearity INL					
10-bit			±1	LSB	B, D grades
			±2	LSB	A, C grades
12-bit			±2	LSB	B, D grades
			±4	LSB	A, C grades
14-bit			±4	LSB	B, D grades
			±8	LSB	A, C grades
16-bit			±16	LSB	B, D grades
			±32	LSB	A, C grades
Linearity DNL			±0.9	LSB	
Repeatability		±1		LSB	
VELOCITY OUTPUT					
Velocity Accuracy[4]					
10-bit			±2	LSB	B, D grades, zero acceleration
			±4	LSB	A, C grades, zero acceleration
12-bit			±2	LSB	B, D grades, zero acceleration
			±4	LSB	A, C grades, zero acceleration
14-bit			±4	LSB	B, D grades, zero acceleration
			±8	LSB	A, C grades, zero acceleration
16-bit			±16	LSB	B, D grades, zero acceleration
			±32	LSB	A, C grades, zero acceleration
Resolution[5]		9, 11, 13, 15		Bits	
DYNAMNIC PERFORMANCE					
Bandwidth					
10-bit	2000		6500	Hz	
	2900		5300	Hz	CLKIN = 8.192 MHz
12-bit	900		2800	Hz	
	1200		2200	Hz	CLKIN = 8.192 MHz
14-bit	400		1500	Hz	
	600		1200	Hz	CLKIN = 8.192 MHz
16-bit	100		350	Hz	
	125		275	Hz	CLKIN = 8.192 MHz

Parameter	Min	Typ	Max	Unit	Conditions/Comments
Tracking Rate					
10-bit			3125	rps	CLKIN = 10.24 MHz
			2500		CLKIN = 8.192 MHz
12-bit			1250	rps	CLKIN = 10.24 MHz
			1000		CLKIN = 8.192 MHz
14-bit			625	rps	CLKIN = 10.24 MHz
			500		CLKIN = 8.192 MHz
16-bit			156.25	rps	CLKIN = 10.24 MHz
			125		CLKIN = 8.192 MHz
Acceleration Error					
10-bit		30		arc min	At 50,000 rps^2, CLKIN = 8.192 MHz
12-bit		30		arc min	At 10,000 rps^2, CLKIN = 8.192 MHz
14-bit		30		arc min	At 2500 rps^2, CLKIN = 8.192 MHz
16-bit		30		arc min	At 125 rps^2, CLKIN = 8.192 MHz
Settling Time 10° Step Input					
10-bit		0.6	0.9	ms	To settle to within ±2 LSB , CLKIN = 8.192 MHz
12-bit		2.2	3.1	ms	To settle to within ±2 LSB, CLKIN = 8.192 MHz
14-bit		6.5	9.0	ms	To settle to within ±2 LSB , CLKIN = 8.192 MHz
16-bit		27.5	40	ms	To settle to within ±2 LSB, CLKIN = 8.192 MHz
Settling Time 179° Step Input					
10-bit		1.5	2.2	ms	To settle to within ±2 LSB , CLKIN = 8.192 MHz
12-bit		4.75	6.0	ms	To settle to within ±2 LSB, CLKIN = 8.192 MHz
14-bit		10.5	14.7	ms	To settle to within ±2 LSB , CLKIN = 8.192 MHz
16-bit		45	66	ms	To settle to within ±2 LSB, CLKIN = 8.192 MHz
EXC, $\overline{\text{EXC}}$ OUTPUTS					
Voltage	3.2	3.6	4.0	V p-p	Load ±100 µA, typical differential output (EXC to $\overline{\text{EXC}}$) = 7.2 V p-p
Center Voltage	2.40	2.47	2.53	V	
Frequency	2		20	kHz	
EXC/$\overline{\text{EXC}}$ DC Mismatch			30	mV	
EXC/$\overline{\text{EXC}}$ AC Mismatch			100	mV	
THD		−58		dB	First five harmonics
VOLTAGE REFERENCE					
REFOUT	2.40	2.47	2.53	V	±I_{OUT} = 100 µA
Drift		100		ppm/°C	
PSRR		−60		dB	
CLKIN, XTALOUT[6]					
V_{IL} Voltage Input Low			0.8	V	
V_{IH} Voltage Input High	2.0			V	
LOGIC INPUTS					
V_{IL} Voltage Input Low			0.8	V	V_{DRIVE} = 2.7 V to 5.25 V
			0.7	V	V_{DRIVE} = 2.3 V to 2.7 V
V_{IH} Voltage Input High	2.0			V	V_{DRIVE} = 2.7 V to 5.25 V
	1.7			V	V_{DRIVE} = 2.3 V to 2.7 V
I_{IL} Low Level Input Current (Non Pull-Up)			10	µA	
I_{IL} Low Level Input Current (Pull-Up)			80	µA	RES0, RES1, $\overline{\text{RD}}$, $\overline{\text{WR}}$/$\overline{\text{FSYNC}}$, A0, A1, and $\overline{\text{RESET}}$ pins
I_{IH} High Level Input Current	−10			µA	
LOGIC OUTPUTS					
V_{OL} Voltage Output Low			0.4	V	V_{DRIVE} = 2.3 V to 5.25 V
V_{OH} Voltage Output High	2.4			V	V_{DRIVE} = 2.7 V to 5.25 V
	2.0			V	V_{DRIVE} = 2.3 V to 2.7 V
I_{OZH} High Level Three-State Leakage	−10			µA	
I_{OZL} Low Level Three-State Leakage			10	µA	

Parameter	Min	Typ	Max	Unit	Conditions/Comments
POWER REQUIREMENTS					
AV_{DD}	4.75		5.25	V	
DV_{DD}	4.75		5.25	V	
V_{DRIVE}	2.3		5.25	V	
POWER SUPPLY					
I_{AVDD}			12	mA	
I_{DVDD}			35	mA	
I_{OVDD}			2	mA	

[1] Temperature ranges are as follows: A, B grades: −40°C to +85°C; C, D grades: −40°C to +125°C.
[2] The voltages, SIN, SINLO, COS, and COSLO, relative to AGND, must always be between 0.15 V and AV_{DD} − 0.2 V.
[3] All specifications within the angular accuracy parameter are tested at constant velocity, that is, zero acceleration.
[4] The velocity accuracy specification includes velocity offset and dynamic ripple.
[5] For example when RES0 = 0 and RES1 = 1, the position output has a resolution of 12 bits. The velocity output has a resolution of 11 bits with the MSB indicating the direction of rotation. In this example, with a CLKIN frequency of 8.192 MHz the velocity LSB is 0.488 rps, that is, 1000 rps/(2^{11}).
[6] The clock frequency of the AD251210 can be supplied with a crystal, an oscillator, or directly from a DSP/microprocessor digital output. When using a single-ended clock signal directly from the DSP/microprocessor, the XTALOUT pin should remain open circuit and the logic levels outlined under the logic inputs parameter in Table 1 apply.

TIMING SPECIFICATIONS

$AV_{DD} = DV_{DD} = 5.0\ V \pm 5\%$, $T_A = T_{MIN}$ to T_{MAX}, unless otherwise noted.[1]

Table 2.

Parameter	Description	Limit at T_{MIN}, T_{MAX}	Unit
f_{CLKIN}	Frequency of clock input	6.144	MHz min
		10.24	MHz max
t_{CK}	Clock period (= $1/f_{CLKIN}$)	98	ns min
		163	ns max
t_1	A0 and A1 setup time before $\overline{RD}/\overline{CS}$ low	2	ns min
t_2	Delay $\overline{CS}$ falling edge to $\overline{WR}/FSYNC$ rising edge	22	ns min
t_3	Address/data setup time during a write cycle	3	ns min
t_4	Address/data hold time during a write cycle	2	ns min
t_5	Delay $\overline{WR}/FSYNC$ rising edge to $\overline{CS}$ rising edge	2	ns min
t_6	Delay $\overline{CS}$ rising edge to $\overline{CS}$ falling edge	10	ns min
t_7	Delay between writing address and writing data	$2 \times t_{CK} + 20$	ns min
t_8	A0 and A1 hold time after $\overline{WR}/FSYNC$ rising edge	2	ns min
t_9	Delay between successive write cycles	$6 \times t_{CK} + 20$	ns min
t_{10}	Delay between rising edge of $\overline{WR}/FSYNC$ and falling edge of $\overline{RD}$	2	ns min
t_{11}	Delay $\overline{CS}$ falling edge to $\overline{RD}$ falling edge	2	ns min
t_{12}	Enable delay $\overline{RD}$ low to data valid in configuration mode		
	V_{DRIVE} = 4.5 V to 5.25 V	37	ns min
	V_{DRIVE} = 2.7 V to 3.6 V	25	ns min
	V_{DRIVE} = 2.3 V to 2.7 V	30	ns min
t_{13}	$\overline{RD}$ rising edge to $\overline{CS}$ rising edge	2	ns min
t_{14A}	Disable delay $\overline{RD}$ high to data high-Z	16	ns min
t_{14B}	Disable delay $\overline{CS}$ high to data high-Z	16	ns min
t_{15}	Delay between rising edge of $\overline{RD}$ and falling edge of $\overline{WR}/\overline{FSYNC}$	2	ns min
t_{16}	$\overline{SAMPLE}$ pulse width	$2 \times t_{CK} + 20$	ns min
t_{17}	Delay from $\overline{SAMPLE}$ before $\overline{RD}/\overline{CS}$ low	$6 \times t_{CK} + 20$	ns min
t_{18}	Hold time $\overline{RD}$ before $\overline{RD}$ low	2	ns min
t_{19}	Enable delay $\overline{RD}/\overline{CS}$ low to data valid		
	V_{DRIVE} = 4.5 V to 5.25 V	17	ns min
	V_{DRIVE} = 2.7 V to 3.6 V	21	ns min
	V_{DRIVE} = 2.3 V to 2.7 V	33	ns min
t_{20}	$\overline{RD}$ pulse width	6	ns min
t_{21}	A0 and A1 set time to data valid when $\overline{RD}/\overline{CS}$ low		
	V_{DRIVE} = 4.5 V to 5.25 V	36	ns min
	V_{DRIVE} = 2.7 V to 3.6 V	37	ns min
	V_{DRIVE} = 2.3 V to 2.7 V	29	ns min
t_{22}	Delay $\overline{WR}/FSYNC$ falling edge to SCLK rising edge	3	ns min
t_{23}	Delay $\overline{WR}/FSYNC$ falling edge to SDO release from high-Z		
	V_{DRIVE} = 4.5 V to 5.25 V	16	ns min
	V_{DRIVE} = 2.7 V to 3.6 V	26	ns min
	V_{DRIVE} = 2.3 V to 2.7 V	29	ns min
t_{24}	Delay SCLK rising edge to DBx valid		
	V_{DRIVE} = 4.5 V to 5.25 V	24	ns min
	V_{DRIVE} = 2.7 V to 3.6 V	18	ns min
	V_{DRIVE} = 2.3 V to 2.7 V	32	ns min
t_{25}	SCLK high time	$0.4 \times t_{SCLK}$	ns min
t_{26}	SCLK low time	$0.4 \times t_{SCLK}$	ns min
t_{27}	SDI setup time prior to SCLK falling edge	3	ns min
t_{28}	SDI hold time after SCLK falling edge	2	ns min

Parameter	Description	Limit at T_{MIN}, T_{MAX}	Unit
t_{29}	Delay $\overline{WR}/\overline{FSYNC}$ rising edge to SDO high-Z	15	ns min
t_{30}	Delay from $\overline{SAMPLE}$ before $\overline{WR}/\overline{FSYNC}$ falling edge	$6 \times t_{CK} + 20$ ns	ns min
t_{31}	Delay $\overline{CS}$ falling edge to $\overline{WR}/\overline{FSYNC}$ falling edge in normal mode	2	ns min
t_{32}	A0 and A1 setup time before $\overline{WR}/\overline{FSYNC}$ falling edge	2	ns min
t_{33}	A0 and A1 hold time after $\overline{WR}/\overline{FSYNC}$ falling edge[2]		
	In normal mode, A0 = 0, A1 = 0/1	$24 \times t_{CK} + 5$ ns	ns min
	In configuration mode, A0 = 1, A1 = 1	$8 \times t_{CK} + 5$ ns	ns min
t_{34}	Delay $\overline{WR}/\overline{FSYNC}$ rising edge to $\overline{WR}/\overline{FSYNC}$ falling edge	10	ns min
f_{SCLK}	Frequency of SCLK input		
	V_{DRIVE} = 4.5 V to 5.25 V	20	MHz
	V_{DRIVE} = 2.7 V to 3.6 V	25	MHz
	V_{DRIVE} = 2.3 V to 2.7 V	15	MHz

[1] Temperature ranges are as follows: A, B grades: –40°C to +85°C; C, D grades: –40°C to +125°C.
[2] A0 and A1 should remain constant for the duration of the serial readback. This may require 24 clock periods to read back the 8-bit fault information in addition to the 16 bits of position/velocity data. If the fault information is not required, A0/A1 may be released following 16 clock cycles.

ABSOLUTE MAXIMUM RATINGS

Table 3.

Parameter	Rating
AV_{DD} to AGND, DGND	−0.3 V to +7.0 V
DV_{DD} to AGND, DGND	−0.3 V to +7.0 V
V_{DRIVE} to AGND, DGND	−0.3 V to AV_{DD}
AV_{DD} to DV_{DD}	−0.3 V to +0.3 V
AGND to DGND	−0.3 V to +0.3 V
Analog Input Voltage to AGND	−0.3 V to AV_{DD} + 0.3 V
Digital Input Voltage to DGND	−0.3 V to V_{DRIVE} + 0.3 V
Digital Output Voltage to DGND	−0.3 V to V_{DRIVE} + 0.3 V
Analog Output Voltage Swing	−0.3 V to AV_{DD} + 0.3 V
Input Current to Any Pin Except Supplies[1]	±10 mA
Operating Temperature Range (Ambient)	
A, B Grades	−40°C to +85°C
C, D Grades	−40°C to +125°C
Storage Temperature Range	−65°C to +150°C
θ_{JA} Thermal Impedance[2]	54°C/W
θ_{JA} Thermal Impedance[2]	15°C/W
RoHS-Compliant Temperature, Soldering Reflow	260(−5/+0)°C
ESD	2 kV HBM

[1] Transient currents of up to 100 mA do not cause latch-up.
[2] JEDEC 2S2P standard board.

Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those indicated in the operational section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ESD CAUTION

ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

PIN CONFIGURATION AND FUNCTION DESCRIPTIONS

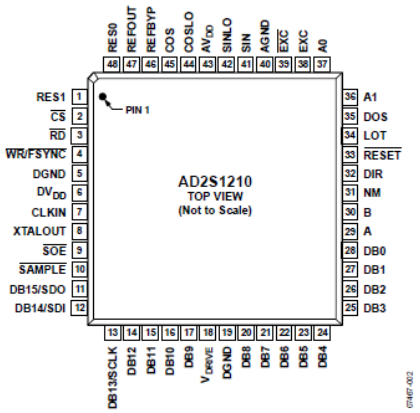


Figure 2. Pin Configuration

Table 4. Pin Function Descriptions

Pin No.	Mnemonic	Description
1	RES1	Resolution Select 1. Logic input. RES1 in conjunction with RES0 allows the resolution of the AD2S1210 to be programmed. Refer to the Configuration of AD2S1210 section.
2	$\overline{CS}$	Chip Select. Active low logic input. The device is enabled when $\overline{CS}$ is held low.
3	$\overline{RD}$	Edge-Triggered Logic Input. When the $\overline{SOE}$ pin is high, this pin acts as a frame synchronization signal and output enable for the parallel data outputs, DB15 to DB0. The output buffer is enabled when $\overline{CS}$ and $\overline{RD}$ are held low. When the $\overline{SOE}$ pin is low, the $\overline{RD}$ pin should be held high.
4	$\overline{WR/FSYNC}$	Edge-Triggered Logic Input. When the $\overline{SOE}$ pin is high, this pin acts as a frame synchronization signal and input enable for the parallel data inputs, DB7 to DB0. The input buffer is enabled when $\overline{CS}$ and $\overline{WR/FSYNC}$ are held low. When the $\overline{SOE}$ pin is low, the $\overline{WR/FSYNC}$ pin acts as a frame synchronization signal and enable for the serial data bus.
5, 19	DGND	Digital Ground. These pins are ground reference points for digital circuitry on the AD2S1210. Refer all digital input signals to this DGND voltage. Both of these pins can be connected to the AGND plane of a system. The DGND and AGND voltages should ideally be at the same potential and must not be more than 0.3 V apart, even on a transient basis.
6	DV_{DD}	Digital Supply Voltage, 4.75 V to 5.25 V. This is the supply voltage for all digital circuitry on the AD2S1210. The AV_{DD} and DV_{DD} voltages ideally should be at the same potential and must not be more than 0.3 V apart, even on a transient basis.
7	CLKIN	Clock Input. A crystal or oscillator can be used at the CLKIN and XTALOUT pins to supply the required clock frequency of the AD2S1210. Alternatively, a single-ended clock can be applied to the CLKIN pin. The input frequency of the AD2S1210 is specified from 6.144 MHz to 10.24 MHz.
8	XTALOUT	Crystal Output. When using a crystal or oscillator to supply the clock frequency to the AD2S1210, apply the crystal across the CLKIN and XTALOUT pins. When using a single-ended clock source, the XTALOUT pin should be considered a no connect pin.
9	$\overline{SOE}$	Serial Output Enable. Logic input. This pin enables either the parallel or serial interface. The serial interface is selected by holding the $\overline{SOE}$ pin low, and the parallel interface is selected by holding the $\overline{SOE}$ pin high.
10	$\overline{SAMPLE}$	Sample Result. Logic input. Data is transferred from the position and velocity integrators to the position and velocity registers, after a high-to-low transition on the $\overline{SAMPLE}$ signal. The fault register is also updated after a high-to-low transition on the $\overline{SAMPLE}$ signal.
11	DB15/SDO	Data Bit 15/Serial Data Output Bus. When the $\overline{SOE}$ pin is high, this pin acts as DB15, a three-state data output pin controlled by $\overline{CS}$ and $\overline{RD}$. When the $\overline{SOE}$ pin is low, this pin acts as SDO, the serial data output bus controlled by $\overline{CS}$ and $\overline{WR/FSYNC}$. The bits are clocked out on the rising edge of SCLK.
12	DB14/SDI	Data Bit 14/Serial Data Input Bus. When the $\overline{SOE}$ pin is high, this pin acts as DB14, a three-state data output pin controlled by $\overline{CS}$ and $\overline{RD}$. When the $\overline{SOE}$ pin is low, this pin acts as SDI, the serial data input bus controlled by $\overline{CS}$ and $\overline{WR/FSYNC}$. The bits are clocked in on the falling edge of SCLK.

Pin No.	Mnemonic	Description
13	DB13/SCLK	Data Bit 13/Serial Clock. In parallel mode, this pin acts as DB13, a three-state data output pin controlled by $\overline{CS}$ and $\overline{RD}$. In serial mode, this pin acts as the serial clock input.
14 to 17	DB12 to DB9	Data Bit 12 to Data Bit 9. Three-state data output pins controlled by $\overline{CS}$ and $\overline{RD}$.
18	V_{DRIVE}	Logic Power Supply Input. The voltage supplied at this pin determines at what voltage the interface operates. Decouple this pin to DGND. The voltage range on this pin is 2.3 V to 5.25 V and may be different to the voltage range at AV_{DD} and DV_{DD} but should never exceed either by more than 0.3 V.
20	DB8	Data Bit 8. Three-state data output pin controlled by $\overline{CS}$ and $\overline{RD}$.
21 to 28	DB7 to DB0	Data Bit 7 to Data Bit 0. Three-state data input/output pins controlled by $\overline{CS}$, $\overline{RD}$, and $\overline{WR}/\overline{FSYNC}$.
29	A	Incremental Encoder Emulation Output A. Logic output. This output is free running and is valid if the resolver format input signals applied to the converter are valid.
30	B	Incremental Encoder Emulation Output B. Logic output. This output is free running and is valid if the resolver format input signals applied to the converter are valid.
31	NM	North Marker Incremental Encoder Emulation Output. Logic output. This output is free running and is valid if the resolver format input signals applied to the converter are valid.
32	DIR	Direction. Logic output. This output is used in conjunction with the incremental encoder emulation outputs. The DIR output indicates the direction of the input rotation and is high for increasing angular rotation.
33	$\overline{RESET}$	Reset. Logic input. The AD2S1210 requires an external reset signal to hold the $\overline{RESET}$ input low until V_{DD} is within the specified operating range of 4.75 V to 5.25 V.
34	LOT	Loss of Tracking. Logic output. LOT is indicated by a logic low on the LOT pin and is not latched. Refer to the Loss of Position Tracking Detection section.
35	DOS	Degradation of Signal. Logic output. Degradation of signal (DOS) is detected when either resolver input (sine or cosine) exceeds the specified DOS sine/cosine threshold or when an amplitude mismatch occurs between the sine and cosine input voltages. DOS is indicated by a logic low on the DOS pin. Refer to the Signal Degradation Detection section.
36	A1	Mode Select 1. Logic input. A1 in conjunction with A0 allows the mode of the AD2S1210 to be selected. Refer to the Configuration of AD2S1210 section.
37	A0	Mode Select 0. Logic input. A0 in conjunction with A1 allows the mode of the AD2S1210 to be selected. Refer to the Configuration of AD2S1210 section.
38	EXC	Excitation Frequency. Analog output. An on-board oscillator provides the sinusoidal excitation signal (EXC) and its complement signal ($\overline{EXC}$) to the resolver. The frequency of this reference signal is programmable via the excitation frequency register.
39	$\overline{EXC}$	Excitation Frequency Complement. Analog output. An on-board oscillator provides the sinusoidal excitation signal (EXC) and its complement signal ($\overline{EXC}$) to the resolver. The frequency of this reference signal is programmable via the excitation frequency register.
40	AGND	Analog Ground. This pin is the ground reference points for analog circuitry on the AD2S1210. Refer all analog input signals and any external reference signal to this AGND voltage. Connect the AGND pin to the AGND plane of a system. The AGND and DGND voltages should ideally be at the same potential and must not be more than 0.3 V apart, even on a transient basis.
41	SIN	Positive Analog Input of Differential SIN/SINLO Pair. The input range is 2.3 V p-p to 4.0 V p-p.
42	SINLO	Negative Analog Input of Differential SIN/SINLO Pair. The input range is 2.3 V p-p to 4.0 V p-p.
43	AV_{DD}	Analog Supply Voltage, 4.75 V to 5.25 V. This pin is the supply voltage for all analog circuitry on the AD2S1210. The AV_{DD} and DV_{DD} voltages ideally should be at the same potential and must not be more than 0.3 V apart, even on a transient basis.
44	COSLO	Negative Analog Input of Differential COS/COSLO Pair. The input range is 2.3 V p-p to 4.0 V p-p.
45	COS	Positive Analog Input of Differential COS/COSLO Pair. The input range is 2.3 V p-p to 4.0 V p-p.
46	REFBYP	Reference Bypass. Connect reference decoupling capacitors at this pin. Typical recommended values are 10 µF and 0.01 µF.
47	REFOUT	Voltage Reference Output.
48	RES0	Resolution Select 0. Logic input. RES0 in conjunction with RES1 allows the resolution of the AD2S1210 to be programmed. Refer to the Configuration of AD2S1210 section.

TYPICAL PERFORMANCE CHARACTERISTICS

T_A = 25°C, AV_{DD} = DV_{DD} = V_{DRIVE} = 5 V, SIN/SINLO = 3.15 V p-p, COS/COSLO = 3.15 V p-p, CLKIN = 8.192 MHz , unless otherwise noted.

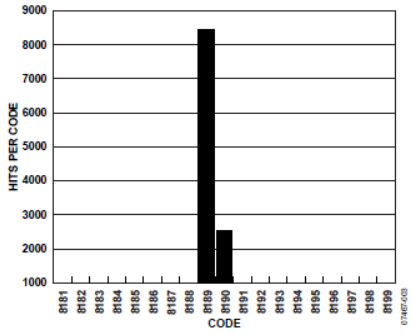


Figure 3. Typical 16-Bit Angular Accuracy Histogram Of Codes, 10,000 Samples

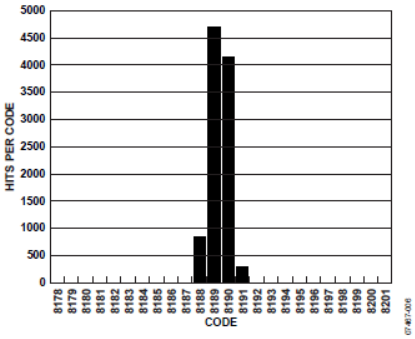


Figure 6. Typical 12-Bit Angular Accuracy Histogram of Codes, 10,000 Samples, Hysteresis Disabled

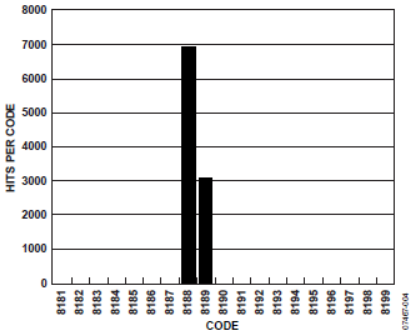


Figure 4. Typical 14-Bit Angular Accuracy Histogram of Codes, 10,000 Samples, Hysteresis Disabled

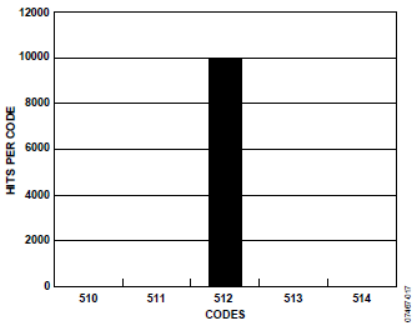


Figure 7. Typical 12-Bit Angular Accuracy Histogram of Codes, 10,000 Samples, Hysteresis Enabled

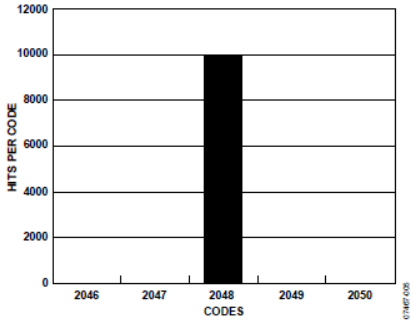


Figure 5. Typical 14-Bit Angular Accuracy Histogram of Codes, 10,000 Samples, Hysteresis Enabled

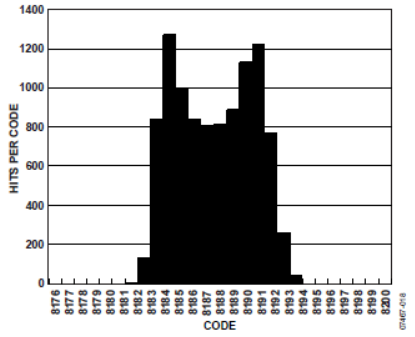


Figure 8. Typical 10-Bit Angular Accuracy Histogram of Codes, 10,000 Samples, Hysteresis Disabled

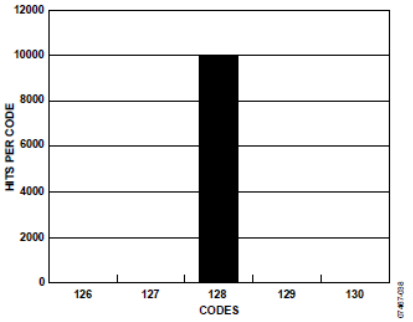


Figure 9. Typical 10-Bit Angular Accuracy Histogram of Codes, 10,000 Samples, Hysteresis Enabled

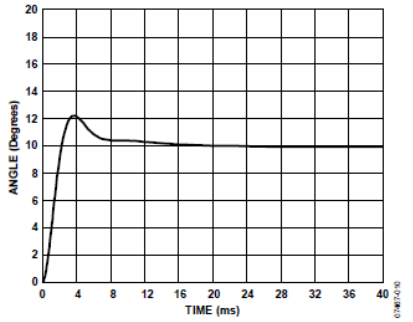


Figure 10. Typical 16-Bit 10° Step Response

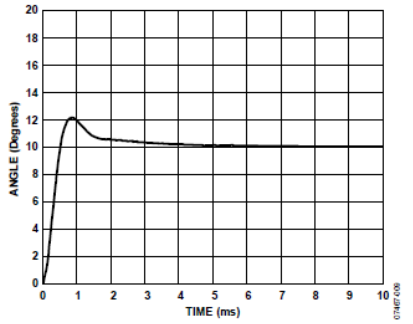


Figure 11. Typical 14-Bit 10° Step Response

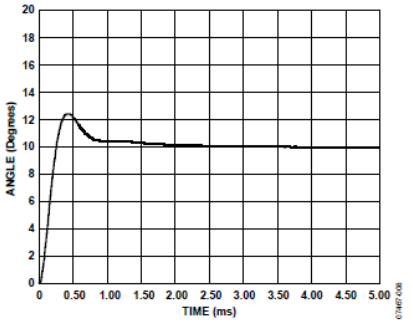


Figure 12. Typical 12-Bit 10° Step Response

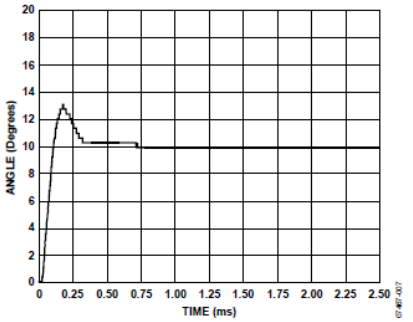


Figure 13. Typical 10-Bit 10° Step Response

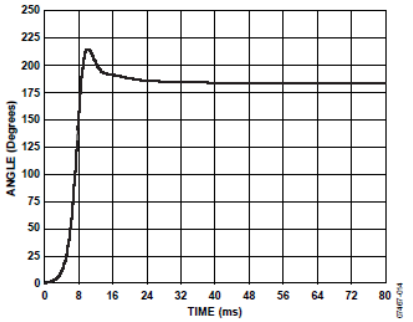


Figure 14. Typical 16-Bit 179° Step Response

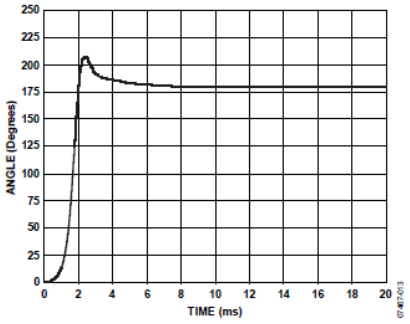


Figure 15. Typical 14-Bit 179° Step Response

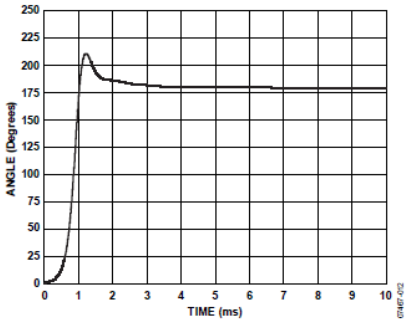


Figure 16. Typical 12-Bit 179° Step Response

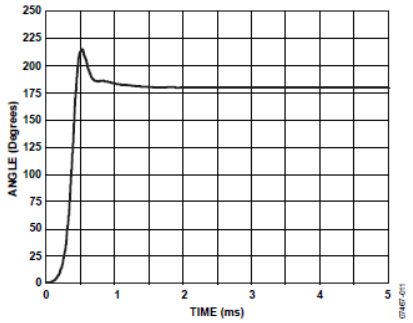


Figure 17. Typical 10-Bit 179° Step Response

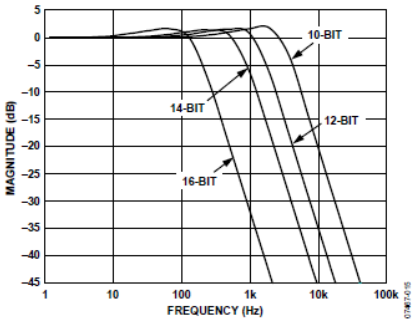


Figure 18. Typical System Magnitude Response

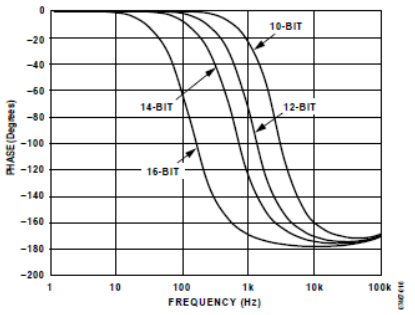


Figure 19. Typical System Phase Response

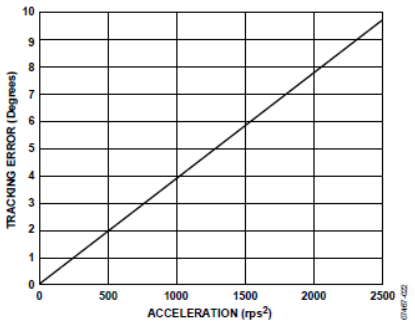


Figure 20. Typical 16-Bit Tracking Error vs. Acceleration

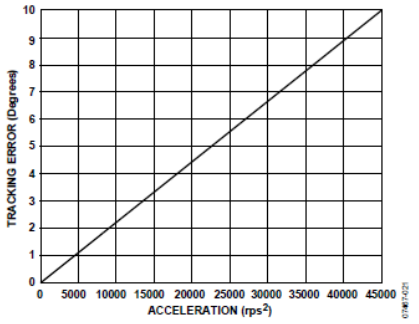


Figure 21. Typical 14-Bit Tracking Error vs. Acceleration

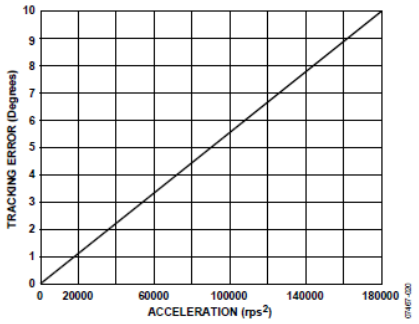


Figure 22. Typical 12-Bit Tracking Error vs. Acceleration

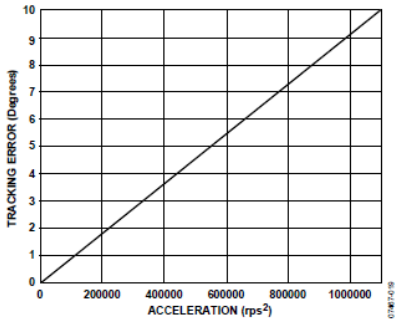


Figure 23. Typical 10-Bit Tracking Error vs. Acceleration

RESOLVER FORMAT SIGNALS

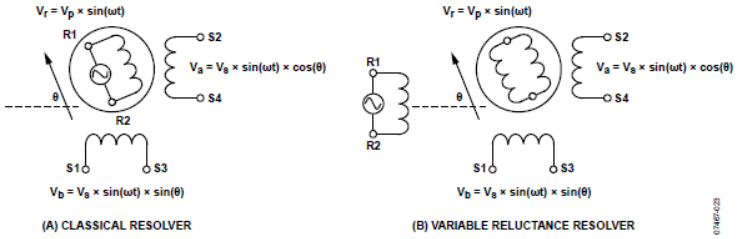


Figure 24. Classical Resolver vs. Variable Reluctance Resolver

A resolver is a rotating transformer, typically with a primary winding on the rotor and two secondary windings on the stator. In the case of a variable reluctance resolver, there are no windings on the rotor, as shown in Figure 24. The primary winding is on the stator as well as the secondary windings, but the saliency in the rotor design provides the sinusoidal variation in the secondary coupling with the angular position. Either way, the resolver output voltages (S3 – S1, S2 – S4) have the same equations, as shown in Equation 1.

$$S3 - S1 = E_0 \sin \omega t \times \sin \theta$$
$$S2 - S4 = E_0 \sin \omega t \times \cos \theta \quad (1)$$

where:
θ is the shaft angle.
$Sin\omega t$ is the rotor excitation frequency.
E_0 is the rotor excitation amplitude.

The stator windings are displaced mechanically by 90° (see Figure 24). The primary winding is excited with an ac reference. The amplitude of subsequent coupling onto the stator secondary windings is a function of the position of the rotor (shaft) relative to the stator. The resolver, therefore, produces two output voltages (S3 – S1, S2 – S4) modulated by the sine and cosine of shaft angle. Resolver format signals refer to the signals derived from the output of a resolver, as shown in Equation 1. Figure 25 illustrates the output format.

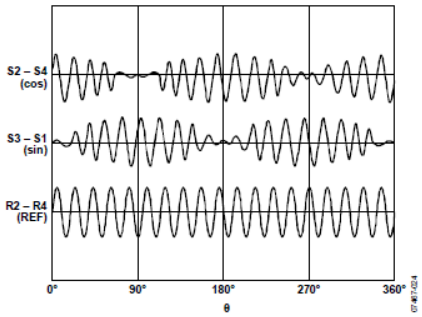


Figure 25. Electrical Resolver Representation

THEORY OF OPERATION

RESOLVER TO DIGITAL CONVERSION

The AD2S1210 operates on a Type II tracking closed-loop principle. The output continually tracks the position of the resolver without the need for external conversion and wait states. As the resolver moves through a position equivalent to the least significant bit weighting, the output is updated by one LSB.

The converter tracks the shaft angle θ by producing an output angle ϕ that is fed back and compared to the input angle θ, and the resulting error between the two is driven towards 0 when the converter is correctly tracking the input angle. To measure the error, S3 – S1 is multiplied by cosϕ and S2 – S4 is multiplied by sinϕ to give

$$E_0 \sin\omega t \times \sin\theta \cos\phi \quad \text{(for S3 – S1)}$$

$$E_0 \sin\omega t \times \cos\theta \sin\phi \quad \text{(for S2 – S4)}$$

The difference is taken, giving

$$E_0 \sin\omega t \times (\sin\theta \cos\phi - \cos\theta \sin\phi) \quad (2)$$

This signal is demodulated using the internally generated synthetic reference, yielding

$$E_0 (\sin\theta \cos\phi - \cos\theta \sin\phi) \quad (3)$$

Equation 3 is equivalent to $E_0 \sin(\theta - \phi)$, which is approximately equal to $E_0(\theta - \phi)$ for small values of $\theta - \phi$, where $\theta - \phi$ = angular error.

The value $E_0 (\theta - \phi)$ is the difference between the angular error of the rotor and the digital angle output of the converter.

A phase-sensitive demodulator, some integrators, and a compensation filter form a closed-loop system that seeks to null the error signal. When this is accomplished, ϕ equals the Resolver Angle θ within the rated accuracy of the converter. A Type II tracking loop is used so that constant velocity inputs can be tracked without inherent error.

FAULT DETECTION CIRCUIT

The AD2S1210 fault detection circuit can sense loss of resolver signals, out-of-range input signals, input signal mismatch, or loss of position tracking; however, in the event of a fault, the position indicated by the AD2S1210 may differ significantly from the actual shaft position of the resolver.

Monitor Signal

The AD2S1210 generates a monitor signal by comparing the angle in the position register to the incoming sine and cosine signals from the resolver. The monitor signal is created in a similar fashion to the error signal described in the Resolver to Digital Conversion section. The incoming signals, sinθ and cosθ, are multiplied by the sin and cos of the output angle, respectively, and then added together.

$$Monitor = A1 \times \sin\theta \times \sin\phi + A2 \times \cos\theta \times \cos\phi \quad (4)$$

where:
A1 is the amplitude of the incoming sine signal (A1 × sinθ).
A2 is the amplitude of the incoming cosine signal (A2 × cosθ).
θ is the resolver angle.
ϕ is the angle stored in the position register.

Note that Equation 4 is shown after demodulation, with the Carrier Signal sinωt removed. Also, note that for matched input signal (that is, a no fault condition), A1 = A2.

When A1 = A2 and the converter is tracking (θ = ϕ), the monitor signal output has a constant magnitude of A1 (Monitor = A1 × ($\sin^2\theta + \cos^2\theta$) = A1), which is independent of shaft angle. When A1 ≠ A2, the monitor signal magnitude varies between A1 and A2 at twice the rate of shaft rotation. The monitor signal is used as described in the following sections to detect degradation or loss of input signals.

Loss of Signal Detection

The AD2S1210 indicates that a loss of signal (LOS) has occurred for four separate conditions.

- When either resolver input (sine or cosine) falls below the specified LOS sine/cosine threshold. This threshold is defined by the user and is set by writing to the internal register, Address 0x88 (see the Register Map section).
- When any of the resolver input pins (SIN, SINLO, COS, or COSLO) are disconnected from the sensor.
- When any of the resolver input pins (SIN, SINLO, COS, or COSLO) are clipping the power rail or ground rail of the AD2S1210. Refer to the Sine/Cosine Input Clipping section.
- When a configuration parity error has occurred. Refer to the Configuration Parity Error section.

A loss of signal is caused if either of the stator windings of the resolver (sine or cosine) are open circuit or have a number of shorted turns. LOS is indicated by both the DOS and LOT pins latching as logic low outputs. The DOS and LOT pins are reset to a no fault state when the user enters configuration mode and reads the fault register. The LOS condition has priority over both the DOS and LOT conditions, as shown in Table 6. To determine the cause of the LOS fault detection, the user must read the fault register, Address 0xFF (see the Register Map section).

When a loss of signal is detected due to the resolver inputs (sine or cosine) falling below the specified LOS sine/cosine threshold, the electrical angle through which the resolver may rotate before the LOS can be detected by the AD2S1210 is referred to as the LOS angular latency. This is defined by the specified LOS sine/cosine threshold set by the user and the maximum amplitude of the input signals being applied to the AD2S1210. The worst-case angular latency can be calculated as follows:

$$Angular\ Latency = 2 \times Arc\cos\left[\frac{LOS\ threshold}{\max\ sine\ /\ cosine\ amplitude}\right] \quad (5)$$

The preceding equation is based on the worst-case angular error, which can be seen by the AD2S1210 before an LOS fault is indicated. This occurs if one of the resolver input signals, either sine or cosine, is lost while the remaining signal is at its peak amplitude, for example, if the sine input is lost while the input angle is 90°. The worst-case angular latency is twice the worst-case angular error.

Signal Degradation Detection

The AD2S1210 indicates that a degradation of signal (DOS) has occurred for two separate conditions.

- When either resolver input (sine or cosine) exceeds the specified DOS sine/cosine threshold. This threshold is defined by the user and is set by writing to the internal register, Address 0x89 (see the Register Map section).
- When the amplitudes of the input signals, sine and cosine, mismatch by more than the specified DOS sine/cosine mismatch threshold. This threshold is defined by the user and is set by writing to the internal register, Address 0x8A (see the Register Map section). The AD2S1210 continuously stores the minimum and maximum magnitude of the monitor signal in internal registers. The difference between the minimum and maximum is calculated to determine if a DOS mismatch has occurred. The initial values for the minimum and maximum internal registers must be defined by the user, at Address 0x8C and Address 0x8B, respectively (see the Register Map section).

DOS is indicated by a logic low on the DOS pin. When DOS is indicated, the output is latched low until the user enters configuration mode and reads the fault register. The DOS condition has priority over the LOT condition, as shown in Table 6. To determine the cause of the DOS fault detection, the user must read the fault register, Address 0xFF (see the Register Map section).

Time Latency for LOS and DOS Detection

Note that the monitor signal is generated on the active edge of the internal AD2S1210 clock. The internal clock is generated by dividing the externally applied CLKIN frequency by 2; for example, when using a CLKIN frequency of 8.192 MHz the internal AD2S1210 clock is 4.096 MHz. The AD2S1210 continuously stores the minimum and maximum magnitude of the monitor signal in internal registers. The values stored in these internal registers are compared to the LOS and DOS thresholds configured by the user at set intervals. This interval, known as the window counter period, is dependent on the excitation frequency configured by the user. It is set to ensure that two window counter periods include at least one full period of the excitation frequency applied to the resolver. The window counter period is defined in terms of internal clock cycles. The window counter periods for the range of excitation frequencies on the AD2S1210 are outlined in Table 5.

Table 5. Window Counter Period vs. Excitation Frequency Range, CLKIN = 8.192 MHz

Excitation Frequency Range	Number of Internal Clock Cycles	Window Counter Period (µs)[1]
2 kHz ≤ Exc Freq < 4 kHz	1065	260
4 kHz ≤ Exc Freq < 8 kHz	554	135.25
8 kHz ≤ Exc Freq ≤ 20 kHz	256	62.5

[1] CLKIN = 8.192 MHz. The window counter period scales with clock frequency and can be calculated by multiplying the number of internal clock cycles by the period of the internal clock frequency, that is, CLKIN/2.

The AD2S1210 detects an LOS or DOS due to the resolver inputs (sine or cosine) falling below or exceeding the LOS and DOS thresholds within two window counter periods. For example, with an excitation frequency of 10 kHz, a fault is detected within 125 µs. A persistent fault is detected within one window counter period of the reading and clearing the fault register.

Note that the time latency to detect the occurrence of a DOS mismatch fault is dependent on the speed of rotation of the resolver. The worst-case time latency to detect a DOS mismatch fault is the time required for one full rotation of the resolver.

Loss of Position Tracking Detection

The AD2S1210 indicates that a loss of tracking (LOT) has occurred when

- The internal error signal of the AD2S1210 has exceeded the specified angular threshold. This threshold is defined by the user and is set by writing to the internal register, Address 0x8D (see the Register Map section).
- The input signal exceeds the maximum tracking rate. The maximum tracking rate depends on the resolution defined by the user and the CLKIN frequency.

LOT is indicated by a logic low on the LOT pin and is not latched. LOT has hysteresis and is not cleared until the internal error signal is less than the value defined in the LOT low threshold register, Address 0x8E (see the Register Map section).

When the maximum tracking rate is exceeded, LOT is cleared only if the velocity is less than the maximum tracking rate and the internal error signal is less than the value defined in the LOT low threshold register. LOT can be indicated for step changes in position (such as after a $\overline{\text{RESET}}$ signal is applied to the AD2S1210). It is also useful as a built-in test to indicate that the tracking converter is functioning properly. The LOT condition has lower priority than both the DOS and LOS conditions, as shown in Table 6. The LOT and DOS conditions cannot be indicated using the LOT and DOS pins at the same time. However, both conditions are indicated separately in the fault register. To determine the cause of the LOT fault detection, the user must read the fault register, Address 0xFF (see the Register Map section).

Table 6. Fault Detection Decoding

Condition	DOS Pin	LOT Pin	Order of Priority
Loss of Signal (LOS)	0	0	1
Degradation of Signal (DOS)	0	1	2
Loss of Tracking (LOT)	1	0	3
No Fault	1	1	N/A

Sine/Cosine Input Clipping

The AD2S1210 indicates that a clipping error has occurred if any of the resolver input pins (SIN, SINLO, COS, or COSLO) are clipping the power rail or ground rail of the AD2S1210. The clipping fault is indicated if the input amplitudes are less than 0.15 V or greater then AV_{DD} – 0.2 V for more than 4 µs.

Sine/cosine input clipping error is indicated by both the DOS and LOT pins latching as logic low outputs. Sine/cosine input clipping error is also indicated by Bit D7 of the fault register being set high. The DOS and LOT pins are reset to a no fault state when the user enters configuration mode and reads the fault register.

Configuration Parity Error

The AD2S1210 includes a number of user programmable registers that allow the user to configure the part. Each read/write register on the AD2S1210 is programmed with seven bits of information by the user. The 8th bit is reserved as a parity error bit. In the event that the data within these registers becomes corrupted, the AD2S1210 indicates that a configuration parity error has occurred. Configuration parity error is indicated by both the DOS and LOT pins latching as logic low outputs. Configuration parity error is also indicated by Bit D0 of the fault register being set high. In the event that a parity error occurs, it is recommended that the user reset the part using the $\overline{\text{RESET}}$ pin.

Phase Lock Error

The AD2S1210 indicates that a phase lock error has occurred if the difference between the phase of the excitation frequency and the phase of the sine and cosine signals exceeds the specified phase lock range. Phase lock error is indicated by a logic low on the LOT pin and is not latched. Phase lock error is also indicated by Bit D1 of the fault register being set high.

ON-BOARD PROGRAMMABLE SINUSOIDAL OSCILLATOR

An on-board oscillator provides the sinusoidal excitation signal (EXC) to the resolver as well as its complemented signal ($\overline{\text{EXC}}$). The frequency of this reference signal is programmable to a number of standard frequencies between 2 kHz and 20 kHz. The amplitude of this signal is 3.6 V p-p and is centered on 2.5 V.

The reference excitation output of the AD2S1210 needs an external buffer amplifier to provide gain and the additional current to drive a resolver.

The AD2S1210 also provides an internal synthetic reference signal that is phase locked to its sine and cosine inputs. Phase errors between the resolver primary and secondary windings can degrade the accuracy of the RDC and are compensated by this synchronous reference signal. This also compensates the phase shifts due to temperature and cabling and eliminates the need of an external preset phase compensation circuit.

SYNTHETIC REFERENCE GENERATION

When a resolver undergoes a high rotation rate, the RDC tends to act as an electric motor and produces speed voltages, along with the ideal sine and cosine outputs. These speed voltages are in quadrature to the main signal waveform. Moreover, nonzero resistance in the resolver windings causes a nonzero phase shift between the reference input and the sine and cosine outputs. The combination of speed voltages and phase shift causes a tracking error in the RDC that is approximated by

$$Error = Phase\ Shift \times \frac{Rotation\ Rate}{Reference\ Frequency} \quad (6)$$

To compensate for the described phase error between the resolver reference excitation and the sine/cosine signals, an internal synthetic reference signal is generated in phase with the reference frequency carrier. The synthetic reference is derived using the internally filtered sine and cosine signals. It is generated by determining the zero crossing of either the sine or cosine (whichever signal is larger, to improve phase accuracy) and evaluating the phase of the resolver reference excitation. The synthetic reference reduces the phase shift between the reference and sine/cosine inputs to less than 10°, and operates for phase shifts of ±44°. If additional phase lock range is required, Bit D5 in the control register can be set to zero to expand the phase lock range to 360° (see the Control Register section).

CONNECTING THE CONVERTER

Ground is connected to the AGND and DGND pins (see Figure 26). A positive power supply (V_{DD}) of 5 V dc ± 5% is connected to the AV_{DD} and DV_{DD} pins, with typical values for the decoupling capacitors being 10 nF and 4.7 µF. These capacitors are then placed as close to the device pins as possible and are connected to both AV_{DD} and DV_{DD}. The V_{DRIVE} pin is connected to the supply voltage of the microprocessor. The voltage applied to the V_{DRIVE} input controls the voltage of the parallel and serial interfaces. V_{DRIVE} can be set to 5 V, 3 V, or 2.5 V. Typical values for the V_{DRIVE} decoupling capacitors are 10 nF and 4.7 µF. Typical values for the oscillator decoupling capacitors are 20 pF, whereas typical values for the reference decoupling capacitors are 10 nF and 10 µF.

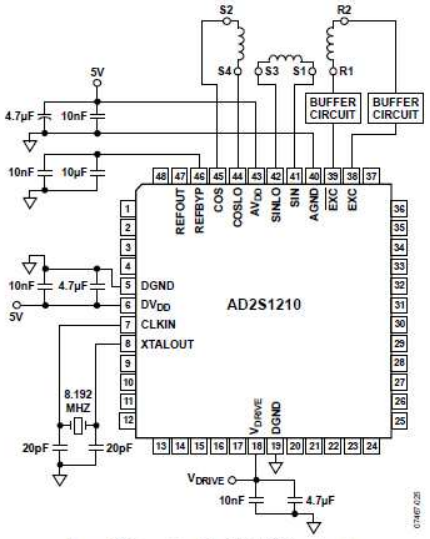


Figure 26. Connecting the AD2S1210 to a Resolver

In this recommended configuration, the converter introduces a $V_{REF}/2$ offset in the SIN, SINLO, COS, and COSLO signal outputs from the resolver. The sine and cosine signals can each be connected to a different potential relative to ground if the sine and cosine signals adhere to the recommended specifications. Note that because the EXC and $\overline{EXC}$ outputs are differential, there is an inherent gain of 2×.

Figure 27 shows a suggested buffer circuit. Capacitor C1 may be used in parallel with Resistor R2 to filter out any noise that may exist on the EXC and $\overline{EXC}$ outputs. Care should be taken when selecting the cutoff frequency of this filter to ensure that phase shifts of the carrier caused by the filter do not exceed the phase lock range of the AD2S1210.

The gain of the circuit is

$$Carrier\ Gain = -(R2/R1)\times(1/(1+R2\times C1\times\omega)) \quad (7)$$

and

$$V_{OUT} = \left(V_{REF}\times\left(1+\frac{R2}{R1}\right)\right)-\left(\frac{R2}{R1}\right)\times\left(\frac{1}{1+R2\times C1\times\omega}\right)V_{IN} \quad (8)$$

where:

ω is the radian frequency of the applied signal.

V_{REF}, a dc voltage, is set so that V_{OUT} is always a positive value, eliminating the need for a negative supply.

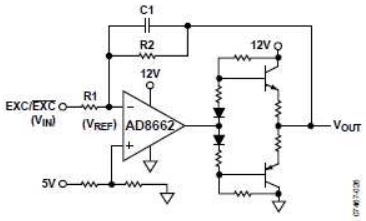


Figure 27. Buffer Circuit

A separate screened twisted pair cable is recommended for the analog input pins, SIN, SINLO, COS, and COSLO. The screens should terminate to either REFOUT or AGND.

CONFIGURATION OF AD2S1210

MODES OF OPERATION

The AD2S1210 has two modes of operation: configuration mode and normal mode. The configuration mode is used to program the registers that set the excitation frequency, the resolution, and the fault detection thresholds of the AD2S1210. Configuration mode is also used to read back the information in the fault register. The data in the position and velocity registers can also be read back while in configuration mode. The AD2S1210 can be operated entirely in configuration mode or, when the initial configuration is completed, the part can be taken out of configuration mode and operated in normal mode. When operating in normal mode, the data outputs can provide angular position or angular velocity data. The A0 and A1 inputs are used to determine whether the AD2S1210 is in configuration mode and to determine whether the position or velocity data is supplied to the output pins, see Table 8.

Setting the Excitation Frequency

The excitation frequency of the AD2S1210 is set by writing a frequency control word to the excitation frequency register, Address 0x91 (see the Register Map section).

$$Excitation\ Frequency = \frac{(FCW \times f_{CLKIN})}{2^{15}}$$

where *FCW* is the frequency control word and f_{CLKIN} is the clock frequency of the AD2S1210.

The specified range of the excitation frequency is from 2 kHz to 20 kHz and can be set in increments of 250 Hz. To achieve the angular accuracy specifications in Table 1, the excitation frequency should be selected as outlined in Table 7.

Table 7. Recommended Excitation Frequency vs. Resolution (f_{CLKIN} = 8.192 MHz)

Resolution	Typical Bandwidth	Min Excitation Frequency	Max Excitation Frequency
10 Bits	4100 Hz	10 kHz	20 kHz
12 Bits	1700 Hz	6 kHz	20 kHz
14 Bits	900 Hz	3 kHz	12 kHz
16 Bits	250 Hz	2 kHz	10 kHz

Note that the recommended frequency range for each resolution and bandwidth, as outlined in Table 7, are defined for a clock frequency of 8.192 MHz. The recommended excitation frequency range scales with the clock frequency of the AD2S1210. The default excitation frequency of the AD2S1210 is 10 kHz when operated with a clock frequency of 8.192 MHz.

A0, A1 Inputs

The AD2S1210 allows the user to read the angular position or the angular velocity data directly from the parallel outputs or through the serial interface. The required information can be selected using the A0 and A1 inputs. These inputs should also be used to put the part into configuration mode. The data from the fault register and the remaining on-chip registers can be accessed in configuration mode.

Table 8. Configuration Mode Settings

A0	A1	Result
0	0	Normal mode—position output
0	1	Normal mode—velocity output
1	0	Reserved
1	1	Configuration mode

RES0, RES1 Inputs

In normal mode, the resolution of the digital output is selected using the RES0 and RES1 input pins. In configuration mode, the resolution is selected by setting the RES0 and RES1 bits in the control register. When switching between normal mode and configuration mode, it is the responsibility of the user to ensure that the resolution set in the control register matches the resolution set by the RES0 and RES1 input pins. Failure to do so may result in incorrect data on the outputs, caused by the differences between the resolution settings.

Table 9. Resolution Settings

RES0	RES1	Resolution (Bits)	Position LSB (Arc min)	Velocity LSB (rps)[1]
0	0	10	21.1	4.88
0	1	12	5.3	0.488
1	0	14	1.3	0.06
1	1	16	0.3	0.004

[1] CLKIN = 8.192 MHz. The velocity LSB size and maximum tracking rate scale linearly with the CLKIN frequency.

REGISTER MAP

Table 10. Register Map

Register Name	Register Address	Register Data	Read/Write Register
Position	0x80	D15 to D8	Read only
	0x81	D7 to D0	Read only
Velocity	0x82	D15 to D8	Read only
	0x83	D7 to D0	Read only
LOS Threshold	0x88	D7 to D0	Read/write
DOS Overrange Threshold	0x89	D7 to D0	Read/write
DOS Mismatch Threshold	0x8A	D7 to D0	Read/write
DOS Reset Max Threshold	0x8B	D7 to D0	Read/write
DOS Reset Min Threshold	0x8C	D7 to D0	Read/write
LOT High Threshold	0x8D	D7 to D0	Read/write
LOT Low Threshold	0x8E	D7 to D0	Read/write
Excitation Frequency	0x91	D7 to D0	Read/write
Control	0x92	D7 to D0	Read/write
Soft Reset	0xF0	D7 to D0	Write only
Fault	0xFF	D7 to D0	Read only

POSITION REGISTER

Table 11. 16-Bit Register

Address	Bit	Read/Write
0x80	D15 to D8	Read only
0x81	D7 to D0	Read only

The position register contains a digital representation of the angular position of the resolver input signals. The values are stored in 16-bit binary format. The value in the position register is updated following a falling edge on the $\overline{\text{SAMPLE}}$ input.

Note that with hysteresis enabled (see the Control Register section), at lower resolutions, the LSBs of the 16-bit digital output are set to zero. For example, at 10-bit resolution, Data Bit D15 to Data Bit D6 provide valid data; D5 to D0 are set to zero. With hysteresis disabled, the value stored in the position register is 16 bits regardless of resolution. At lower resolutions, the LSBs of the 16-bit digital output can be ignored. For example, at 10-bit resolution, Data Bit D15 to Data Bit D6 provide valid data; D5 to D0 can be ignored.

VELOCITY REGISTER

Table 12. 16-Bit Register

Address	Bit	Read/Write
0x82	D15 to D8	Read only
0x83	D7 to D0	Read only

The velocity register contains a digital representation of the angular velocity of the resolver input signals. The value in the velocity register is updated following a falling edge on the sample input. The values are stored in 16-bit, twos complement format. The maximum velocity that the AD2S1210 can track for each resolution is specified in Table 1. For example, the maximum tracking rate of the AD2S1210 at 16 bits resolution, with an 8.192 MHz input clock, is ±125 rps. A velocity of +125 rps results in 0x7FFF being stored in the velocity register; a velocity of −125 rps results in 0x8000 being stored in the velocity register.

The value stored in the velocity register is 16 bits regardless of resolution. At lower resolutions, the LSBs of the 16-bit digital output should be ignored. For example, at 10-bit resolution, Data Bit D15 to Data Bit D6 provide valid data; D5 to D0 should be ignored. The maximum tracking rate of the AD2S1210 at 10-bit resolution with an 8.192 MHz input clock is ±2500 rps. A velocity of +2500 rps results in 0x1FF being stored in Bit D15 to Bit D6 of the velocity register; a velocity of −2500 rps results in 0x3FF being stored in Bit D15 to Bit D6 of the velocity register. In this 10-bit example, the LSB size of the velocity output is 4.88 rps.

LOS THRESHOLD REGISTER

Table 13. 8-Bit Register

Address	Bit	Read/Write
0x88	D7 to D0	Read/write

The LOS threshold register determines the loss of signal threshold of the AD2S1210. The AD2S1210 allows the user to set the LOS threshold to a value between 0 V and 4.82 V. The resolution of the LOS threshold is seven bits, that is, 38 mV. Note that the MSB, D7, should be set to 0. The default value of the LOS threshold on power-up is 2.2 V.

DOS OVERRANGE THRESHOLD REGISTER

Table 14. 8-Bit Register

Address	Bit	Read/Write
0x89	D7 to D0	Read/write

The DOS overrange threshold register determines the degradation of signal threshold of the AD2S1210. The AD2S1210 allows the user to set the DOS overrange threshold to a value between 0 V and 4.82 V. The resolution of the DOS overrange threshold is seven bits, that is, 38 mV. Note that the MSB, D7, should be set to 0. The default value of the DOS overrange threshold on power-up is 4.1 V.

DOS MISMATCH THRESHOLD REGISTER

Table 15. 8-Bit Register

Address	Bit	Read/Write
0x8A	D7 to D0	Read/write

The DOS mismatch threshold register determines the signal mismatch threshold of the AD2S1210. The AD2S1210 allows the user to set the DOS mismatch threshold to a value between 0 V and 4.82 V. The resolution of the DOS mismatch threshold is seven bits, that is, 38 mV. Note that the MSB, D7, should be set to 0.The default value of the DOS mismatch threshold on power-up is 380 mV.

DOS RESET MAXIMUM AND MINIMUM THRESHOLD REGISTERS

Table 16. 8-Bit Registers

Address	Bit	Read/Write
0x8B	D7 to D0	Read/write
0x8C	D7 to D0	Read/write

The AD2S1210 continuously stores the minimum and maximum magnitude of the monitor signal in internal registers. The difference between the minimum and maximum is calculated to determine if a DOS mismatch has occurred. The initial values for the minimum and maximum internal registers must be defined by the user. When the fault register is cleared, the registers that store the maximum and minimum amplitudes of the monitor signal are reset to the values stored in the DOS reset maximum and minimum threshold registers. The resolution of the DOS reset maximum and minimum thresholds is seven bits each, that is, 38 mV. Note that the MSB, D7, should be set to 0.To ensure correct operation, it is recommended that the DOS reset minimum threshold register be set to at least 1 LSB less than the DOS overrange threshold, and the DOS reset maximum threshold register be set to at least 1 LSB greater than the LOS threshold register. The default value of the DOS reset minimum threshold register and the DOS reset maximum threshold register are 3.99 V and 2.28 V, respectively.

LOT HIGH THRESHOLD REGISTER

Table 17. 8-Bit Register

Address	Bit	Read/Write
0x8D	D7 to D0	Read/write

The LOT high threshold register determines the loss of position tracking threshold for the AD2S1210. The LOT high threshold is a 7-bit word. Note that the MSB, D7, should be set to 0. The range of the LOT high threshold, the LSB size, and the default value of the LOT high threshold on power-up are dependent on the resolution setting of the AD2S1210, and are outlined in Table 19.

LOT LOW THRESHOLD REGISTER

Table 18. 8-Bit Register

Address	Bit	Read/Write
0x8E	D7 to D0	Read/write

The LOT low threshold register determines the level of hysteresis on the loss of position tracking fault detection. Loss of tracking (LOT) occurs when the internal error signal of the AD2S1210 exceeds the LOT high threshold. LOT has hysteresis and is not cleared until the internal error signal is less than the value defined in the LOT low threshold register. The LOT low threshold is a 7-bit word. Note that the MSB, D7, should be set to 0. The range of the LOT high threshold, the LSB size, and the default value of the LOT high threshold on power-up are dependent on the resolution setting of the AD2S1210, and are outlined in Table 19.

Table 19. LOT High/Low Threshold

Resolution (Bits)	Range (Degrees)	LSB Size (Degrees)	LOT Low Default (Degrees)	LOT High Default (Degrees)
10	0 to 45	0.35	2.5	12.5
12	0 to 18	0.14	1.0	5.0
14	0 to 9	0.09	0.5	2.5
16	0 to 9	0.09	0.5	2.5

EXCITATION FREQUENCY REGISTER

Table 20. 8-Bit Register

Address	Bit	Read/Write
0x91	D7 to D0	Read/write

The excitation frequency register determines the frequency of the excitation outputs of the AD2S1210. A 7-bit frequency control word is written to the register to set the excitation frequency. Note that the MSB, D7, should be set to 0.

$$FCW = \frac{\left(Excitation\ Frequency \times 2^{15}\right)}{f_{CLKIN}} \quad (9)$$

where FCW is the frequency control word and f_{CLKIN} is the clock frequency of the AD2S1210. The specified range of the excitation frequency is from 2 kHz to 20 kHz and can be set in increments of 250 Hz. To ensure that the AD2S1210 is operated within the specified frequency range, the frequency control word should be a value between 0x4 and 0x50.

For example, if the user requires an excitation frequency of 5 kHz and has an 8.192 MHz clock frequency, the code that needs to be programmed is given by

$$FCW = \frac{\left(5\ \text{kHz} \times 2^{15}\right)}{8.192\ \text{MHz}} = 14\ \text{(hexadecimal)}$$

The default excitation frequency of the AD2S1210 on power-up is 10 kHz.

CONTROL REGISTER

Table 21. 8-Bit Register

Address	Bit	Read/Write
0x92	D7 to D0	Read/write

The control register is an 8-bit register that sets the AD2S1210 control modes. The default value of the control register on power-up is 0x7E.

Table 22. Control Register Bit Descriptions

Bit	Description
D7	Address/data bit
D6	Reserved; set to 1
D5	Phase lock range 0 = 360°, 1 = ±44°
D4	0 = disable hysteresis, 1 = enable hysteresis
D3	Set Encoder Resolution EnRES1
D2	Set Encoder Resolution EnRES0
D1	Set Resolution RES1
D0	Set Resolution RES0

Address/Data Bit

The MSB of each 8-bit word written to the AD2S1210 indicates whether the 8-bit word is a register address or data. The MSB (D7) of each register address defined on the AD2S1210 is high. The MSB of each data word written to the AD2S1210 is low.

Note that when a data word is written to the AD2S1210, the MSB is internally reconfigured as a parity bit. When reading data from any of the read/write registers (see Table 10), the parity of Bit D6 to Bit D0 is recalculated and compared to the previously stored parity bit. The MSB of the 8-bit output is used to indicate whether a configuration error has occurred. If the MSB is returned high, this indicates that the data read back from the device does not match the configuration data written to the device in the previous write cycle.

Phase Lock Range

The phase lock range allows the AD2S1210 to compensate for phase errors between the excitation frequency and the sine/cosine inputs. The recommended mode of operation is to use the default phase lock range of ±44°. If additional phase lock range is required, a range of 360° can be set. However, in this mode of operation, the AD2S1210 should be reset following a loss of signal error. Failure to do so may result in a 180° error in the angular output data.

Hysteresis

The AD2S1210 includes a hysteresis function, ±1 LSB, between the output of the position integrator and the input to the position register. When operating in a noisy environment, this can be used to prevent flicker on the LSB. On the AD2S1210, the maximum tracking rate is defined by the bandwidth. Each resolution setting is internally configured with a different bandwidth, as outlined in Table 1. The maximum tracking rate and the bandwidth are inversely proportional to the resolution, that is, the maximum tracking rate increases as the resolution is decreased. The option of disabling the hysteresis allows the user to oversample the position output and to achieve a higher resolution output within the specified bandwidths through external averaging.

The hysteresis function can be enabled or disabled through setting Bit D4 in the control register. Hysteresis is enabled by default on power-up.

Set Encoder Resolution

The resolution of the encoder outputs of the AD2S1210 can be set to the same resolution as the digital output or it can also be set to a lower resolution. For example, when the resolution of the AD2S1210 position outputs is set to 16 bits, the resolution of the encoder outputs may be set to 14, 12, or 10 bits. This allows the user to take advantage of the lower bandwidth and improved performance of the 16-bit resolution setting without requiring external divide down of the A-quad-B encoder outputs. The default resolution of the encoder outputs on power-up is 16 bits. Refer to the Incremental Encoder Outputs section.

Table 23. Encoder Resolution Settings

EnRES0	EnRES1	Resolution (Bits)
0	0	10
0	1	12
1	0	14
1	1	16

Set Resolution

In normal mode, the resolution of the digital output is selected using the RES0 and RES1 input pins (see Table 9). In configuration mode, the resolution is selected by setting the RES0 and RES1 bits in the control register. When switching between normal mode and configuration mode, it is the responsibility of the user to ensure that the resolution set in the control register matches the resolution set by the RES0 and RES1 input pins. The default resolution of the digital output on power-up is 12 bits.

SOFTWARE RESET REGISTER

Table 24. 8-Bit Register

Address	Bit	Read/Write
0xF0	D7 to D0	Write only

Addressing the software reset register, that is writing the 8-bit address, 0xF0, of the software reset register to the AD2S1210 while in configuration mode, allows the user to initiate a software reset of the AD2S1210. The software reset reinitializes the excitation frequency outputs and the internal Type II tracking loop. The data stored in the configuration registers is not overwritten by a software reset. However, it should be noted that the data in the fault register is reset. In an application that uses two or more resolver-to-digital converters, which are both driven from the same clock source, the software reset can be used to synchronize the phase of the excitation frequencies across the converters.

FAULT REGISTER

Table 25. 8-Bit Register

Address	Bit	Read/Write
0xFF	D7 to D0	Read only

The AD2S1210 has the ability to detect eight separate fault conditions. When a fault occurs, the DOS and/or the LOT output pins are taken low. By reading the fault register, the user can determine the cause of the triggering of the fault detection output pins. Note that the fault register bits are active high, that is, the fault bits are taken high to indicate that a fault has occurred.

Table 26. Fault Register Bit Descriptions

Bit	Description
D7	Sine/cosine inputs clipped
D6	Sine/cosine inputs below LOS threshold
D5	Sine/cosine inputs exceed DOS overrange threshold
D4	Sine/cosine inputs exceed DOS mismatch threshold
D3	Tracking error exceeds LOT threshold
D2	Velocity exceeds maximum tracking rate
D1	Phase error exceeds phase lock range
D0	Configuration parity error

DIGITAL INTERFACE

The angular position and angular velocity are represented by binary data and can be extracted either via a 16-bit parallel interface or via a 4-wire serial interface that operates at clock rates of up to 25 MHz. The AD2S1210 programmable functions are controlled using a set of on-chip registers. Data is written to these registers using either the serial or the parallel interface.

SOE INPUT

The serial output enable pin, $\overline{SOE}$, is held high to enable the parallel interface. The $\overline{SOE}$ pin is held low to enable the serial interface, which places Pin DB0 to Pin DB12 in the high impedance state. Pin DB13 is the serial clock input (SCLK), Pin DB14 is the serial data input (SDI), Pin DB15 is the serial data output (SDO), and $\overline{WR}/\overline{FSYNC}$ is the frame synchronization input.

SAMPLE INPUT

The AD2S1210 operates on a Type II tracking closed-loop principle. The loop continually tracks the position and velocity of the resolver without the need for external conversion and wait states. The position and velocity registers are external to the loop and are updated with a high-to-low transition of the $\overline{SAMPLE}$ signal. This pin must be held low for at least t_{16} ns to guarantee correct latching of the data.

DATA FORMAT

The digital angle data represents the absolute position of the resolver shaft as a 10-bit to 16-bit unsigned binary word. The digital velocity data is a 10-bit to 16-bit twos complement word, which represents the velocity of the resolver shaft rotating in either a clockwise or a counterclockwise direction.

PARALLEL INTERFACE

The parallel interface is selected holding the $\overline{SOE}$ pin high. The chip select pin, $\overline{CS}$, must be held low to enable the interface.

Writing to the AD2S1210

The on-chip registers of the AD2S1210 are written to, in parallel mode, using an 8-bit parallel interface, D7 to D0, and the $\overline{WR}/\overline{FSYNC}$ pin. The MSB of each 8-bit word written to the AD2S1210 indicates whether the 8-bit word is a register address or data. The MSB (D7) of each register address defined on the AD2S1210 is high (see the Register Map section). The MSB of each data word written to the AD2S1210 is low. To write to one of the registers, the user must first place the AD2S1210 into configuration mode using the A0 and A1 inputs. Then the 8-bit address should be written to the AD2S1210 using Pin DB7 to Pin DB0, and latched using the rising edge of the $\overline{WR}/\overline{FSYNC}$ input. The data can then be presented on Pin DB7 to Pin DB0 and again latched into the part using the $\overline{WR}/\overline{FSYNC}$ input. Figure 28 shows the timing specifications to follow when writng to the configuration registers. Note that the $\overline{RD}$ input should be held high when writing to the AD2S1210.

Reading from the AD2S1210

The following data can be read back from the AD2S1210:

- Angular position
- Angular velocity
- Fault register data
- Status of on-chip registers

The angular position and angular velocity data can be read back in either normal mode or configuration mode. To read the status of the fault register or the remaining on-chip registers, the part must be put into configuration mode.

Reading from the AD2S1210 in Configuration Mode

To read back data stored in one of the on-chip registers, including the fault register, the user must first place the AD2S1210 into configuration mode using the A0 and A1 inputs. The 8-bit address of the register to be read should then be written to the part, as described in the Writing to the AD2S1210 section. This transfers the relevant data to the output register. The data can then be read using the $\overline{RD}$ input as described previously. When reading back data from any of the read/write registers (see Table 10), the 8-bit word consists of the seven bits of data in the relevant register, D6 to D0, and an error bit, D7. If the error bit is returned high, this indicates that the data read back from the device does not match the configuration data written to the device in the previous write cycle.

If the user wants to read back the angular position or velocity data while in configuration mode, a falling edge of the $\overline{SAMPLE}$ input is required to update the information in the position and velocity registers. The data in these registers can then be read back by addressing the required register and reading back the data as described previously. Figure 29 shows the timing specifications to follow when reading from the configuration registers.

Reading from the AD2S1210 in Normal Mode

To read back position or velocity data from the AD2S1210, the information stored in the position and velocity registers should first be updated using the $\overline{SAMPLE}$ input. A high-to-low transition on the $\overline{SAMPLE}$ input transfers the data from the position and velocity integrators to the position and velocity registers. The fault register is also updated on the high-to-low transition of the $\overline{SAMPLE}$ input. The status of the A0 and A1 inputs determines whether the position or velocity data is transferred to the output register. The $\overline{CS}$ pin must be held low to transfer the selected data to the output register. Finally, the $\overline{RD}$ input is used to read the data from the output register and to enable the output buffer. The output buffer is enabled when $\overline{CS}$ and $\overline{RD}$ are held low. The data pins return to a high impedance state when $\overline{RD}$ returns to a high state. If the user is reading data continuously, $\overline{RD}$ can be reapplied a minimum of t_{20} ns after it was released.

The timing requirements for the read cycle are shown in Figure 30. Note that the $\overline{WR}/\overline{FSYNC}$ input should be high when $\overline{RD}$ is low.

Clearing the Fault Register

The LOT pin and/or the DOS pin of the AD2S1210 are taken low to indicate that a fault has been detected. The AD2S1210 is capable of detecting eight separate fault conditions. To determine which condition triggered the fault indication, the user is required to enter configuration mode and read the fault register. To reset the fault indicators, an additional $\overline{\text{SAMPLE}}$ pulse is required. This ensures that any faults that may occur between the initial sampling and subsequent reading of the fault register are captured. Therefore, to read and clear the fault register, the following sequence of events is required:

1. A high-to-low transition of the $\overline{\text{SAMPLE}}$ input.
2. The $\overline{\text{SAMPLE}}$ input should be held low for t_{16} ns and then can be returned high.
3. The AD2S1210 should be put into configuration mode, that is, A0 and A1 are both set to logic high.
4. The fault register should be read as described in the Reading from the AD2S1210 in Configuration Mode section.
5. A second high-to-low transition of the $\overline{\text{SAMPLE}}$ input clears the fault indications on the DOS and/or LOT pins.
6. Note that in the event of a persistent fault, the fault indicators are reasserted within the specified fault time latency.

Figure 31 shows the timing specifications to follow when clearing the fault register.

Note that the last valid register address written to the AD2S1210 prior to exiting configuration mode is again valid when reentering configuration mode. It is therefore recommended that when initial configuration of the AD2S1210 is complete, the fault address should be written to the AD2S1210 before leaving configuration mode. This simplifies the reading and clearing of the fault register in normal operation because it is now possible to access the position, velocity, and fault information by toggling the A0 and A1 pins without requiring additional register addressing.

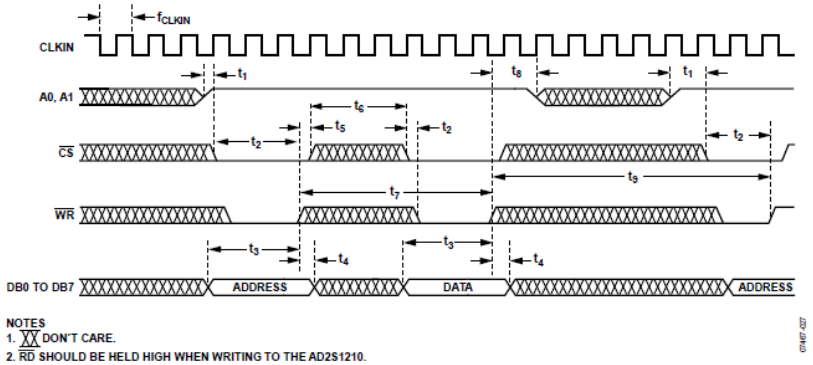


Figure 28. Parallel Port Write Timing—Configuration Mode

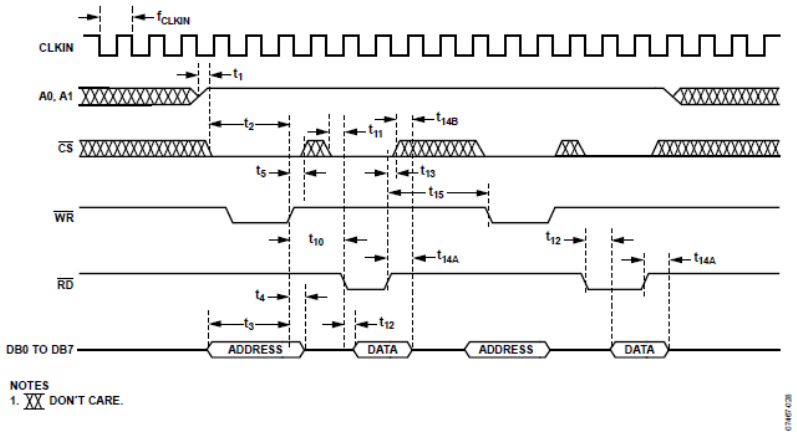


Figure 29. Parallel Port Read Timing—Configuration Mode

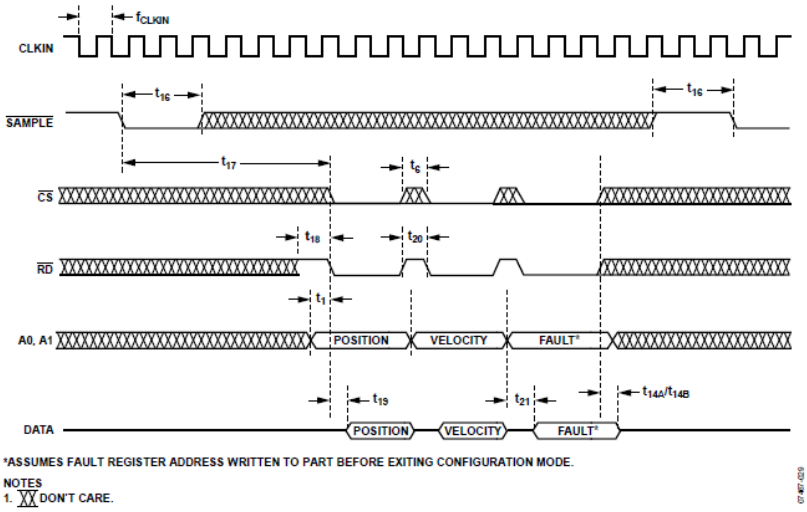


Figure 30. Parallel Port Read Timing

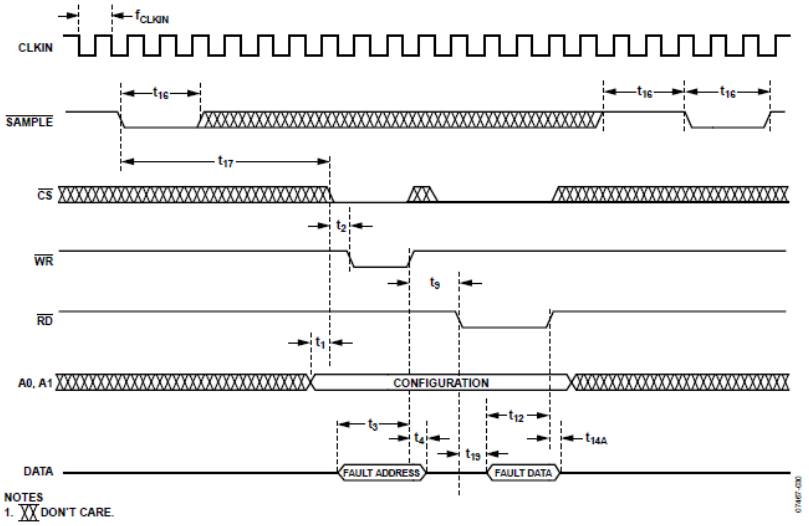


Figure 31. Parallel Port—Clear Fault Register

SERIAL INTERFACE

The serial interface is selected by holding the $\overline{SOE}$ pin low. The AD2S1210 serial interface consists of four signals: SDO, SDI, $\overline{WR}/\overline{FSYNC}$, and SCLK. The SDI is used for transferring data into the on-chip registers whereas the SDO is used for accessing data from the on-chip registers, including the position, velocity, and fault registers. SCLK is the serial clock input for the device, and all data transfers (either on SDI or SDO) take place with respect to this SCLK signal. $\overline{WR}/\overline{FSYNC}$ is used to frame the data. The falling edge of $\overline{WR}/\overline{FSYNC}$ takes the SDI and SDO lines out of a high impedance state. A rising edge on $\overline{WR}/\overline{FSYNC}$ returns the SDI and SDO to a high impedance state. The $\overline{CS}$ input is not required for the serial interface and should be held low.

SDO Output

In normal mode of operation, data is shifted out of the device as a 24-bit word under the control of the serial clock input, SCLK. The data is shifted out on the rising edge of SCLK. The timing diagram for this operation is shown in Figure 32.

SDI Input

The SDI input is used to address the on-chip registers and as a daisy-chain input in configuration mode. The data is shifted into the part on the falling edge of SCLK. The timing diagram for this operation is shown in Figure 32.

Writing to the AD2S1210

The on-chip registers of the AD2S1210 can be accessed using the serial interface. To write to one of the registers, the user must first place the AD2S1210 into configuration mode using the A0 and A1 inputs. The 8-bit address should be written to the AD2S1210 using the SDI pin and latched using the rising edge of the $\overline{WR}/\overline{FSYNC}$ input. The data can then be presented on the SDI pin and again latched into the part using the $\overline{WR}/\overline{FSYNC}$ input. The MSB of the 8-bit write indicates whether the 8-bit word is a register address, MSB set high, or the data to be written, MSB set low. Figure 33 shows the timing specifications to follow when writing to the configuration registers.

Reading from the AD2S1210 in Configuration Mode

To read back data stored in one of the on-chip registers, including the fault register, the user must first place the AD2S1210 into configuration mode using the A0 and A1 inputs. The 8-bit address of the register to be read should then be written to the part, as described in the Writing to the AD2S1210 section. This transfers the relevant data to the output register.

In configuration mode, the output shift register is eight bits wide. Data is shifted out of the device as an 8-bit word under the control of the serial clock input, SCLK. The timing diagram for this operation is shown in Figure 34. When reading back data from any of the read/write registers (see Table 10), the 8-bit word consists of the seven bits of data in the relevant register, D6 to D0, and an error bit, D7. If the error bit is returned high, this indicates that the data read back from the device does not match the configuration data written to the device in the previous write cycle.

To read back the angular position or velocity data while in configuration mode, a falling edge of the $\overline{SAMPLE}$ input is required to update the information in the position and velocity registers.

Reading from the AD2S1210 in Normal Mode

To read back position or velocity data from the AD2S1210, the information stored in the position and velocity registers should first be updated using the $\overline{SAMPLE}$ input. A high-to-low transition on the $\overline{SAMPLE}$ input transfers the data from the position and velocity integrators to the position and velocity registers. The fault register is also updated on the high-to-low transition of the $\overline{SAMPLE}$ input. The status of the A0 and A1 inputs determines whether the position or velocity data is transferred to the output register.

In normal mode, the output shift register is 24 bits wide. The 24-bit word consists of 16 bits of angular data (position or velocity data) followed by the 8-bit fault register data. Data is read out MSB first (Bit 23) on the SDO pin. Bit 23 through Bit 8 correspond to the angular information. The angular position data format is unsigned binary, with all 0s corresponding to 0 degrees and all 1s corresponding to 360 degrees – 1 LSB. The angular velocity data format is twos complement binary, with the MSB representing the rotation direction. Bit 7 through Bit 0 correspond to the fault information. If the user does not require the fault information, the $\overline{WR}/\overline{FSYNC}$ can be pulled high after the16th SCLK rising edge.

Clearing the Fault Register

The LOT pin and/or the DOS pin of the AD2S1210 are taken low to indicate that a fault has been detected. The AD2S1210 is capable of detecting eight separate fault conditions. To determine which condition triggered the fault indication, the user is required to enter configuration mode and read the fault register. To reset the fault indicators, an additional $\overline{SAMPLE}$ pulse is required. This ensures that any faults that may occur between the initial sampling and subsequent reading of the fault register are captured. Therefore, to read and clear the fault register, the following sequence of events is required:

1. A high-to-low transition of the $\overline{SAMPLE}$ input.
2. Hold the $\overline{SAMPLE}$ input low for t_{16} ns and then it can be returned high.
3. Put the AD2S1210 into configuration mode, that is, A0 and A1 are both set to logic high.
4. Read the fault register as described in the Reading from the AD2S1210 in Configuration Mode section.
5. A second high-to-low transition of the $\overline{SAMPLE}$ input clears the fault indications on the DOS and/or LOT pins. Note that in the event of a persistent fault, the fault indicators are reasserted within the specified fault time latency.

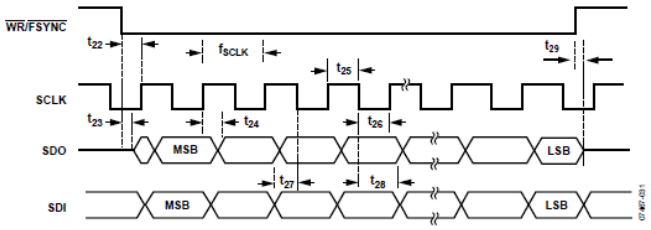


Figure 32. Serial Interface Timing Diagram

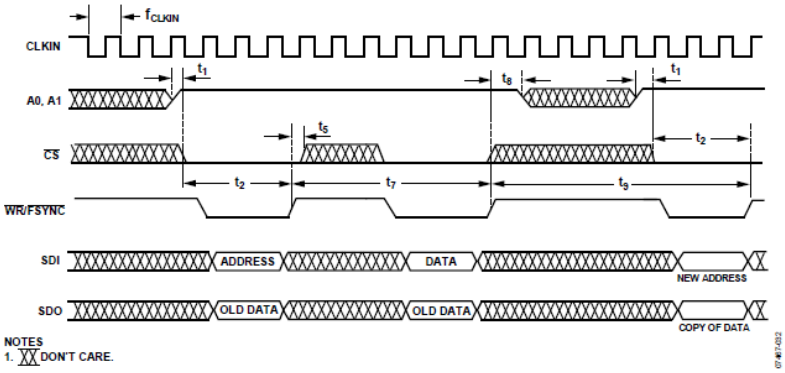


Figure 33. Serial Interface Write Timing—Configuration Mode

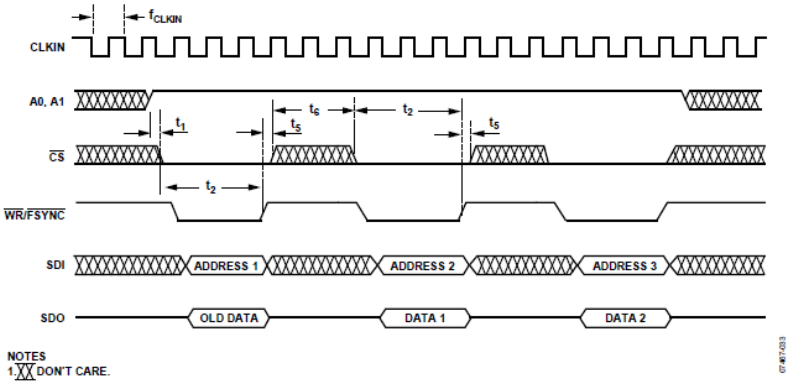
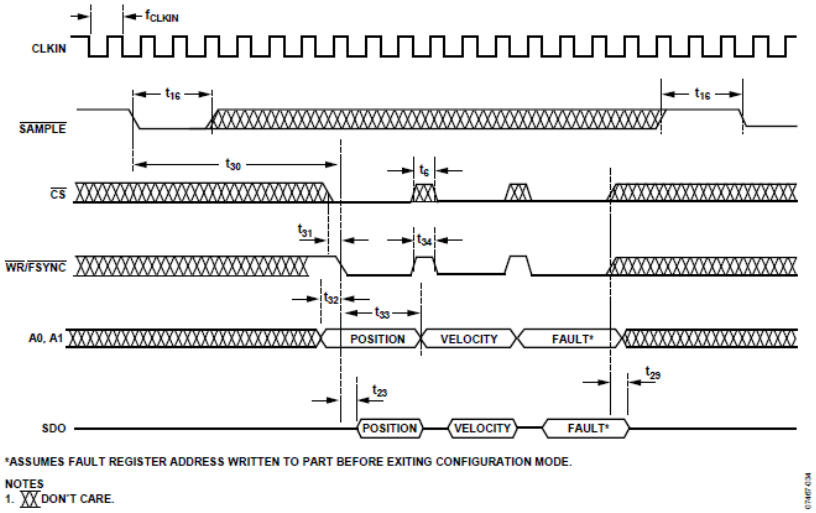


Figure 34. Serial Interface Read Timing—Configuration Mode



*ASSUMES FAULT REGISTER ADDRESS WRITTEN TO PART BEFORE EXITING CONFIGURATION MODE.

NOTES
1. XX DON'T CARE.

Figure 35. Serial Interface Read Timing

INCREMENTAL ENCODER OUTPUTS

The A, B, and NM incremental encoder emulation outputs are free running and are valid if the resolver format input signals applied to the converter are valid.

The AD2S1210 can be configured to emulate a 256-line, a 1024-line, a 4096-line, or a 16,384-line encoder. For example, if the AD2S1210 is configured for 12-bit resolution, one revolution produces 1024 A and B pulses. Pulse A leads Pulse B for increasing angular rotation (that is, clockwise direction).

The resolution of the encoder emulation outputs of the AD2S1210 is generally configured to match the resolution of the digital output. However, the encoder emulation outputs of the AD2S1210 can also be configured to have a lower resolution than the digital outputs. For example, if the AD2S1210 is configured for 16-bit resolution, then the encoder emulation outputs can also be configured for 14-bit, 12-bit, or 10-bit resolution. However, the resolution of the encoder emulation outputs cannot be higher than the resolution of the digital output. If the AD2S1210 is configured such that the resolution of the encoder emulation outputs is higher than the resolution of the digital outputs, the AD2S1210 internally overrides this configuration. In this event, the resolution of the encoder outputs is set to match the resolution of the digital outputs. The resolution of the encoder emulation outputs can be programmed by writing to Bit D3 and Bit D2 of the control register.

The north marker pulse is generated as the absolute angular position passes through zero. The north marker pulse width is set internally for 90° and is defined relative to the A cycle. Figure 36 details the relationship between A, B, and NM.

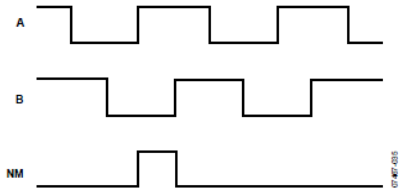


Figure 36. A, B, and NM Timing for Clockwise Rotation

The inclusion of A and B outputs allows the AD2S1210 with resolver solution to replace optical encoders directly without the need to change or upgrade existing application software.

SUPPLY SEQUENCING AND RESET

The AD2S1210 requires an external reset signal to hold the $\overline{\text{RESET}}$ input low until V_{DD} is within the specified operating range of 4.5 V to 5.5 V.

The $\overline{\text{RESET}}$ pin must be held low for a minimum of 10 µs after V_{DD} is within the specified range (shown as t_{RST} in Figure 37). Applying a $\overline{\text{RESET}}$ signal to the AD2S1210 initializes the output position to a value of 0x000 (degrees output through the parallel, serial, and encoder interfaces) and causes LOS to be indicated (LOT and DOS pins pulled low), as shown in Figure 37.

Failure to apply the correct power-up/reset sequence may result in an incorrect position indication.

After a rising edge on the $\overline{\text{RESET}}$ input, the device must be allowed at least t_{TRACK} ms (see Figure 37) for the internal circuitry to stabilize and the tracking loop to settle to the step change of the input position. For the duration of t_{TRACK} fault indications may occur on the LOT and DOS pins due to the step response caused by the $\overline{\text{RESET}}$. The duration of t_{TRACK} is dependent on the converter resolution as outlined in Table 27. After t_{TRACK}, the fault register should be read and cleared as outlined in the Clearing the Fault Register section. The time required to read and clear the fault register is indicated as t_{FAULT}, and is defined by the interface speed of the DSP/microprocessor used in the application. (Note that if position data is acquired via the encoder outputs, these can be monitored during t_{TRACK}.)

Table 27. t_{TRACK} vs. Resolution (f_{CLKIN} = 8.192 MHz)

Resolution (Bits)	t_{TRACK} (ms)
10	10
12	20
14	25
16	60

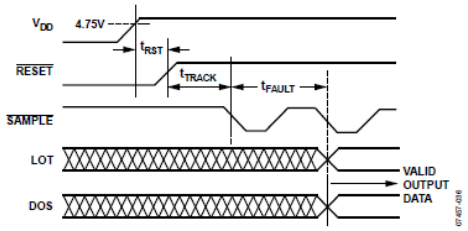


Figure 37. Power Supply Sequencing and Reset

CIRCUIT DYNAMICS

LOOP RESPONSE MODEL

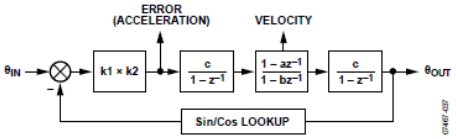


Figure 38. RDC System Response Block Diagram

The RDC is a mixed-signal device that uses two ADCs to digitize signals from the resolver and a Type II tracking loop to convert these to digital position and velocity words.

The first gain stage consists of the ADC gain on the sine/cosine inputs and the gain of the error signal into the first integrator. The first integrator generates a signal proportional to velocity. The compensation filter contains a pole and a zero that are used to provide phase margin and reduce high frequency noise gain. The second integrator is the same as the first and generates the position output from the velocity signal. The sin/cos lookup has unity gain. The values for the k1, k2, a, b, and c parameters are outlined in Table 28.

The following equations outline the transfer functions of the individual blocks as shown in Figure 38, which then combine to form the complete RDC system loop response.

Integrator1 and Integrator2 transfer function

$$I(z) = \frac{c}{1 - z^{-1}} \tag{10}$$

Compensation filter transfer function

$$C(z) = \frac{1 - az^{-1}}{1 - bz^{-1}} \tag{11}$$

RDC open-loop transfer function

$$G(z) = k1 \times k2 \times I(z)^2 \times C(z) \tag{12}$$

RDC closed-loop transfer function

$$H(z) = \frac{G(z)}{1 + G(z)} \tag{13}$$

The closed-loop magnitude and phase responses are that of a second-order low-pass filter (see Figure 11 and Figure 12).

To convert G(z) into the s-plane, an inverse bilinear transformation is performed by substituting the following equation for z:

$$z = \frac{\frac{2}{t} + s}{\frac{2}{t} - s} \tag{14}$$

where t is the sampling period (1/4.096 MHz ≈ 244 ns).

Substitution yields the open-loop transfer function, G(s).

$$G(s) = \frac{k1 \times k2(1-a)}{a-b} \times \frac{1 + st + \frac{s^2t^2}{4}}{s^2} \times \frac{1 + s \times \frac{t(1+a)}{2(1-a)}}{1 + s \times \frac{t(1+b)}{2(1-b)}} \tag{15}$$

This transformation produces the best matching at low frequencies ($f < f_{SAMPLE}$). At such frequencies (within the closed-loop bandwidth of the AD2S1210), the transfer function can be simplified to

$$G(s) \cong \frac{K_a}{s^2} \times \frac{1 + st_1}{1 + st_2} \tag{16}$$

where:

$$t_1 = \frac{t(1+a)}{2(1-a)}$$

$$t_2 = \frac{t(1+b)}{2(1-b)}$$

$$K_a = \frac{k1 \times k2(1-a)}{a-b}$$

Solving for each value gives t_1, t_2, and K_a as outlined in Table 29.

Table 28. RDC System Response Parameters

Parameter	Description	10-bit resolution	12-bit resolution	14-bit resolution	16-bit resolution
k1 (nominal)	ADC gain	1.8/2.5	1.8/2.5	1.8/2.5	1.8/2.5
k2	Error gain	$6 \times 10^6 \times 2\pi$	$18 \times 10^6 \times 2\pi$	$82 \times 10^6 \times 2\pi$	$66 \times 10^6 \times 2\pi$
a	Compensator zero coefficient	8187/8192	4095/4096	8191/8192	32,767/32,768
b	Compensator pole coefficient	509/512	4085/4096	16,359/16,384	32,757/32,768
c	Integrator gain	1/1,024,000	1/4,096,000	1/16,384,000	1/65,536,000

Table 29. Loop Transfer Function Parameters vs. Resolution (f_{CLKIN} = 8.192 MHz)

Resolution (Bits)	t_1 (ms)	t_2 (ms)	K_a (sec^{-2})
10	0.4	42	39.6×10^6
12	1	91	6.5×10^6
14	2	160	1.6×10^6
16	8	728	92.7×10^3

Note that the closed-loop response is described as

$$H(s) = \frac{G(s)}{1+G(s)} \quad (17)$$

By converting the calculation to the s-domain, it is possible to quantify the open-loop dc gain (K_a). This value is useful to calculate the acceleration error of the loop (see the Sources of Error section).

The step response to a 10° input step is shown in Figure 10, Figure 11, Figure 12, and Figure 13. The step response to a 179° input step is shown in Figure 14, Figure 15, Figure 16, and Figure 17. In response to a step change in velocity, the AD2S1210 exhibits the same response characteristics as it does for a step change in position.

Figure 18 and Figure 19 in the Typical Performance Characteristics section show the magnitude and phase responses of the AD2S1210 for each resolution setting.

SOURCES OF ERROR

Acceleration

A tracking converter employing a Type II servo loop does not have a lag in velocity. There is, however, an error associated with acceleration. This error can be quantified using the acceleration constant (K_a) of the converter.

$$K_a = \frac{Input\ Acceleration}{Tracking\ Error} \quad (18)$$

Conversely,

$$Tracking\ Error = \frac{Input\ Acceleration}{K_a} \quad (19)$$

The units of the numerator and denominator must be consistent. The maximum acceleration of the AD2S1210 is defined by the maximum acceptable tracking error in the users application. For example, if the maximum acceptable tracking error is 5°, then the maximum acceleration is defined as the acceleration that creates an output position error of 5° (that is, when LOT is indicated).

An example of how to calculate the maximum acceleration in a 12-bit application with a maximum tracking error of 5° is

$$Maximum\ Acceleration = \frac{K_a(sec^{-2}) \times 5°}{360(°/rev)} \cong 90{,}300\ rps^2 \quad (20)$$

Figure 20 to Figure 23 in the Typical Performance Characteristics section show the tracking error vs. acceleration response of the AD2S1210 for each resolution setting.

OUTLINE DIMENSIONS

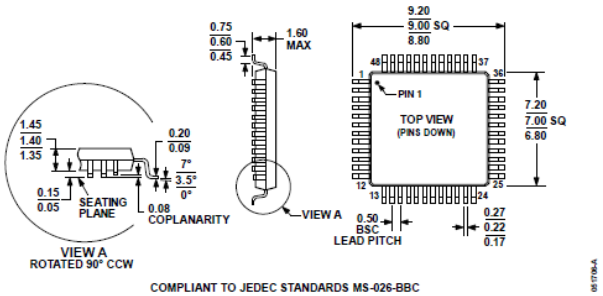


Figure 39. 48-Lead Low Profile Quad Flat Package [LQFP]
(ST-48)
Dimensions shown in millimeters

ORDERING GUIDE

Model[1]	Temperature Range	Package Description	Package Option
AD2S1210ASTZ	–40°C to +85°C	48-Lead LQFP	ST-48
AD2S1210BSTZ	–40°C to +85°C	48-Lead LQFP	ST-48
AD2S1210CSTZ	–40°C to +125°C	48-Lead LQFP	ST-48
AD2S1210DSTZ	–40°C to +125°C	48-Lead LQFP	ST-48
AD2S1210WDSTZ[2]	–40°C to +125°C	48-Lead LQFP	ST-48
AD2S1210WDSTZRL7[2]	–40°C to +125°C	48-Lead LQFP	ST-48
EVAL-AD2S1210EDZ		Evaluation Board	

[1] Z = RoHS Compliant Part.
[2] Qualified for Automotive.

APPENDIX H: DEVELOPED PRINTED CIRCUIT BOARD FIGURES

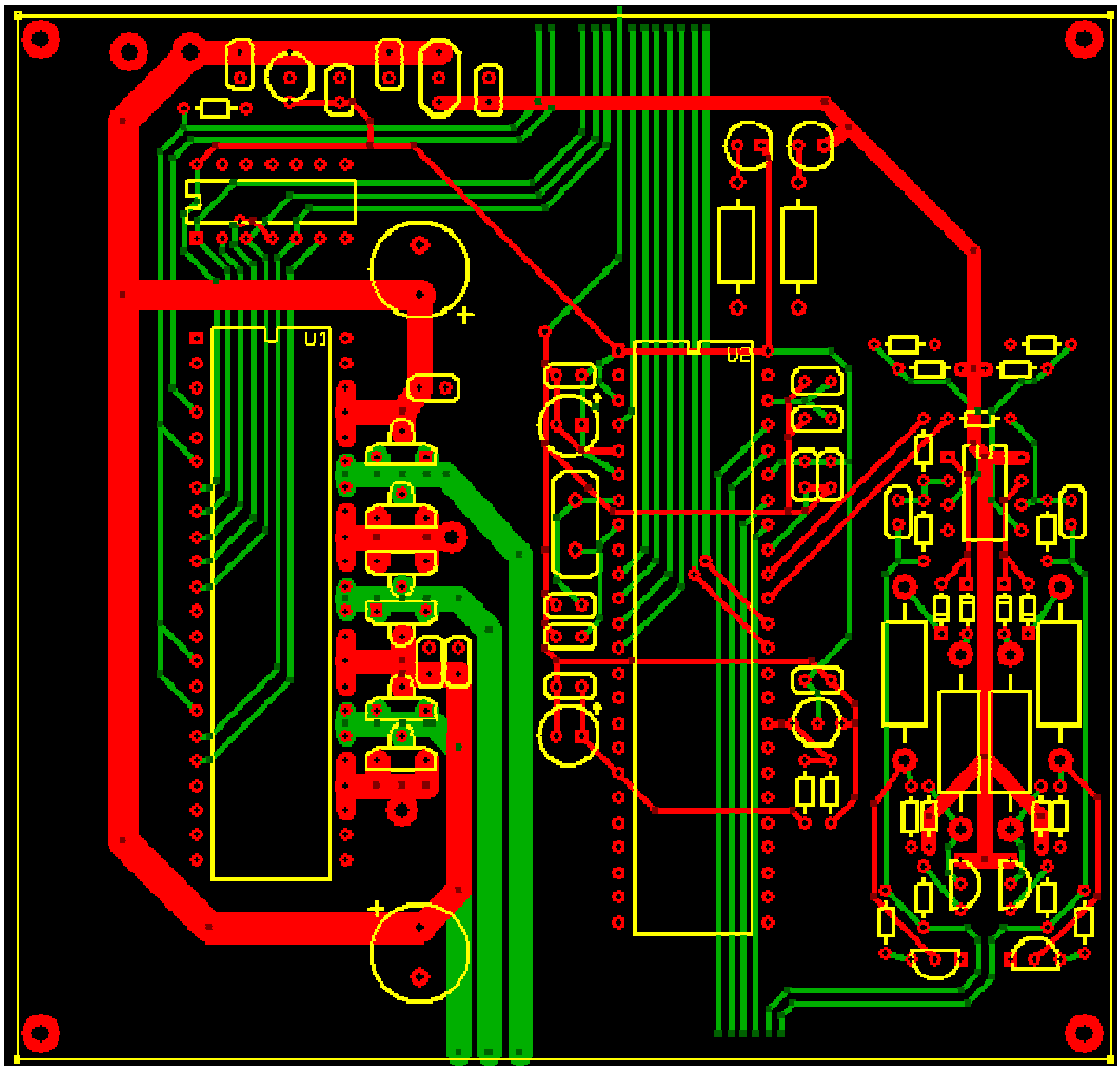


Figure H 1: Bottom (green lines), top (red lines), and top components (outlined in yellow) associated with designed circuit board.

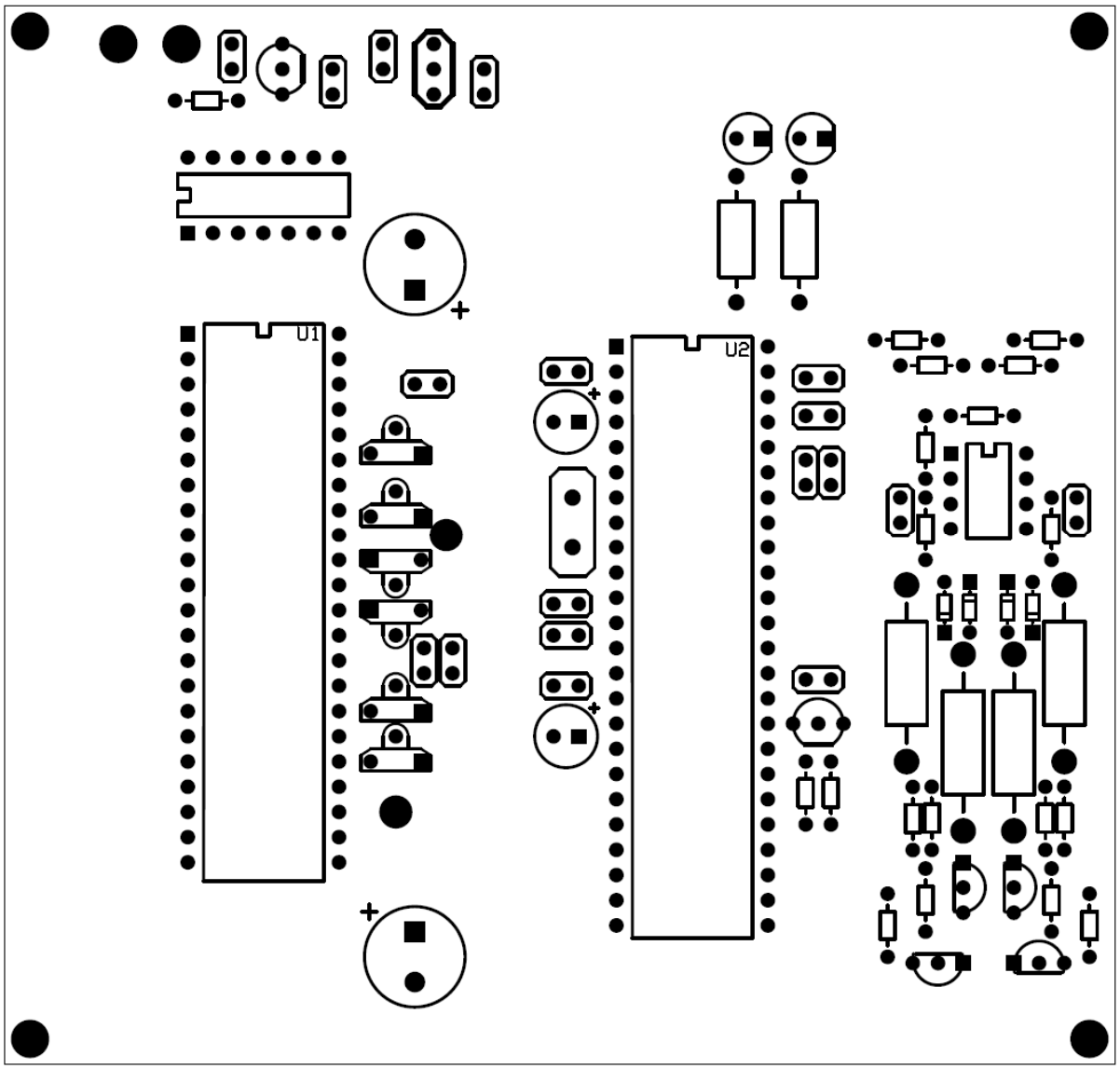


Figure H 2: Black and white copy showing component and hole outline on top of designed printed circuit board as viewed from top.

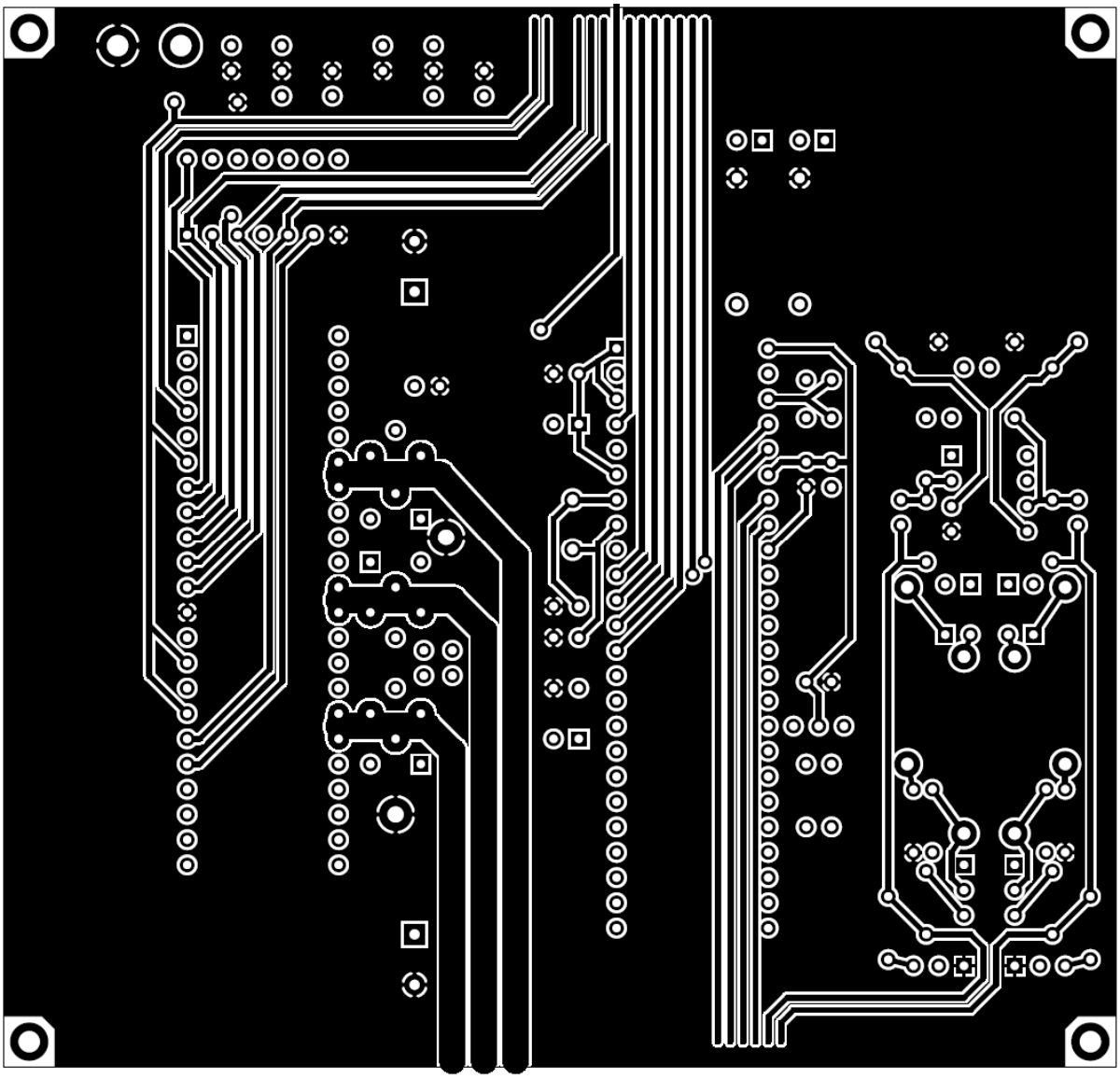


Figure H 3: Black and white copy showing top of designed printed circuit board as viewed from top.

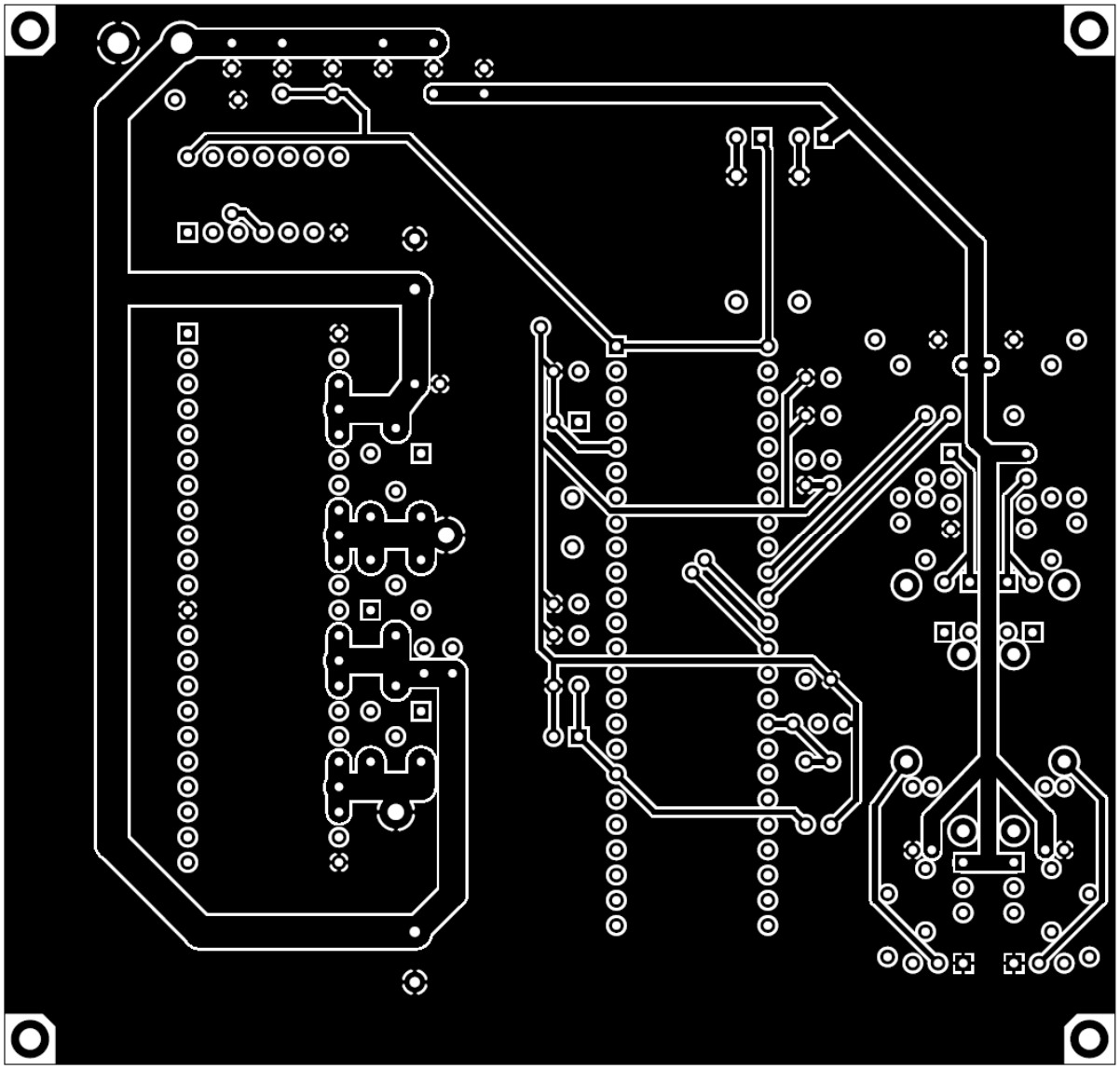


Figure H 4: Black and white copy showing bottom of designed printed circuit board as viewed from top.

APPENDIX I: PHOTOS OF IMPLEMENTED HARDWARE

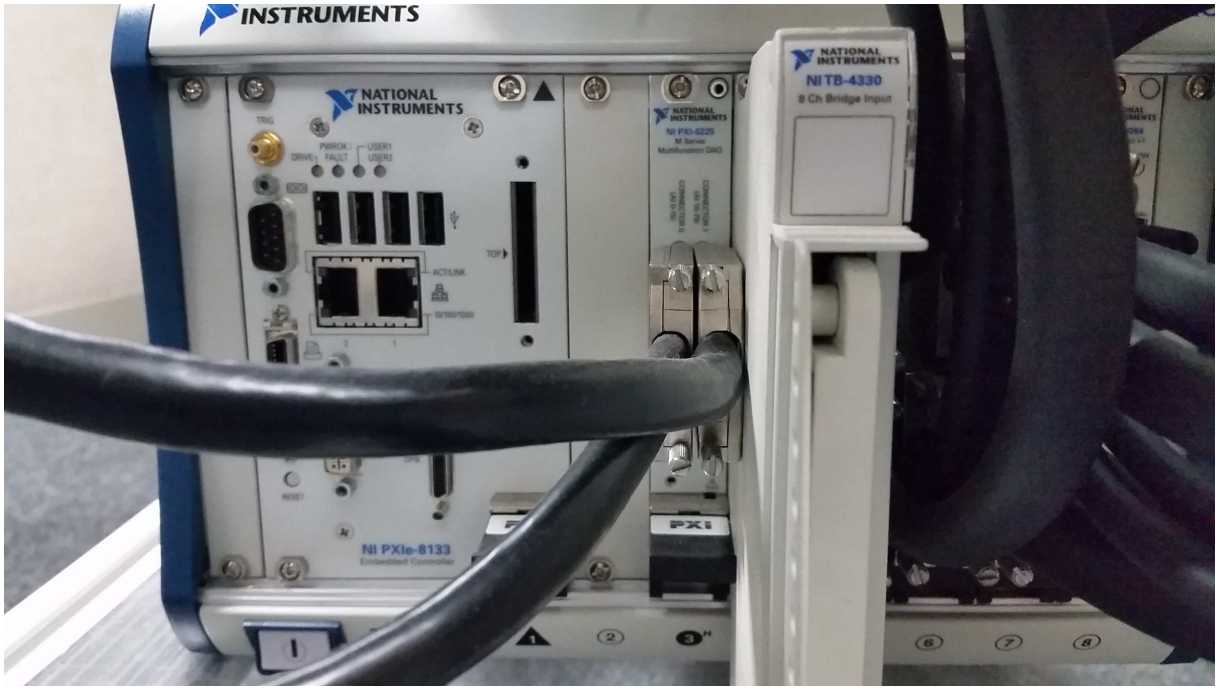


Figure I 1: NI PXIe-8133 embedded controller and NI PXI-6225 M Series Multifunction DAQ connecting to array of SCB-68 M Series Devices Connectors.

Figure I 2: Array of SCB-68 M Series Devices Connectors used to link driver and resolver circuit with NI system.

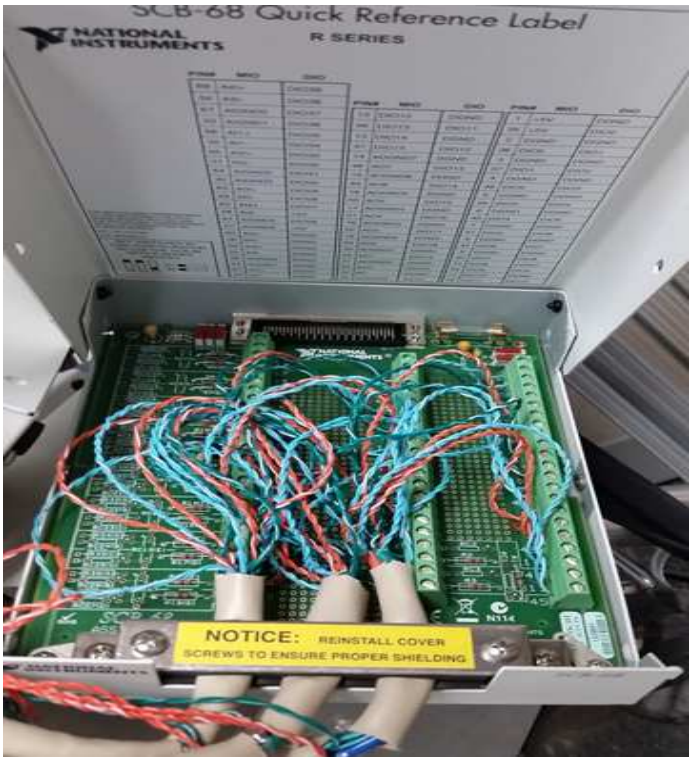


Figure I 3: Labeled SCB-68 M Series Devices Connectors used to link driver and resolver circuit with NI system.

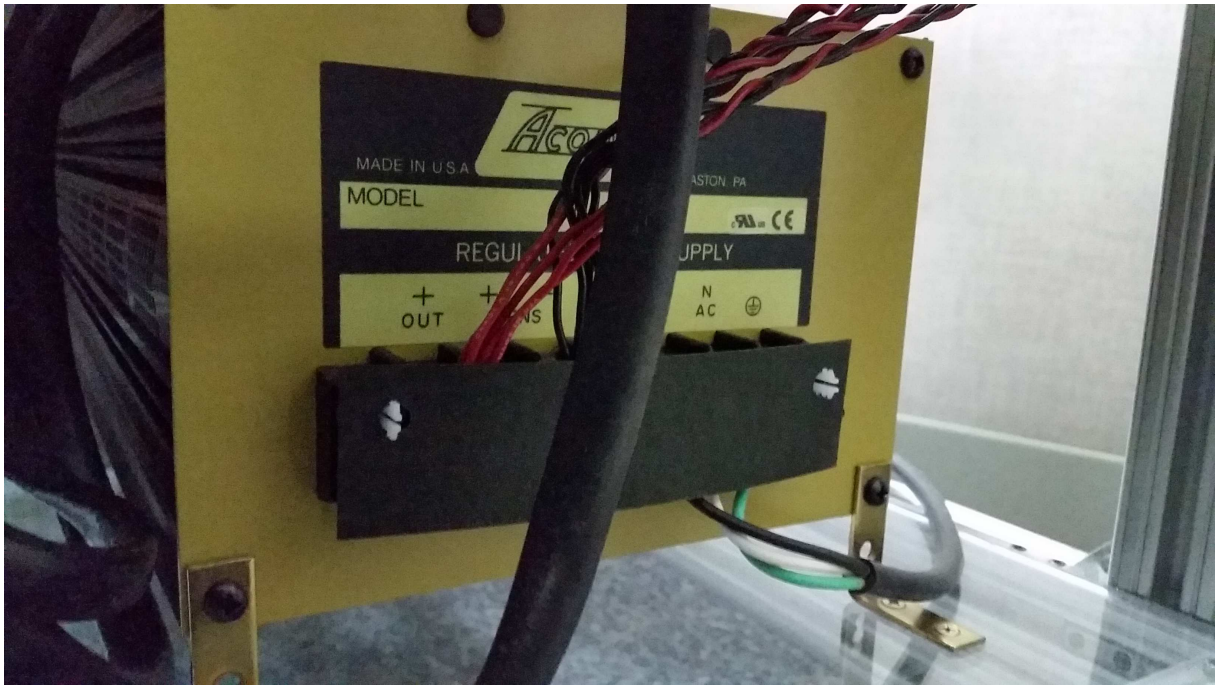


Figure I 4: Acopian 24V power supply implemented in this project.

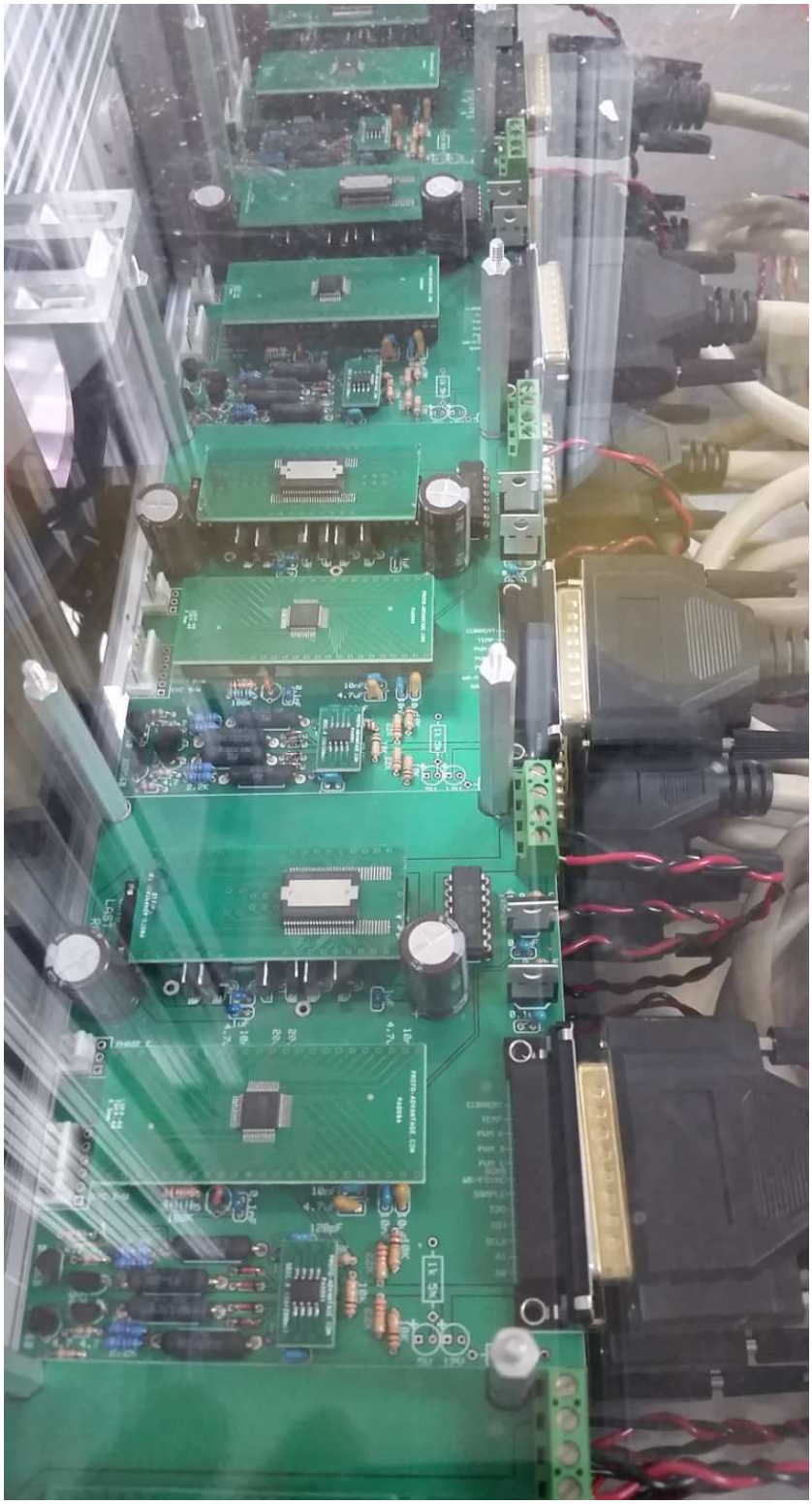


Figure I 5: Array of brushless motor drivers connected to SCB-68 M Series Devices Connectors.

Figure I 6: Maxon EC 22 brushless motor

Figure I 7: Tamagawa Smartsyn TS2605N31E64 resolver employed in this project.