Modeling and Design of a DFIG Testbed for Protection Design Purposes

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Authorization to Submit Thesis

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Abstract

In this thesis, a Type III (Doubly Fed Induction Generator) wind generation system is analyzed and modeled. The results of this analysis are used to design and build a testbed for protection design and testing. The specific generator modeled is the four-pole, 10HP DFIG driven by a four-pole, 10HP induction machine powered by an adjustable speed drive. The testbed is made for research and development to analyze the DFIG during fault conditions. A future goal for the overall project is to design protection equipment for wind farms.

The thesis presents the steady-state modelling and dynamic modelling of the DFIG, followed by a detailed switching model of the two-level voltage source converter (VSC). Two VSCs form a back-to-back converter which connects between the rotor windings and the power system. The grid side converter (GSC) interacts with the power system and the DC bus and is designed to maintain a constant DC bus voltage. The GSC is controlled to exchange power between the DC bus and the power system while tracking the system frequency. The power circuit, sensor circuit and control circuit for GSC are first designed and validated in simulation, then implemented in hardware. The protection logic is designed to protect the power electronics from overcurrent and overvoltage. The power control of the DFIG is achieved by rotor side converter (RSC) control strategies. The functionality of the RSC control is validated with simulation and could be implemented in hardware with similar hardware setups as the GSC.

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CHAPTER 1

Introduction

A wind Energy Conversion System (WECS) is the overall system for converting wind energy into useful mechanical energy that can be used to power an electrical generator for generating electricity. This chapter provides an overview of the WECS. The general background and market trends are discussed. Grid codes were developed to ensure uniform standards for power system integration of renewable generation sources. The wind energy generators can generally be categorized into four types, and the Type III wind turbine is the focus of this thesis.

1.1 Wind Turbine Technology Trends

Wind turbines are constructed with different numbers, shapes and sizes of blades. A typical wind unit consists of three blades connected to the rotor by a hub. The hub is usually connected to the generator rotor shaft through a gearbox. Since the terminal voltage at the generator is often low, a step-up transformer is usually implemented at the point of common coupling (PCC). This process can also be achieved through power convertors to synchronize with the appropriate grid frequency and voltage.

In the last quarter century, wind turbines have advanced in physical size and generation capacities. In the early 80's, wind turbine blade used to be typically $15 - 20\ m$ in diameter and their generators produced 50 kW on average. Now, over 7 MW of electrical power can be produced with a single machine with the turbine blade diameter over 100 m. The largest capacity turbines are typically around $7 - 9\ MW$, and are being commissioned off-shore. A 25 years comparative graphical representation for turbine sizes over time is shown in Fig. 1.1 [1].

Increases in conventional fuel cost have been driving research and development in renewable technology to grow exponentially, especially wind generation. Great

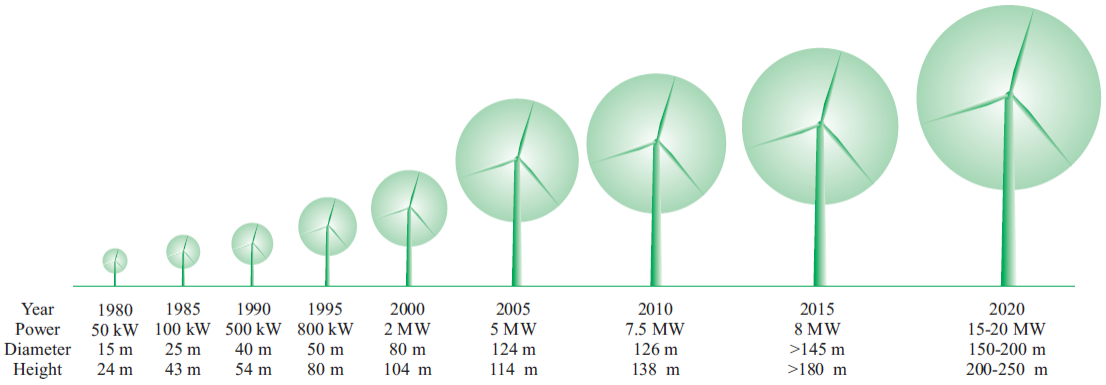

Figure 1.1: Growth in Capacity and Blade Diameter of Wind Turbines 1985-2016 [1]

advances in the wind energy generation area have enabled manufacturers to develop turbines that are larger, have greater generation capabilities, and higher operating efficiencies. These advances lead to a lower cost per megawatt and result in the development of additional safety and protection features, enabling a higher level of integration of wind energy around the globe. Table 1.1 [2] outlines some of the world's

Table 1.1: Top 10 Wind Turbine Manufactures of 2009, Generator Type and Power Ranges

Manufacture	Generator Types	Rotor Diameter	Power Range
Vestas (Denmark)	DFIG GFC PM	52-90m 112m	850kW-3 MW 3 MW
General Electric (US)	DFIG GF CPM DD PM	70.5-82.5m 100m 110m	1.5 MW 2.5 MW 4.0 MW
Sinovel (China)	DFIG	60-113m	1.5-3 MW
Enercon (Germany)	DD EE	33-126m	300kW-7.5 MW
Goldwind (China)	DD PM	70-100m	1.5 MW-2.5 MW
Gamesa (Spain)	DFIG GFC PM	52-97m 128m	850kW-2 MW 4.5 MW
DongFeng (China)	DFIG		1-2.5 MW
Suzlon (India)	CS	52-88m	600kW-2.1 MW
Siemens (Germany)	GFC IG DD PM	82-107m 101m	2.3-3.6 MW 3 MW
Repower (Germany)	DFIG	82-126m	2-6 MW

major wind turbine manufacturers and the main features of their turbines.

CS Type I: constant speed with gearbox and induction generator, possibly with extended slip or two speeds

DFIG Type III: variable speed with gearbox, doubly-fed induction generator and partly rated converter

DD EE Type IV: variable speed direct-drive synchronous generator with electrical excitation and full converter

DD PM Type IV: variable speed direct-drive permanent-magnet generator and full converter

GFC PM Type IV: variable speed with gearbox, permanent-magnet generator and full converter

GFC IG Type IV: variable speed with gearbox, induction generator and full converter

1.2 Grid Code

Grid code requirements typically apply to large wind farms that are connected to the transmission system, rather than smaller wind stations that are connected to the distribution system. Recent grid codes specify that wind farms must contribute to power system frequency and voltage control, to the same extent as conventional power generation stations. Wind farms are required to withstand abnormal conditions such as voltage dips. Grid Codes also address fault tolerance, real/reactive power control requirements, voltage control requirements, frequency control requirements, protective devices requirements, and power quality requirements. These requirements apply to the point of common coupling (PCC) which is the connection point of the wind farm and the power system [3].

1.2.1 Fault Ride-through (FRT) Requirements

A disturbance from the grid caused by faults can cause a power generation unit to disconnect leading to system instability. To avoid this, the codes often require the wind farm to stay connected to the grid during a fault across a specified voltage envelope. The depth and duration of the voltage dips are defined by a diagram such as the one shown in Fig. 1.2. Faults often cause temporary voltage sags at the point of interconnect. The withstand capability of wind generation to keep operating during voltage sags is referred as Low Voltage Ride-Through (LVRT) or Fault Ride-Through (FRT) capability. These requirements are specified in terms of voltage versus time characteristics at the PCC point.

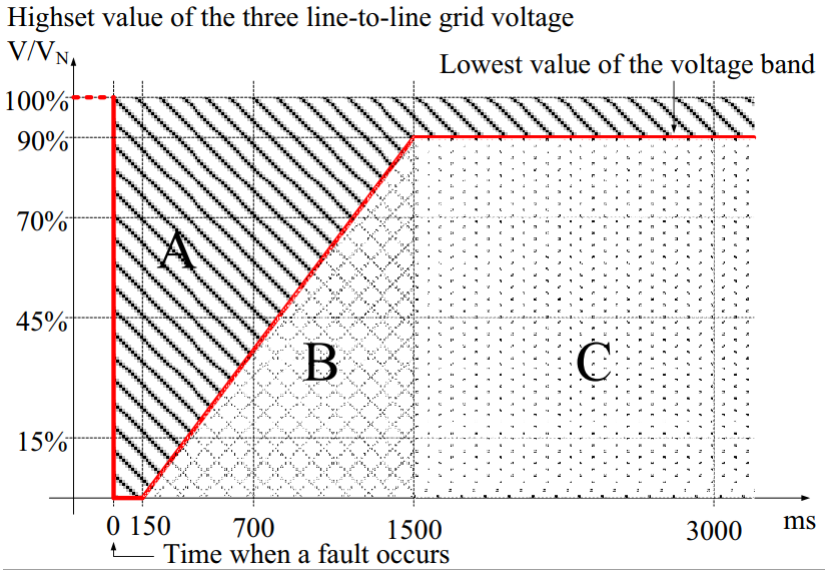

Figure 1.2: Typical Grid Code requirements for Low-Voltage Ride-Through [4]

FRT requirements are the essential element of the existing grid codes. The transmission system requires wind farms to remain in operation during any disturbance or fault in which voltage variation ratio versus duration is in area A in Fig. 1.2. The system is allowed to be disconnected from the grid for cases B and C. However, in case B, resynchronization must be complete within 2 seconds after fault clearance. Reactive power ramped at the rate of 10% of rated power per second should be supplied to the

grid. For all wind generation systems that are in service during faults, active power should be supplied to the grid and increased to nominal value with minimum rate of 20% of rated power per second after fault clearance [4]. The wind turbines may experience considerable electrical and mechanical stress during the a FRT event and the power electronic devices might be damaged. Therefore, in order to fulfill the grid code requirements, the wind energy generation system must be protected to allow it to stay on line during transmission system faults when possible while also preventing damage to the WECS.

1.2.2 Reactive Power Requirement

Large wind plants are generally required to maintain the power factor between +/- 0.95 power factor with voltage magnitudes between 0.95 to 1.05 p.u. at the PCC. Additional reactive compensation is often required in order for the wind generation plants to meet the voltage and power factor requirements [5]. The reactive power compensation can be achieved using various devices. The most common forms are the capacitor banks or STATCOM devices. These requirements are also being met by turbine power factor and voltage control techniques in newest applications. [6].

1.2.3 Real Power Requirement

When wind generation replaces conventional synchronous generation, the power system inertia decreases. This is due to the fact that most types of variable speed wind turbines decouple the mechanical system from the electrical system. The reduction of system inertia could cause more severe problems in the early stage of a frequency disturbance. The active power control requirement is defined as the ability to adjust the active power supplied to the system with respect to the frequency deviations, as well as the orders received from the control center. According to this requirement, wind power plants should be able to respond to participate in both primary and secondary

frequency control. The primary and secondary frequency control are both automatic control systems. The primary frequency control system's response times are in order of seconds and that of the secondary are in minutes. Inertia and the droop speed controllers are now being used to maintain the system frequency [7].

1.3 Introduction to Double Fed Induction Generator(DFIG)

Wind turbines can be generally classified into four types as shown in Fig. 1.3. Type I wind generators are squirrel cage induction generators which connect to the system directly. This type of wind generator does not require power electronic devices, but dynamic reactive power compensation might be added. However, the uncertainty of the wind speed is reflected in the power output directly. Type II wind generators use wound rotor induction generators with a controllable rotor resistance. This type of generator has greater ability to control the output power as wind speed varies. Both type I and type II wind turbines rely on reactive power from the power system, usually in the form of require external reactive power compensation, such as capacitor banks. Type III wind turbines also use wound rotor induction machines and are referred to as doubly fed induction generators (DFIGs). The generator stator is connected to the grid directly and the rotor is connected to the gird though a back-to-back voltage source converter. The back-to-back voltage source converter provides more flexibility to operate over a wide range of wind speeds, typically up to $\pm 30\%$ of nominal. Therefore, the VSCs are usually rated to 30% of the machines's total rated power. Type IV wind turbines use either synchronous generators or squirrel cage induction machines that connect to the power system though a back-to-back voltage source converter rated for the full output of the machine, increasing the cost of power electronic devices compared to the Type III wind turbine.

The doubly fed induction generators (DFIGs) are preferred among all kinds of wind generation for land based applications because of their low cost [8], higher energy

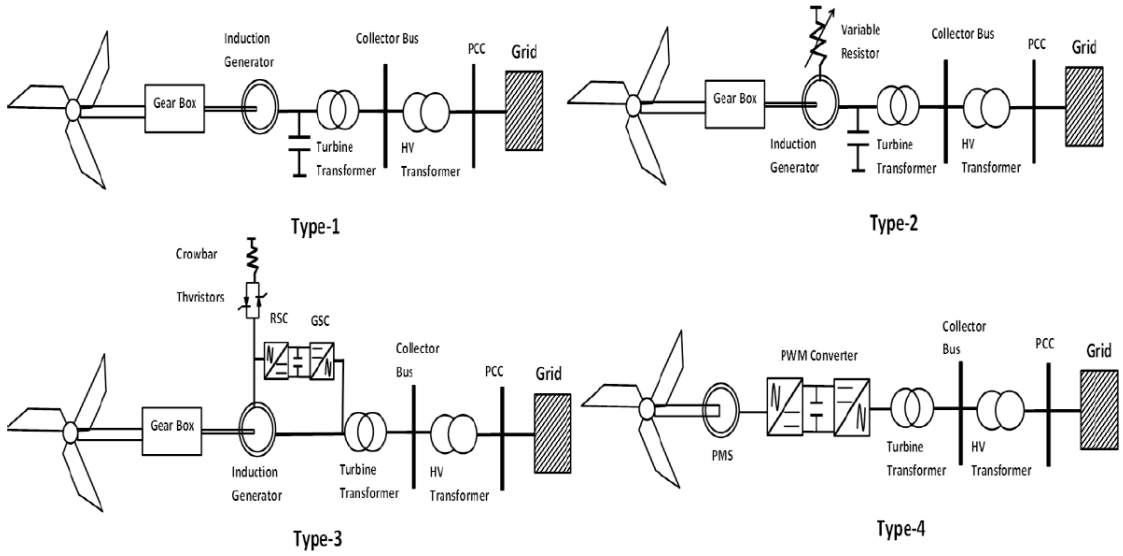

Figure 1.3: Four Types of Wind Turbine

output, lower converter rating, and better utilization of the machines [9]. DFIGs can also provide good damping performance for a weak grid [10]. Independent control of active and reactive power is achieved by the decoupled vector control algorithm implemented in the power converter as presented in [11] and [12]. The DFIG is essentially a wound rotor induction generator in which the rotor circuit is controlled by an external controllable variable frequency voltage source to achieve variable speed operation. The stator of the generator delivers power from the wind turbine to the grid by direct connection, therefore, the power flow is unidirectional. However, the power flow in the rotor circuit is bidirectional depending on the rotor speed. The bidirectional power flow is achieved by using a back-to-back voltage source converter connected to the rotor.

1.3.1 DFIG General Configuration

A DFIG consist of a wound rotor induction generator with slip ring, a partial scale power electronic converter and a common DC-link capacitor as shown in Fig. 1.3. The rotor side power electronic circuit consists of a back to back AC-DC-AC voltage

source converter which has two main parts: grid side converter (GSC) that rectifies grid voltage and rotor side converter (RSC) which feeds the rotor circuit. The power converter only processes slip power which is at most 30% of generator rated power [13].

1.3.2 Maximum Power Point Tracking (MPPT)

To obtain the maximum available power from the wind at different wind speeds, the turbine blades are adjusted to the specific pitch angle to achieve the optimal speed to ensure the wind power generation is maximized. A wind speed sensor is installed to measure real time wind speed. According to the MPPT profile provided by the manufacturer, the power reference is generated by mathematical algorithms and sent to the generator control system. The power controller compares the power reference with the measured power from the generator to produce the control signals for the power converters [14]. In this thesis, the power reference is calculated based on rotor speed and torque applied by the squirrel cage induction motor and drive. Using the back-to-back converter to control the generator, it is possible to match the output power of the generator to the MPPT reference power at steady-state, from which the maximum power operation is achieved.

1.3.3 Power converter control

Many different structures and control algorithms can be used to control the power converter. One of the most common control techniques is to apply dq-reference frame which obtains active and reactive power control of DFIG separately.

The converter IGBT's switching signals are generated by pulse width modulation. The project uses space vector pulse width modulation (SVPWM) which has many advantages as compared to sinusoidal PWM. SVPWM allows easier vector control and produces a higher output Moreover it is easier to implement digitally. In this

thesis, both modulation methods are introduced and SVPWM is used in both the simulation and hardware control.

1.4 Objectives

This thesis focuses on the control theory and implementation for the DFIG rotor circuit back-to-back converters. The first objective of this thesis is to develop a dynamic DFIG model and analyze the steady-state performance using PSIM software. The specific objectives are to:

1. Model the existing induction motor in simulation
2. Create a speed-controlled induction motor drive for the driver motor.
3. Set up a steady-state equivalent circuit based on the given DFIG parameters. The rotor-side converter is initially modeled by an equivalent impedance.
4. Calculate for active and reactive power control references of DFIG in different power factor. Evaluate the power flow and the machine efficiency.
5. Build dynamic and steady-state machine models of the DFIG in PSIM.
6. Implement power control to the rotor back-to-back converter circuit to track calculated optimal power references while maintaining synchronization to the power system.
7. The back-to-back converter is modeled using switching models and space vector PWM are implemented to provide switching commands to the power electronic devices.
8. Validate the steady-state and dynamic performance of the control system by comparing the numerical calculation results with the PSIM simulation results.

The secondary objective of this thesis is to build a hardware testbed to demonstrate the grid side converter control. The specific objectives are to:

1. Control the charging and discharging of the DC bus capacitors.
2. Maintain a constant DC bus voltage at the reference voltage level.
3. Achieve AC system frequency tracking.
4. Supply controlled reactive power to the system and track the given reactive power reference.
5. Achieve both current control and overcurrent protection logic to prevent overcurrent.
6. Apply protection logic to prevent DC bus overvoltage.

To accomplish the desired objectives, the thesis is organized as follows. The thesis first introduces power system theories and mathematical methods for the derivation of the machine model equations in Chapter 2. A detailed description of the machine modeling and control for a DFIG connected to the power grid is presented so that its behavior and interaction with the power grid during steady-state and dynamic conditions can be determined. In Chapter 3, the two-level voltage converter topology and the modulation methods are explained. In Chapter 4, the complete modeling and control of grid side converter connected to the power grid is developed to analyze its interaction with the DFIG wind turbine system. Based on the theory and simulation development, the hardware testbed is next built and tested. Details of the tested circuits are provided as well as the tests and operational procedures. A rotor side converter model is then built in the simulation and combined with the rest of the system in Chapter 5. The result of the simulated system performance is validated with the numerical calculations based on the system model developed in previous sections.

CHAPTER 2

Doubly Fed Induction Machine Modeling

In this chapter, both steady-state and dynamic models of doubly fed induction machines are presented. From the steady-state equivalent circuit it is possible to analyze the power relations of a DFIG. Different modes of operation are studied based on the power relation. However, the steady-state model is not sufficient to reach the modeling objectives of this research. The dynamic and transient behaviors of the DFIG must be examined for development of the machine control scheme.

2.1 Steady-State Equivalent Circuit of DFIG and Power Losses

For the particular DFIG that is located at the University of Idaho power lab, both the stator and the rotor are connected in star configurations. In the steady-state model, only one phase of the stator and rotor windings is represented. The stator is supplied by the grid at constant and balanced three-phase AC voltage and frequency (220V, 60Hz). The rotor is supplied by the grid through a back-to-back voltage source converter. The ideal one phase steady-state equivalent electric circuit can be drawn as shown in Fig. 2.1. This equivalent circuit is developed by adding the converter equivalent impedance to the squirrel cage induction machine steady-state model.

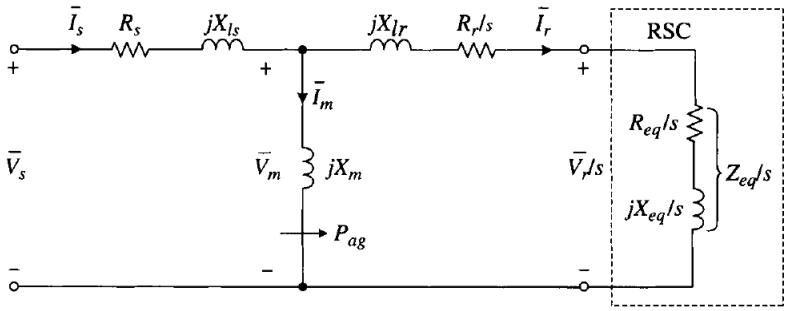

Figure 2.1: One-phase Steady-state equivalent circuit of DFIG with the rotor-side converter represented by R_{eq} and X_{eq}.

In Fig. 2.1, the steady-state operation of a DFIG wind energy system is shown with the rotor side converter modeled as an equivalent impedance that is a function of slip. The subscripts r and s represent rotor related parameters and stator related parameters respectively. Slip is a concept commonly used in asynchronous machines, denoted as s. It is defined as the normalized relation between the speed of the stator and the rotor angular frequencies. The equivalent impedance of the converter is defined by (2.1).

$$Z_{eq} = R_{eq} + jX_{eq} = R_{eq} + j\omega_{sl}L_{eq} \tag{2.1}$$

Where ω_{sl} is the angular slip frequency and L_{eq} is the equivalent inductance of the RSC. Since the frequency of the rotor current in the actual rotor winding flowing into the converter is ω_{sl}, and the converter equivalent impedance in the equivalent circuit is based on the stator angular frequency ω_s, the impedance, Z_{eq}, need to be divided by slip, s. The equivalent impedance referred to the stator side is then given by (2.2)

$$Z_{eq}/s = R_{eq}/s + jX_{eq}/s = R_{eq}/s + j\omega_s L_{eq} \tag{2.2}$$

Where ω_{sl}=$s\omega_s$. The angle of the stator current with reference to the stator voltage is determined by the given operating power factor. For example, when the DFIG is operating at unity power factor:

$$\vec{V_s} = V_s\angle 0^\circ \quad and \quad \vec{I_s} = I_s\angle 180^\circ \tag{2.3}$$

The stator voltage and current are 180° out of phase, indicating that the DFIG is in the generating mode and the stator power factor (PF_s) is unity. Since the stator is operating at a unity power factor and assuming R_s is small enough to be neglected, the air-gap power of the generator can be determined by (2.4).

$$P_{ag} = 3\left(V_s - I_s R_s\right) I_s \approx 3V_s I_s \tag{2.4}$$

According to the induction machine theory, the air-gap power can also be calculated by (2.5).

$$P_{ag} = \frac{\omega_s T_m}{P} \tag{2.5}$$

Where T_m is the mechanical torque and P is the number of pole pairs in the generator. Substituting (2.5) into (2.4) and solve for the stator current magnitude, I_s, result in (2.6).

$$I_s = \frac{V_s \pm \sqrt{V_s^2 - \frac{4R_s\omega_s T_m}{3P}}}{2R_s} \tag{2.6}$$

Where V_s is the phase-to-neutral voltage magnitude at the PCC. Using the equivalent circuit in Fig. 2.1, the voltage across the magnetizing branch can be calculated based on the stator current.

$$\vec{V_m} = \vec{V_s} - \vec{I_s}\,(R_s + j\omega_s L_{ls}) \tag{2.7}$$

The current in the magnetizing branch can be determined based on the magnetizing inductance.

$$\vec{I_m} = \frac{\vec{V_m}}{j\omega_s L_m} \tag{2.8}$$

The rotor current and rotor voltage can then be calculated using (2.9) and (2.10).

$$\vec{I_r} = \vec{I_s} - \vec{I_m} \tag{2.9}$$

$$V_r = sV_m - I_r\,(R_r + js\omega_s L_{lr}) \tag{2.10}$$

2.2 Four Quadrant Modes of Operation

The DFIG can operate under different conditions depending on the power and the speed. Fig. 2.2 graphically illustrates the four quadrant for modes of operation and Table 2.1 describes the four modes of operation for the DFIG in more detail.

The goal of this research is to mimic wind generation using the DFIG. Therefore,

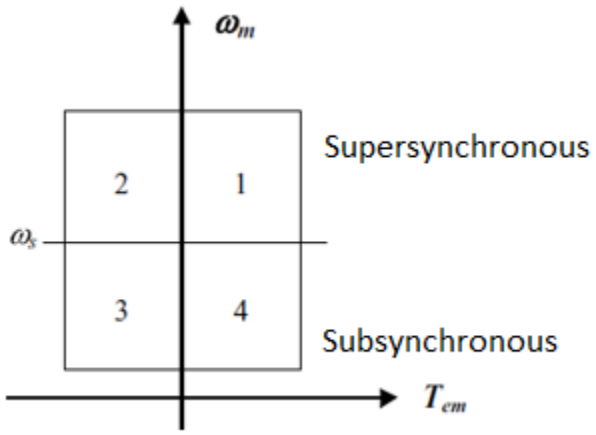

Figure 2.2: Four quadrant for modes of operation of the DFIG

Table 2.1: Four modes of operation for DFIG in related power, torque and rotor speed

Mode	Speed (s, ω)	Mechanical Power (P_{mec})	Stator Power (P_s)	Rotor Power (P_r)
1. Motor ($P_{em}>0$)	$s<0$ $\omega_m>\omega_s$ Supersynchronous	$P_{mec}>0$, (the machine delivers mechanical power)	$P_s>0$ (the machine receives power through stator)	$P_r>0$ (the machine receives power through rotor)
2. Generator ($P_{em}<0$)	$s<0$ $\omega_m>\omega_s$ Supersynchronous	$P_{mec}<0$, (the machine receives mechanical power)	$P_s<0$ (the machine delivers power through stator)	$P_r<0$ (the machine delivers power through rotor)
3. Generator ($P_{em}<0$)	$s>0$ $\omega_m<\omega_s$ Subsynchronous	$P_{mec}<0$, (the machine receives mechanical power)	$P_s<0$ (the machine delivers power through stator)	$P_r>0$ (the machine receives power through rotor)
4. Motor ($P_{em}>0$)	$s>0$ $\omega_m<\omega_s$ Subsynchronous	$P_{mec}>0$, (the machine delivers mechanical power)	$P_s>0$ (the machine receives power through stator)	$P_r<0$ (the machine delivers power through rotor)

the two generator modes will be discussed in more detail in the later chapters. Note that in the supersynchronous generator mode (Mode 2) power is delivered through both the stator and the rotor windings to the grid. In the subsynchronous generator mode (Mode 3), the stator delivers power to grid while the rotor receives power. Under the generator modes, the stator delivers power from the wind turbine to the grid. Therefore, in generator mode the stator power flow is unidirectional. However, the power flow in the rotor circuit is bidirectional, depending on the rotor speed. With variable speed operation, a wind generation system using a doubly fed induction generator can harvest more energy from the wind than a fixed-speed wind generation system when the wind speed is above its rated value [15].

2.3 Power Flow Steady-State Operation During Generation Modes

Based on the steady-state equivalent circuit derived in the previous section, all power can be calculated by a general equation of $P = I^2R$. Fig. 2.3 shows the power flow within the DFIG operating under the super- and sub-synchronous modes [16].

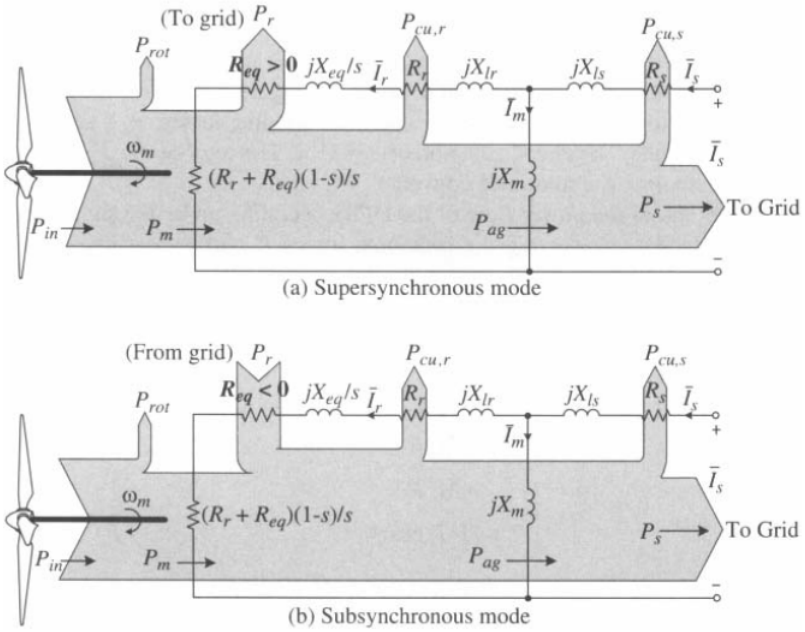

Figure 2.3: Power flow of DFIG with rotor-side converter represented by R_{eq} and X_{eq}.

Neglecting the rotational losses P_{rot} of the turbine, the power delivered and dissipated in the generator can be calculated by (2.11).

$$\begin{cases} P_m = 3I_r^2(R_r + R_{eq})(1-s)/s \\ P_r = 3I_r^2 R_{eq} \\ P_{cu.r} = 3I_r^2 R_r \\ P_{cu.s} = 3I_s^2 R_s \\ P_s = 3V_s I_s cos\phi_s \end{cases} \tag{2.11}$$

Where P_m is the mechanical power applied to the rotor; P_r is the power exchanged between the power system and the rotor-side converters; $P_{cu,r}$ and $P_{cu,s}$ are the cupper winding loss of the rotor and the stator respectively; P_s is the power exchanged between the power system and the stator and ϕ_s is the stator power factor angle. The power delivered to the grid, P_g, is the sum of the stator and rotor power, given by (2.12).

$$|P_g| = \begin{cases} |P_s| + |P_r| \quad for \quad super - synchronous \quad mode \\ |P_s| - |P_r| \quad for \quad sub - synchronous \quad mode \end{cases} \tag{2.12}$$

When the DFIG is operating in the super-synchronous operating mode shown in Fig. 2.3(a), the equivalent resistance R_{eq} of the rotor-side converter is calculated to be positive so that the rotor power, P_r, is also positive. This indicates that the resistance R_{eq} consumes power similar to the winding resistances R_r and R_s, meaning that power, P_r, is transferred from the rotor to the grid through the converters. However, when operating in the sub-synchronous mode as shown in Fig. 2.3(b), R_{eq} is calculated to be negative and the rotor power, P_r, is also negative. This implies that the rotor circuit receives power from the grid through the converters.

2.4 The Park's Reference Frame Transformation

Consider a general set of three-phase electrical variables, x_a, x_b, and x_c, which can represent voltage, current or flux linkages that vary in time and space. The three-phase variables can be represented as a space vector $\vec{x}$ in a three-phase stationary reference frame where the three axes are $2\pi/3$ radians apart in space. At any instant in time, the projection of the space vector $\vec{x}$ on to the corresponding *a*-, *b*-, and *c*-axes gives the phases value of x_a, x_b, and x_c as shown in Fig. 2.4. The space vector $\vec{x}$ rotates at an arbitrary speed ω with respect to the *abc* stationary frame.

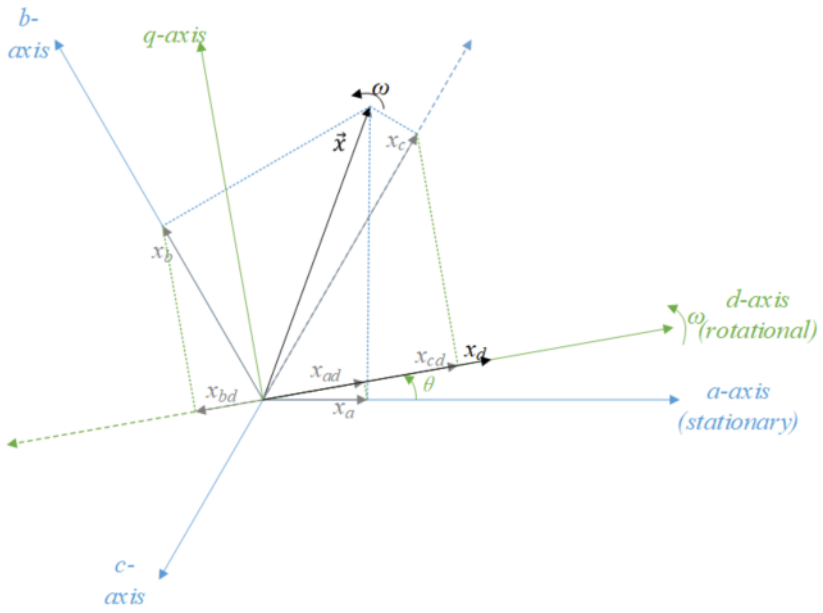

Figure 2.4: The *abc*- and *dq*-frame Coordinate System

A set of three variables in *abc* stationary frame can be transformed into a set of two independent variables in the *dq*-frame plus a 0-sequence term, where d and q refer to axes. In this case q-axis lead the d-axis by 90 degrees. The *dq*-frame is also known as the arbitrary rotating reference frame because it has an arbitrary position with respect to the *abc* stationary frame given by the angle $\theta(t)$. The *dq*-frame rotates in space at an arbitrary speed ω, which relates to $\theta(t)$ by $\omega = d\theta(t)/dt$. The zero-sequence term represents the component of the unbalanced phasors that is equal in magnitude and phase. In this thesis, the three-phase system is assumed to be three-phase balanced and, therefore, the zero-sequence term will always sum to be zero.

The variables in the abc stationary frame can be transformed to the *dq* rotational frame by projecting x_a, x_b, and x_c to the *dq*-axes as shown in Fig. 2.4. The sum of the projections onto the d-axis corresponds to the transformed x_d, and the sum of all projections on the q-axis corresponds to the transformed x_q. Only x_d is shown in Fig. 2.4. The transformation between the *abc* stationary frame and the *dq* rotational frame,

referred as abc/dq transformation, can be expressed using the Park's transformation (2.13).

$$\begin{bmatrix} x_d \\ x_q \\ x_0 \end{bmatrix} = \frac{2}{3} \begin{bmatrix} \cos\theta(t) & \cos\left(\theta(t) - 2\pi/3\right) & \cos\left(\theta(t) - 4\pi/3\right) \\ -\sin\theta(t) & -\sin\left(\theta(t) - 2\pi/3\right) & -\sin\left(\theta(t) - 4\pi/3\right) \\ 1/2 & 1/2 & 1/2 \end{bmatrix} \cdot \begin{bmatrix} x_a \\ x_b \\ x_c \end{bmatrix} \tag{2.13}$$

In the above abc/dq transformation:

- The coefficient of $2/3$ is a scalar added to the equation. There are two commonly used values: $2/3$ and $\sqrt{2/3}$. The advantage of using $2/3$ is that the amplitudes of the two-phase voltage components are equal to the three-phase voltage amplitudes under balanced operation after the transformation. On the other hand, the inverse transformation will have a simpler form. The advantage of using $\sqrt{2/3}$ is that the multiplication factor and net three-phase power remain unchanged after the transformation. $\sqrt{2/3}$ as a coefficient also enables the matrix to be Hermitian. The inverse of a Hermitian matrix is simply its transpose.

- The dq variables after the transformation contain the complete information of the three-phase abc variables if the 0-term sums to zero. However, for some types of unbalanced conditions, the 0-term will be nonzero.

The equation for the inverse transformation in (2.14), referred as the $dq0/abc$ transformation, can be obtained through matrix operations.

$$\begin{bmatrix} x_a \\ x_b \\ x_c \end{bmatrix} = \begin{bmatrix} \cos\theta(t) & -\sin\theta(t) & 1 \\ \cos\left(\theta(t) - 2\pi/3\right) & -\sin\left(\theta(t) - 2\pi/3\right) & 1 \\ \cos\left(\theta(t) - 4\pi/3\right) & -\sin\left(\theta(t) - 4\pi/3\right) & 1 \end{bmatrix} \cdot \begin{bmatrix} x_d \\ x_q \\ x_0 \end{bmatrix} \tag{2.14}$$

Assuming that $\vec{x}$ rotates at the same speed as the reference for the dq-frame, then

the angle from d-axis to $\vec{x}$ is constant. This is referred to as a synchronous reference frame. The resultant x_d and x_q are constant under balanced steady-state operation. This is one of the advantages of the abc/dq transformation, where the steady-state three-phase AC variables can be replaced by two constant terms.

Both the control strategy and the dynamic model of DFIG are going to be presented in the synchronous reference frame. In this case, the rotating speed of the arbitrary reference frame, ω, given by $\omega = 2\pi f$, is chosen differently depending on the application. For instance, "f" is set to 60 Hertz for the grid side converter and to the slip frequency for the rotor side converter. The angle $\theta_s(t)$ used in the grid side converter control can be found from (2.15), where θ_0 is the initial angular position of reference with respect to the AC system.

$$\theta_s(t) = \int_0^t \omega_s(t)dt + \theta_0 \tag{2.15}$$

The benefits of implementing the control strategy and dynamic models in synchronous dq-frame are listed as follows:

- The transformation reduces a three-phase AC system to an equivalent two-phase DC system in steady-state. The three-phase sinusoidal command tracking problem in the controller is transformed to two equivalent DC commands in the dq-frame, which can be easily controlled by a PI compensator. A PI regulator can achieve zero steady-state phase error when the reference is constent.

- Control of instantaneous power can be achieved in the dq-frame.

- In the dq-frame, the time-varying mutually coupled inductances of the DFIG are transformed to equivalent constant parameters.

- Components of large systems are formulated and analyzed in dq-frame. Therefore, representing the VSC system and the machine in dq-frame allows analysis and

design tasks of the power system to be performed in a unified framework.

2.5 Dynamic Model of DFIG in dq-Frame

For this particular machine, assume three phase windings are balanced for both the stator and the rotor. That is, all three stator windings are assumed to have the same number of effective turns, N_s, and the three windings are symmetrically displaced 120° apart. The rotor windings are arranged the same, but with N_r turns. The subscript 's' is used to denote the parameters for the stator, the subscript 'r' is used to denote the parameters for the rotor, and the symbol ψ is used to denote the flux. The machine is also assumed to be supplied by a constant and balanced three-phase AC voltage. Under an idealized model, the relationship between instantaneous stator voltages, currents, and fluxes of the machine can be described in the stationary abc-reference frame by the following electrical equations [17]:

$$V_{as}(t) = R_s i_{as}(t) + \frac{d\psi_{as}(t)}{dt} \tag{2.16}$$

$$V_{bs}(t) = R_s i_{bs}(t) + \frac{d\psi_{bs}(t)}{dt} \tag{2.17}$$

$$V_{cs}(t) = R_s i_{cs}(t) + \frac{d\psi_{cs}(t)}{dt} \tag{2.18}$$

Similarly, the rotor equations are described by:

$$V_{ar}(t) = R_r i_{ar}(t) + \frac{d\psi_{ar}(t)}{dt} \tag{2.19}$$

$$V_{br}(t) = R_r i_{br}(t) + \frac{d\psi_{br}(t)}{dt} \tag{2.20}$$

$$V_{cr}(t) = R_r i_{cr}(t) + \frac{d\psi_{cr}(t)}{dt} \tag{2.21}$$

The differential equations representing the DFIG model can be redefined in the synchronous dq reference frame. According to Section 2.3, this rotational reference

frame rotates at the synchronous speed ω_s, and the space vector associated with it does not rotate. The 0-sequence term is calculated to be zero since the system is three-phase balanced for this development. The response to unbalanced faults will be examined later.

The voltage equations in dq-frame are:

$$v_{sd} = R_s i_{sd} + \frac{d\psi_{sd}}{dt} - \omega_s \psi_{sq} \tag{2.22}$$

$$v_{sq} = R_s i_{sq} + \frac{d\psi_{sq}}{dt} + \omega_s \psi_{sd} \tag{2.23}$$

$$v_{rd} = R_r i_{rd} + \frac{d\psi_{rd}}{dt} - s\omega_s \psi_{rq} \tag{2.24}$$

$$v_{rq} = R_r i_{rq} + \frac{d\psi_{rq}}{dt} + s\omega_s \psi_{rd} \tag{2.25}$$

The flux linkage equations in the dq-frame are:

$$\psi_{ds} = L_s i_{ds} + L_m i_{dr} \tag{2.26}$$

$$\psi_{qs} = L_s i_{qs} + L_m i_{qr} \tag{2.27}$$

$$\psi_{dr} = L_m i_{ds} + L_s i_{dr} \tag{2.28}$$

$$\psi_{qr} = L_m i_{qs} + L_s i_{qr} \tag{2.29}$$

The electrical model of the DFIG in the dq-frame is shown in Fig. 2.5 [18].

Using the model above, the equations for the electric power flow on the stator and rotor can be stated in the synchronous reference frame as follows, assume $i_{0s} = i_{0r} = 0$, $V_{ds0} = 0$ and $V_{dr0} = 0$:

$$P_s = 3Re\left\{\vec{V_s} \cdot \vec{I_s^*}\right\} = \frac{3}{2}(v_{ds} \cdot i_{ds} + v_{qs} \cdot i_{qs}) \tag{2.30}$$

$$P_r = 3Re\left\{\vec{V_r} \cdot \vec{I_r^*}\right\} = \frac{3}{2}(v_{dr} \cdot i_{dr} + v_{qr} \cdot i_{qr}) \tag{2.31}$$

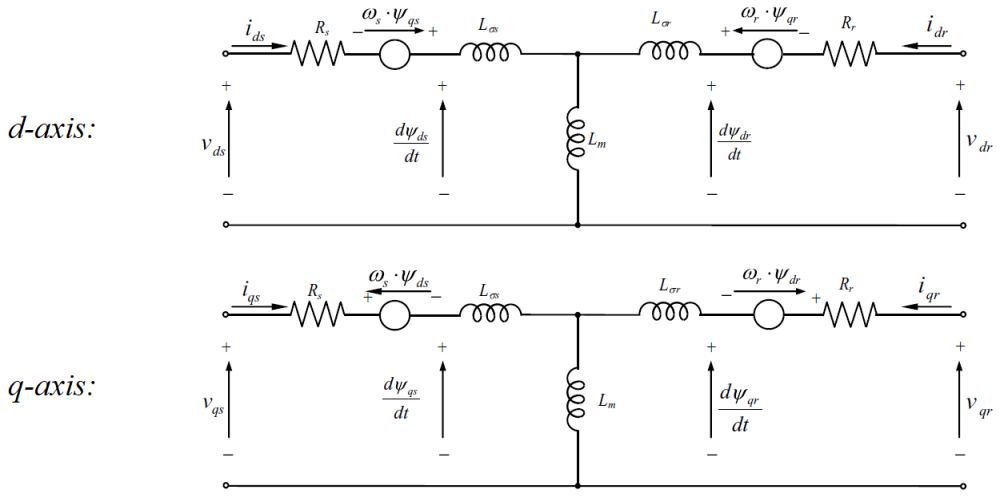

Figure 2.5: The electrical model of DFIG in dq-frame.

$$Q_s = 3Im\left\{\vec{V_s} \cdot \vec{I_s^*}\right\} = \frac{3}{2}(v_{qs} \cdot i_{ds} - v_{ds} \cdot i_{qs}) \tag{2.32}$$

$$Q_r = 3Re\left\{\vec{V_r} \cdot \vec{I_r^*}\right\} = \frac{3}{2}(v_{qr} \cdot i_{dr} - v_{dr} \cdot i_{qr}) \tag{2.33}$$

Finally, the electromagnetic torque can be expressed as:

$$T_r = \frac{3}{2}P\frac{L_m}{L_s}Im\left\{\vec{\psi_r} \cdot \vec{i_r^*}\right\} = \frac{3}{2}P\frac{L_m}{L_s}(\psi_{qs} \cdot i_{dr} - \psi_{ds} \cdot i_{qr}) \tag{2.34}$$

This dynamic model can be written in state-space equations which will be useful for computer-based simulation purposes.

CHAPTER 3

Two-Level Voltage Source Converter Topology

The voltage source converter topology is widely used in industry for many different applications. When the converter transforms a fixed DC voltage to a three-phase AC voltage with controlled magnitude and frequency and transfers power from DC to AC, it is referred as an inverter. When the converter transforms an AC voltage to an adjustable DC voltage, it is referred as an active rectifier. The power flow in the converter is bidirectional. The VSC system can be implemented using two-level converters or multilevel converters (more than two levels). The multilevel converter can produce less harmonics and provide higher voltage capability than the two-level converters, but they require more switches and are harder to control. In the DFIG, two two-level VSC systems are implemented and connected in a back-to-back configuration, as shown in Fig. 3.1. In most common configurations, the converters can each perform as both inverters and rectifiers. However, in some old designs, power flow may not be bidirectional.

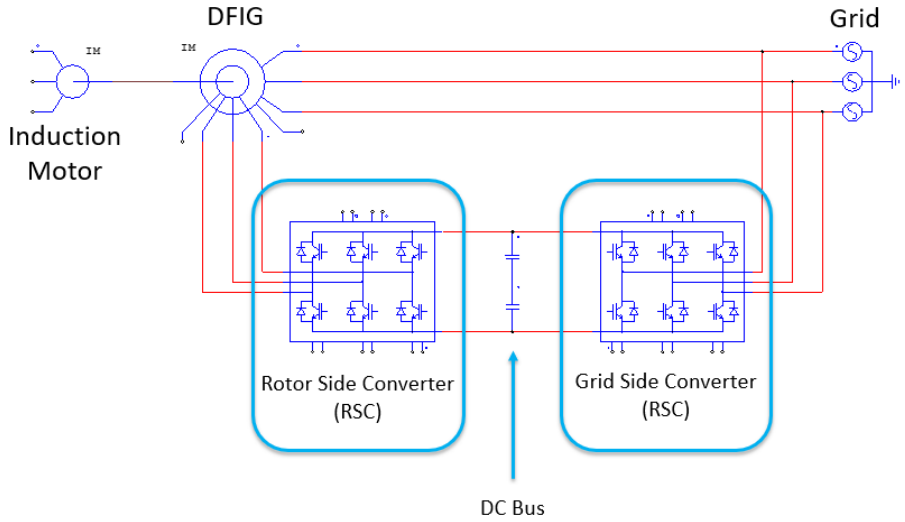

Figure 3.1: Configuration of DFIG Wind Generation System

In this chapter, the two-level three phase VSC is modeled. Since pulse width modulation (PWM) schemes can improve the performance of both the inverter and

rectifier, PWM schemes are implemented for each converter in the back-to-back converter.

The VSC is difficult to control with simple proportional-integral (PI) compensator because the variables in the AC power system are sinusoidal functions of time. The steady-state phase error of PI controllers in a stationary reference frame is large. As a result, the converter is modeled and controlled in dq-frame to simplify control design and accomplish better accuracy as discussed in Section 2.3.

3.1 Converter Model

The converter is composed of six switches, S_1 to S_6, with an antiparallel diode for each switch, as shown in Fig. 3.2. The switches can be IGBT or MOSFET devices, or other gate turn-off capable devices, depending on the power and voltage rating of the converter.

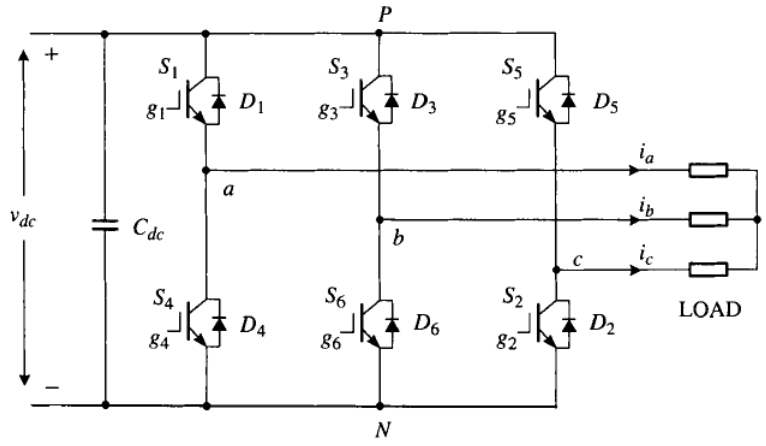

Figure 3.2: Two-level voltage-source converter (VSC) Topology [19]

The VSC contains three legs where each produces one of the three phase voltages. Each leg is a half-bridge converter, and it operates based on alternate switching. Both sinusoidal PWM and space vector PWM are real-time modulation technique that can be used to control the grid side converter (GSC) and the rotor side converter (RSC).

3.2 Modulation Schemes

In this section, carrier-based sinusoidal PWM scheme is first introduced, followed by a detailed analysis of space vector modulation algorithms.

3.2.1 Sinusoidal PWM

Sinusoidal PWM is the most common PWM strategy for converters and is easier to implement than SVPWM. It produces switching commands by comparing a high-frequency periodic triangular waveform with the desired signal. In the hardware implementation in this thesis, the switching command is calculated and controlled by a microcontroller .

A. Switching Pulse Generation

In this scheme, the switching commands of the upper and lower switches on a leg are issued through comparison of two signals: a high frequency periodic triangular waveform referred as carrier signal, and a slow- varying waveform known as the modulating signal. The intersections of the carrier wave and the modulating signal determine switching instants for the devices. The PWM process is illustrated in Fig. 3.3, with a very low carrier frequency for clarity of illustration.

As shown in Fig. 3.3, v_{ma}, v_{mb}, and v_{mc}, are the three-phase sinusoidal modulating waveforms and v_{cr} is the triangular carrier signal. Since each of the three legs operates in an identical fashion, only phase-a and phase-b are shown in detail in Fig. 3.3 as an example. When the modulating signal intersects the carrier signal, a turn-on command and a turn-off command is issued for each switch in the leg respectively. The upper and lower switches on the same leg operate in a complimentary manner. When implementing the switches in hardware, a dead time should be implemented, where both switches on the same leg are turned off to avoid possible short-circuiting

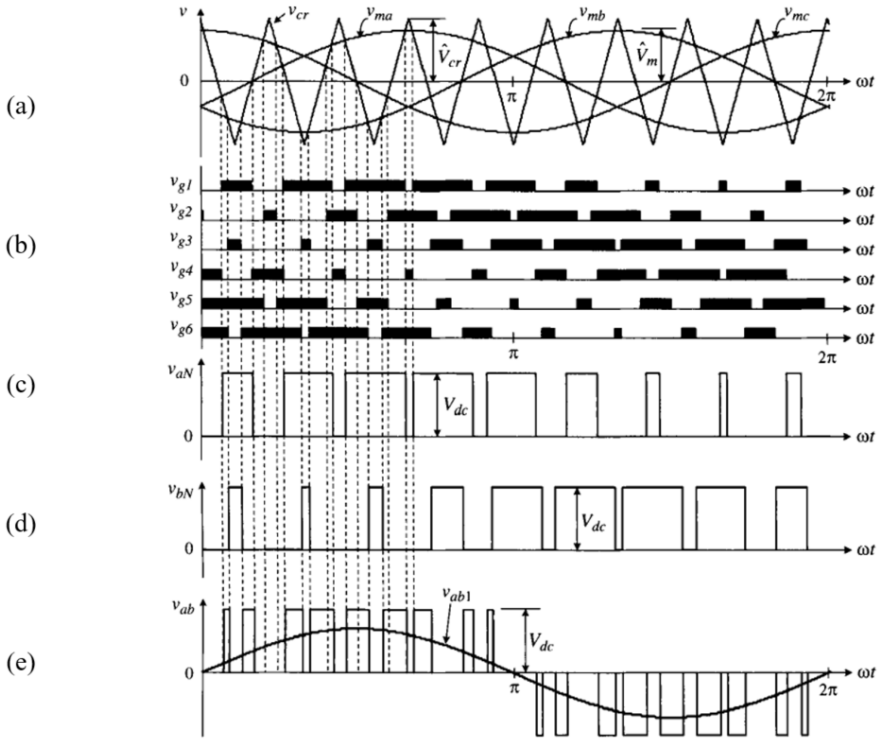

Figure 3.3: Sinusoidal Pulse Width Modulation (SPWM) [20]

of the DC bus by one leg during switching transients. Dead time also enables the device that is turning off to regain its ability to block voltage before the other device is turned on.

B. Modulation Index and Limitations

The low frequency component of each phase of the inverter output voltage can be described by the amplitude-modulation index (3.1),

$$m_a = \frac{\hat{V}_m}{\hat{V}_{cr}} \tag{3.1}$$

where $\hat{V}_m$ and $\hat{V}_{cr}$ are the peak magnitude of the modulating and carrier waves, respectively. The subscript "a" denotes phase-a. The amplitude of $\hat{V}_{cr}$ is usually kept constant, and the amplitude-modulation index m_a is adjusted by varying $\hat{V}_m$. Note that for the converter to work properly, m_a should be kept between 0 and 1. The

frequency modulation index is defined by (3.2).

$$m_f = \frac{f_{cr}}{f_m} \tag{3.2}$$

Where f_m and f_{cr} are the frequencies of the modulating and carrier waves, respectively. The switching frequency f_{sw} is same as f_{cr}. When carrier frequency is an integer multiple of the modulating frequency, the modulation is known as synchronous PWM, where only harmonics of integer multiples of frequency of modulation wave will be generated. Non-integer subharmonics, as generated by this method, are more of a problem in power generation, transmission, and distribution. The carrier frequency of an asynchronous PWM is fixed and independent of its modulating frequency. However, it may generate non-integer harmonics.

The resultant converter terminal voltages v_{aN}, v_{bN} and v_{cN}, which are the voltages at the terminal of each of the converter phases with respect to the negative DC bus N. The converter is referred as a two-level voltage source converter since the waveforms of v_{aN}, v_{bN} and v_{cN} have only two levels, V_{dc} and 0. The fundamental components of v_{aN}, v_{bN} and v_{cN} can be defined as sinusoidal waves oscillating at the modulation frequency and a peak to peak voltage of $m_a \cdot V_{dc}$. The inverter line-to-line voltage v_{ab} can be determined by $v_{aN} - v_{bN}$. The fundamental component of v_{ab} is shown in Fig. 3.3(e) as v_{ab1}.

3.2.2 Space Vector Pulse Width Modulation

As an alternative to the sinusoidal PWM method, the switching command can be calculated using space vector pulse width modulation (SVPWM). The SVPWM scheme significantly reduces switching harmonics compared to the SPWM [22]. It is because SVPWM varies the phase voltage level by changing switching state on only one leg at a time. SVPWM scheme also reduces switching loss and allows a higher peak output

Table 3.1: Space Vector Switching States

Switch States				
No.	Encode	On Switches	Off Switches	Space Vector
1	100	S_1, S_6 and S_2	S_4, S_3 and S_5	$\vec{V_1} = \frac{2}{3}V_{dc}e^{j0}$
2	110	S_1, S_3 and S_2	S_4, S_6 and S_5	$\vec{V_2} = \frac{2}{3}V_{dc}e^{j\frac{\pi}{3}}$
3	101	S_4, S_3 and S_2	S_1, S_6 and S_5	$\vec{V_3} = \frac{2}{3}V_{dc}e^{j\frac{2\pi}{3}}$
4	011	S_4, S_3 and S_5	S_1, S_6 and S_2	$\vec{V_4} = \frac{2}{3}V_{dc}e^{j\pi}$
5	001	S_4, S_6 and S_5	S_1, S_3 and S_2	$\vec{V_5} = \frac{2}{3}V_{dc}e^{j\frac{4\pi}{3}}$
6	101	S_1, S_6 and S_5	S_4, S_3 and S_2	$\vec{V_6} = \frac{2}{3}V_{dc}e^{j\frac{5\pi}{3}}$
7	111	S_1, S_3 and S_5	S_4, S_6 and S_2	$\vec{V_0} = 0$
8	000	S_4, S_6 and S_2	S_1, S_3 and S_5	$\vec{V_0} = 0$

voltage compared to SPWM.

Switching States and Dwell Time Calculation

The space vector modulation method generates the pulses for the controlled switches based on the space vector based principle. The operating status of the switches in the two-level inverter are represented by eight switching states. The eight switching states are described in Table 3.1.

The column "Encode" indicates the switching states of the six switches. A "1" denotes that the upper switch in an inverter leg is on and lower switch in the same leg is off. The inverter terminal voltage (v_{aN}, v_{bN} or v_{cN}) at the instant is positive ($+V_{dc}$). Whereas "0" is the opposite case of "1". The eight switching states can be divided into six active states and two zero states. When plotted on an $\alpha\beta$-plane, the active state vectors describe the vertices of a regular hexagon with sides of length equal to $\frac{2}{3}V_{dc}$, as shown in Fig. 3.4, where the two zero state vectors lie at the center of the hexagon.

Assume that the operation of the inverter is always going to be three-phase balanced, we can write (3.3).

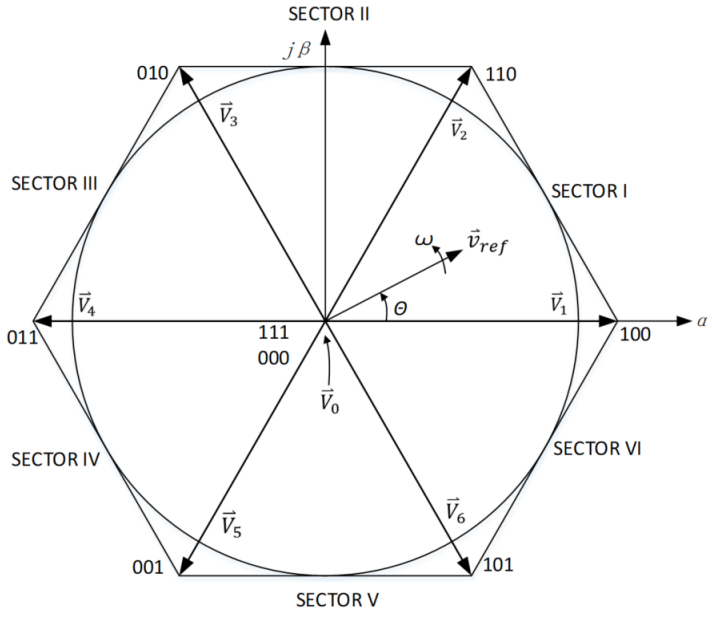

Figure 3.4: Space-Vector Diagram

$$V_a(t) + V_b(t) + V_c(t) = 0 \tag{3.3}$$

Where V_a, V_b, and V_c are the instantaneous phase output voltages at the AC inverter terminals. Based on (3.3), from a mathematical point of view, one of the phase voltages is redundant. Therefore, the $\alpha\beta$-frame transformation to a two axis stationary frame is implemented using (3.4). Note that this is a special case of equation (2.13) where $\theta = 0$.

$$\begin{bmatrix} v_\alpha(t) \\ v_\beta(t) \end{bmatrix} = \frac{2}{3} \begin{bmatrix} 1 & -\frac{1}{2} & -\frac{1}{2} \\ 0 & \frac{\sqrt{3}}{2} & \frac{\sqrt{3}}{2} \end{bmatrix} \cdot \begin{bmatrix} v_a(t) \\ v_b(t) \\ v_c(t) \end{bmatrix} \tag{3.4}$$

The $\alpha\beta$-frame will map the three-phase voltage into a two-dimensional Cartesian vector (3.5).

$$\vec{v}(t) = v_\alpha(t) + jv_\beta(t) = 0 \tag{3.5}$$

In the $\alpha\beta$-frame, the zero and active state vectors do not move in space, as described in Table 3.1. The reference vector $\vec{v}_{ref}$ in Fig. 3.4 rotates in space at an angular velocity ω. The angular displacement between $\vec{v}_{ref}$ and the α-axis of the $\alpha\beta$-frame can be obtained by θ. If the sampling period Tsw is small enough, the reference vector $\vec{v}_{ref}$ can be considered constant during Tsw. Under this assumption, $\vec{v}_{ref}$ can be approximated by the superposition of two adjacent active vectors and one zero vector. Based on this assumption, the switching states of the inverter is selected and gate signals for the active switches can be generated. For example, when $\vec{v}_{ref}$ falls into sector I, as shown in Fig. 3.5, it can be synthesized by a time based combination of $\vec{V}_1$, $\vec{V}_2$, and $\vec{V}_0$.

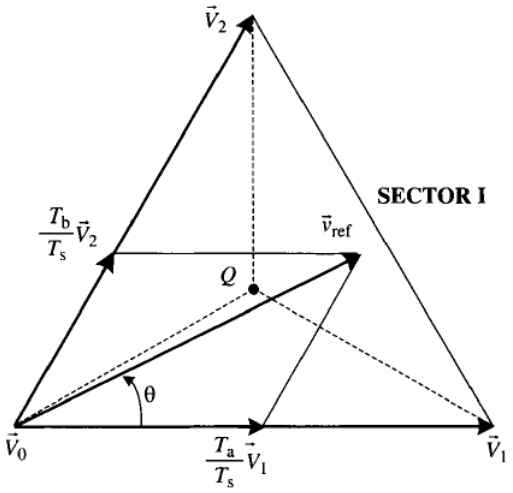

Figure 3.5: $\vec{v}_{ref}$ Synthesized by $\vec{V}_1$, $\vec{V}_2$, and $\vec{V}_0$ [23]

Where the dwell time in the states, T_a, T_b, and T_0 can be calculated using (3.6), where v_{ref} represents the magnitude of $\vec{v}_{ref}$.

$$\begin{cases} T_a = \frac{\sqrt{3}T_{sw}v_{ref}}{V_{dc}} \sin\left(\frac{\pi}{3} - \theta\right) \\ T_b = \frac{\sqrt{3}T_{sw}v_{ref}}{V_{dc}} \sin\left(\theta\right), \quad for \quad 0 \leq \theta \leq \frac{\pi}{3} \\ T_0 = T_{sw} - T_a - T_b \end{cases} \tag{3.6}$$

Similarly, when $\vec{v}_{ref}$ is in sector II, the calculated dwell times T_a, T_b, and T_0 are

for vectors $\vec{V}_1$, $\vec{V}_2$, and $\vec{V}_0$ and so on. When $\vec{v}_{ref}$ is in sectors II, III, ...VI, a multiple of $\pi/3$ is subtracted from the actual angular displacement θ such that the modified angle falls into the range between zero and $\pi/3$, where the number of multiples is one less than the sector number.

When $\vec{v}_{ref}$ passes through the sectors one by one, different sets of switches will be turned on or off. As a result, when $\vec{v}_{ref}$ rotates one revolution in space, the inverter output voltage varies though one fundamental frequency cycle over time. The inverter output frequency corresponds to the rotating speed of $\vec{v}_{ref}(\omega)$, whereas its output voltage can be adjusted by the magnitude of $\vec{v}_{ref}$.

As stated, the reference $\vec{v}_{ref}$ can be synthesized by three stationary vectors. The dwell times for each of the stationary vectors represent the duty-cycle of the chosen switches during a sampling period T_{sw}. The dwell time calculation is based on the volt-second balance principle, where product of the reference voltage $\vec{v}_{ref}$ and sampling period T_{sw} equals the sum of the voltage multiplied by the time interval of the chosen space vectors. Using the results of (3.6), T_a, T_b, and T_0 in (3.7) are the dwell times for the vectors $\vec{V}_1$, $\vec{V}_2$, and $\vec{V}_0$, respectively.

$$\begin{cases} \vec{v}_{ref} T_{sw} = \vec{V}_1 T_a + \vec{V}_2 T_b + \vec{V}_0 T_0 \\ T_{sw} = T_a + T_b + T_0 \end{cases} \tag{3.7}$$

B. Switching Sequence for SVPWM

In general, the switching sequence design for a given $\vec{v}_{ref}$ is not unique, however, to minimize the switching frequency, the switching sequence should satisfy the following two requirements:

- The transition from one switching state to the next involves only two switches in the same inverter leg, one being switched on and the other switched off.

- The transition for $\vec{v}_{ref}$ moving from one sector in the space vector diagram to the next requires no or a minimum number of switch transitions.

A typical switching sequence is listed in Table 3.2.

Table 3.2: Switching Sequence and Time

	Switch States						
Sector No.	$T_0/4$	T_a	T_b	$T_0/2$	T_b	T_a	$T_0/4$
Sector I	7	2	1	8	1	2	7
Sector II	7	2	3	8	3	2	7
Sector III	7	4	3	8	3	4	7
Sector IV	7	4	5	8	5	4	7
Sector V	7	6	5	8	5	6	7
Sector VI	7	6	1	8	1	6	7

C. Modulation Index and Limitations for SVPWM

Next, apply a modified definition of the modulation index, m, in (3.8), where v_{ref} represents the peak value of the fundamental frequency component in the inverter output phase voltage.

$$m = \frac{\sqrt{3}v_{ref}}{V_{dc}} \tag{3.8}$$

The relationship between m and the rms value of the phase voltage v_{ph} can be expressed with (3.9). For a given DC voltage, V_{dc}, the modulation index ,m, is inversely proportional to the output voltage.

$$m = \frac{\sqrt{3}v_{ref}}{V_{dc}} = \frac{\sqrt{6}V_{ph}}{V_{dc}} \tag{3.9}$$

The maximum length of the reference vector, $\vec{v}_{ref,max}$, corresponds to the radius of the largest circle that can be inscribed within the hexagon, as shown in Fig. 3.4. Since the hexagon is formed by six active vectors having a length of $2V_{dc}/3$, $\vec{v}_{ref,max}$ can be found from (3.10).

$$v_{\vec{ref},max} = \frac{2}{3}V_{dc} \times \frac{\sqrt{3}}{2} = \frac{V_{dc}}{\sqrt{3}} \tag{3.10}$$

Substituting (3.10) into the definition of m (3.8), gives the maximum modulation index equals to 1 and the range of the modulation index for the SVPWM scheme is (3.11).

$$0 \leq m \leq 1 \tag{3.11}$$

3.3 Modelling Two-Level Voltage Source Converter

The two-level three phase voltage source converter is the main building block of the back-to-back converter that connects the rotor of DFIG to the power grid. Both the rotor side converter (RSC) and the grid side converter (GSC) will produce controllable three phase signals through their AC side terminals. In this thesis, space vector modulation is implemented in experimental hardware tests due to its benefits in reduced power loss. Therefore, the AC side terminal voltages can be written as (3.12-14).

$$V_{ta}(t) = \frac{V_{DC}}{\sqrt{3}} m_a(t) \tag{3.12}$$

$$V_{tb}(t) = \frac{V_{DC}}{\sqrt{3}} m_b(t) \tag{3.13}$$

$$V_{tc}(t) = \frac{V_{DC}}{\sqrt{3}} m_c(t) \tag{3.14}$$

Where $m_a(t)$, $m_b(t)$, and $m_c(t)$ each represent one of the three phase modulation signals (3.15-17).

$$m_a(t) = \hat{m}(t) \cos\left[\varepsilon(t)\right] \tag{3.15}$$

$$m_b(t) = \hat{m}(t)\cos\left[\varepsilon(t) - 120^\circ\right] \tag{3.16}$$

$$m_c(t) = \hat{m}(t)\cos\left[\varepsilon(t) + 120^\circ\right] \tag{3.17}$$

Where $\varepsilon(t)$ indicates the phase angle and frequency of each sinusoidal signal. As mentioned in Chapter 2, when a three-phase system is modeled in the synchronous dq-frame, the sinusoidal command is transformed to an equivalent DC command. A PI compensator would have a hard time controlling a sinusoidal wave due to the steady-state phase error, however, a PI controller can acheive zero steady-state phase error when tracking a DC command. Hence, the VSC is modelled and controlled in the synchronous dq-frame.

3.3.1 Model of Two-Level VSC in dq-frame

A dq-frame representation of the two-level VSC can be developed by using the methodology introduced in Section 2.3. Substituting for the three-phase voltage equations and modulation equations in (2.13) will result in (3.18) and (3.19).

$$V_t(t) = (V_{td} + jV_{tq})\, e^{j\varepsilon(t)} \tag{3.18}$$

$$m(t) = (m_d + jm_q)\, e^{j\varepsilon(t)} \tag{3.19}$$

Equations (3.12-14) describe the relationship between the modulation signal and its corresponding terminal voltage of a two-level VSC. In the dq-frame, the multiplication factor does not change. Substituting (3.18) and (3.19) into $\vec{V_t}(t) = \frac{V_{DC}}{2}\vec{m}(t)$, results in (3.20).

$$(V_{td} + jV_{tq})\, e^{j\varepsilon(t)} = \frac{V_{DC}}{\sqrt{3}}\,(m_d + jm_q)\, e^{j\varepsilon(t)} \tag{3.20}$$

Therefore, the terminal voltage can be rewritten in dq-frame as (3.21) and (3.22).

$$V_{td}(t) = \frac{V_{DC}}{\sqrt{3}} m_d(t) \tag{3.21}$$

$$V_{tq}(t) = \frac{V_{DC}}{\sqrt{3}} m_q(t) \tag{3.22}$$

Equations (3.21) and (3.22) indicate that the d-axis and q-axis components of the VSC AC-terminal voltage are linearly proportional to the d-axis and q-axis components of the modulation signal. The two-level VSC can be described by two linear, time-varying subsystems in dq-frame. The AC-side terminal instantaneous power can be written in the dq-frame as (3.23) and (3.24), assuming $i_0 = 0$ and $V_0 = 0$.

$$P_t(t) = \frac{3}{2} \left(V_{td}(t) i_d(t) + V_{tq}(t) i_q(t) \right) \tag{3.23}$$

$$Q_t(t) = \frac{3}{2} \left(-V_{td}(t) i_q(t) + V_{tq}(t) i_d(t) \right) \tag{3.24}$$

Where $i_d(t)$ and $i_q(t)$ are the d-axis and q-axis components of the AC side terminal current. In the above power equations, if $V_{tq}(t) = 0$, the real and reactive power components are directly proportional to $i_d(t)$ and $i_q(t)$ respectively. This concept is very useful in the control of the grid side converter (GSC), as will be explained in detail in Chapter 4.

3.3.2 Classification and Application of VSC system

Two-level VSC systems can be classified to three main groups depending on their operating frequency and application: grid-imposed frequency VSC system; controlled-frequency VSC system; and variable-frequency VSC system. As the name implied, a grid-imposed frequency VSC system is connected to a stiff AC power system and the operating frequency is determined by a system tracking phase-locked loop. This operating frequency should be fairly constant. In a controlled-frequency VSC system, the AC terminal voltage frequency is directly controlled and regulated by the control

system. In a variable-frequency VSC system, the VSC is interfaced with an electric machine. The operating frequency is a state variable that depends on the system operating point and not directly controlled.

The grid-imposed frequency VSC system and variable-frequency VSC system are connected together to provide reliable control of the back-to-back converter that connects the rotor of the DFIG to the grid. The rotor side converter (RSC) is a variable-frequency VSC system that controls the voltage and current fed into the machine rotor depending on the machine rotating speed. The grid side converter (GSC) is a grid-imposed frequency VSC system that transfers controllable active and reactive power to a constant frequency grid. The control schemes for the RSC and GSC will be explained in detail and tested later in this thesis.

CHAPTER 4

Grid Side Converter

In this chapter, the control of the GSC is analyzed in detail. The GSC is a VSC system whose prime function is to exchange active power between the DC-bus and the AC system. When the DFIG is in the supersynchronous mode, the RSC is providing power to the DC-bus which results in a voltage rise on the DC-bus. The GSC regulates the DC-bus voltage to a constant reference value and transfers power from the DC-bus to the AC system to facilitate that regulation. When the DFIG is in the subsynchronous mode, the RSC is consuming power from the DC-bus and results in a voltage drop on the DC-bus. The GSC regulates the DC-bus voltage and transfers power from the AC system to the DC-bus to compensate for that drop. The GSC can also act like a STATCOM that provides reactive power to AC system. By doing so it can be used to increase the line power transmission, or to enhance the voltage/angle stability.

The control strategy of GSC is based on the grid-imposed frequency VSC system. The control theory is explained in detail, simulated in PSIM and then demonstrated in hardware.

4.1 Control Theory of Grid Side Converter

The active and reactive power in a two-level VSC system can be controlled by two methods, voltage-mode control or current-mode control. The voltage-mode control method controls the output active and reactive power by the phase angle and amplitude of the VSC AC-side terminal voltage relative to the PCC (Point of Common Coupling) voltage. This method is very simple and needs only one control loop, however, there is no control over the VSC line current. With this method, the VSC will not be protected against overcurrent. Since the switching devices in the VSC are

highly vulnerable to excess current, this proves to be problematic [24]. For this reason the current-mode control is implemented due to its fast line current regulation ability. By implementing the current-mode control, the VCS is protected against overcurrent conditions. The real and reactive power are separately controlled by adjusting the phase angle and the amplitude of the VSC line current with respect to the PCC voltage. The current control scheme will have two control loops, inner current control and power control. The current control scheme will be implemented in both the GSC and RSC .

4.1.1 Control Structure of Grid Side Converter

In the theoretical analysis, a two-level VSC is modeled by a lossless power processor including an equivalent DC-bus capacitor, a current source representing the VSC switching power loss and a series on-state resistance at the AC side representing the VSC conduction loss. Each phase of the VSC is interfaced with the AC system via a series RL branch. The AC power system is considered to be infinitely stiff. Therefore, it can be modeled as an ideal three-phase voltage source. It is also assumed to be balanced and operating at a relatively constant frequency around 60Hz. This AC system voltages at the point of common coupling (PCC) can be expressed as (4.1-3),

$$V_{sa}(t) = \hat{V}_s \cos(\omega_0 t + \theta_0) \tag{4.1}$$

$$V_{sb}(t) = \hat{V}_s \cos\left(\omega_0 t + \theta_0 - \frac{2\pi}{3}\right) \tag{4.2}$$

$$V_{sc}(t) = \hat{V}_s \cos\left(\omega_0 t + \theta_0 - \frac{4\pi}{3}\right) \tag{4.3}$$

where $\hat{V}_s$ is the peak value of the line to neutral voltage, ω_0 is the AC system source frequency, and θ_0 is the source initial phase angle. Each phase of the VSC is interfaced with the AC system via a series RL branch. The resistance is mostly wire

resistance between the VSC and the system. However, a fairly big inductor is needed to ensure the power transfer. Additionally, the RL combination acts as a lowpass filter which reduces switching harmonics at the point of interconnect.

Fig. 4.1 shows a schematic diagram of a current-controlled real/reactive power controller. Note that the control is performed in the synchronous dq-frame, with the benefits of using dq-frame control as discussed in Section 2.3. The power P_s and Q_s are controlled by the line current components i_d and i_q. The feedback current signals are measured at the converter terminals and the feedback voltage signals are measured at the line side PCC point. These signals are first transformed to the synchronous dq-frame based on the resultant angle from the PLL and then processed by PI compensators to produce the control signals. The control signals are transformed to the $\alpha\beta$-frame and fed to the SVPWM generator to control the switches. The reference current commands i_{dref} and i_{qref} are limited by saturation blocks to protect the VSC from overcurrent. Saturation blocks also protect against windup error of the PI compensatior. The real power reference P_{sref} is given by DC-bus voltage controller, and the reactive power reference Q_{sref} can be set to any desired value within the VSC system current limit. This control strategy is explained in detail in this chapter.

4.1.2 Dynamic Model of Real/Reactive Power Controller

The dynamics of the AC side of the VSC system in Fig. 4.1 are described by (4.4),

$$L\frac{d\vec{i}_{abc}}{dt} = -\left(R + r_{on}\right)\vec{i}_{abc} + \vec{V}_{tabc} - \hat{V}_{sabc}e^{j(\omega_0 t+\theta_0)} \tag{4.4}$$

where $\hat{V}_{sabc}e^{j(\omega_0 t+heta_0)}$ is the space-phasor representation of equations (4.1-3), and $\hat{V}_{sabc}$ is the peak value of the three-phase voltages. Then, expressing (4.4) in the dq-frame using $\vec{i}_{abc} = \vec{i}_{dq}e^{j\rho}$ and $\vec{V}_{tabc} = \vec{V}_{tdq}e^{j\rho}$ results in (4.5). Note that $f_{dq} = f_d + jf_q$.

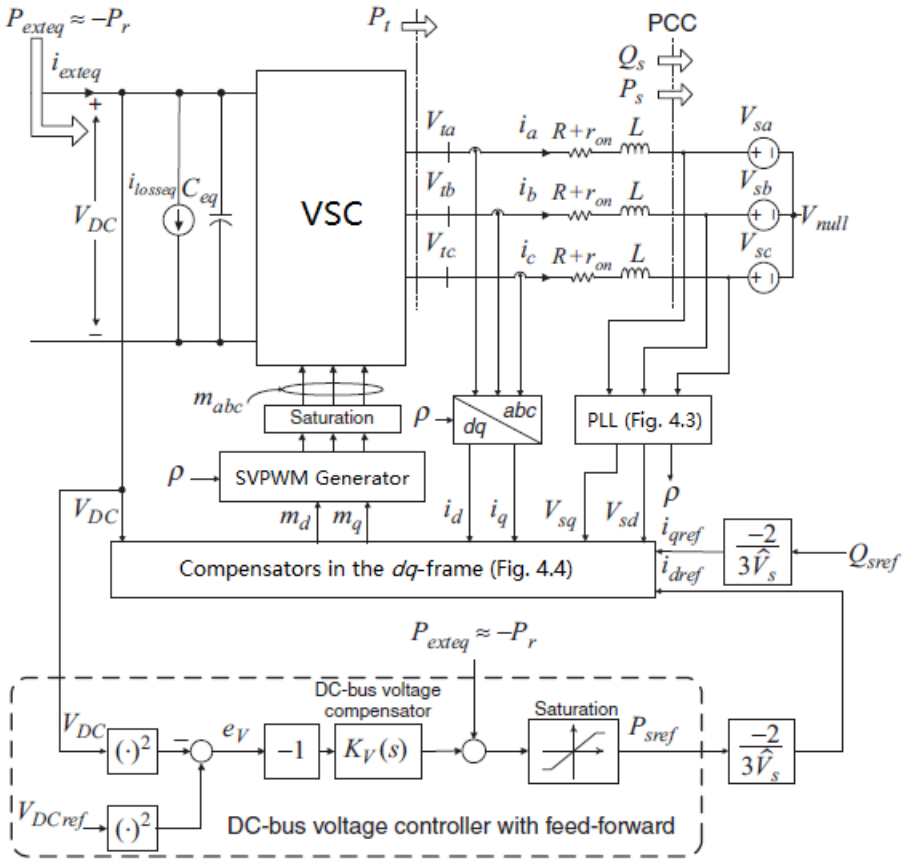

Figure 4.1: Schematic Diagram of a Current-controlled Real/Reactive Power Controller with a Controlled DC-Voltage Power Port in dq-frame[21]

$$L\frac{d\vec{i}_{dq}}{dt} = -j\left(L\frac{d\rho}{dt}\right)\vec{i}_{dq} - (R + r_{on})\,\vec{i}_{dq} + \vec{V}_{tdq} - \hat{V}_{sabc}e^{j(\omega_0 t+\theta_0-\rho)} \tag{4.5}$$

Then (4.5) is decomposed into real and imaginary components. In order to write the decomposed equations in standard state-space form, a new control variable ω is introduced, where $\omega = d\rho/dt$. This yields (4.6 - 8), where i_d, i_q, and ρ are the state variables, and V_{td}, V_{tq} and ω are the control inputs.

$$L\frac{di_d}{dt} = L\omega(t)i_q - (R + r_{on})\,i_d + V_{td} - \hat{V}_s\cos(\omega_0 t + \theta_0 - \rho) \tag{4.6}$$

$$L\frac{di_q}{dt} = -L\omega(t)i_d - (R + r_{on})\,i_q + V_{tq} - \hat{V}_s\sin(\omega_0 t + \theta_0 - \rho) \tag{4.7}$$

$$\frac{d\rho}{dt} = \omega(t) \tag{4.8}$$

Transforming the three-phase AC system voltages at the PCC expressed in the *abc*-frame in equations (4.1-3) into *dq*-frame results in (4.9) and (4.10).

$$V_{sd}(t) = \hat{V}_s \cos\left(\omega_0 t + \theta_0 - \rho\right) \tag{4.9}$$

$$V_{sq}(t) = \hat{V}_s \sin\left(\omega_0 t + \theta_0 - \rho\right) \tag{4.10}$$

The significance of performing control in *dq*-frame depends on proper selection of ω and ρ. Observing (4.9) and (4.10), if $\omega = \omega_0$, and $\rho(t) = \omega_0 t + \theta_0$, then $V_{sd}(t) = \hat{V}_s$ and $V_{sq} = 0$. Using $V_{sq} = 0$ rewrite (4.6-7), as (4.11-12).

$$L\frac{di_d}{dt} = L\omega_0 i_q - \left(R + r_{on}\right) i_d + V_{td} - V_{sd} \tag{4.11}$$

$$L\frac{di_q}{dt} = -L\omega_0 i_d - \left(R + r_{on}\right) i_q + V_{tq} \tag{4.12}$$

The equations above described a second order linear system that is excited by the constant input V_{sd}, where V_{sd} is the peak amplitude of the AC source phase voltage. Therefore, if control inputs V_{td} and V_{tq} are DC variables, state variables i_d and i_q should be also DC variables in steady-state. This is usually achieved through a synchronization mechanism which ensures $\rho(t) = \omega_0 t + \theta_0$. This mechanism is usually implemented as the phase-locked loop (PLL). When a PLL is applied, the control frequency is synchronized with the AC system frequency. Note that the V_{sq} term in (4.12) would disappear when a properly designed PLL is applied to align V_d with the peak of V_a. The structure, model and simulation of the PLL is presented in the following section.

4.1.3 Phase-Locked Loop (PLL)

Based on (4.10), $V_{sq} = 0$ results in $\rho(t) = \omega_0 t + \theta_0$. Therefore, a feedback controller is designed to regulate V_{sq} to zero based on (4.13).

$$\omega(t) = H(p)V_{sq}(t) \tag{4.13}$$

Where $H(p)$ is a linear transfer function (compensator) and $p = d(\cdot)/dt$ is a differentiation operator. Substituting for V_{sq} from (4.10) and (4.13), and substituting for $\omega(t)$ from (4.13) in (4.8), results in (4.14).

$$\frac{d\rho}{dt} = H(p)\hat{V}_s \sin\left(\omega_0 t + \theta_0 - \rho\right) \tag{4.14}$$

The above equation is referred as a PLL, and it is a nonlinear dynamic system. Under certain conditions, the PLL may lose track of system frequency. For example, given an initial condition of $\rho(0) = 0$ and $\omega(0) = 0$, then (4.14) is a sinusoidal function with frequency ω_0. If $H(p)$ is preforming a lowpass frequency response, a sinusoidal function with low frequency such as ω_0 will exhibit small perturbation, causing the PLL to fall into a limit cycle, and ρ does not track $\omega_0 t + \theta_0$. To prevent this, the initial condition of ω is set to ω_0, and it is limited to the lower and upper limits of ω_{min} and ω_{max} respectively. Where ω_{min} and ω_{max} are selected to be close to ω_0 since the power system frequency should only vary within a range of $\pm 5\%$. The control law can be expressed in (4.15).

$$\omega(0) = \omega_0, \quad and \quad \omega_{min} \leq \omega \leq \omega_{max} \tag{4.15}$$

If the PLL successfully tracks $\omega_0 t + \theta_0$, the term $\omega_0 t + \theta_0 - \rho$ is close to zero and $sin(\omega_0 t + \theta_0 - \rho) \approx (\omega_0 t + \theta_0 - \rho)$, and (4.14) can be simplified to (4.16).

$$\frac{d\rho}{dt} = H(p)\hat{V}_s\left(\omega_0 t + heta_0 - \rho\right) \tag{4.16}$$

The simplified equation creates a feedback control loop shown in Fig. 4.2, where $\omega_0 t + \theta_0$ is the reference input, ρ is the output, and $\hat{V}_s H(p)$ is the transfer function of the compensator.

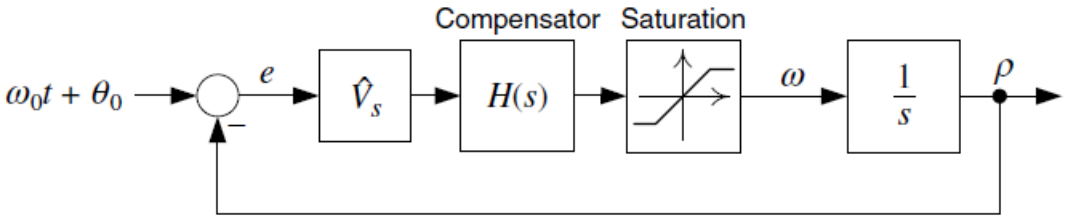

Figure 4.2: Basic Control Block Diagram of the PLL

Fig. 4.3 illustrates a PLL is implemented for a three-phase system which can be used in the GSC. Transformation from $\vec{V}_{sabc}$ to $\vec{V}_{sdq}$ is based on equations (4.8) and (4.10), and the resultant angle from the PLL.

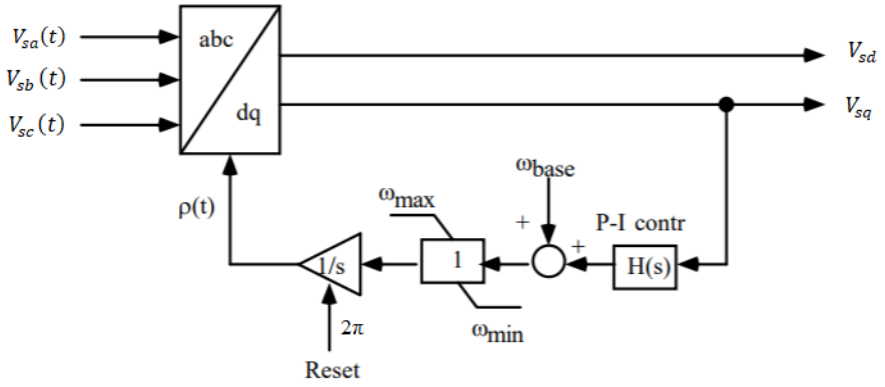

Figure 4.3: Three-Phase Implementation of the PLL

The rotational speed of the dq-frame is adjusted to the system frequency and V_{sq} is regulated to zero at steady-state. The end result is that $\rho(t) = \omega_0 t + \theta_0$ and $V_{sd}(t) = \hat{V}_s$. In the block diagram of Fig. 4.3, the resettable integrator whose output ρ is reset to zero whenever it reaches 2π.

4.1.4 Real and Reactive Power Control

Recall from Section 3.3.1, the AC-side terminal instantaneous power can be written in the *dq*-frame as (3.22) and (3.23). In the GSC, the feedback voltage signals are measured at the line side PCC point, where V_{sd} and V_{sq} are the AC system voltages in *dq*-frame and are not controlled by the VSC in this application. Equations (3.22) and (3.23) are rewritten with the system voltages as (3.20) and (3.21).

$$P_s(t) = \frac{3}{2}\left(V_{sd}(t)i_d(t) + V_{sq}(t)i_q(t)\right) \tag{4.17}$$

$$Q_s(t) = \frac{3}{2}\left(-V_{sd}(t)i_q(t) + V_{sq}(t)i_d(t)\right) \tag{4.18}$$

Implementing the PLL using the Park's transformation such that, $V_{sq} = 0$, allows (4.17) and (4.18) to be rewritten as (4.19) and (4.20).

$$P_s(t) = \frac{3}{2}V_{sd}(t)i_d(t) \tag{4.19}$$

$$Q_s(t) = -\frac{3}{2}V_{sd}(t)i_q(t) \tag{4.20}$$

Observing the equations above, $V_{sd}(t)$ is nearly constant and $i_d(t)$ and $i_q(t)$ can be controlled by the current controller, that is $i_d \approx i_{dref}$, and $i_q \approx i_{qref}$, then $P_s(t) \approx P_{sref}(t)$ and $Q_s(t) \approx Q_{sref}(t)$. Rearranging (4.19) and (4.20), leads to (4.21) and (4.22), and the current reference for inner-current control is calculated based on desired power references $P_{sref}(t)$ and $Q_{sref}(t)$.

$$i_{dref}(t) = \frac{2}{3V_{sd}}P_{sref}(t) \tag{4.21}$$

$$i_{qref}(t) = -\frac{2}{3V_{sd}}Q_{sref}(t) \tag{4.22}$$

If the processing speed of the controller allows fast reference tracking, the above equations indicate that $P_s(t)$ and $Q_s(t)$ can be independently controlled by $i_d(t)$ and

$i_q(t)$ respectively. Since $V_{sd}(t)$ is a DC variable in steady-state, current references $i_{dref}(t)$ and $i_{qref}(t)$ are also DC variables when power references $P_{sref}(t)$ and $Q_{sref}(t)$ are constant signals. Therefore, the VSC power control is achieved with DC variables in the dq-frame.

4.1.5 VSC Current Control

In this thesis, space vector modulation is implemented to provide switching commands due to its advantages on converter utilization and reduction of switching harmonics. Based on this modulation rule, the relationship of output voltages of GSC at the VSC terminals and modulation index can be expressed as (4.23) and (4.24).

$$V_{td}(t) = \frac{V_{DC}}{\sqrt{3}} m_d(t) \tag{4.23}$$

$$V_{tq}(t) = \frac{V_{DC}}{\sqrt{3}} m_q(t) \tag{4.24}$$

The voltage feedback measurements are at the AC system PCC instead of the VSC terminals. Recall equations (4.11) and (4.12), where i_d and i_q are state variables, V_{td} and V_{tq} are control inputs, and V_{sd} and V_{sq} are the feedback voltage signals that are measured. Due to the presence of $L\omega_0$ terms, the dynamics of i_d and i_q are cross-coupled. To decouple the dynamics, they are subtracted when determining m_d and m_q as shown in (4.25) and (4.26) respectively.

$$m_d = \frac{\sqrt{3}}{V_{DC}} \left(u_d - L\omega_0 i_q + V_{sd} \right) \tag{4.25}$$

$$m_q = \frac{\sqrt{3}}{V_{DC}} \left(u_q + L\omega_0 i_d + V_{sq} \right) \tag{4.26}$$

Where u_d and u_q are two new control signals. The purpose of decoupling the current components is to apply control to i_d and i_q independently through two PI compensators. Substituting m_d and m_q from (4.25) and (4.26) into the space vector

modulation law calculates VSC terminal voltages. Then substitute the resulting V_{td} and V_{tq} in the steady-state operation conditions into (4.11) and (4.12), leading to (4.27) and (4.28).

$$L\frac{di_d}{dt} = -\left(R + r_{on}\right) i_d + u_d \tag{4.27}$$

$$L\frac{di_q}{dt} = -\left(R + r_{on}\right) i_q + u_q \tag{4.28}$$

The result equations describe two decoupled, first order, linear systems. Fig. 4.4 illustrates the block diagram of the VSC current controller. The control signals u_d and u_q are the outputs of two compensators.

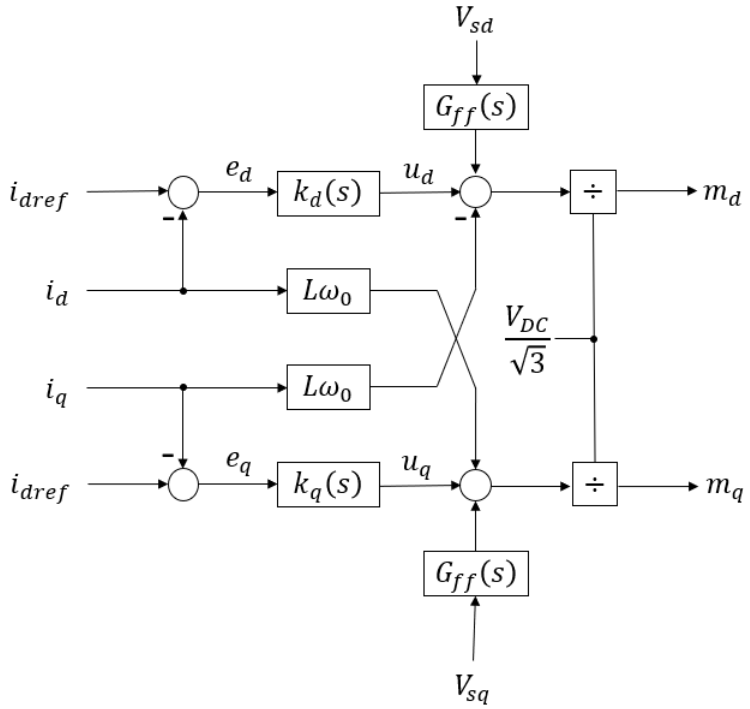

Figure 4.4: Control Block Diagram of a Current-Controlled VSC System

In Fig. 4.4, i_{dref} and i_{qref} are the current references calculated from the power reference, and i_d and i_q are the measured VSC terminal current components in the dq-frame. The d-axis compensator processes the error signal $e_d = i_{dref} - i_d$, and provides u_d. Similarly, the q-axis compensator processes the error signal $e_q = i_{qref} - i_q$, and

provides u_q. Based on equations (4.25) and (4.26), modulation signals m_d and m_q are calculated from u_d and u_q with measured voltage and current components. Finally, switching signals are generated through the space vector modulation scheme with m_d and m_q. The VSC generates V_{td} and V_{tq} corresponding to m_d and m_q, and controls i_d and i_q as a result.

It is significant to point out that in Fig. 4.4, the i_d and i_q current control loops are identical if the system is normally three-phase balanced. As a result, the corresponding compensators are identical, for instance $k_d(s) = k_q(s)$. Since the compensators are designed to track DC reference commands, $k_d(s)$ and $k_q(s)$ can be simple PI compensators. Given the typical structure of a PI compensator (4.29).

$$k_d(s) = \frac{k_p s + k_i}{s} \tag{4.29}$$

Where k_p is the proportional gain and k_i is the integral gain of the compensator. The open current loop gain in 4.4 is (4.30).

$$e(s) = \left(\frac{k_p}{Ls}\right) \frac{s + \frac{k_i}{k_p}}{s + \frac{R+r_{on}}{L}} \tag{4.30}$$

The open-loop transfer function shows that the plant pole is at $s = -(R+r_{on})/L$. Since $R + r_{on}$ is significantly smaller than L, this real pole is located close to the origin. The phase of the open loop gain starts to drop from a low frequency and it is cancelled by the compensator zero at $s = k_i/k_p$. Assuming the open-loop gain has the form of $e(s) = k_p/L_s$, the close-loop transfer function $e(s)/(1 + e(s))$ can be written as (4.31).

$$\frac{I_d(s)}{I_{dref}(s)} = \frac{1}{\tau_i s + 1} \tag{4.31}$$

Where k_p and k_i are calculated by (4.32) and (4.33).

$$k_p = \frac{L}{\tau_i} \tag{4.32}$$

$$k_i = \frac{R + r_{on}}{\tau_i} \tag{4.33}$$

Where τ_i is the time constant of the resultant closed-loop system. The parameter τ_i can be chosen depending on the design goals. The integral time constant τ_i should be made small for fast current control response. In this thesis, the bandwidth of the closed-loop control system $1/\tau_i$ is 10 times the switching frequency (in rad/s).

The same PI compensator values can be used in $k_q(s)$ for q-axis current regulation.

4.1.6 DC-Bus Voltage Level Selection and Control

The previous section presented the current control loop of the real-/reactive-power controller, whose function is to control the bidirectional real and reactive power exchanged between the AC system and the DC-bus by current regulation. Since there is no DC voltage source to maintain the DC voltage level, the DC-bus voltage must be regulated by an outer voltage loop based on the AC current control. The GSC is modeled very similar to a typical STATCOM with the RSC is replaced by a controlled power source shown in Fig. 4.1. The power source is assumed to exchange a time varying power with the DC-bus. The feedback mechanism compares V_{DC} with its reference command and accordingly adjusts P_s, such that the net power exchanged with the DC-bus capacitor is kept at zero. As explained in previous sections, P_s and Q_s can be independently controlled. In this thesis, Q_s is regulated to zero. As a result, the GSC will be operating at unity power factor.

A. Selection of DC-bus voltage level

The selection of DC-bus voltage is based on the gate control method implemented. In the case of SVPWM, the DC-bus voltage relationship to the AC voltage can be

expressed by (4.34), where $\vec{v}_{ref,max}$ is the maximum voltage magnitude of the fundamental frequency component in the inverter output phase voltage.

$$\vec{v}_{ref,max} = \frac{2}{3} V_{dc} \times \frac{\sqrt{3}}{2} = \frac{V_{dc}}{\sqrt{3}} \tag{4.34}$$

In practice, DC-bus voltage is selected larger than $\sqrt{3} \cdot \vec{v}_{ref,max}$ to make sure that the GSC does not experience overmodulation.

B. Model of Controlled DC-Voltage Power Port

The main control objective of the DC-voltage power port is to regulate the DC-bus voltage, V_{DC}. In the system shown in Fig. 4.1, the power balance is formulated as (4.35), where $P_{loss} = V_{DC} \cdot i_{loss}$, $P_t = P_{DC} = V_{DC} \cdot i_{DC}$, and the derivative term is the rate of change in energy stored in the DC-bus capacitor.

$$\left(\frac{C}{2}\right) \frac{dV_{DC}^2}{dt} = P_{ext} - P_{loss} - P_t \tag{4.35}$$

In the equation above, P_t is the control input, P_{ext} and P_{loss} are the disturbance inputs, and V_{DC}^2 is the state variable and the output. Since the GSC system of Fig. 4.1 enables control of P_s and Q_s independently, the control input P_t is expressed in terms of P_s. Consider the system in the $\alpha\beta$-frame, where (4.4) is written without the rotational term $e^{j(\omega_0 t + \theta_0)}$. Then multiply both sides of (4.4) in $\alpha\beta$-frame by $(3/2)\vec{i}^*$to get power. The real-part of the resultant equation is solved for P_t as (4.36).

$$P_t = P_s + \frac{3}{2}\left(R + r_{on}\right)\hat{i}^2 + \frac{3L}{2} Re\left\{\frac{d\hat{i}^2}{dt}\right\} \tag{4.36}$$

The term $\frac{3L}{2} Re\left\{\frac{d\hat{i}^2}{dt}\right\}$ is the instantaneous power absorbed by the three-phase inductor bank L which averages to zero, and $\frac{3}{2}\left(R + r_{on}\right)\hat{i}^2$ is the instantaneous power dissipated by the resistance of the three-phase inductor. Practically, $(R + r_{on})$ is a

small resistance and its associated power is negligible compared to P_t and P_s. However, the three-phase inductor is relatively large due to its ability to ensure power transfer. Since in a high-power VSC the switching frequency is limited by power loss considerations, L must be adequately large to also suppress the voltage switching harmonics. Furthermore, since the dq-frame current controllers are fast, $\vec{i}$ can undergo rapid phase and amplitude changes, during the real/reactive-power command tracking process. The definition of the instantaneous active/reactive power and the instantaneous complex power is written as (4.37).

$$S(t) = P(t) + jQ(t) = \frac{3}{2}\vec{v}(t)\vec{i^*}(t) \tag{4.37}$$

Applying the complex-conjugate operator to (4.37) and multiplying the resultant by (4.37), leads to (4.38).

$$P_s^2 + Q_s^2 = \frac{9}{4}\hat{V}_s^2\hat{i}^2 \tag{4.38}$$

Transferring $\hat{i}$ in dq-frame and substituting in (4.38) in (4.36) we obtain (4.39).

$$P_t = P_s + \left(\frac{2L}{3\hat{V}_{sd}^2}\right) P_s \frac{dP_s}{dt} + \left(\frac{2L}{3\hat{V}_{sd}}\right) Q_s \frac{dQ_s}{dt} \tag{4.39}$$

Substituting for P_t from (4.39) back into (4.35), we have (4.40).

$$\frac{dV_{DC}^2}{dt} = \frac{2}{C}\left[P_{ext} - P_{loss} - P_s + \left(\frac{2LP_s}{3\hat{V}_{sd}^2}\right)\frac{dP_s}{dt} + \left(\frac{2LQ}{3\hat{V}_{sd}^2}\right)\frac{dQ_s}{dt}\right] \tag{4.40}$$

As shown in Fig. 4.1, V_{DC}^2 is compared with V_{DCref}^2, the error signal is processed by the compensator $K_v(s)$, and the command P_{sref} is issued for the real-power controller. The real-power controller, in turn, regulates P_s at P_{sref}, while Q_s can be independently controlled. Q_{sref} can be set to a nonzero value if an exchange of

reactive power with the AC system is required.

4.2 GSC Circuit Simulation Implementation

The RSC is simulated in PSIM (PowerSim). PSIM is a software specifically designed for power electronics. A few PSIM add-on packages were useful when designing the DFIG driver system, such as the Motor Drive Module containing built-in electric machine models and mechanical load models for motor drive system studies. The Digital Control Module provides discrete library elements such as zero-order hold, z-domain transfer function, etc. The SimCoder package contains library elements that enable automatic code generation for various DSPs from Texas Instruments.

PSIM provides a convenient method for iterative hardware testing as shown in Fig 4.5. PSIM allows engineers to design, simulate, and ultimately implement functional hardware for use in power systems [26]. First, the schematic of the main power circuit is implemented with PSIM model elements and the control algorithms described earlier in the chapter are implemented with control algorithm blocks. Next based on the results from the simulation plots, the control parameters can be finalized. Finally, with the auto code generation feature, the control performance on the DSP can be validated with a processor-in-loop test, where validation is simplified by using the computer to simulate a power system. The hardware is then ready to be tested if the processor-in-loop results meet the design requirements and performance is as expected. Overall, PSIM provides an efficient and safe environment for iterative power-system hardware design. Note that SIMVIEW is a waveform processing program that plots the results from the simulator engines.

The GSC circuit can be categorized into four main blocks: power circuit, input measurement circuit, control circuit, and protection logic circuit. The power circuit consists of the isolation transformer, inductor bank; switching devices and two capacitors. They are connected as shown in Fig. 4.6. Sensors are used to measure voltages

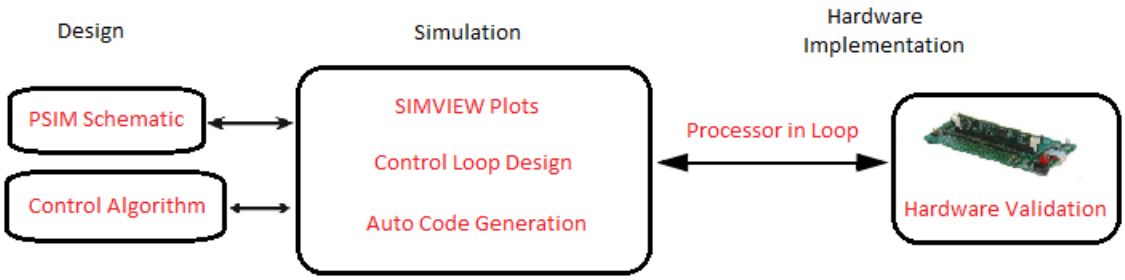

Figure 4.5: Control Design Procedure

and currents from the power circuit and pass them to the control circuit. Possible measurement errors are considered in the sensor circuit. The control circuit is represented in block diagrams. Components such as computational blocks and digital control blocks are used in the control circuit. Gating signals are generated from the control circuit and sent to the switching devices through the 3-phase PWM block. A minimum required protection circuit is implemented to protect the GSC from internal faults in the IGBT module and overcurrent/overvoltage due to possible control errors. Both the power circuit and sensor circuit part of the schematic simulate the hardware testbed, but no code will be generated for the DSP at this stage. The control circuit and the protection logic will later be generated into code and eventually flashed onto the DSP to achieve the control of the GSC.

4.2.1 Power Circuit

The power circuit is simulated in PSIM as shown in Fig. 4.6. The three-phase power system is ideal, meaning the frequency of the system is fixed at 60Hz and it could supply infinite power. The transformers are connected delta-to-delta as shown in the configuration to provide isolation from the converter to the power system. The ratio of the transformers is set to be 1:1, since system voltages do not need to be stepped up or down. The short circuit test and open circuit test were performed on the transformer to get the winding parameters to enter in the simulation.

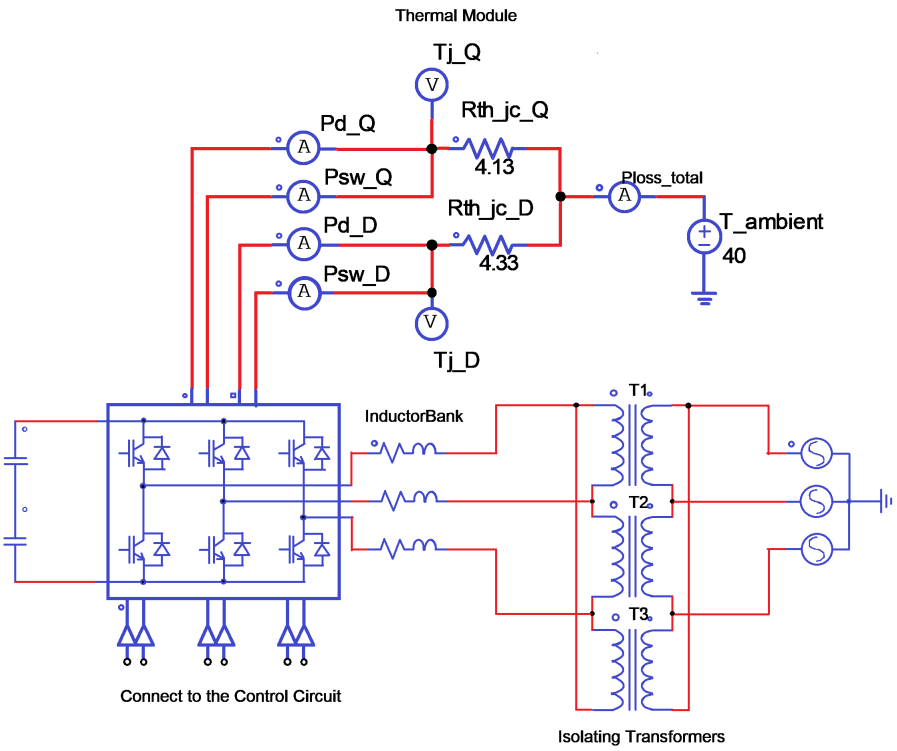

Figure 4.6: Power Circuit in PSIM

The three-phase inductor values are set to actual measurements of a physical inductor bank in the lab. They are connected in series with the power system to add more inductance to the transformer. The control variables are very sensitive to the resistance between the converter to the system, and the main contributors of this resistance are the winding resistance of the transformer and the inductor bank, so sizing of the inductor bank could be very critical. Changing the inductor would require retuning of the control variables. The inductor bank is necessary here for two main reasons; (1) the inductor allows power transfer by creating a phase shift to the voltage angle in respect to the current, and (2) it acts as a filter on the AC side that mitigates the high frequency noise created by the converter switching.

The switching device characteristic is modeled in the simulation based on the plots from the 6-pack IGBT module datasheet for the devices to be implemented in hardware testing. The 6-pack IGBT module consists of 5 power ports that connect

to the DC bus and the three-phase system, and 6 signal ports that receive switching commands from the control circuit. The additional circuitry at the top of Fig. 4.6 makes up the thermal module. The thermal module models the heat losses of the IGBT. The switching and conduction losses have been broken into four current signals shown as the additional outputs above the IGBT module. Two of them are the switching and conduction losses of the switch, and the other two are the switching and conduction losses of the diodes. Voltage in the thermal circuit is the temperature value in degrees-Celsius, and current in the thermal circuit is the power losses in Watts. The resistors represent thermal equivalent junction impedance from the switch/diode to the case. The total losses are calculated as summed currents at one node and going into the ambient temperature of 40 degrees Celsius. The junction temperature measured is used to pick the right loss characteristic point as the IGBT losses are very thermally dependent. Note that these are just for simulating the losses and do not exist in the physical connection of the power circuit.

The voltage rating of the two capacitors are added to be big enough to tolerate the DC bus voltage ripple and the initial charging overshoot. The minimum capacitor value is calculated in (4.41) based on the maximum possible current flow in the back-to-back converter; the switching frequency and the tolerable voltage ripple.

$$C_{DC_{min}} = \frac{i_{r_{max}}}{\Delta V_d \cdot f_{sw}} \tag{4.41}$$

The capacitors used in this experiment are the two existing capacitors in the lab which are both rated at $4600\mu F$ and 450V.

4.2.2 Measurement Circuit

To provide control to the GSC, only two out of three phase voltages and currents need to be measured. The measurements of the third phase are only used for the

protective circuit to detect overvoltage and overcurrents. Both voltage and current measurements are polarity sensitive. The measurements are brought to DSP in a few steps as shown in Fig 4.7. The first half is done within the sensor circuit and is modeled to match the physical hardware. The second half is achieved in code. The power circuit voltages and currents are usually too high to be measured directly, therefore they are first stepped down to control signals though transducers. Then, an offset circuit is implemented to provide dc offset, so that the DSP A/D inputs are within 0-3 V. The signal is converted to a digital value in the DSP A/D, and mathematical calculations are applied to scale the measurements back to their original values. In this section, these steps will be explained in detail.

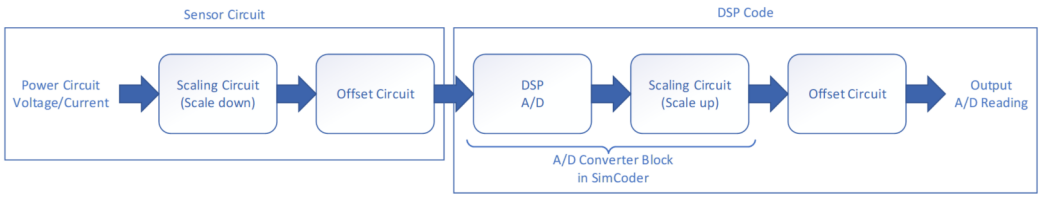

Figure 4.7: Input Measurement Flowchart

In PSIM all sensors provided are ideal. However, sensors never perform ideally in the same manner in reality. Different gains and offsets of the sensors need to be considered and voltage sensors and current sensors are modeled separately as follows:

(1) Voltage Sensor Model:

The voltage sensors are modeled in PSIM as shown in Fig. 4.8. The three-phase line voltages and the DC-bus voltage are measured with the same method. The ideal sensor is connected to the system voltages through a set of resistive voltage dividers. The gain and offset are then added to the ideal sensor based on the physical sensor calibration. Since voltage level of the DC-bus is different from the line-voltages, the resistor values are chosen differently. Offset is needed in this case because the DSP only reads 0-3 V analog signals.

(2) Current Sensor Model:

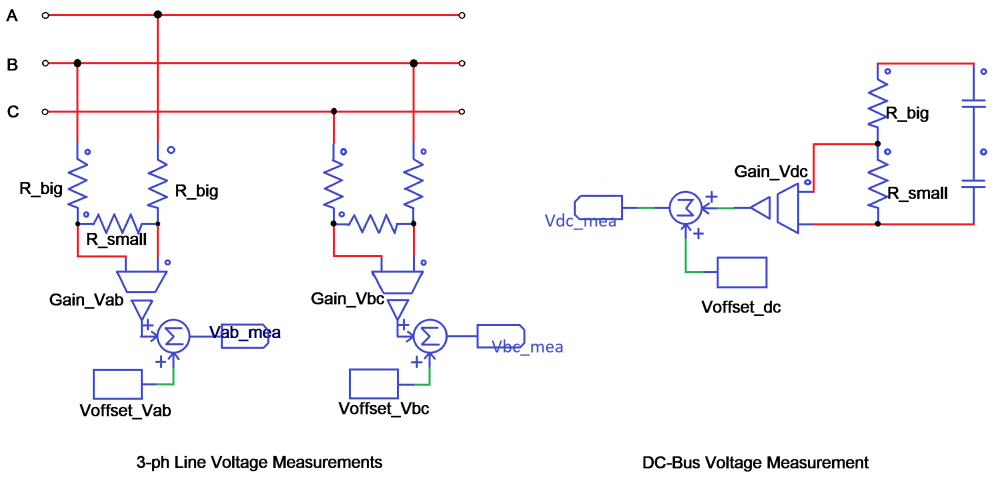

Figure 4.8: Voltage Sensor Models in PSIM

There are two methods for measuring the three-phase current, as shown in Fig. 4.9. In the first method, an ideal sensor is added in series with the line to be measured. The ideal sensor works the same way as a current transformer and it is assumed to measure the exact current flow in the phase with a simple gain ratio. In the second method, voltage is measured instead of current from the small resistive shunt in series with the three-phase system. The current is calculated from voltage and resistance by a simple divider. To obtain control signals in the range of 0-3 V, offsets are added to both methods based on the physical sensor calibration. Note that only phase A is shown in this example.

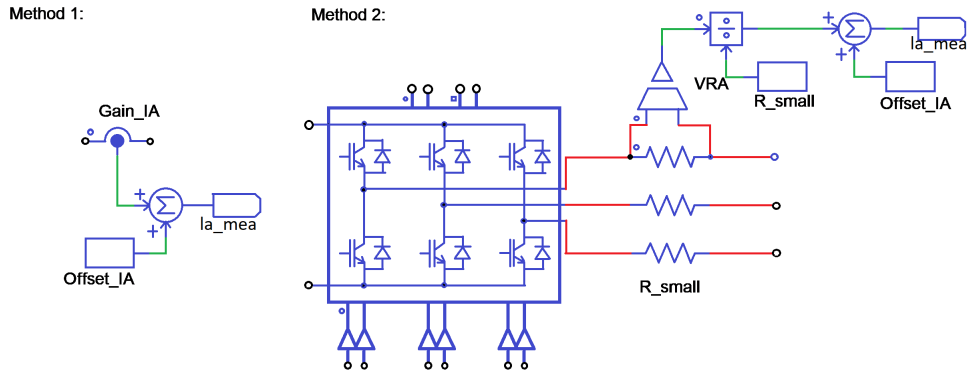

Figure 4.9: Current Sensor Model in PSIM

The measured voltage and current signals are taken to the DSP through the A/D

converter block as shown in Fig 4.10. The A/D converter block under the SimCoder package enables analog to digital signal conversion of the physical 12-bit 16-channel A/D converter on the DSP. The converter is set to the "Continuous Mode" so that the conversion is performed autonomously. The A/D converter block also has a built in scaling function and an offset function. The internal offset function has two modes: DC Mode and AC mode. The DC Mode will read 0-3 V signal without applying offset. The AC Mode will read -1.5 V to +1.5 V, and an offset of 1.5 V is applied by the converter block. In the circuit shown in Fig. 4.10, all ADC pins are set to DC Mode because each hardware sensor is calibrated and has slightly different offsets. The output is scaled and offset based on the calibration result. The input pins that are not in use will be connected to ground, so they read zeros instead of floating. In addition, a zero-order-hold (ZOH) block is used to determine sampling rate. The ZOH samples the input at the beginning of a clock cycle and holds the sampled value until the next clock cycle. For example, if the sampling frequency of ZOH is 10kHz, the samples will occur at 0., 0.0001 sec., 0.0002 sec., etc.

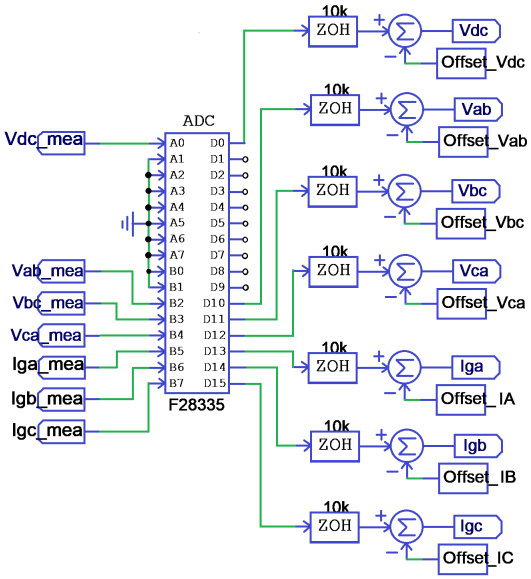

Figure 4.10: Analog to Digital Conversion (ADC) Process

4.2.3 Control Circuit

The control algorithm implemented in the simulation and hardware is simplified from the control theory explained earlier in the chapter. The simulated control circuit can be divided into three different steps: (1) phase locked loop and Park's transformation calculation, (2) the inner and outer control loops, and (3) the PWM switching signal generation. In this section, each step will be explained, and a simulation result is plotted with SIMVIEW.

(1) Phase locked loop and Park's transformation calculation:

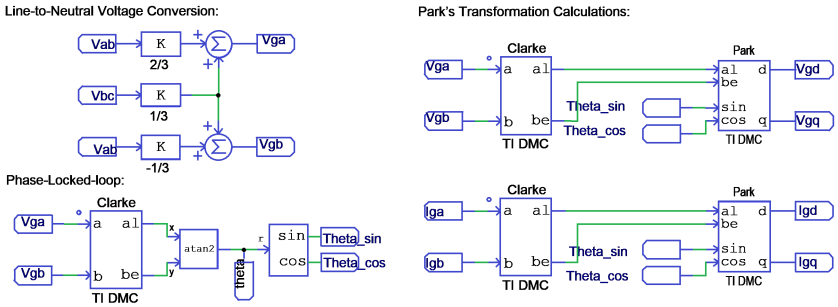

Figure 4.11: Phase Locked Loop and Park's Transformation Calculations in PSIM

According to the sensor section, line-to-line voltages are measured and sent to the control circuit with labels as shown in Fig. 4.11. Labels provide another way of connecting two or more nodes together. If nodes are connected to labels having the same name, these nodes are connected. Line-to-neutral voltage measurements are required to provide control calculations but line-to-line voltage are measured. This conversion is achieved by a gain block and an addition block according to (4.42). The line-to-neutral voltage is not scaled by a factor of $\sqrt{3}$.

$$\begin{bmatrix} V_{ga} \\ V_{gb} \end{bmatrix} = \begin{bmatrix} V_{an} \\ V_{bn} \end{bmatrix} = \frac{1}{3} \begin{bmatrix} 2 & 1 \\ -1 & 1 \end{bmatrix} \cdot \begin{bmatrix} V_{ab} \\ V_{bc} \end{bmatrix} \tag{4.42}$$

In the simulation, the phase-locked-loop is implemented with an arctangent function as shown in Fig 4.11. The Clarke transformation is applied to the phase voltages

where three-phase quantities are converted into balanced two-phase quadrature quantities. The results of the transformation are alpha and beta components, where alpha is in phase with the phase-A voltage and beta is 90 degree lagging the phase-A voltage. Since only two-phase voltages are taken as the input of the control circuit, and the system is assumed to be three-phase balanced, the abbreviated Clarke transformation equations are written as (4.43).

$$\begin{bmatrix} V_\alpha \\ V_\beta \end{bmatrix} = \begin{bmatrix} 1 & 0 \\ \frac{1}{\sqrt{3}} & \frac{2}{\sqrt{3}} \end{bmatrix} \cdot \begin{bmatrix} V_a \\ V_b \end{bmatrix} \tag{4.43}$$

Assume that the power system phasors are defined as a cosine function, meaning v_α (phase-A voltage) can be written as $cos(\omega t + \theta)$, and v_β can be written as $sin(\omega t + \theta)$ which is 90 degrees lagging phase-A. Apply "arctangent 2 block" to the signals, where the output of the block is given by $atan(y/x)$ as shown in Fig 4.11. The output of the block is an angle $\theta(t)$ in radians, ranging from $-\pi$ to $+\pi$. The result of system frequency is converted back to sine functions and used in the Park's transformation block to map measured voltage and current onto the dq-frame. The Park's transformation equations are in (4.44).

$$\begin{bmatrix} v_d \\ v_q \end{bmatrix} = \begin{bmatrix} cos\theta & sin\theta \\ -sin\theta & cos\theta \end{bmatrix} \begin{bmatrix} v_\alpha \\ v_\beta \end{bmatrix} \tag{4.44}$$

The result is plotted in Fig. 4.12 as function of time. The phase-A voltage is plotted as a reference. As expected, the output of the "atan" function is synchronized with the system frequency. The signal "V_{gd}" is the grid side voltage mapped on d-axis and the signal "V_{gq}" is the grid side voltage mapped on q-axis. When the system frequency does not vary significantly as shown in the plot, "V_{gd}" is constantly at the peak of system voltage; and "V_{gq}" it is constantly 0. This scheme will struggle a bit following disturbances compared to a PLL.

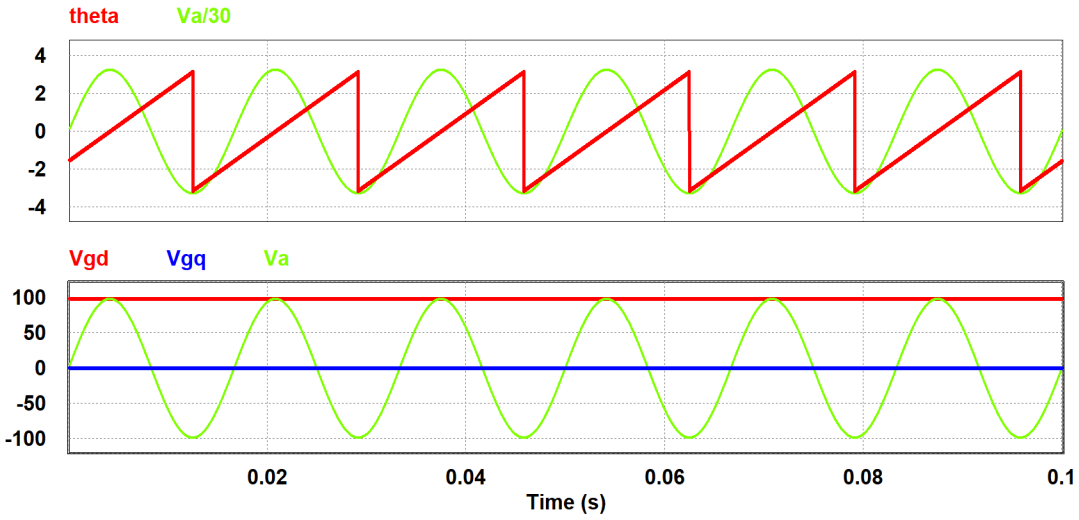

Figure 4.12: Plots of System Angle and Park's Transformation Calculation in SIMVIEW

(2) Inner and outer control loops:

The control scheme has a set of outer voltage/power control loops and inner current control loops shown in Fig. 4.13. Only active power can be transferred through the DC bus, so the DC bus voltage is directly influenced by active power flow. The measured DC bus voltage is compared with the DC bus voltage reference and the controller outputs the d-axis current reference through a PI controller block. Note this is a different scheme than the DC bus control scheme derived in Section 4.1.6.

Using (4.22), the q-axis current reference is directly calculated from the reactive power reference.

The inner control loops take the difference between the current references from the outer controls and the measured quantities to the PI controller and output modulating signals in the dq-frame. The inverse Park's transformation is applied to the modulating signals based on the system frequency. Since SVPWM scheme requires modulation signals to be in the stationary $\alpha\beta$-reference frame, the output of the control loops are the RSC terminal voltages in the stationary $\alpha\beta$-reference frame.

Note that the feedforward control and the current decoupling circuit need to very accurately model the system parameters, and are not implemented in the simulation at this stage. This will only influence the dynamic response of the system. Further testing is needed to finalize the circuit parameters, and the accurate control system can then be built.

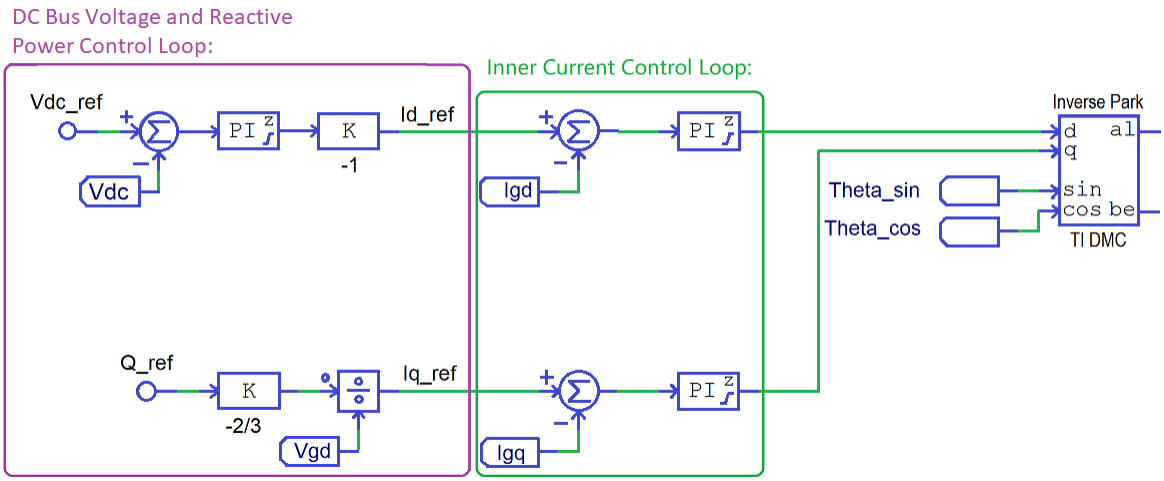

Figure 4.13: Control Loops in PSIM

The simulation results are shown in Fig. 4.14. The system starts with $V_{DC} = 0$ and the AC currents at 0. This does not represent a controlled start up. The signals in blue are the reference values and the signals in red are the measurements.Plot (a) shows the measured converter AC side current on d-axis and its reference; plot (b) shows the measured converter AC side current on q-axis and its reference; plot (c) shows the measured DC bus voltage and its reference; and plot (d) shows the measured reactive power and its reference. When the PI controllers are properly tuned, the measured signal should be tracking the reference signal.

As shown in (c), the DC bus voltage reference is set to 210 V and the measured voltage overshot for 0.15 seconds before settled down to the reference. The d-axis currents in (a) followed a similar trend as the DC bus voltage. The reactive power reference is set to zero at all times with the measured value exhibiting a start up

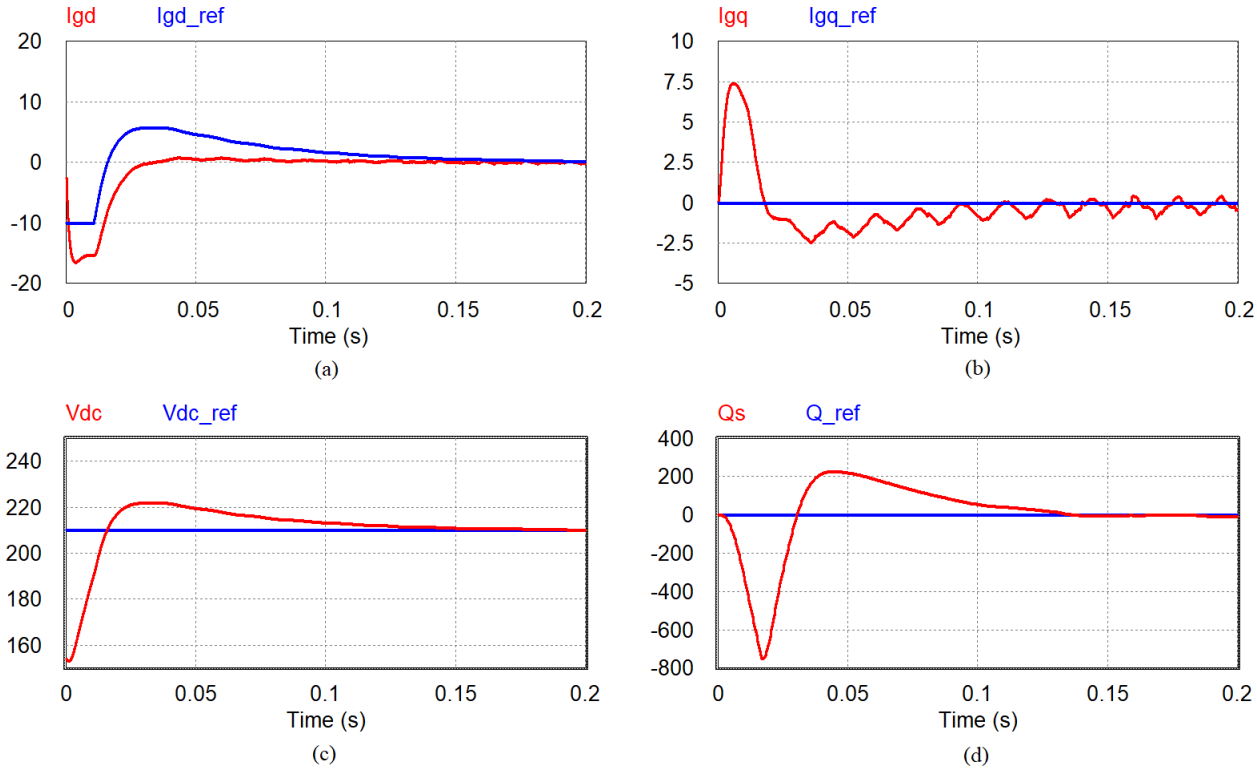

Figure 4.14: Plots of Controlled Variables in SIMVIEW: (a) Grid side converter terminal current on d-axis; (b) Grid side converter terminal on q-axis; (c) DC bus voltage; (d) Supplied reactive power

transient. The measured reactive power in (d) first flowed from the system into the converter when the capacitor is charging from 170 V to 222 V, and then reversed due to the DC voltage overshoot. Since the q-axis current reference is calculated from the reactive power reference by a constant factor of $-2/3$ and the reactive power reference is set to zero, q-axis current reference is zero as shown in (b). The measured q-axis current will follow a similar trend as the measured reactive power because the reactive power is related to the inductor and current by $Q = I^2 X_L$. The variation is not directly related to capacitor charging. It is because the converter terminal voltage is low until capacitors are charged.

(3) PWM switching signal generation:

The resultant stationary $\alpha\beta$-reference frame modulating signals from current regulators in Fig. 4.13 are then fed into the space vector generation block in PSIM shown

in Fig. 4.15. This block calculates the appropriate switching duty ratios needed to generate a given reference voltage using the space vector PWM technique in Section 3.2.2. The reference voltage is calculated by mapping its vector components in a stationary reference frame on the direct axis (alpha) and on the quadrature axis (beta) voltage commands. The outputs T_a, T_b, and T_c are duty ratio references for the switching functions in phases a, b, and c. The 3-ph PWM block is then used to generate PWM gating signals based on switching times. These signals are used as the commands for the six-switch converter. In the PSIM PWM generation block, a dead time can be set depending on the tolerance of the switching devices. It is very important to know if the switching device is active low or active high when setting up the PWM generation block. The result of an incorrect setting will not show in the simulation, and won't be visible until get to hardware implementation.

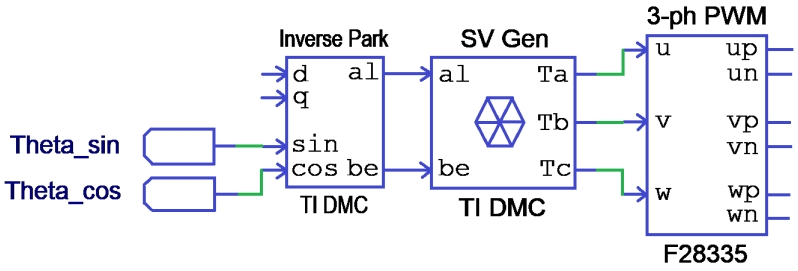

Figure 4.15: PWM Switching Command Generation in PSIM

In Fig. 4.15, "u", "v", and "w" refer to the three phases "a", "b", and "c". The letter "p" refers to the positive output, and "n" refers to the negative output.

4.2.4 Protection Logic Circuit

Since the simulation generates code for hardware, protection for circuit components should be modelled and tested in the simulation. In the GSC circuit, protection is mainly focused on the DC bus capacitors and the switching devices. The protection schemes implemented in PSIM are shown in Fig. 4.16 and Fig 4.17. Since the

capacitors are vulnerable to high voltage and the switching devices are vulnerable to high current, overvoltage protection is applied to the capacitor and overcurrent protection is applied to the converter. For the DC bus protection, a chopper circuit is chosen to discharge the excessive power on the DC bus. The switching signal of the chopper switch is generated by the microprocessor.

The main idea of the converter protection is when overcurrent is detected, the PWM generation stops and all converter switches are set to block all current. The PWM generation can only be re-enabled when human input and protection circuit agree. This protection scheme only applies when the switching devices are still in service. If this level of protection fails, back up protection is required to isolate the circuit from the AC system.

(1) DC Bus Overvoltage Protection:

Fig. 4.16 shows the PSIM schematic of DC bus overvoltage protection scheme. The magnitude of measured DC bus voltage (V_{dc}) is compared with the maximum tolerance of the capacitor voltage rating ($V_{dc_{max}}$) and the normal operation voltage level ($V_{dc_{ref}}$). The output of a comparator is high (value = 1) when the non-inverting input is higher than the inverting input, meaning when an overvoltage has been detected, signal "x1" goes high. The same goes for "x2" which is set low during the over voltage and will only go back to high once V_{dc} falls below the reference voltage. A FSM (Finite State Machine) is used to mimic the behavior of flip-flop circuit. The FSM code is written in C as:

If overvoltage is detected, the output signal "y1" will stay low (value = 0) until "x2" is activated. The output signal "y1" and the signal "manual trip" are taken into an "AND" gate to generate the digital switching signal of the chopper circuit. Note that the signal "manual trip" is a human input that is normally high until human action. The digital output will be generated at one of the GPIO ports from GPIO0 to GPIO87.

```
1
2   static int OV_state=0; //Over voltage state
3
4     switch (OV_state){
5       case 0:
6         if(x1 ){ //Above 430V
7           OV_state = 1; //Change to Over voltage state
8         }
9       break;
10      case 1:
11        if(x2 ){ //Below 400V
12          OV_state = 0; //
13        }
14      break;
15    }
16
17    switch (OV_state){
18      case 0:
19        y1 = 1; //Good state is output High
20      break;
21      case 1:
22        y1 = 0; //Bad state  is output Low
23      break;
24    }
```

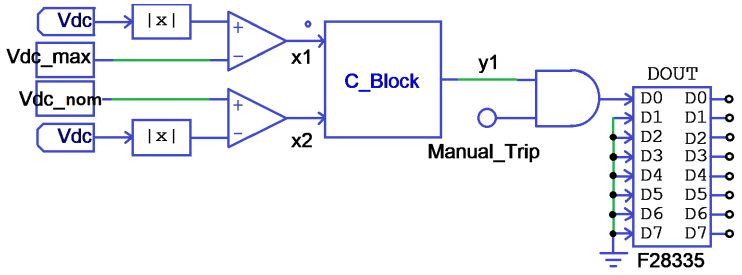

Figure 4.16: DC Bus Overvoltage Protection in PSIM

(2) Converter Overcurrent Protection:

Fig. 4.17 shows the PSIM schematic of converter overcurrent protection scheme. The measured three-phase instantaneous current amplitudes at the converter terminals are compared to the IGBT module current rating with the margin for control response. The outputs of the comparators are high during normal operation, therefore the output of "AND" gate is normally high until an overcurrent is detected. Most IGBT module have the ability to detect internal faults and output a digital trip signal. The trip signal is read by the digital input block, which is associated in the hardware with one of the GPIO pins from GPIO0 to GPIO87. This pin is then capable of generating an interrupt to the DSP in the case of a level change. Since both the internal fault trip signal and the trip-zone signal are active low in this case,

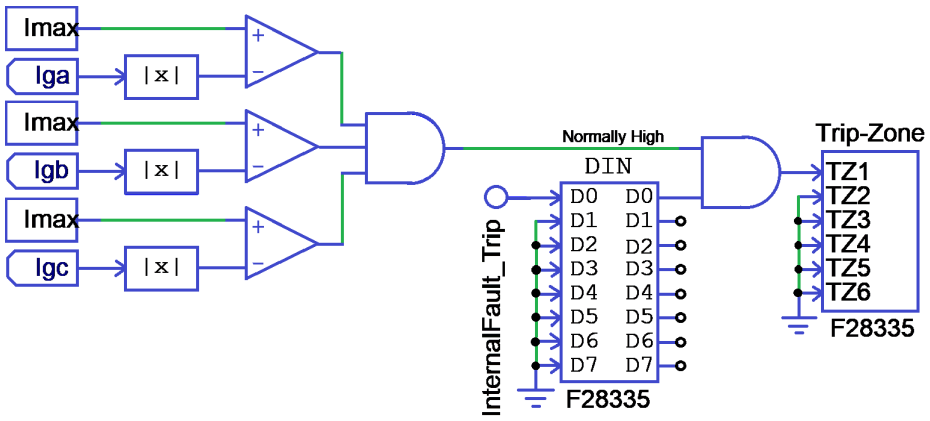

Figure 4.17: Converter Overcurrent Protection in PSIM

the trip-zone signal can be generated by an "AND" gate as shown in Fig. 4.17. The trip-zone 1 is activated in one-shot mode meaning once an overcurrent is detected, an interrupt will terminate PWM generation permanently, and set all converter switches to off mode. The PWM generator must be restarted to resume the operation.

4.3 Processor in Loop (PIL) Testing

Processor in Loop (PIL) testing is a important test stage where the PSIM generated code is tested on the DSP. In the simulation stage, both the power circuit and the control algorithm are simulated by the computer. In the PIL stage, the power circuit is simulated by the computer while the control algorithm is executed by the DSP. This adds a degree of validation to the control design without risk of connecting to the power system. After the controller is properly tuned in the simulation and the DSP code is generated, the code is saved in a separate folder, a plotting function needs to be added before the code is flashed onto DSP through code composer studio (CCS).

To connect the simulation to the DSP, a separate simulation file needs to be made with a PIL block. The PIL block links the variables in code to the signals generated in PSIM by mapping variable names. The variables used as inputs and outputs need

to be declared in code as global variables. The ADC fetch statements in the code need to be commented out so the DSP will not try to get readings from its ADC ports. Since the gating signals will not show in the PIL simulation, the dead time can only be checked by connecting the corresponding pins on the DSP to an oscilloscope. Note that sensor gains used in simulation need to be reentered in the PIL block.

4.4 Lab Prototype GSC Hardware Components

The simulated power circuit and measurement circuit are made in hardware for testing. The hardware testing circuit can be roughly separated into two parts: the power circuits, and the sensor circuits. Since the previous team who worked on this project has left a set of current sensors (LEMs), the conditioning circuits for the LEMs are added to the prototype PCB design as backup sensors. The quality of layout is very essential when integrating these three circuit onto one PCB. Since high frequency current is involved in the converter circuit, electromagnetic interference (EMI) can influence measurement. The integrated circuit needs multiple isolated power supplies, therefore on-board power supply circuits are required .

4.4.1 Power Circuit

The power circuit consists of all of the high voltage side components of the GSC system. The high voltage side components are defined as components that are running at system voltage level, and the low voltage side components that are running at signal voltage level (0-5V). The four main components looking from the power system into the converter circuit are: (1) the isolation transformer; (2) the inductor bank; (3) the power converter module; and (4) DC bus capacitors.

(1) Isolation Transformer:

Transformer bank No.1 in the University of Idaho power lab is used as the isolation

transformer. The purpose of the transformer is to provide galvanic isolation for the converter rather than voltage step up or step down, therefore the transformer has an ratio of 1: 1 and is connected in the delta-to-delta configuration as shown in Fig. 4.18. The open-circuit test and short-circuit test is applied on each transformer to determine its parameters. The transformer parameters are calculated by the short circuit and open circuit tests, and are listed in Table. 4.1.

Table 4.1: Transformer NO.1 Parameters with Transformation Ratio of 1:1

	Transformer A (Phase A)	Transformer B (Phase B)	Transformer C (Phase C)
R_c	1175.723Ω	1178.38Ω	1263.5Ω
L_m	3568.99mH	3567.757mH	3822.163mH
X_m	1345.478Ω	1345.013Ω	1440.921Ω
R_1	0.211Ω	0.19943Ω	0.209Ω
R_2'	0.211Ω	0.19943Ω	0.209Ω
L_1	0.437mH	0.4mH	0.413mH
X_1	0.165Ω	0.151Ω	0.156Ω
L_2	0.437mH	0.4mH	0.413mH
X_2'	0.165Ω	0.151Ω	0.156Ω

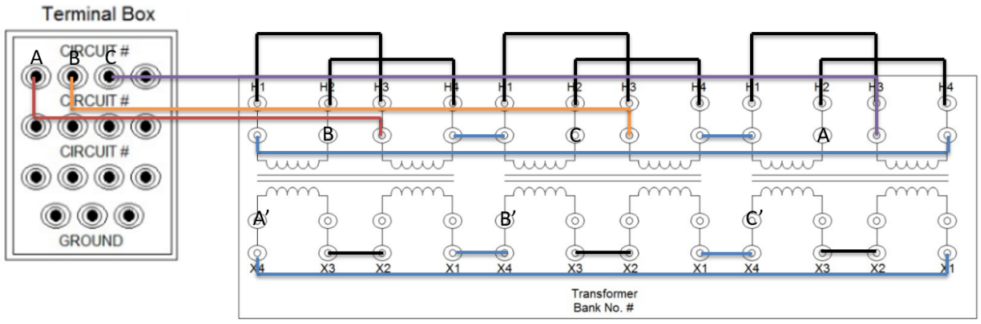

Figure 4.18: Isolation Transformer Connection

The two primary windings are connected in parallel and the two secondary windings are connected in series due to the fact that the single phase transformers are connected with a ratio of 2:1 instead of 1:1. Since the delta-to-delta configuration will not introduce a phase shift the primary terminals "A", "B", and "C" are used to measure the system voltages and they are connected to voltage measurement circuit

directly. The secondary "A'", "B'", and "C'" are the output terminals of the transformer that connect to the inductor bank.

(2) Inductor Bank:

Only one inductor per phase in the three-phase inductor bank No.2 is used. The single inductor is measured to be $12.4mH$ and 0.425Ω. The first switch in each phase is switched in the up position, the second switch in each phase is switched in the down position, and the other three switches in each phase are in the middle position. The inductors are connected in series with the system, so the bottom switch shown in Fig. 4.19 is kept in the middle position.

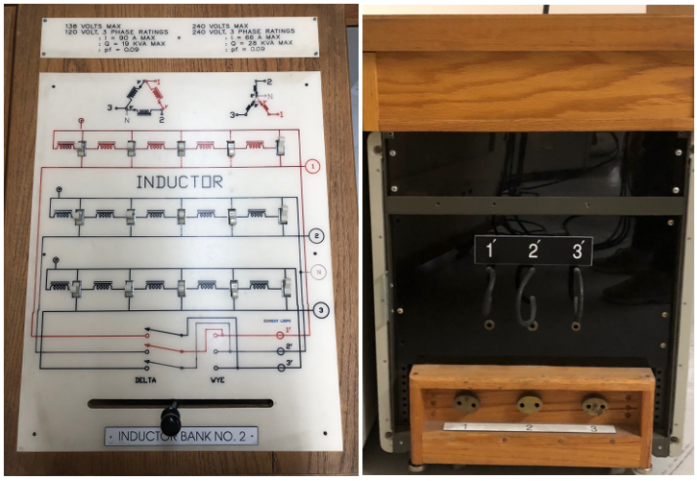

Figure 4.19: Inductor Bank

The transformer outputs are connected to terminals 1, 2, and 3 in Fig. 4.19, and terminals 1', 2', and 3' are connected to the power converter module.

(3) Power Converter Module:

The CIPOS Mini (IKCM30F60HA) from Infineon is used as power converter module. The converter module is rated for 30 A at 600 V for continuous operation, and can sustain a jump to 60 A for 1 μs. The module is a 21 mm x 36 mm on board chip consists of six IGBTs combined with an optimized silicon-on-insulator (SOI) gate driver. The integrated gate driver architecture greatly simplifies the design requirements by not having to develop an additional gate driver circuit. The schematic of

the outside circuit needed for the converter module is shown in Fig. 4.20.

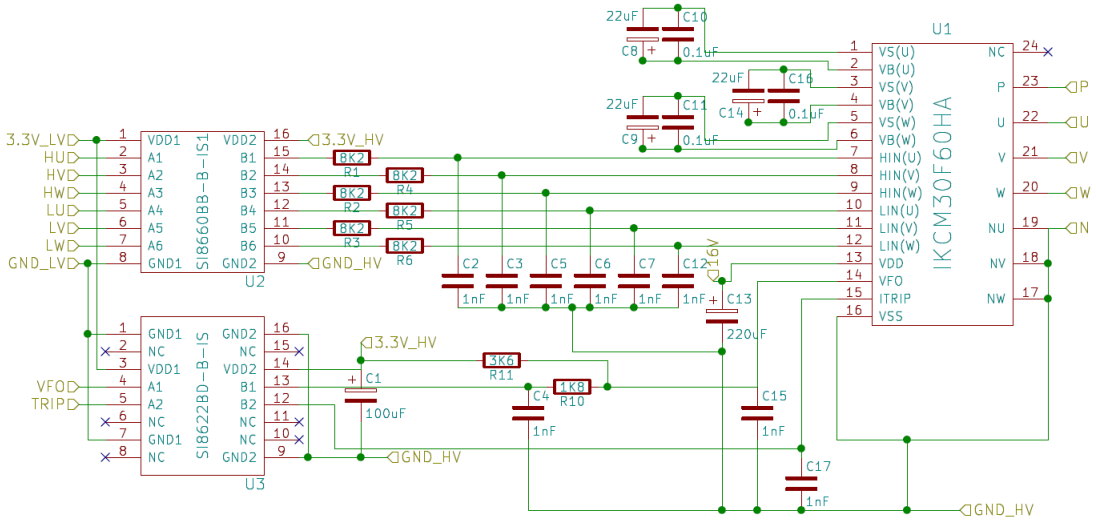

Figure 4.20: CIPOS Circuit

There are 16 signal pins and 8 power pins on the chip. Pins 7 - 12 are the six individual IGBT control pins. Since pull-down resistors are provided internally to pre-bias the inputs, a high (3.3 V) signal should be applied to the pin to turn on the IGBT. A low-pass filter is added to reduce high speed switching noise while passing the switching signal. Pin 13 is the 16 V power supply that provides power to the internal driver circuit. Pin 15 is an input overcurrent trip signal (ITRP) generated by the controller that provides a high speed trip of all outputs of the gate driver. The fault-clear time is at minimum 40 μs. Pin 14 is the fault-output signal (VFO) that indicates internal fault of the module and overcurrent detection at ITRIP. This signal needs to be pulled up to the positive side of the 3.3 V logic power supply with an external resistor R11. Pin 16 is a shared ground between the 16 V power supply and the high voltage DC bus ground (N). The ground plane is shared due to the charge pump. In general the chip is targeted towards applications where there the DC bus capacitor is replaced with a DC source and the chip is inverting it to power an AC device. Pins 1-6 are used to connect to discrete capacitors for the charge pump gate

drivers. This internal gate driver circuitry uses the external capacitors to store a charge which is then used to trigger the gates at the command of the 3.3 V PWM inputs (pins 7-12). Pins 17-19 (NU, NV, and NW) are the emitters of the three lower IGBTs as shown in Fig. 4.21. Pins 20-22 (U, V, and W) are the three-phase voltages that connect to the inductor bank terminals 1', 2', and 3'. Pin 23 (P) and pins 17-19 (NU, NV, and NW) are connected to the capacitors which provide the positive terminals and negative terminal to the DC bus.

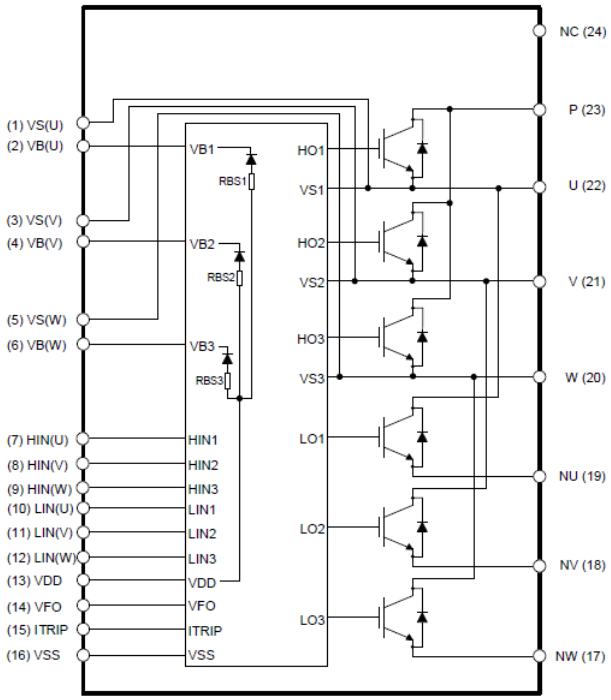

Figure 4.21: Internal Schematic of CIPOS Mini

In Fig. 4.20, two isolation chips (SI8660BB and SI8622BD) from Silicon Labs provide 5000 V_{rms} isolation from the power circuit to the DSP. Both isolators can operate at 150 Mbps. The low voltage side of the isolation chips are supplied by the DSP. Since the DSP is isolated from the converter module and cannot supply the high voltage side of the isolator, an additional 3.3 V power supply is required to power the high voltage side. The ground of the additional 3.3 V power supply and the ground of 16 V power supply for the converter module are shared.

(4) DC bus capacitors:

There are 2 capacitors connect in series to form the DC bus. The capacitors are both 4600uF and rated at 450VDC. Note that the mid-point of the capacitors is not grounded.

4.4.2 Sensor Circuit

Each of the voltages and currents are measured by an AMC1100 isolation amplifier from Texas Instruments. The AMC1100 is an isolation amplifier with the output separated from the input circuity by galvanic isolation of up to 4250 V_{pk}. The optimized range of the differential analog input for a shunt resistor application of the AMC1100 is between +/-250 mV. The AMC1100 is powered on when the supplies are connected. The device is operated off a 5 V isolated supply on the high side and the 3.3 V DSP supply on the low side. The common-mode voltage is automatically set to 1.29 V when 3.3 V is being supplied on the low side. The potential of the high side ground reference (GND1) is tied to one side of the shunt resistor to maintain the operating common-mode range requirements of the device. Since the ground potentials for all measurements are different and may change with time, each AMC1100 device will need a separate 5 V isolated high side power supply.

According to the AMC1100 application datasheet, current measurement through the phase of a power line is done via the voltage drop across the resistive shunt R_{SHUNT} as shown in Fig. 4.22. The differential input signal is filtered using RC filters (R_2, R_3, and C_2). In this application, since the targeting peak current is at 60 A, the shunt resistor R_{SHUNT} is chosen to be $4m\Omega$. Three-phase currents are measured at the converter terminals.

When AMC1100 is used for voltage measurements, a resistive voltage divider is used in the same way as described in the simulation part. The resistor values are picked to match the relatively small input range of the AMC1100 (+/-250 mV). The

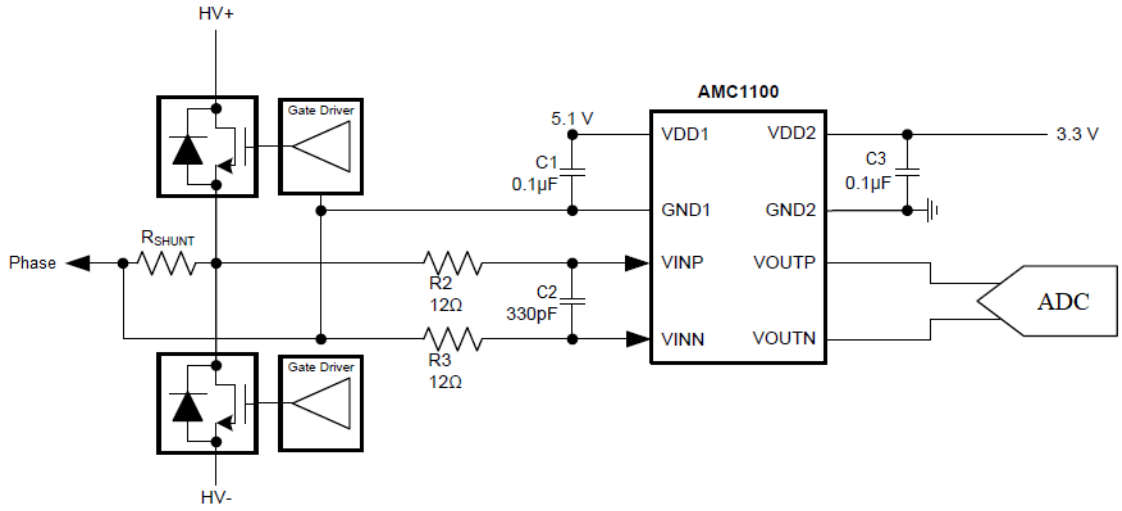

Figure 4.22: Current Sensing with AMC1100

voltage across the measuring resistor (R_2) is connected to pins VINP and VINN directly on the AMC1100. The voltage between L1 and L2 is measured in Fig. 4.23, where L1 and L2 can be both DC or AC voltages.

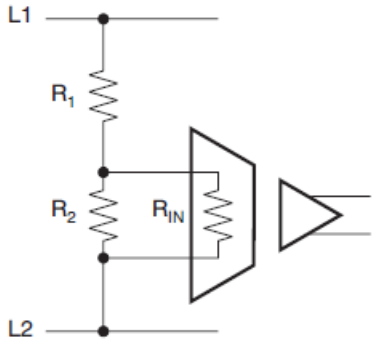

Figure 4.23: Voltage Measurement

As shown in Fig. 4.23, both the measuring resistor (R_2) and the AMC1100 input resistance (R_{IN}) are the factors influencing the additional gain error. With the fact that the resistance value of R_1 (picked in the $k\Omega$ range depending on the targeting voltage level) and R_{IN} (28 $k\Omega$) are considerably higher than R_2 (a few hundred Ω), the resulting total gain error can be estimated using (4.45). According to the datasheet, G_{ERR} is $\pm 0.5\%$ maximum.

$$G_{ERRORTOT} = G_{ERR} + \frac{R_2}{R_{IN}} \tag{4.45}$$

In the prototype board, two three-phase line voltages are measured at different points in the circuit. One at the system terminals and one at the converter terminals. These can be used to determine the phase shift due to voltage drop across the inductor bank and the transformer and so a different control method can be implemented in the future that utilizes the converter terminal voltage measurements if needed.

As mentioned earlier, conditioning circuits for the LEMs are added to the prototype PCB design as backup sensors. The LEM100P is powered by +/-12 V power supply, and it can measure up to +/-100 A rms. According to the datasheet, the measuring resistance is 50ohm with +/-12 V power supply at 70 degrees Celsius. The turns ratio is 1:2000 meaning when measuring 100 A rms AC current, the secondary nominal current is 50 mA rms. The output voltage of the LEM is calculated by multiplying secondary current and the measuring resistance which is 50 ohms, matching the manufacturer recommendations. The output voltage is determined to range from -2.5 V to +2.5 V and it is linearly related to the measured current. Since the DSP only accepts analog signals from 0-3.3 V, a conditioning circuit is required to scale and offset the +/-2.5 V range to the required 0-3.3 V. This conversion circuit is shown in Fig. 4.24.

The circuit consists of two op-amps where the gain and offset can both be tuned using variable resistors. Variable resistors are used instead of fixed value resistors for the LEM conditioning circuit to get more accurate readings. The op-amps are connected in a non-inverting configuration where the gain can be calculated by (4.46).

$$\frac{V_{out}}{V_{in}} = 1 + \frac{R_2}{R_1} \tag{4.46}$$

The first op-amp has gain of 1.2 when the 5 $k\Omega$ variable resistor is tuned to

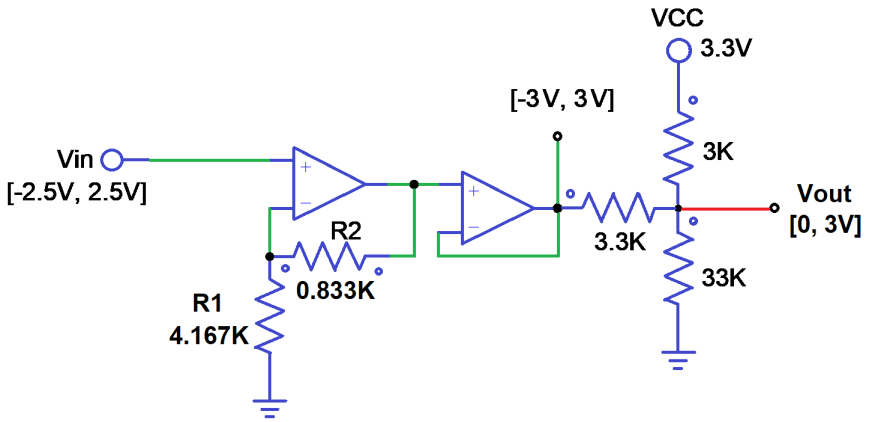

Figure 4.24: LEM Conditioning Circuit

4.166 $k\Omega$. The output of the second op-amp is connected directly to the noninverting terminal result in a unity gain. The rest of the variable resistors are tuned to the values in Fig. 4.20 to provide 0-3.3 V analog signals.

4.4.3 PCB Layout

The converter module and all components in the sensor circuit have been laid out on a two-layer printed circuit board. The board only needs a single external 16V power supply. The board consists four types of on board voltage converters: a 16 V-to-5 V voltage converter; a 5 V-to-5 V isolated voltage converter; a 5 V-to-3.3 V voltage converter; and a 16 V-to +/-12 V voltage converter. All voltage converters are powered by a 16 V external power supply. The 16 V to 5 V voltage converter provide a 5 V supply to the 5 V-to-5 V isolated voltage converters and the 5 V-to-3.3 V voltage converter. Since each AMC1100 device will require a separate power supply as explained in the previous section and ten AMC1100 devices are used, ten 5 V-to-5 V isolated voltage converters are required. The 5 V-to-3.3 V voltage converter will provide the 3.3 V high side voltage for the isolators and the converter module. Since the RSC could require the same high side 3.3 V supply, the high side 3.3 V power supply is made accessible though jumper pins. The 16 V-to +/-12 V voltage converter

is responsible for powering the LEMs and the LEM conditioning circuits (i.e. the op-amps). The power supply debugging circuit shown in Fig. 4.25 is implemented to all of the voltage converter outputs to make sure the output voltage levels meet the requirement. The voltage rating of the LED and the Zener diode should add up to the test voltage, so the LED would light up when the output voltage level is high enough.

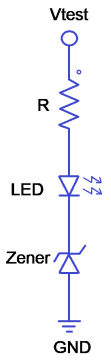

Figure 4.25: Power Supply LED

The power traces and signal traces are different in width and spacing. The width of the trace depends on the current that it's carrying. The spacing between conductor depends on both the voltage and current. The spacing for the power traces are set to a minimum of 3 mm, and the power traces are made as wide as possible. The measurement signals connecting the resistive shunts have trace widths of 0.5 mm, and clearances of 0.5 mm since the current flow is low. The 16 V main power supply for has 0.5 mm traces and clearances of 0.5 mm. All other signal traces are set to be 0.2 mm and clearances of 0.2 mm. A high voltage ground plane under the power circuit is designed to absorb possible high frequency noise generated by the converter module. High voltage measurements are brought onto the board by banana plugs and screw terminals. All measurements are accessible though testing probe points, and jumper pins are used for signal I/Os. The KiCad schematic and the Gerber file of the PCB are attached in the Appendix.

4.5 Hardware Testing Procedure and Results

In this section, the test procedure steps are listed. The startup operation procedure is divided into 3 parts: the test preparation procedure; the sensor testing procedure; and the powering procedure. The preparation procedure will ensure all test equipment are ready to use before powering any component. The sensor testing procedure is to test to check if all sensor readings are correct. Finally, the circuit is ready to be powered up though the powering procedure. A few plots are shown as reference.

4.5.1 Test Preparation Procedure

1. Connect the 3-phase transformer bank No.1 in Δ-to-Δ configuration and make sure 240V:240V ratio is applied.

2. Switch the inductor bank switches to the correct position according to Section 4.4.1(2) and connect the bank between the transformer bank and one of the measurement tables in the lab. Make sure that the three-phase switches on the measurement table are open.

3. Power on the converter PCB with 16V-18V DC power supply and check for LEDs to light up. Especially the blue LEDs indicating the 5V power supply for the sensors are correct.

4. Connect the grid side 3-phase voltages to the measurement terminals, “A”, “B” and “C” on the converter PCB.

5. Connect the converter DC terminals “P” and “N” to the DC capacitors. The two capacitors are connected in series and ungrounded. Also connect the converter DC terminals “P” and “N” to a multimeter to read the DC voltage.

6. Connect input/output pins from the PCB to the DSP development board pins according to the table below:

Table 4.2: Pin Configuration of the GSC Testbed

GSC PCB	ADC	GSC PCB	GPIO
V_{ab}	B2	HU	00
V_{bc}	B3	HV	02
V_{ca}	B4	HW	04
I_A	B5	LU	01
I_B	B6	LV	03
I_C	B7	LW	05
V_{dc}	A0	VFO	11
		TRIP	12

   Note that the pin configuration is not fixed, it can be modified in the PSIM with the code generation.

7. Connect the DSP development board to the computer.

4.5.2 Sensor Testing Procedure

Sensor testing with the LEM100P and the AMC1100 are both explained in this section.

LEM100P:

1. Connect the test points on the PCB to oscilloscope and set the range to read 0-3.3V analog signals.

2. Edit CCS code to plot 3-phase voltages, currents and DC bus voltage. Plot the calculated V_{gd} and V_{gq} as a check. The I_{gd} and I_{gq} can also be plotted.

3. Connect the output of the measurement table, “A”, “B” and “C” to the 3-phase resistor bank. The measured per phase resistance of the 3-phase resistor bank should be more than 4 Ω.

4. Follow the procedure in power lab to turn on the 120 V AC supply.

5. Setup the CCS plot window settings after executed the code. Compare the captures from the oscilloscope and the CCS plots. Make sure the magnitude matches. Also check the DC voltage measurement on the multimeter to make sure it matches the CCS readings within 5 V error.

A 3-phase wye connected 11.6 Ω resistive load used as an example, and the plots from CCS are shown in the Fig. 4.26. The horizontal axis is in real-time samples and the sampling rate is 10 kHz in code. As shown below, 1000 samples are plotted meaning 6 fundamental frequency cycles should be shown in the plots.

AMC1100:

The AMC1100 sensors can be tested two at a time:

1. Disconnect the converter board from the system.

2. Short the 3-phase terminals “U”, “V” and “W” together with a wire.

3. Connect a DC power supply with limited current to the DC terminals, “P” and “N”.

4. Apply a logic high to switch “HU” and “LV”.

5. Read phase A and phase B current reading from the oscilloscope. The sensor gain can be determined based on the oscilloscope reading and the DC power supply limiting current.

6. Apply a logic high to switch “HU” and “LW”.

7. Repeat Step 5 with phase A and phase C.

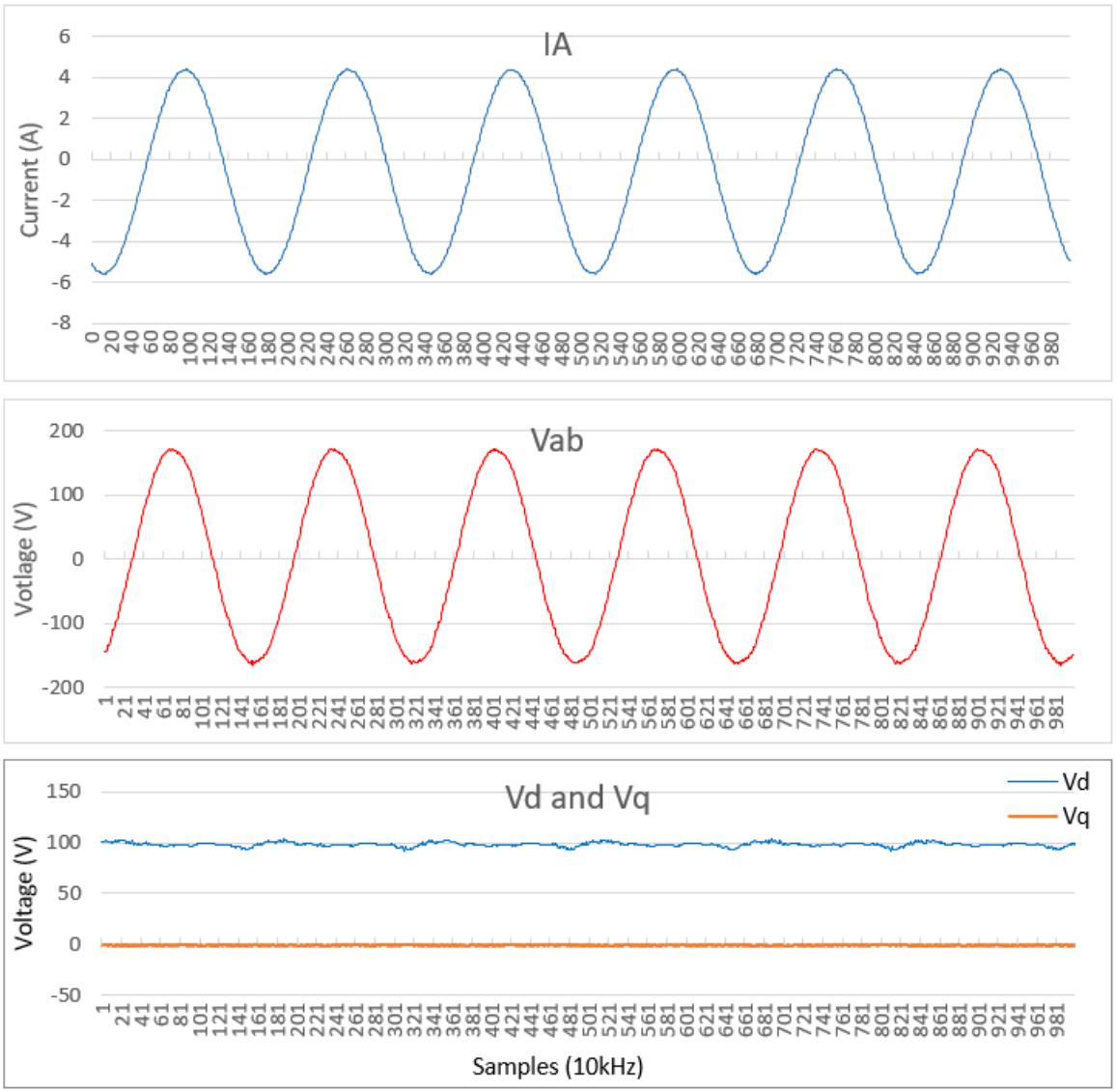

Figure 4.26: CCS Plots of 11.6Ω Resistive Load Connected

4.5.3 Powering Procedure

1. Disconnect the 3-phase resistor bank and connect the output of the measurement table, “A”, “B” and “C” to the converter PCB 3-phase terminals “U”, “V” and “W” respectively.

2. Connect the 3-phase charging resistor and a bypass contactor in between the transformer and the grid power supply to limit the initial passive rectifier charg-

ing current.

3. Close the switches on the measurement table and then close the main power supply switch.

4. Watch the voltage on the multimeter to reaches 170V then switch out the 3-phase charging resistor using the contactor.

5. Change the variable "START" form "0" (stop) to "1" (start) in the CCS command block to charge the capacitor bank to the reference value.

The example result of DC bus voltage reference set to 210V is shown in Fig. 4.27. Again, the data from the first 0.1s is plotted. The controlled voltage will fall to 210V within 1 second and stay constantly at 210V. The noise levels are considerably high due to the EMI emission from the high-speed switching.

As shown in Fig. 4.27, the normal operating current will stay within the 30A operating range of the converter rating.

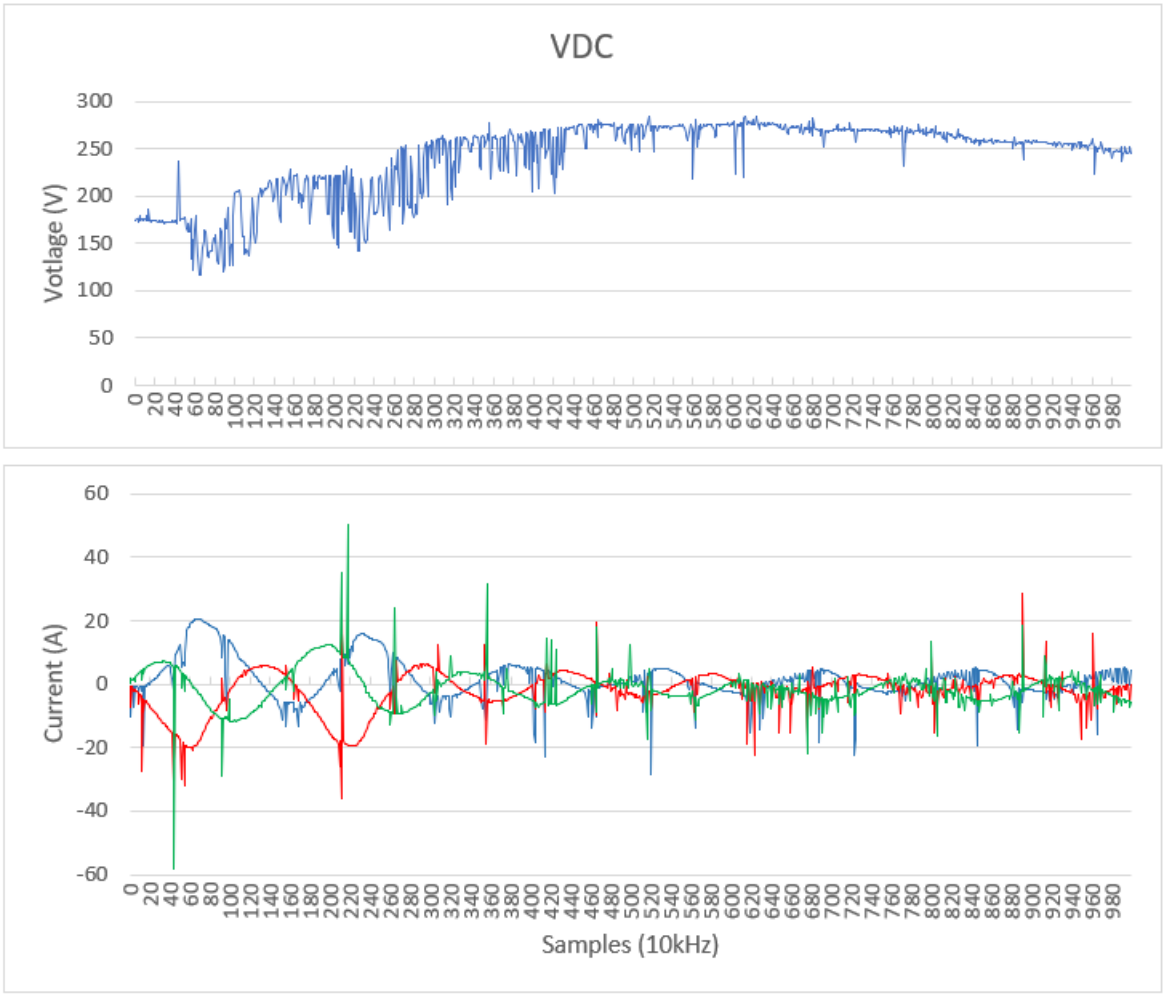

Figure 4.27: CCS Result Plots of a 210V DC Reference

CHAPTER 5

Rotor Side Converter

In this chapter, the control of the RSC is analyzed with the DC bus tied to the GSC model. The RSC is implemented using a variable-frequency VSC system. The AC side of the RSC is interfaced with the rotor windings of the DFIG and the DC side of the RSC connect to the DC bus whose voltage is controlled by the GSC. The RSC controls the rotor flux frequency such that the machine torque is optimal for the current wind speed. Depending on the application, the optimal torque is usually calculated by another control loop such as a MPPT (Maximum Power Point Tracking Scheme). In a wind-power unit, a torque reference also can be forced to change proportional to the square of the machine rotor speed to maximize the output power. Since the machine flux is regulated by the direct connection between the machine stator and the power system, it is convenient to use stator voltage-oriented control (SVOC).

In this chapter, the steady-state performance of the DFIG with stator voltage-oriented control is analyzed. Since the MPPT tracking algorithm has not yet been developed for the test machine, the power control references are calculated based on the DFIG system in steady-state. Different power factors are analyzed separately with various rotor speed. The mathematical calculation results of the DFIG under each operating condition are provided in tables to explain the principle of the DFIG wind energy system. A case where the machine switches from supersynchronous mode to subsynchronous mode is analyzed using the dynamic machine model to evaluate the control response. The calculation results are then validated with PSIM simulation.

5.1 Stator Voltage Oriented Control

In DFIG wind energy system, stator voltage-oriented control is achieved by aligning the d-axis of the synchronous reference frame with the stator terminal voltage vector $\vec{v_s}$. The resultant d- and q-axis stator voltages can be written as (5.1),

$$v_{qs} = 0 \quad and \quad v_{ds} = v_s \tag{5.1}$$

where v_s is the peak amplitude of the system voltage $\vec{v_s}$. The rotor voltage and rotor current can be mapped onto dq-axes using the Park's transformation using the slip frequency as the rotational angle reference: v_{qr} and v_{dr} denotes rotor voltages and i_{dr} and i_{qr} denotes rotor currents. According to equation (2.31) in Chapter 2, the electrical torque of the generator can be related to rotor current and stator flux as:

$$T_{em} = \frac{3}{2}P\frac{L_m}{L_s}Im\left\{\vec{\psi}_r \cdot \vec{i}_r^*\right\} = \frac{3}{2}P\frac{L_m}{L_s}\left(\psi_{qs}i_{dr} - \psi_{ds}i_{qr}\right) \tag{5.2}$$

As discussed in Chapter 2, the stator voltage vector of the generator in dq-frame can be written as (5.3) and (5.4).

$$v_{sd} = R_s i_{sd} + \frac{d\psi_{sd}}{dt} - \omega_s \psi_{sq} \tag{5.3}$$

$$v_{sq} = R_s i_{sq} + \frac{d\psi_{sq}}{dt} + \omega_s \psi_{sd} \tag{5.4}$$

Since the stator is directly connected to the grid, the stator voltage can be considered constant during steady-state operation, meaning the stator flux derivative terms are zero. The equations can be rearranged as:

$$\begin{cases} \psi_{ds} = \frac{v_{qs} - R_s i_{qs}}{\omega_s} \\ \psi_{qs} = \frac{v_{ds} - R_s i_{ds}}{\omega_s} \end{cases} \tag{5.5}$$

Substituting (5.5) into the torque equation (5.2), results in equation (5.6)

$$T_e = \frac{3PL_m}{2\omega_s L_s} \left(-i_{qr} v_{qs} + R_s i_{qs} i_{qr} + R_s i_{ds} i_{dr} - i_{dr} v_{ds}\right) \tag{5.6}$$

with stator voltage-oriented control, $v_{qs} = 0$, and the torque equation, (5.6), is simplified to (5.7)

$$T_e = \frac{3PL_m}{2\omega_s L_s} \left(R_s i_{qs} i_{qr} + R_s i_{ds} i_{dr} - i_{dr} v_{ds}\right) \tag{5.7}$$

The rotor resistance is generally small and can be neglected without significant error in most cases. The torque equation can then be further simplified to (5.8).

$$T_e = \frac{3PL_m}{2\omega_s L_s} i_{dr} v_{ds} \tag{5.8}$$

The equation shows that the electromagnetic torque is a function of d-axis rotor current and stator voltage magnitude. If the torque is given as a reference and v_{ds} is known, the d-axis rotor current reference can be calculated by rewriting (5.8).

According to Chapter 4, when $V_{sq} = 0$, the active and reactive power can be written as (5.9)

$$\begin{cases} P_s = \frac{3}{2} v_{ds} i_{ds} \\ Q_s = -\frac{3}{2} v_{ds} i_{qs} \end{cases} \quad for \quad v_{qs} = 0 \tag{5.9}$$

where the dq-axis stator current can be substituted with a function of stator flux and rotor current:

$$\begin{cases} i_{ds} = \frac{\psi_{ds} - L_m i_{dr}}{L_s} \\ i_{qs} = \frac{\psi_{qs} - L_m i_{qr}}{L_s} \end{cases} \tag{5.10}$$

Substitute (5.10) into (5.9), and rearrange:

$$\begin{cases} i_{dr} = -\frac{2L_s}{3v_{ds}L_m} P_s + \frac{1}{L_m}\psi_{ds} \\ i_{qr} = \frac{2L_s}{3v_{ds}L_m} Q_s + \frac{1}{L_m}\psi_{qs} \end{cases} \tag{5.11}$$

Again, substituting the flux equations (5.5) and (5.6) into the above equations and neglecting the stator winding resistance, we have:

$$i_{dr} = -\frac{2L_s}{3v_{ds}L_m} P_s \tag{5.12}$$

$$i_{qr} = \frac{2L_s}{3v_{ds}L_m} Q_s - \frac{v_{ds}}{\omega_s L_m} \tag{5.13}$$

The above equations show that for a given stator voltage, the stator active and reactive power can be controlled by the dq-axis rotor current independently.

5.2 System Block Diagram

The block diagram of DFIG with stator voltage-oriented control is shown in Fig. 5.1. The rotor position angle θ_r is measured by an encoder mounted on the shaft of the generator. The rotor based dq-axis reference frame rotates at the slip angle, and the machine slip angle is calculated by $\theta_s - \theta_r$. The reference torque T_e^* is usually generated by the MPPT block based on the optimal torque method. The reference for the d-axis rotor current i_{dr}^* is calculated based on equation (5.8). For a given stator reactive power reference Q_s^*, the q-axis rotor current reference can be calculated based on equation (5.13). The dq-axis reference currents are then compared with the measured values. The error is processed by PI controllers. The output of the PI controller v_{dr}^*,

and v_{qr}^* are the dq-axis rotor voltage references. The rotor voltage references in the synchronous frame rotating at the slip frequency are transformed back to three-phase stationary reference frame, v_{ar}^*, v_{br}^*, and v_{cr}^*. The three-phase rotor references can be used as the three-phase modulating signals for sinusoidal modulation or converted into a space vector for space vector modulation. The gating signals are generated by the PWM block.

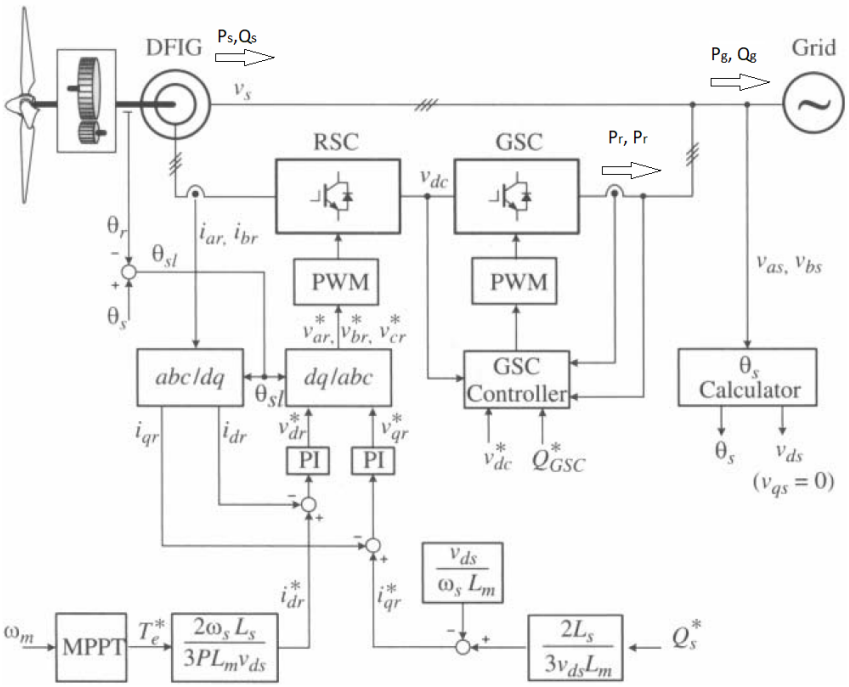

Figure 5.1: Block Diagram of DFIG with Stator Voltage-Oriented Control [25]

The main function of the grid side converter is to keep the DC bus voltage constant and provide reactive power to the grid when required. The grid side reactive power reference Q_{GSC}^* can be set differently than the rotor side reactive power reference Q_s^*. When the application does not require reactive power supply, the grid side reactive power is usually set to zero for unity power factor operation of the converter. The overall power factor of DFIG is determined based on the rotor side converter reactive power reference Q_s^*. The stator voltage vector angle θ_s is same as the grid voltage angle and it's calculated by the "atan" function explained in Chapter 4. Since the

operation principle of the grid side converter controller has been explained in Chapter 4, it is not repeated here.

5.3 RSC Simulation Circuit

The test machine is driven by a 4-pole squirrel cage induction motor. The field-oriented control is applied to the induction motor. The control scheme is based from one of the example control files in PSIM. The rotor speed is controlled by controlling i_q as shown in Fig. 5.2. The motor is working in the 1st quadrant meaning both torque and speed are positive. Since i_q from the motor feedback has a negative value due to polarity of measurement, a gain of -1 is added.

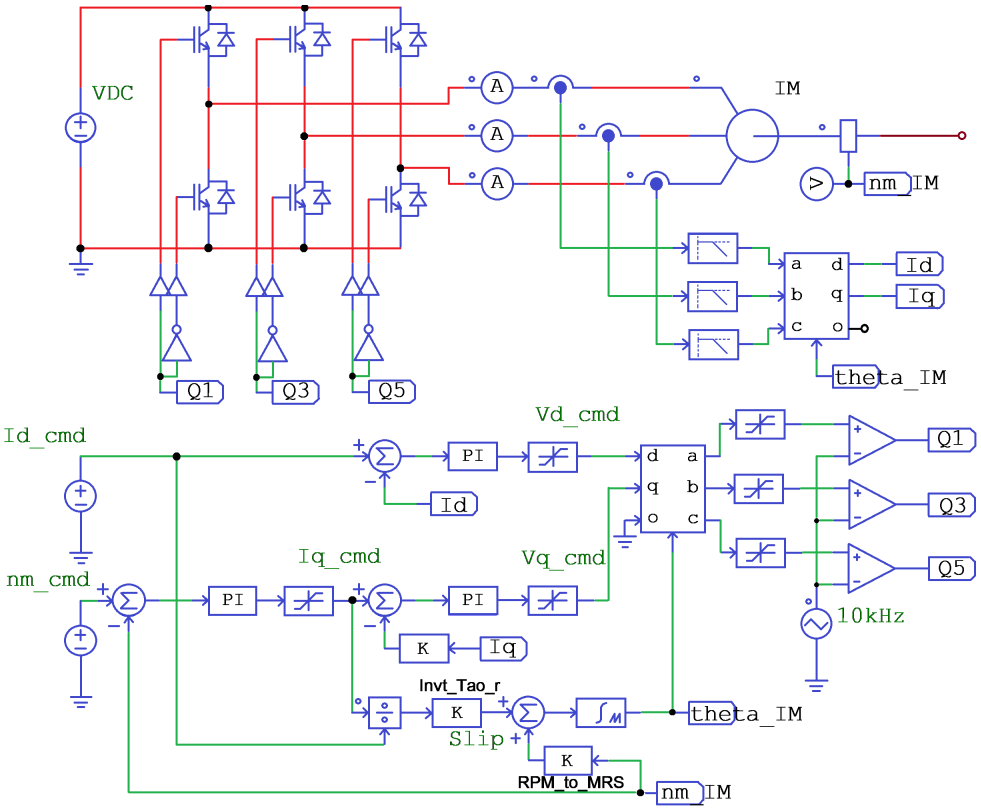

Figure 5.2: Field-Oriented Control of Induction Motor Drive

The slip of the induction motor is calculated by taking i_q divided by i_d and then multiplying by the inverted rotor time constant, $R_r/(L_m + L_r)$. The sensed shaft

speed in RPM (revolution per minute), mn_{IM}, is converted to magnetic revolution per second by the gain block. RPM is first converted to radian per second by a gain of $2\pi/60$. This is then multiplied by the number of pole pairs of the motor to get the mechanical speed of the rotor. The slip is added to the mechanical speed to give the electrical system speed. The "theta" used by the dq transformation blocks is given by the integration of the electrical system speed. The resettable integrator has a lower limit of 0 and an upper limit of 2π to avoid possible memory overflow.

In the simulation two machine shafts are not allowed to be connected, therefore the squirrel cage induction motor and DFIG are connected through a 1:1 gearbox as shown in Fig. 5.3. The rotor speed of DFIG, mn, is measured with a speed sensor and

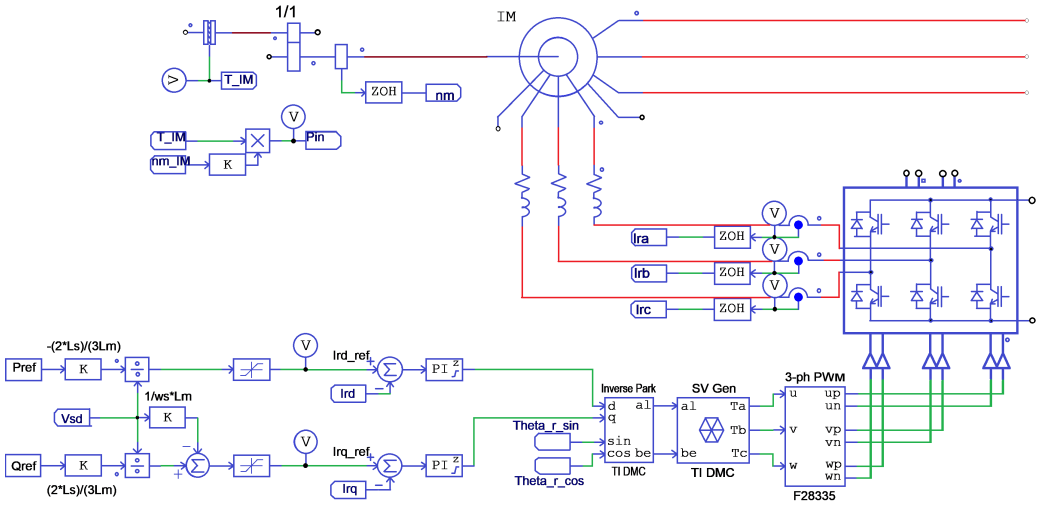

Figure 5.3: Rotor Side Converter Control Loops

should be equivalent to the rotor speed of the induction machine, mn_{IM}. The slip is calculated as is shown in Fig. 5.4. Since the test machine is a 4-pole machine and the nominal rotor speed is 1800RPM, the slip can be calculated by $(1800 - nm)/1800$. The rotational reference frame reference angle, θ_r, for rotor side converter is generated by the ramp generator based on the calculated slip. The measured rotor current are then mapped onto the dq-axis based on the generated ramp, θ_r.

The result of a steady-state operation case is plotted in Fig. 5.3 as function of

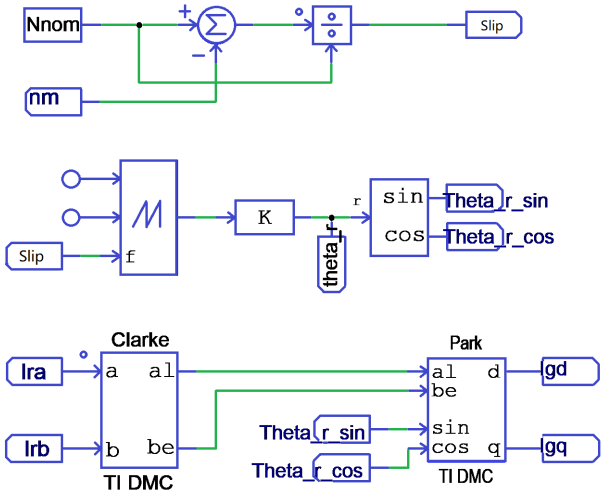

Figure 5.4: Slip Calculation and Park's Transformation Calculation

time. The rotation speed of the machine is set to be at 1750 rpm in the example. As shown in the rotor angle plot, the ramp is generated counting from $-\pi$ to π at the frequency of $1.667Hz$. This result is expected since the slip is 0.02778 and the frequency of the slip is calculated to be $1.667Hz$. The rotor current is also plotted to show that the rotor input current is measured to be at the slip frequency. Since the rotor inductance is not big enough to completely limit the current ripple due to the converter switching, the current ripple in the rotor current is still noticeable.

The rotor side converter control is built in PSIM as shown in Fig. 5.3. It is built in a similar fashion to the grid side converter. The active power and reactive power reference are set as constants, and the power system frequency is assumed to be 60 Hz. The MPPT block in Fig. 5.1 is replaced by the constant power reference, P_{ref}. and the d-axis rotor current reference i^*_{dr} is calculated based on (5.12). The q-axis rotor current reference i^*_{qr} is calculated based on (5.13).

The dq-axis current references are compared with the measured rotor currents and then processed by the PI controller. The control loops are valid if the PI controllers are tuned correctly. Sample simulation results for operation at 1750 rpm are shown in Fig. 5.6. The signals in blue are the reference values and the signals in red are

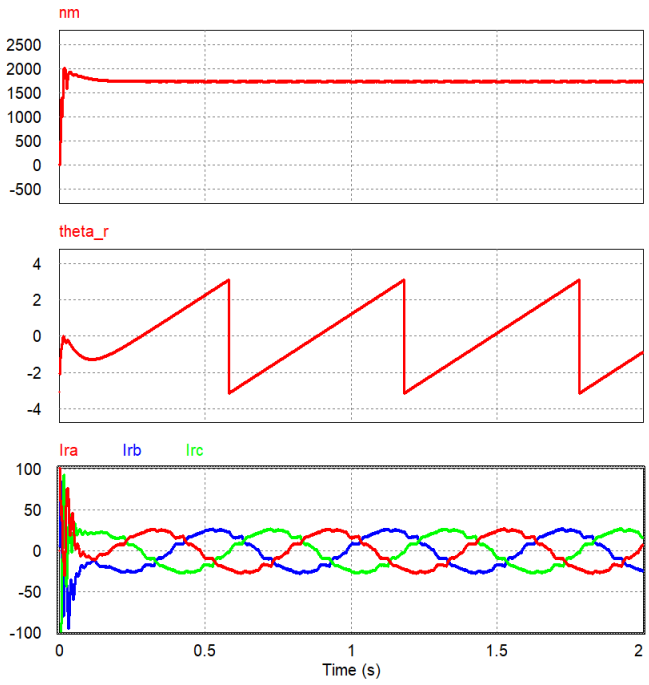

Figure 5.5: Plot of Rotor Speed, Rotor Angle and Rotor Current in SIMVIEW

the measurements. The plot (a) shows the measured rotor current on d-axis and its reference; plot (b) shows the measured rotor current on q-axis and its reference. As shown in (a), d-axis current reference is calculated for a given power reference and the measured rotor current on the d-axis is tracking the reference after a short start up transient lasting about 0.1 second. The q-axis current reference is calculated for the given reactive power reference shown in plot (b) and the q-axis rotor current settles to its calculated reference after the starting transient within 0.1 second. Note that the power and reactive power references for the RSC are the stator power generated by the DFIG. The net reactive power generated by the system can be controlled by the GSC through the reactive power reference by the GSC controller. The controlled voltage signals in rotating reference frame are converted back to stationary reference frame based on the slip frequency, and then applied to the SVPWM block to generate appropriate switching command for the RSC.

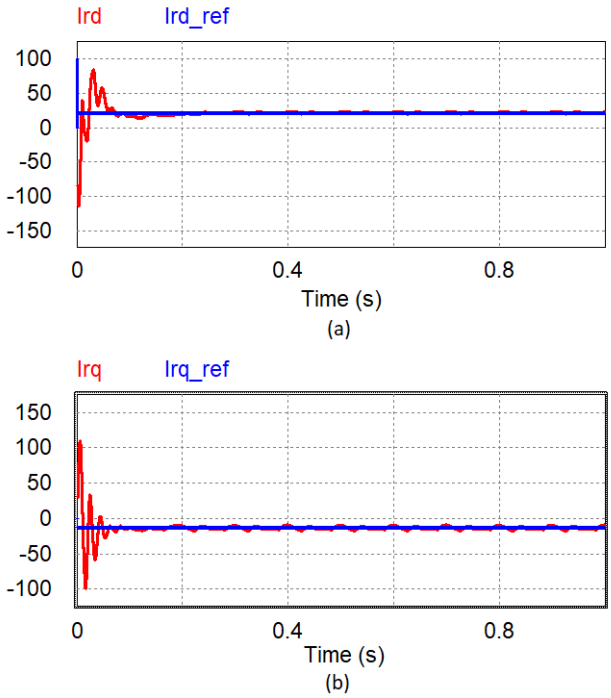

Figure 5.6: Plots of Rotor Side Converter Controlled Variables in SIMVIEW: (a) Rotor side converter AC terminal current on d-axis; (b) Rotor side converter AC terminal current on q-axis.

5.4 Unity Power Factor Operation

The calculation results of the rotor current, rotor voltage, and equivalent impedance of the rotor-side converter when the slip of the DFIG varies from positive to negative are listed in Table 5.1. The machine parameters can be found in Table 5.2.

Table 5.1: Equivalent Impedance of RSC in 10hp/220V DFIG (PF=1)

Operating Mode	Subsynchronous	Subsynchronous	Synchronous	Supersynchronous	Supersynchronous
$RPM(rpm)$	1440	1620	1800	1980	2100
$Slip$	0.2	0.1	0	-0.1	-0.1667
$T_m(Nm)$	-15.944	-20.179	-24.913	-30.144	-33.909
$V_r(V)$	$29.35\angle -2.5°$	$16.79\angle -6.6°$	$5\angle -36.5°$	$9.81\angle -152°$	$18.18\angle -161°$
$I_r(A)$	$12.24\angle 131°$	$13.75\angle 138°$	$15.58\angle 143°$	$17.72\angle 148°$	$19.32\angle 151°$
$R_{eq}(\Omega)$	-1.658	-0.992	-0.321	0.282	0.631
$X_{eq}(\Omega)$	-1.732	-0.713	0	0.476	0.698

These parameters were determined by a previous student through lab testing. All the parameters listed in these tables are referred to the stator side.

The rotor current, I_r, decreases with increasing slip, while the rotor voltage, V_r, is

Table 5.2: 10hp 220V 60Hz Double Fed Induction Generator Parameter

Rated Mechanical Power	10hp	1.0pu
Rated Stator Line-to-line Voltage (rms)	220V	
Rated Stator Phase Voltage (rms)	127V	1.0pu
Rated Rotor Phase Voltage (rms)	18.175V	0.064pu
Rated Stator Current (rms)	16.293A	0.923pu
Rated Rotor Current (rms)	19.318A	1.071pu
Rated Stator Frequency	60Hz	1.0pu
Rated Rotor Speed	2100 rpm	1.0pu
Nominal Rotor Speed Range	1260-2100 rpm	0.636-1.0pu
Rated Slip (as generator)	-0.1667	
Number of Pole Pairs	2	
Rated Mechanical Torque	$33.909kN \cdot m$	1.0pu
Stator Winding Resistance, R_s	0.23Ω	0.035pu
Rotor Winding Resistance, R_r	0.321Ω	0.093pu
Stator Leakage Inductance, L_{ls}	0.001395H	0.08pu
Rotor Leakage Inductance, L_{rs}	0.001395H	0.08pu
Magnetizing Inductance, L_m	0.037109H	2.15pu
Base Current, $I_B = 10hp/\sqrt{3}V_{LL,rms}$	19.5675A	1.0pu
Base Impedance, Z_B	6.49Ω	1.0pu
Base Inductance, L_B	17.22mH	1.0pu

not a monotonic function of slip. The rotor voltage, V_r, should decrease to zero when the slip drops from 0.2 to 0. The rotor voltage will then increase with a negative slip from 0 to -0.1667 assuming that the rotor impedance is negligible.

In an MPPT controlled wind energy system, the mechanical torque is proportional to the square of the generator speed ($T_m \propto \omega^2$), as discussed in Chapter 2. This relationship is illustrated by analyzing the data in Table 5.1.

When the generator is in the subsynchronous mode, R_{eq} is negative, signifying that the rotor absorbs active power from the system. When the DFIG operates in the supersynchronous mode, the equivalent resistance R_{eq} of the RSC is positive while the rotor resistance, R_r, can be neglected. Positive R_{eq} indicating that active power is delivered from the rotor to the system. The general trend of power flow is shown in Table 5.3, which indicates that the power flow between the rotor and the system is directly influenced by the rotor speed. The subscript, "s", denotes the

power generated from the machine stator, and the subscript, "g", denotes the overall power generated by the machine to the grid.

Table 5.3: Power Flow of 10hp/220V DFIG (PF=1)

Operating Mode	Subsynchronous	Subsynchronous	Synchronous	Supersynchronous	Supersynchronous
RPM(rpm)	1440	1620	1800	1980	2100
P_m(kW)	-2.404	-3.423	-4.696	-6.25	-7.457
P_r(kW)	-0.745	-0.562	0.234	0.266	0.706
Q_r(kW)	-0.779	-0.404	0	0.448	0.782
$P_{cu.r}$(kW)	0.144	0.182	0.234	0.302	0.359
$P_{cu.s}$(kW)	0.042	0.066	0.100	0.145	0.183
P_s(kW)	-2.964	-3.737	-4.596	-5.536	-6.209
Q_s(kVAR)	0	0	0	0	0
P_g(kW)	2.218	3.175	4.362	5.802	6.914
Q_g(kVAR)	-0.779	-0.404	-5.628	0.449	0.782
η	92.26%	92.75%	92.89%	92.83%	92.72%

Similar conclusions can be drawn from Fig. 5.7. One can see that this DFIG has a negative equivalent resistance, R_{eq}, when slip is greater than approximately 0.02. This phenomenon is most likely to be caused by the relatively high rotor winding resistance R_r. This implies the rotor resistance R_r dissipated more power than the slip power of P_r at synchronous speed. Further testing is warranted to check this.

Fig. 5.7 shows the rotor current, rotor voltage, and equivalent impedance of the rotor-side converter when the slip of the DFIG varies from positive to negative. The rotor current, I_r, increases with the slip, while the rotor voltage V_r decreases when the slip approaches zero, and reaches near zero at s = -0.02, and increases with a positive slip.

5.5 Lagging and Leading Power Factor Operation

When the generator operates with a leading or lagging power factor, the equivalent impedance of the rotor-side converter can be obtained following the same procedures given in Chapter 2. Table 5.4, and Table 5.5 give the calculated converter equivalent impedance, rotor voltage and current for the DFIG operating under the supersynchronous and subsynchronous modes with 0.95 lagging and leading power factors.

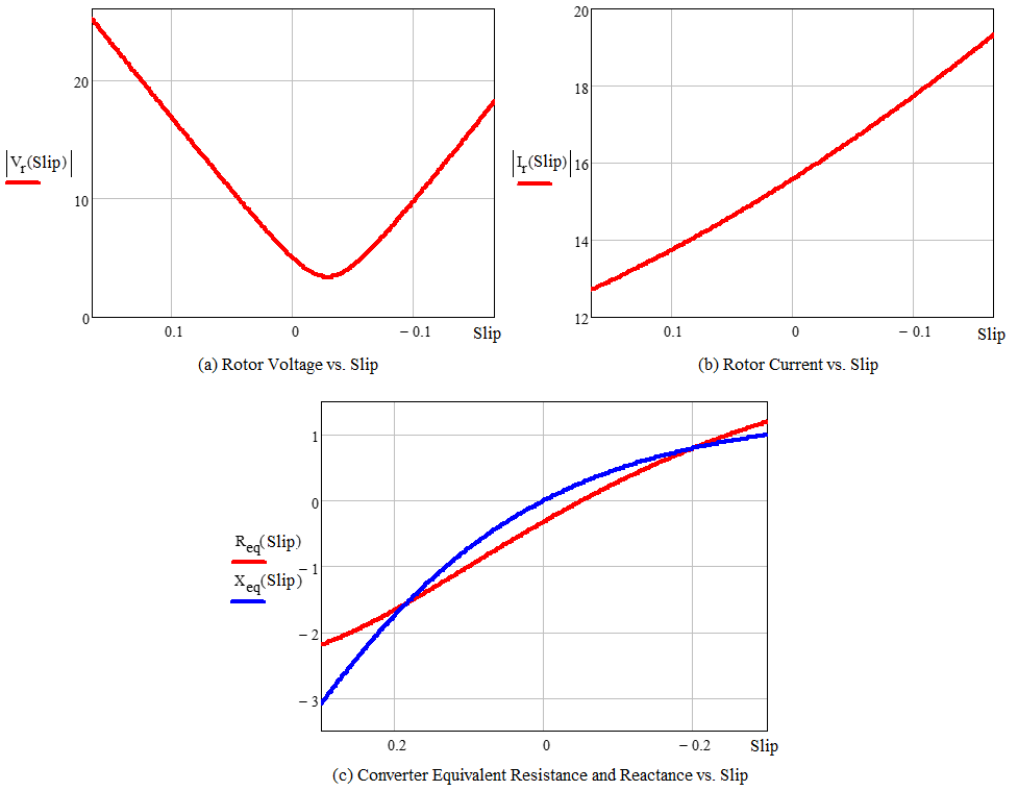

Figure 5.7: Calculated Rotor Variables: (a) Rotor voltage as function of slip; (b) Rotor current as function of slip; (c) Equivalent converter resistance and reactance as function of slip

Table 5.4: Equivalent Impedance of RSC in 10hp/220V DFIG (PF=0.95 lagging, $\varphi_s = -161.8°$)

Operating Mode	Subsynchronous	Subsynchronous	Synchronous	Supersynchronous	Supersynchronous
$RPM(rpm)$	1440	1620	1800	1980	2100
$Slip$	0.2	0.1	0	-0.1	-0.1667
$T_m(Nm)$	-15.944	-20.179	-24.913	-30.144	-33.909
$V_r(V)$	$28.79\angle -0.6°$	$16.37\angle -2.7°$	$4.4\angle -22°$	$8.71\angle -159°$	$16.78\angle -165°$
$I_r(A)$	$10.43\angle 141°$	$11.81\angle 150°$	$13.60\angle 158°$	$15.77\angle 164°$	$17.41\angle 167°$
$R_{eq}(\Omega)$	-2.166	-1.232	-0.321	0.443	0.854
$X_{eq}(\Omega)$	-1.711	-0.635	0	0.33	0.446

Table 5.5: Equivalent Impedance of RSC in 10hp/220V DFIG (PF=-0.95 leading, $\varphi_s = 161.8°$)

Operating Mode	Subsynchronous	Subsynchronous	Synchronous	Supersynchronous	Supersynchronous
$RPM(rpm)$	1440	1620	1800	1980	2100
$Slip$	0.2	0.1	0	-0.1	-0.1667
$T_m(Nm)$	-15.944	-20.179	-24.913	-30.144	-33.909
$V_r(V)$	$29.94\angle -4.3°$	$17.28\angle -10°$	$5.87\angle -47°$	$11.0\angle -147°$	$19.65\angle -168°$
$I_r(A)$	$14.32\angle 124°$	$16.15\angle 129°$	$18.28\angle 133°$	$20.70\angle 136°$	$22.47\angle 138°$
$R_{eq}(\Omega)$	-1.299	-0.808	-0.321	0.122	0.384
$X_{eq}(\Omega)$	-1.638	-0.702	0	0.518	0.785

In a MPPT controlled wind energy system, the mechanical torque only depends on the rotor speed squared. Therefore, the mechanical torque is the same as the torque in unity power factor operation. The steady-state power generation of the DFIG wind energy system is slightly different from the performance in unity power factor. The differences can be seen by analyzing the power flow data in Table 5.6 and Table 5.7.

Table 5.6: Power Flow of 10hp/220V DFIG (PF=0.95 lagging, φ_s=-161.8deg)

Operating Mode	Subsynchronous	Subsynchronous	Synchronous	Supersynchronous	Supersynchronous
RPM(rpm)	1440	1620	1800	1980	2100
P_m(kW)	-2.404	-3.423	-4.696	-6.25	-7.457
P_r(kW)	-0.706	-0.515	-178	0.330	0.776
Q_r(kW)	-0.558	-0.404	0	0.246	0.405
$P_{cu.r}$(kW)	0.104	0.134	0.178	0.239	0.292
$P_{cu.s}$(kW)	0.046	0.074	0.111	0.161	0.202
P_s(kW)	-2.964	-3.737	-4.596	-5.536	-6.209
Q_s(kVAR)	0.974	1.288	1.51	1.82	2.041
P_g(kW)	2.257	3.222	4.418	5.867	6.985
Q_g(kVAR)	-1.153	-1.494	-1.51	-1.573	-1.635
η	93.87%	94.12%	94.07%	93.86%	93.67%

When operating at 0.95 lagging power factor, the power factor angle of the stator is calculated to be $\varphi = -161.80°$ where unity power factor is at 180°. The real power, P_g, and reactive power, Q_g, delivered to the grid are listed in Table 5.6. The reactive power, Q_s, is positive in all cases listed in the table, meaning the machine absorbs reactive power from the grid. The total real power, P_g, delivered to the grid is slightly higher than the real power delivered to the grid at unity power factor, while the stator real power P_s is the same in both cases. With lagging power factor, high overall efficiency about 94% is achieved by the reduced rotor winding losses. The machine input power is calculated base on the machine speed and the machine torque on it's shaft. The efficiency, η, is the fraction of total power generated by the machine, P_g, over the machine input power.

When operating at 0.95 leading power factor, the power factor angle of the stator is $\varphi = 161.80°$. The real power, P_g, and reactive power, Q_g, delivered to the grid is listed as shown in Table 5.7. In this case, the DFIG outputs reactive power to

Table 5.7: Power Flow of 10hp/220V DFIG (PF=-0.95 leading, φ_s=161.8deg)

Operating Mode	Subsynchronous	Subsynchronous	Synchronous	Supersynchronous	Supersynchronous
$RPM(rpm)$	1440	1620	1800	1980	2100
$P_m(kW)$	-2.404	-3.423	-4.696	-6.25	-7.457
$P_r(kW)$	-0.799	-0.632	-0.322	0.157	0.582
$Q_r(kW)$	-1.008	-0.549	0	0.666	1.190
$P_{cu.r}(kW)$	0.198	0.251	0.322	0.413	0.486
$P_{cu.s}(kW)$	0.046	0.073	0.111	0.161	0.202
$P_s(kW)$	-2.964	-3.737	-4.596	-5.536	-6.209
$Q_s(kVR)$	0.974	1.288	1.51	1.82	2.041
$P_g(kW)$	2.164	3.105	4.271	5.693	6.791
$Q_g(kVAR)$	-0.034	0.679	1.51	2.486	3.231
η	90.01%	90.70%	91.01%	91.09%	91.07%

the grid. Comparing to the unity power factor case, the real power, P_g, delivered to the grid is slightly lower. Again, the stator real power, P_s, is the same regardless of power factor angles. The efficiency has fallen to low 90% due to higher loss in the rotor windings. The increase in winding losses is due to the increase in rotor current.

5.6 Dynamic Response

The transient of a step change in wind speed at unity power factor is simulated and analyzed as an example. The step change of wind speed from 1980 RPM to 1620 RPM will occur after 5 seconds into the simulation. A rapid change in wind speed was simulated to show an extreme but unrealistic case. The machine is operating in steady-state at 1980 RPM before the change. The mechanical speed of the rotor cannot change instantaneously due to the moment of inertia. The change in wind speed will force the generator switch from supersynchronous generation mode to the subsynchronous generation mode. In the simulation, the calculated power corresponding to the rotor speed is used as power reference.

The waveform of the dynamic response is shown in Fig. 5.8. The rotational speed of the shaft is shown as a reference. At $t = 5sec$, the wind speed decreases and the mechanical torque applied on DFIG $T_{em,DFIG}$ decreases proportional to the speed squared. The speed ramp was chosen to demonstrate the ability to respond

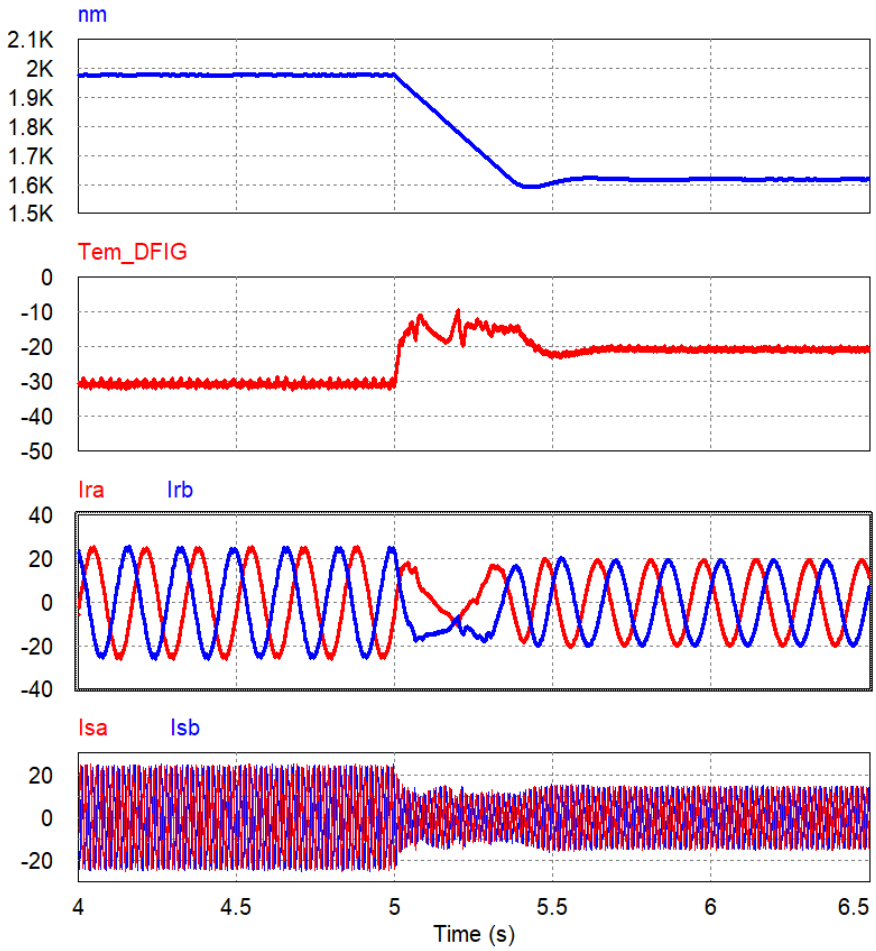

Figure 5.8: The Dynamic Response of the DFIG in SIMVIEW: (a) Rotor speed; (b) Mechanical/Electrical torque of the DFIG; (c) Rotor currents and (d) Stator Currents

to a ramp. The rate of change shown is somewhat unrealistic. The power reference should also be a ramp following the rotation speed of the machine, however, the power reference is currently implemented using a step function instead of a proper MPPT algorithm. The electrical torque fluctuation during the transient state is due to having a step change in the power reference while the speed change has a ramp. The rotor current, i_{ra} and i_{rb} are shown in Fig. 5.8(c). The frequency of the rotor current varies with the rotor speed. Phase-b current lead the phase-a current until the operation mode changes to supersynchronous mode, meaning the rotor current went from ABC rotation to ACB rotation. When the machine operates at the synchronous speed, the

rotor frequency is close to zero. The phase-a and phase-b stator current, are shown in Fig. 5.8(d). The current magnitude decreases as the wind speed decreases, meaning power generated will also decrease if voltage at the PCC remains unchanged. The value measured in the result plot matches the calculation in Table 5.3.

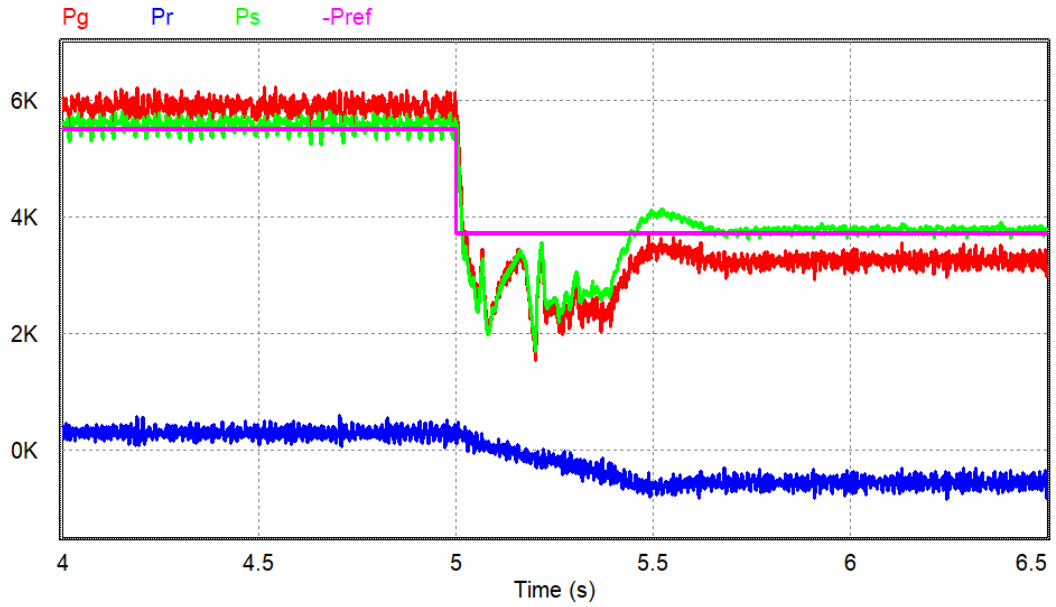

Figure 5.9: DFIG Power Plots in SIMVIEW

The total power generated by the machine, P_g, the power generated by the stator, P_s, the power generated by the rotor, P_r and the power reference, P_{ref} for RSC are shown in Fig. 5.9. The power generated follows the similar shape as the torque plot shown in Fig. 5.8(b). The power reference should have been calculated by a MPPT algorithm tracking the rotor speed, this is also the main reason that the torque transient does not follow the shape of the speed ramp. The result shown in figure shows that the generated power tracks the reference value very closely.

The results presented in this section are preliminary. More work is needed to set up realistic scenarios representing the response to a ramp in wind speed. This is discussed in the future work section.

CHAPTER 6

Summary, Conclusions and Future Work

6.1 Summary and Conclusions

In this thesis, the principles of operation and control of a doubly fed induction generator have been discussed. The DFIG is modeled in both the steady-state operation and the dynamic operation. The equivalent circuits are provided, and formulas are derived based on the model. The switching model of a two-level voltage source converter topology was then introduced with the converter modulation either achieved by sinusoidal PWM or space vector PWM. The two methods were explained in detail and the pros and cons for each method was discussed. The back-to-back converter was described in two parts, the grid side converter (GSC), and the rotor side converter (RSC). The switching signals of both voltage converters are produced by SVPWM. The GSC and RSC control are explained in detail separately since the only connection between them is the DC bus. Various steady-state operation points are analyzed. A case where the machine switches from supersynchronous generation mode to subsynchronous generation mode was analyzed using the dynamic machine model.

The primary function of the GSC control is to exchange power between the DC-bus and the AC system depending on the operating conditions of the DFIG. The active and reactive control are decoupled and controlled separately by two closed control loops. The innercurrent control loop is achieved by proportional and integral control (PI control). The d-axis current reference oversees the active power exchange to maintain the DC bus voltage level while the q-axis current reference is controlling the reactive power generated by the converter. The current control references are generated by the DC bus voltage and the reactive power reference. The DC bus voltage is controlled and maintained at a constant voltage reference by the GSC control algorithm. The reactive power compensation can be achieved by the GSC, meaning

the converter is capable of supplying reactive power to the system when requested. The control theory was first explained in detail and then simulated in PSIM. Simulation results were analyzed, and DSP code was generated after the simulation was validated. A hardware testbed for the GSC was built in the lab incorporating some the existing components such as the transformer and the inductor bank. The voltage converter and driver; measurement sensors; and the sensor conditioning circuit were integrated into one PCB. The rotor side converter can be designed in the same fashion.

The RSC is interfaced with the machine rotor. The RSC is capable of controlling the rotor voltage and current such that the machine torque is optimal for the current wind speed. Maximum power tracking can be achieved using the current model after a MPPT algorithm is developed. The active and reactive power generated by the machine is controlled thought the innercurrent control in a similar fashion as the grid side converter. The rotor current references are calculated based on the given stator power references, Ps, and Qs. The DFIG was modeled in PSIM driven by a speed controlled induction motor as will be the case in the lab. The dynamic model of DFIG was simulated by applying a step change to the driving induction motor speed. The PSIM simulation results demonstrated that the designed controller can effectively maintain the power factor at unity and is robust to input disturbance. Further tests related to the DFIG protection design can be applied to the dynamic simulation model.

6.2 Future Work

To complete the testbed for further studies towards studying the impacts of DFIGs on protection schemes, additional work will be required. This can be roughly divided into four main parts, the MPPT algorithm; the DC bus chopper circuit; the rotor side converter testbed design and the crowbar circuits. In this section, the future work is

introduced, and major components needed are described.

MPPT Algorithm

The main goal of the MPPT is to maximize the power generated at different wind speeds. Techniques presented in literature incluede using the turbine power profile; optimal tip speed ratio or optimal torque control [27]. Since the DFIG in this application is driven by a frequency-controlled induction machine, the optimal tip speed ratio which requires the knowledge of the wind speed is not recommended. The turbine power profile method is based on the power versus wind speed curve provided by the manufacturer for a given wind turbine as explain in Section 2.4 of [27]. Even though the manufacture information is not available in this case, the power versus rotor speed curve can be generated based on the calculations explained in Chapter 2. A look up table can be easily calculated to generate the optimal power reference. The optimal torque control is the most reasonable method to use in this case since both the torque and rotor speed can be measured on the machine shaft. The turbine mechanical torque is a quadratic function of the turbine speed, where optimal torque can be generated by a simple gain coefficient, K_{opt}. The gain coefficient K_{opt} can be calculated according to the rated parameters of the generator.

DC bus chopper circuit

As explained in Section 4.2.4, the logic circuit for the chopper circuit has already been designed and implemented in the GSC controller. However, the driver board for the intended chopper IGBT board, has been modified in the past. When testing the driver board, it did not operate as expected. It is suggested to implement a high power MOSFET instead of fixing the existing chopper board with an IGBT. The N-Type MOSFET with a discharge resistor and a simple driver with an optocoupler would be sufficient for this design.

Rotor Side Converter Testbed Design

The rotor side converter component of the testbed can be designed in a similar fashion as to the GSC testbed. The voltage/current measurement circuit, as well as the converter circuit can be set up using the GSC integrated circuit board. The DSP can access voltage and current information after sensor calibration. The power supplies can be set up in a similar fashion as the GSC. Additional information such as the rotor speed is required by the rotor side controller. The rotor speed can be acquired from the decoder on the machine shaft. The output of the decoder needs to be calibrated and either a digital or analog signal sent to the controller. The information of the mechanical torque is also required in the MPPT determination if the optimal torque control method is used. The output of the torque sensor on the machine shaft also needs to be sent to the DSP to enable optimal torque control. The PSIM program needs to be configured in the correct way to cooperate with the speed and torque sensor.

Crowbar Circuit

A thyristor crowbar is an older method than the conventional method to enhance the LVRT capability of the wind turbines. During AC system voltage sag, the rotor circuit is disconnected and the DFIG run as a round rotor induction machine with a resistive load on the rotor winding. The crowbar circuit consists of the resistors and thyristor switches. The crowbar resistance can be adjusted by controlling the switching. The main aim is to reduce the rotor voltage by means of providing an additional path to dissipate power from the rotor to maintain the DFIG in operation while preventing damage to the system. It is the simplest method which has the advantage of low cost and high simplicity. The main problem is its high short circuit current at the RSC thereby drawing more reactive power from the network [28]. There

are a few alternative methods to improve the stability and continuity of the DFIG such as passive crowbar, active crowbar and stator crowbar.

Fault Studies

The objective of this testbed is to implement a lab scale DFIG for fault studies. The complete DFIG should be interfaced with the model power systems and then run though fault scenarios, including the DC bus chopper and crowbar circuit response. The response should be compared to the existing approaches used in industry for setting protection relays to validate the approaches in developing new protection schemes.

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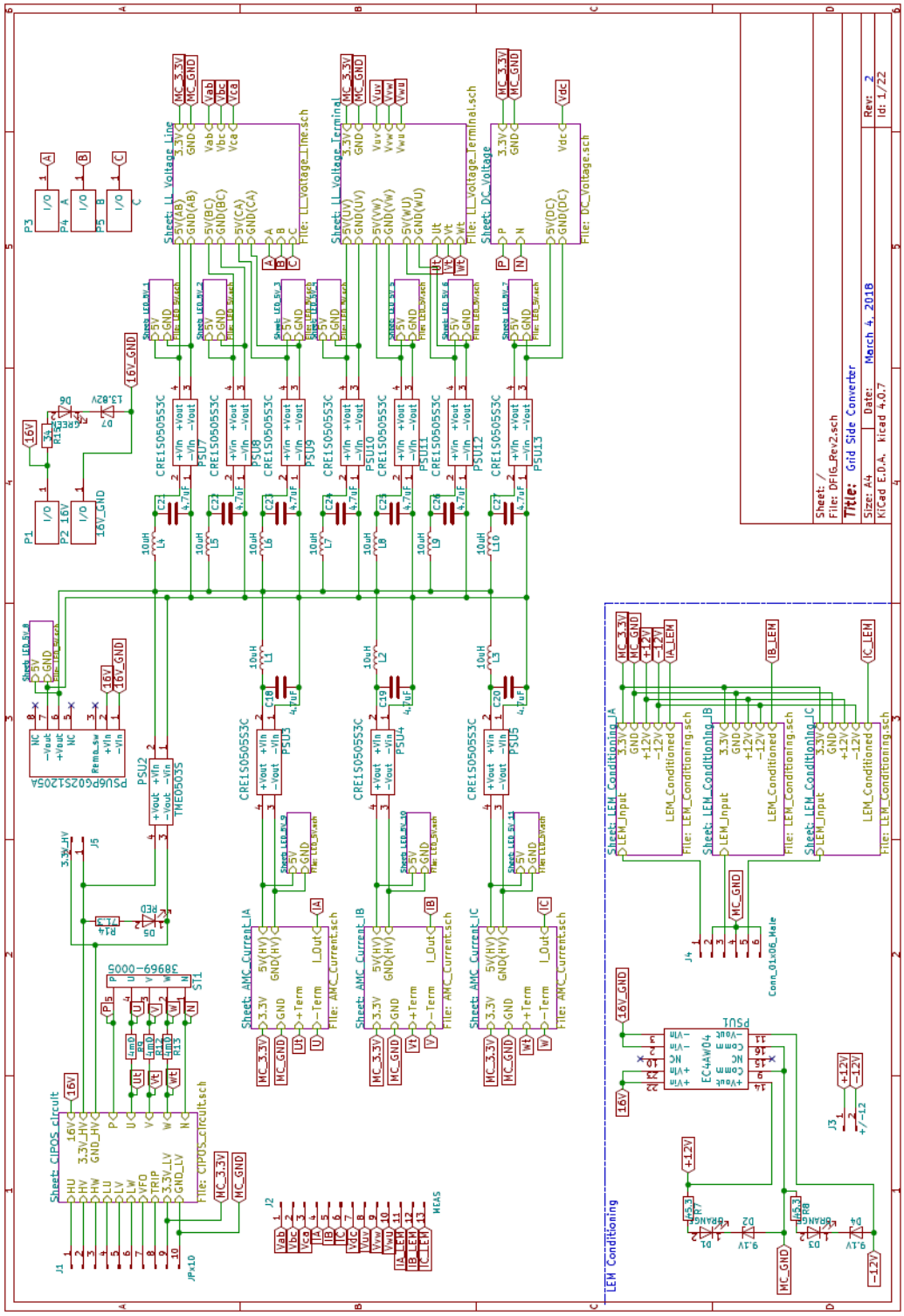
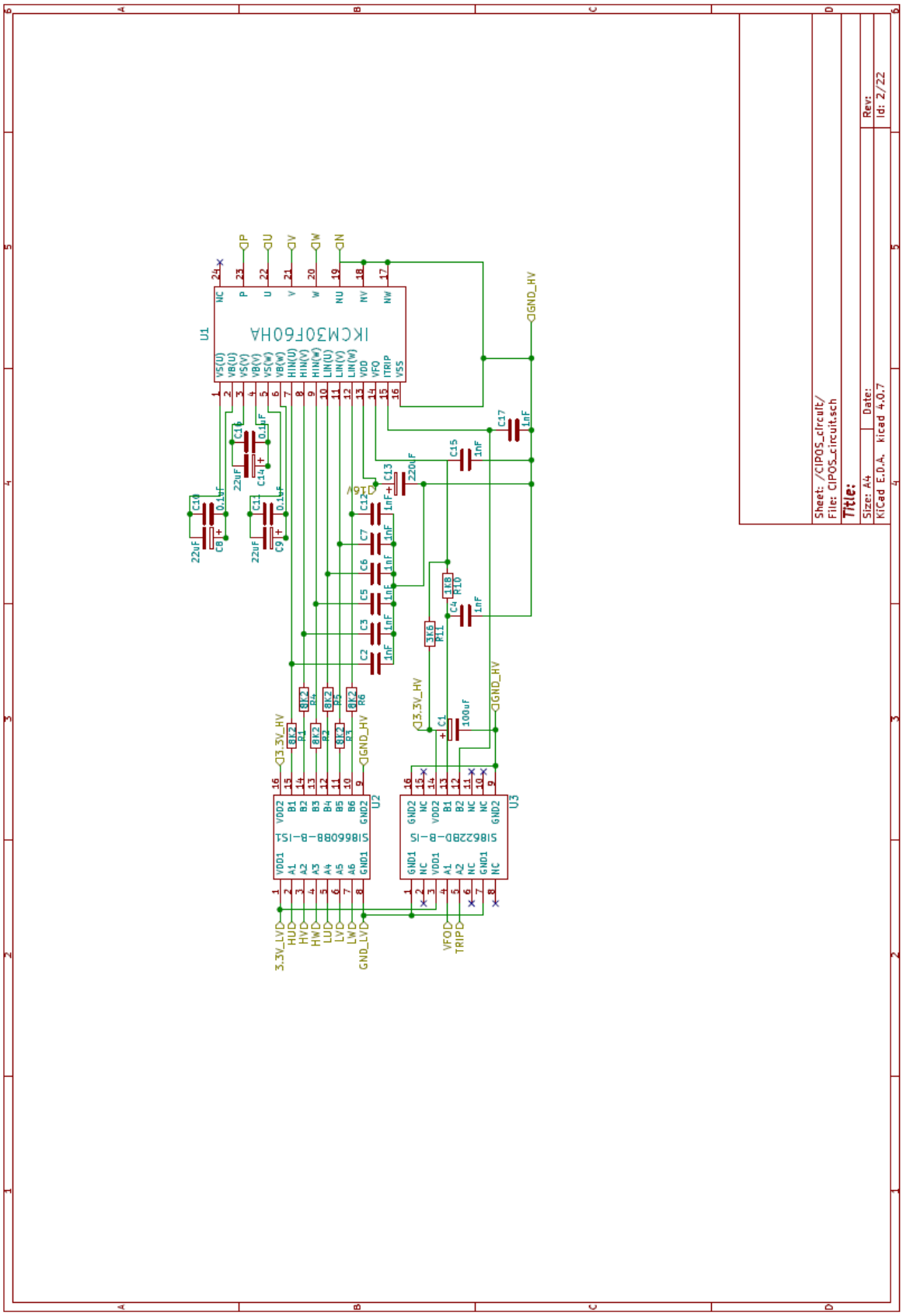
Appendix: KiCad Schematics

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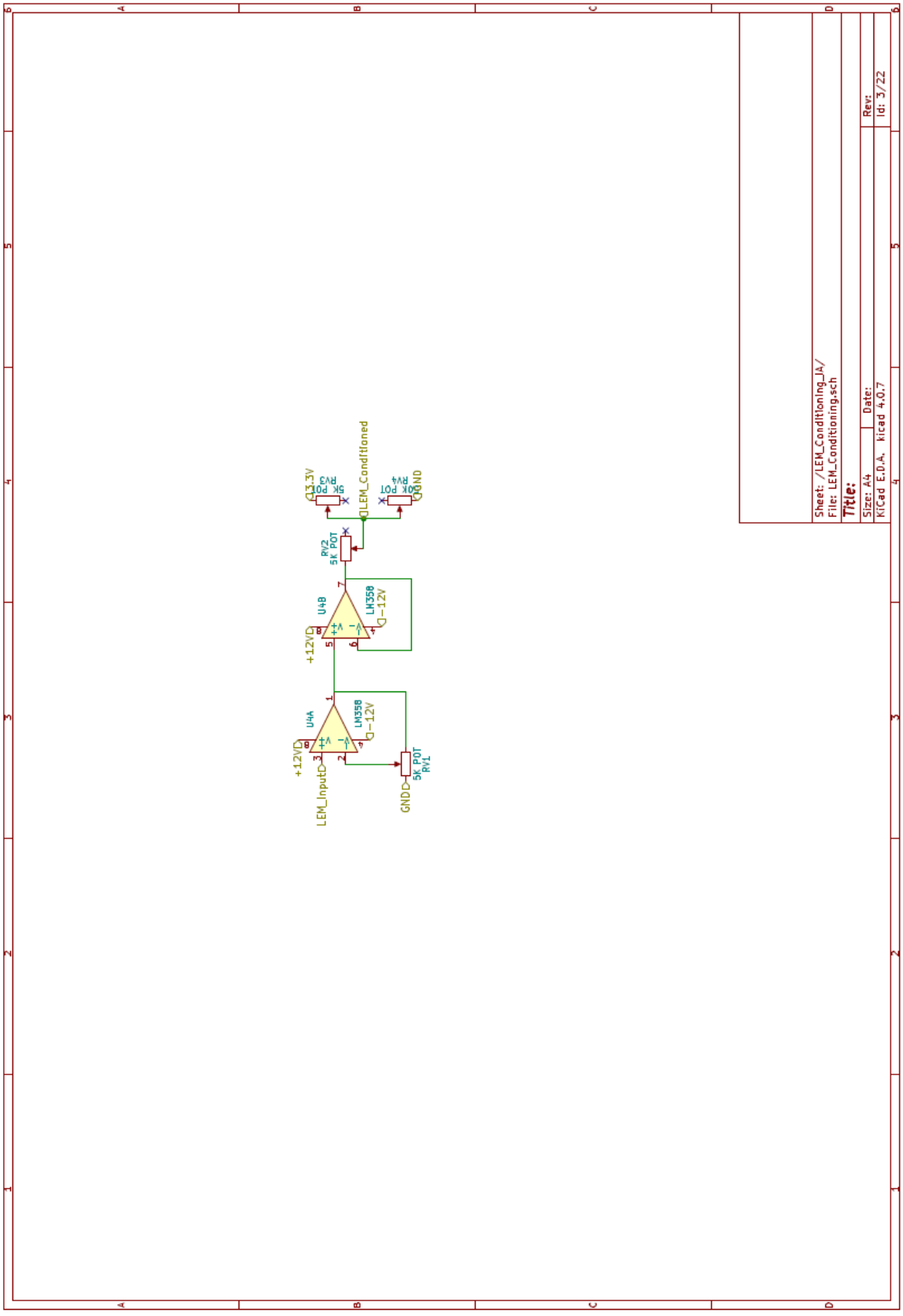
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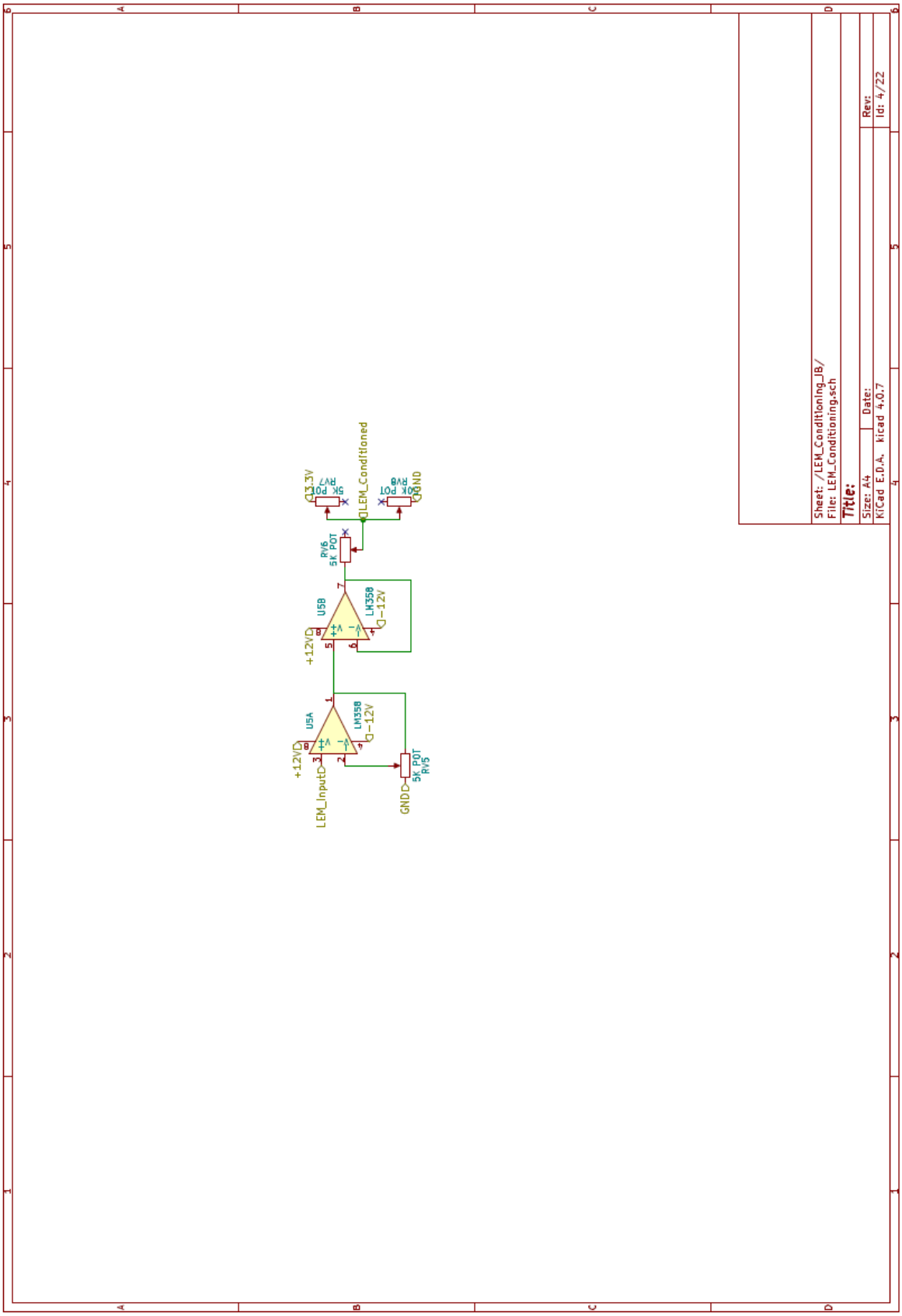
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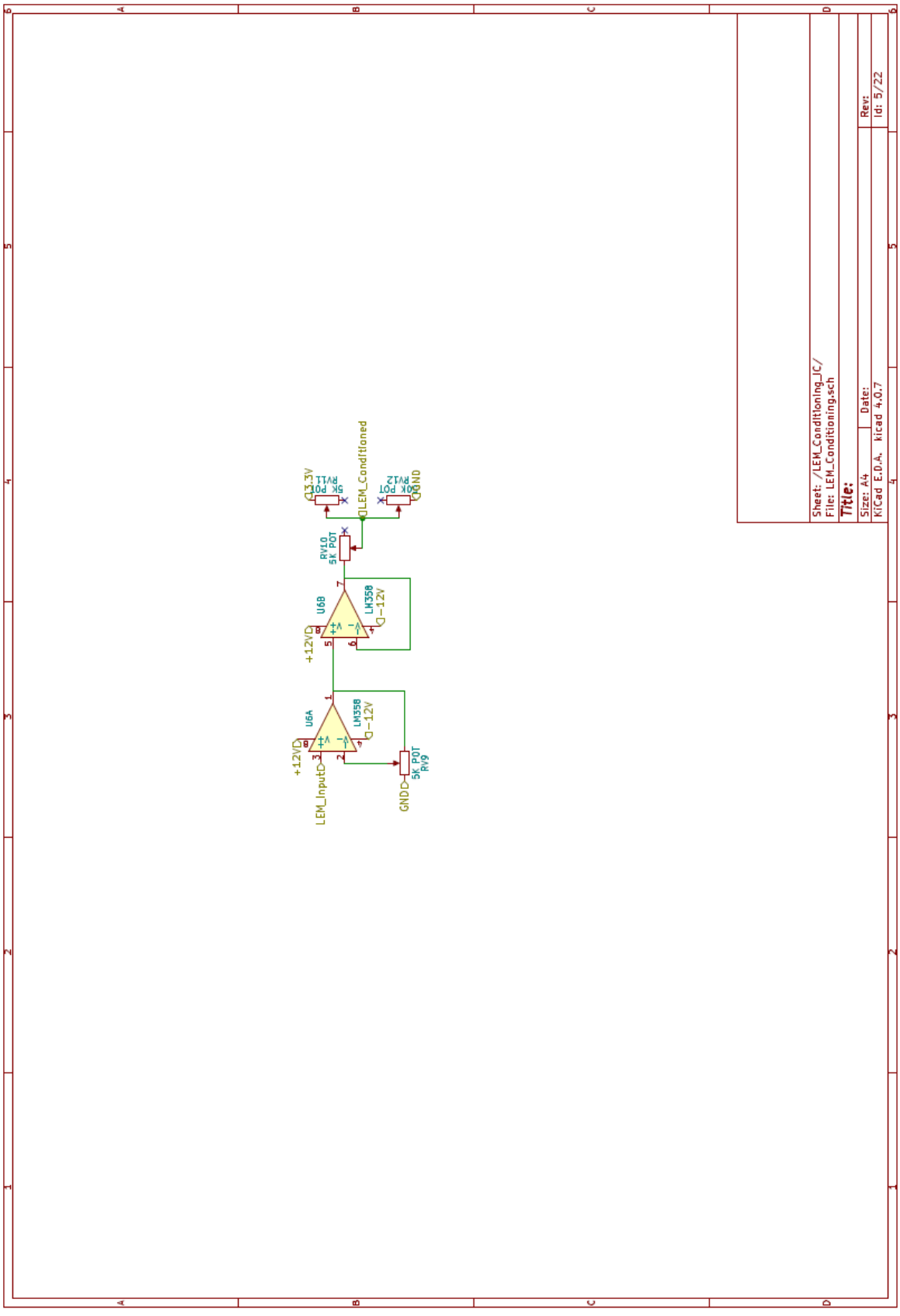
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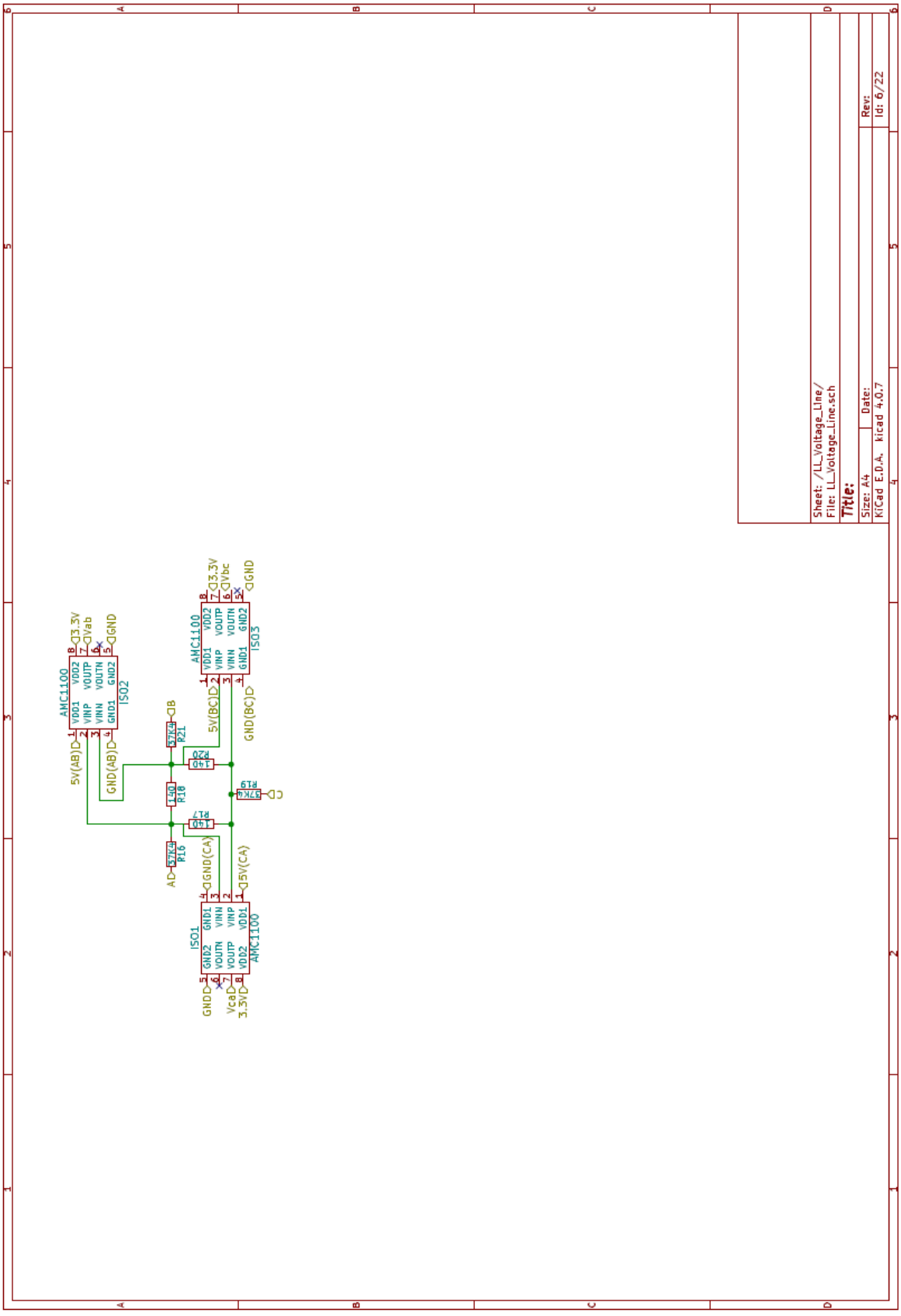
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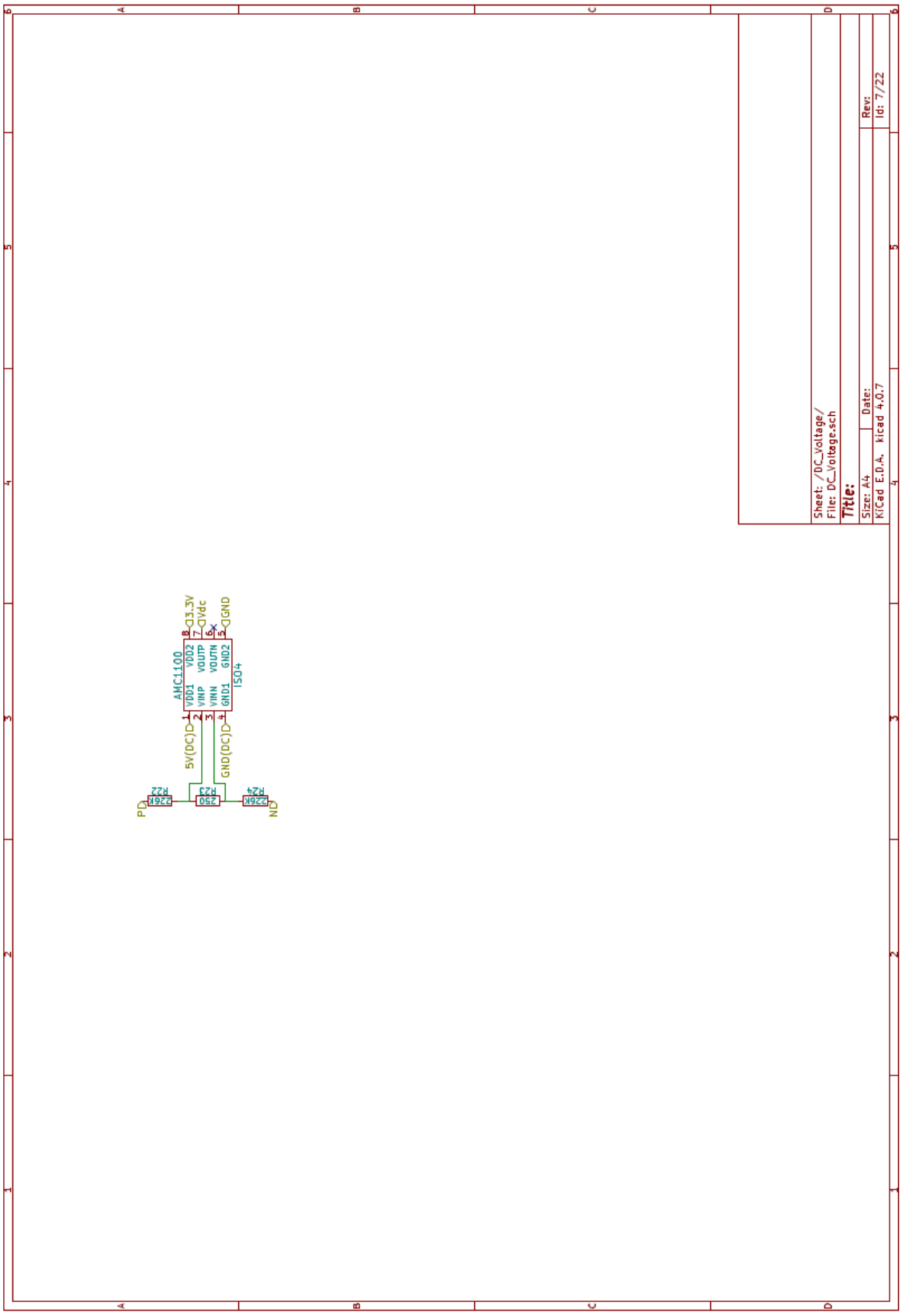
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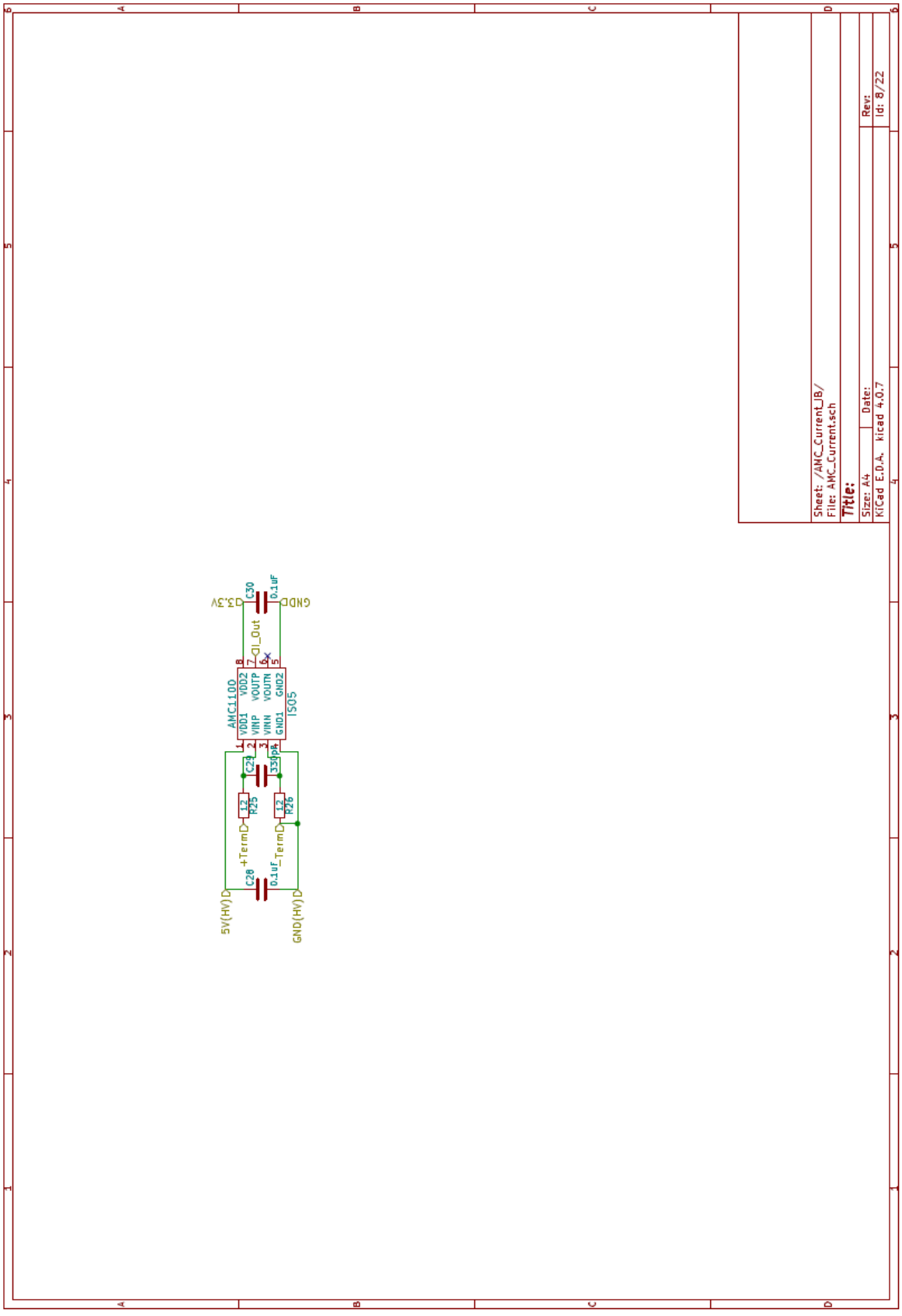
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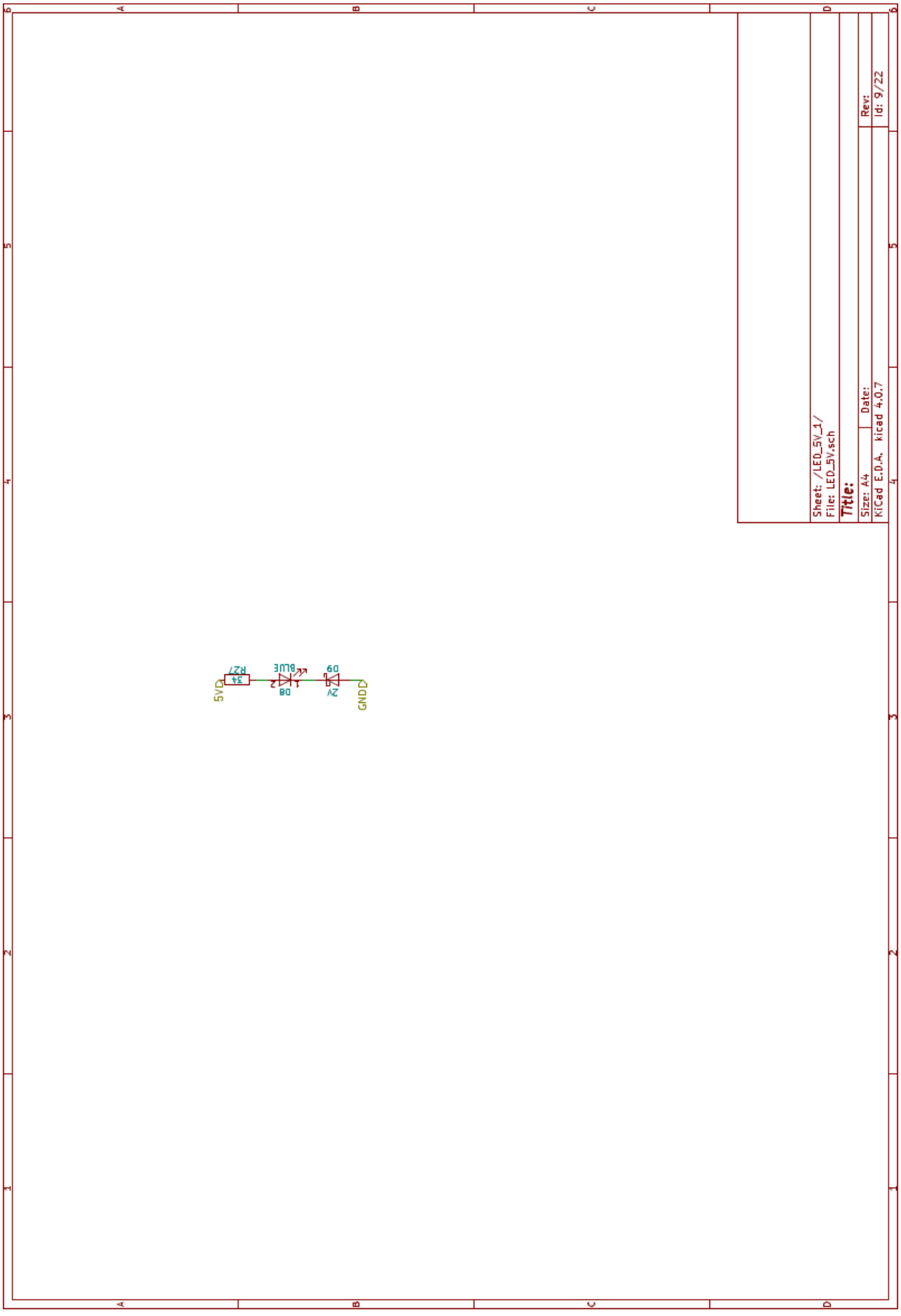
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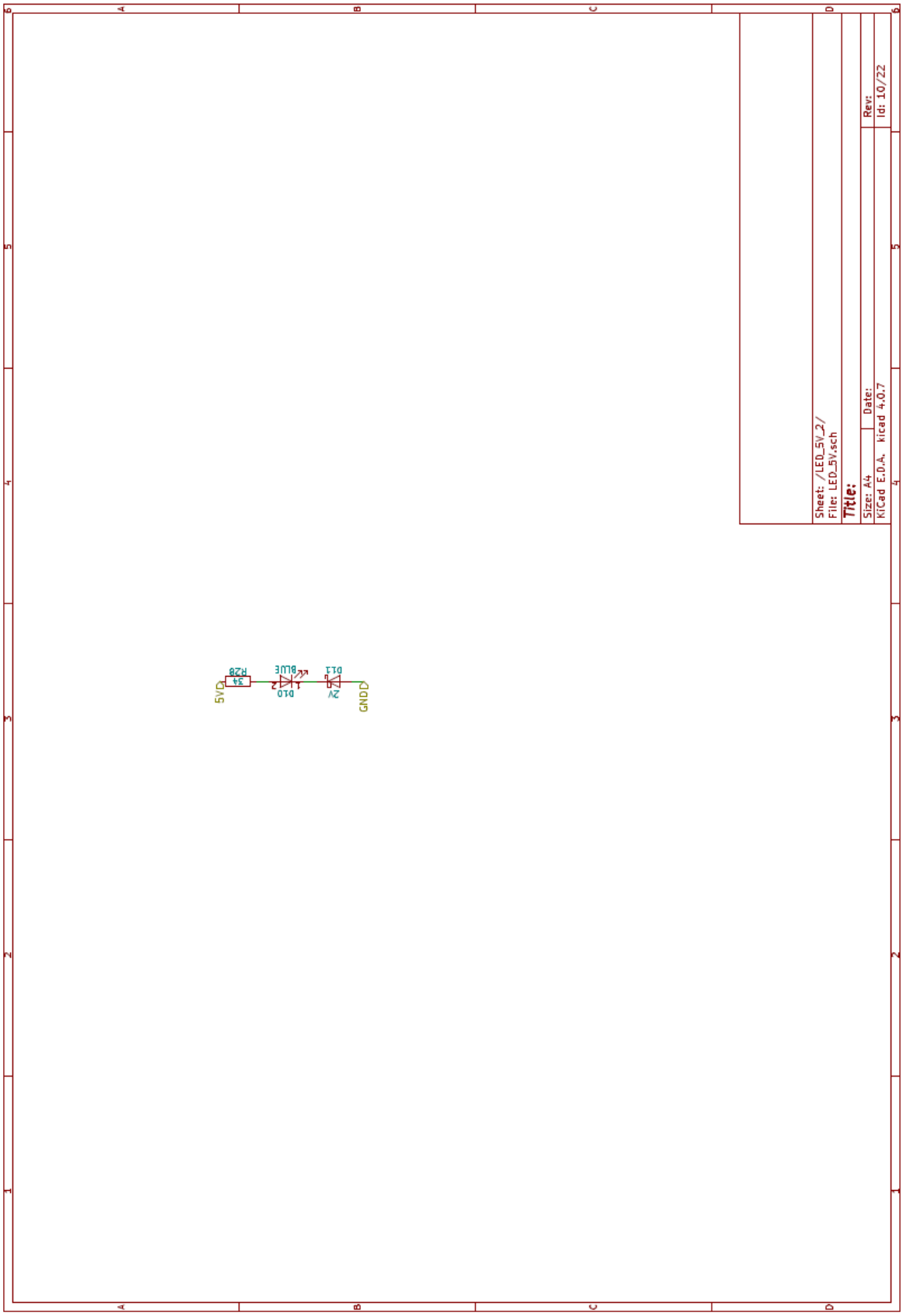
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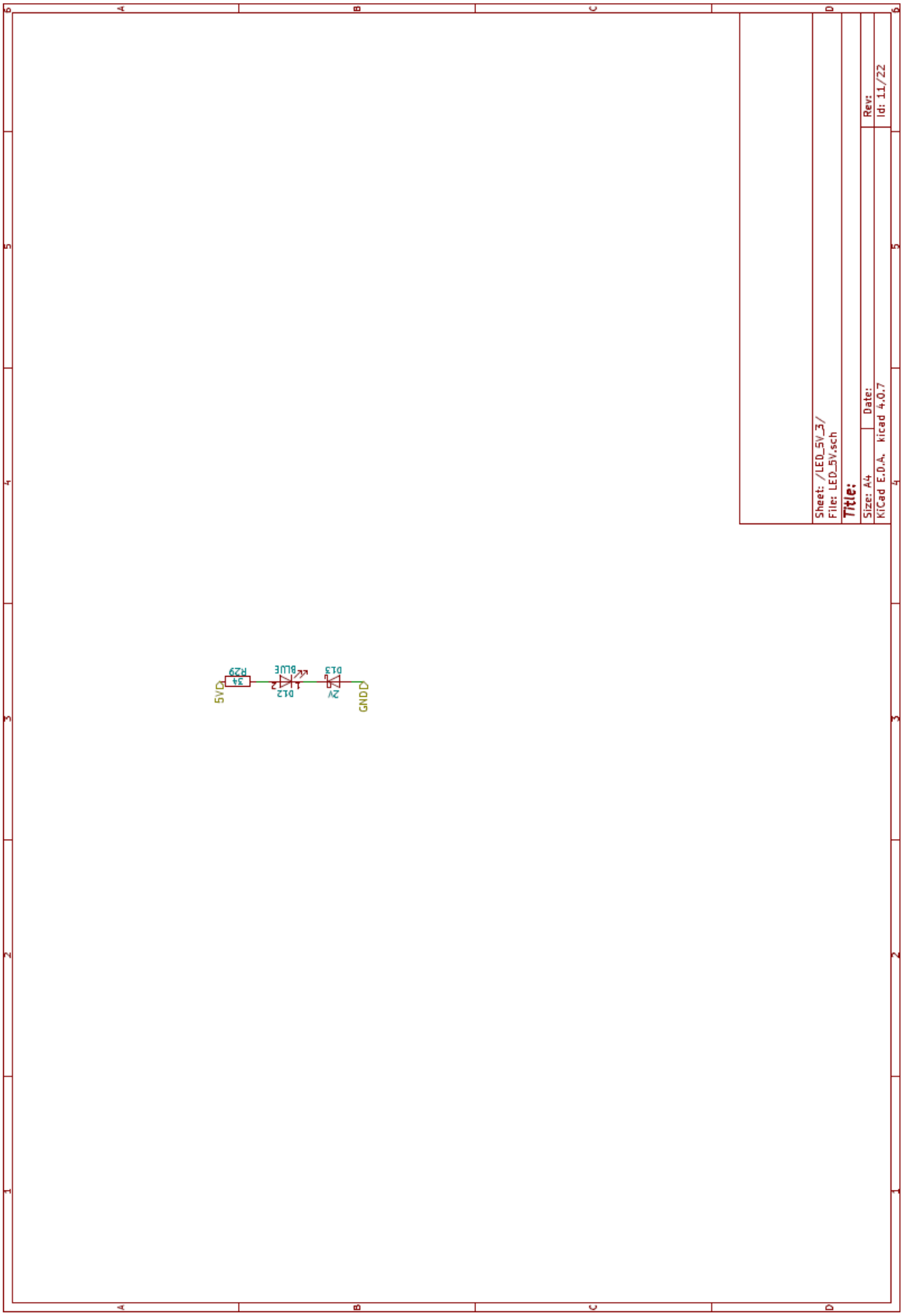
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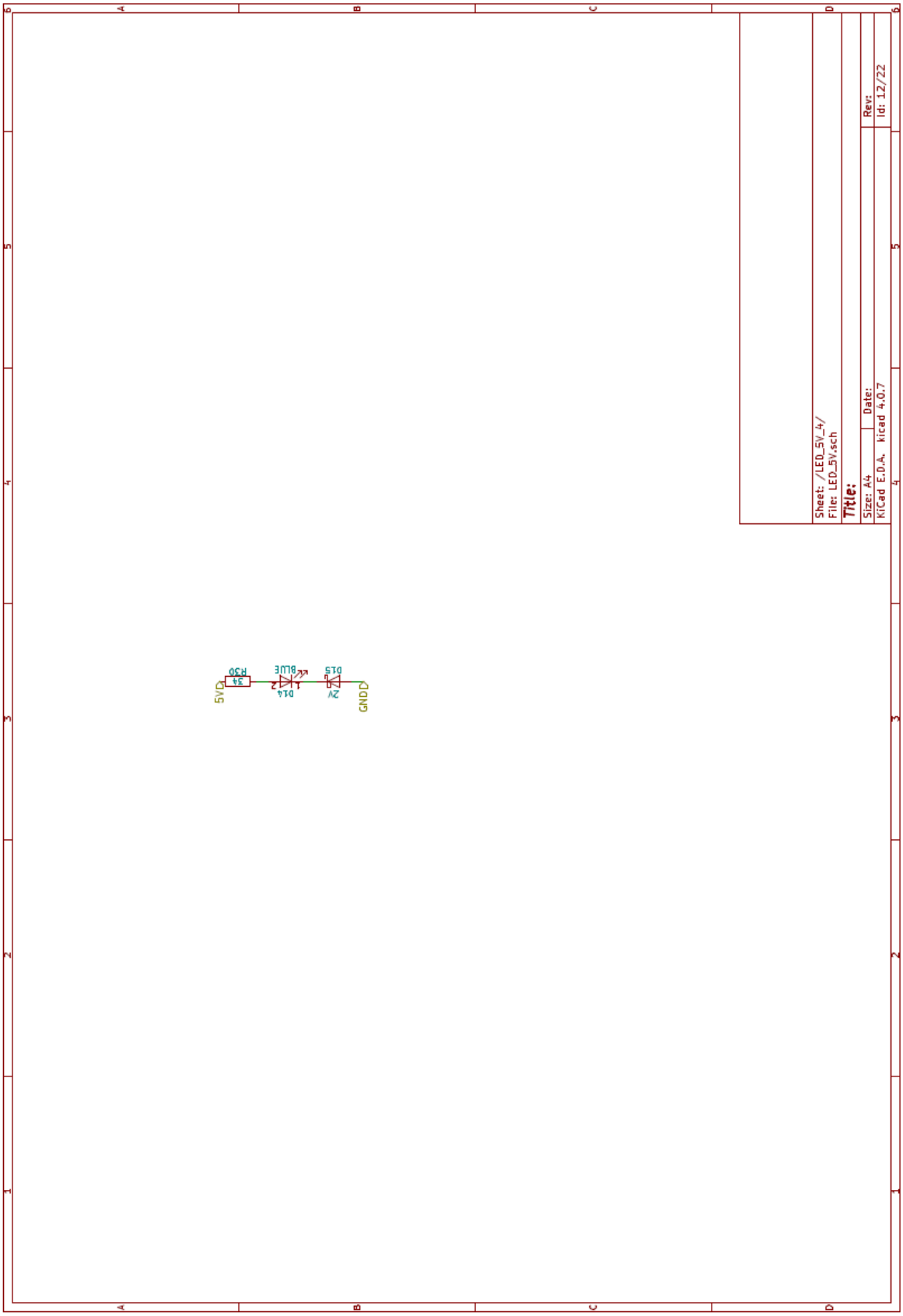
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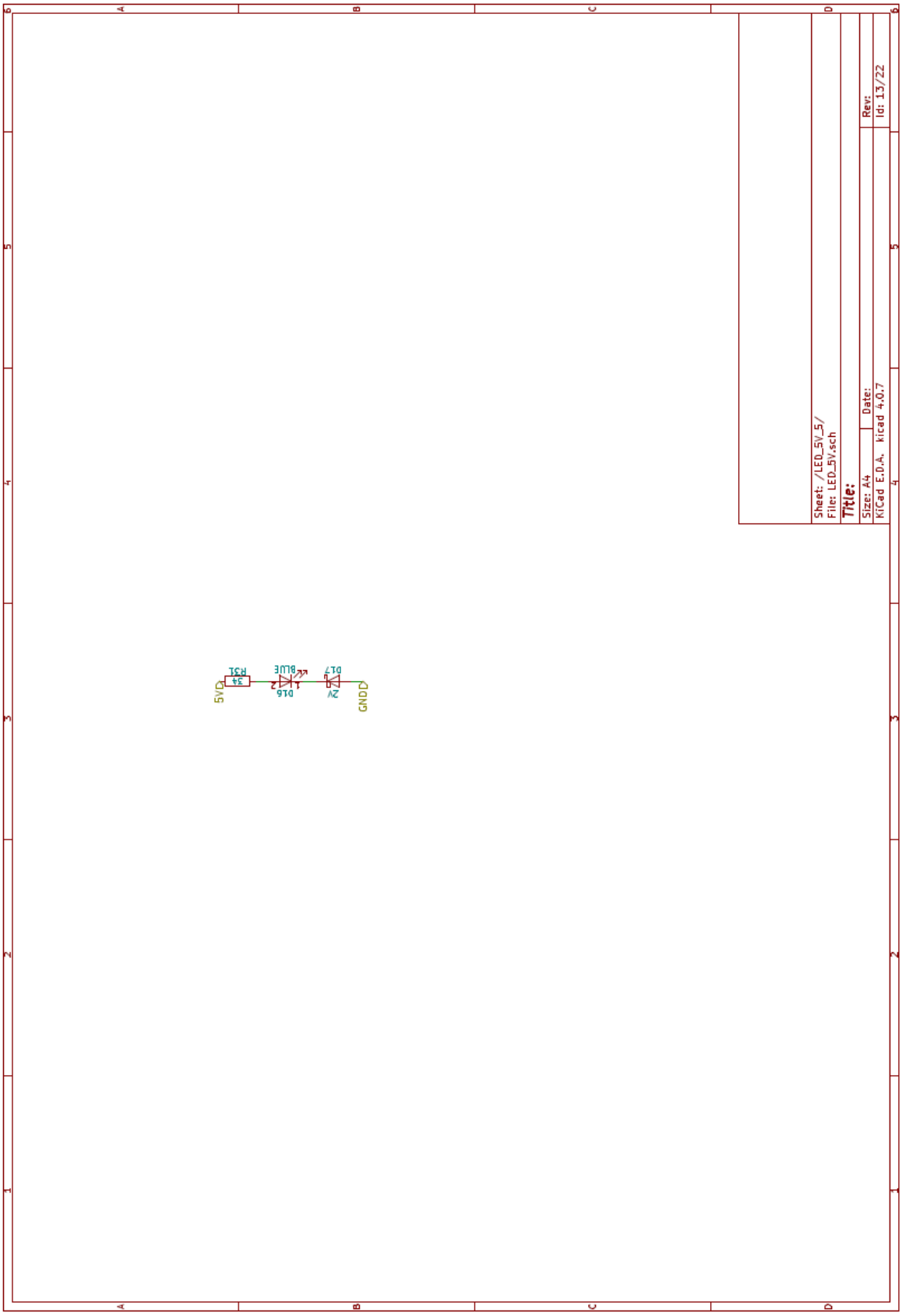
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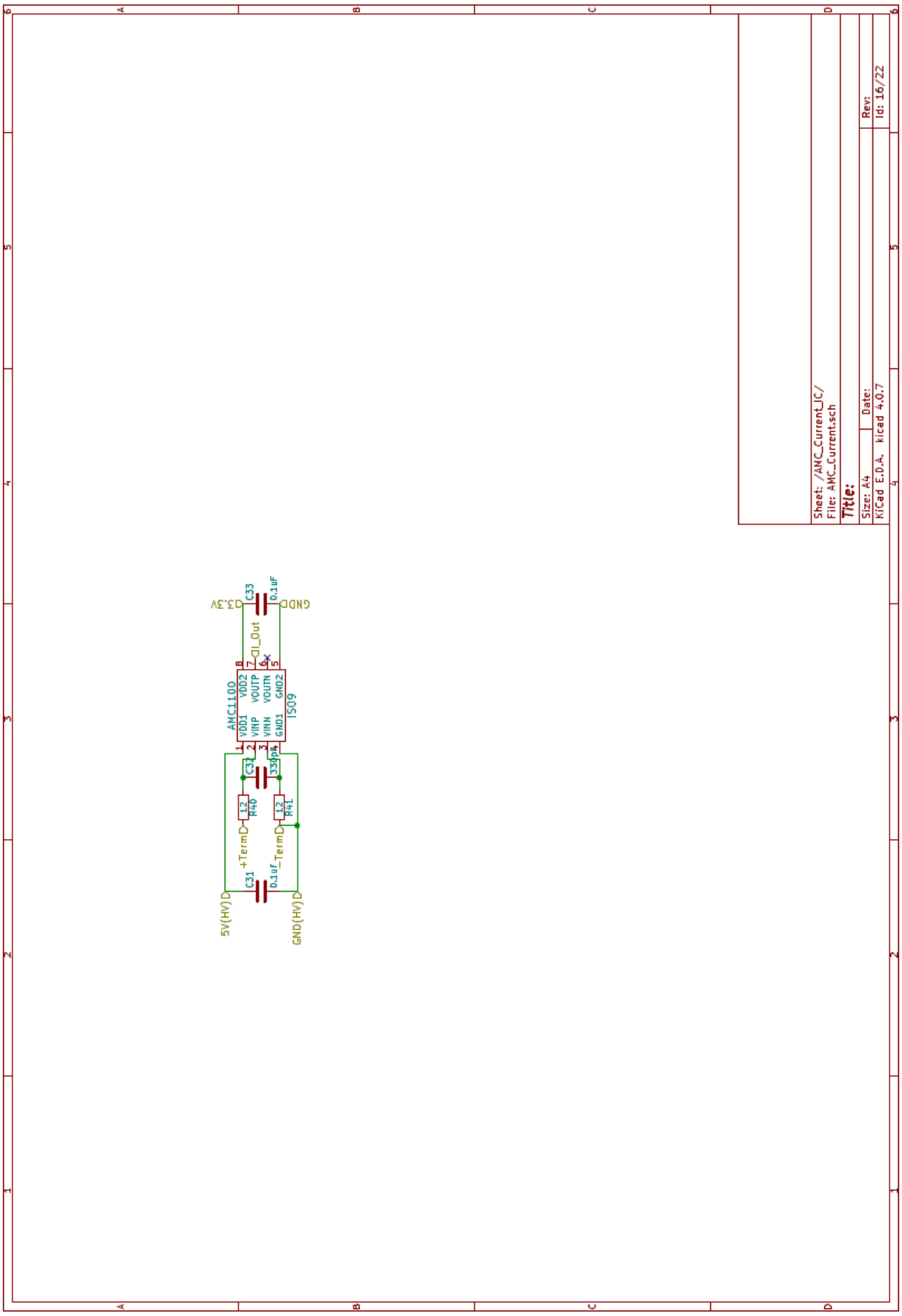
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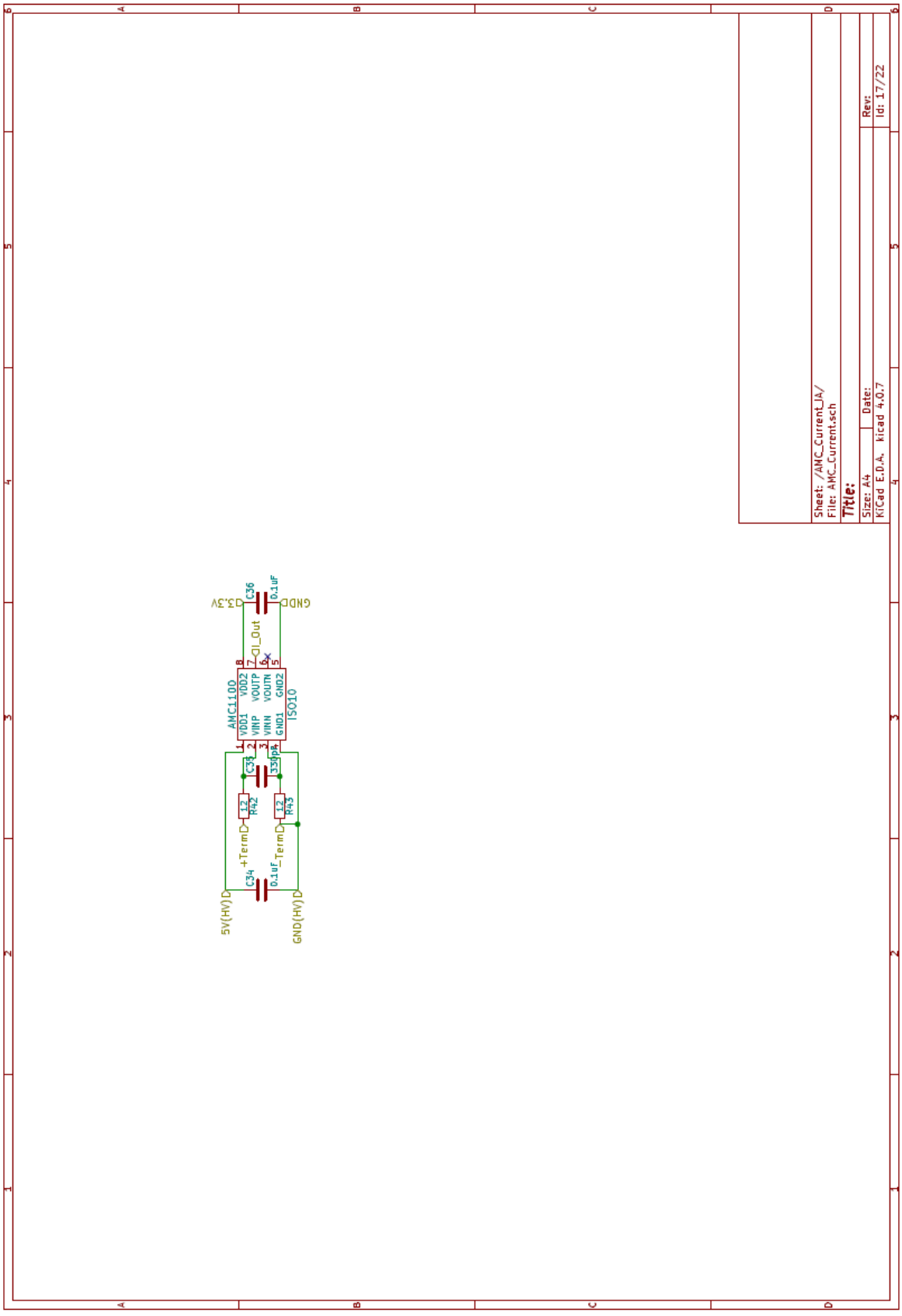
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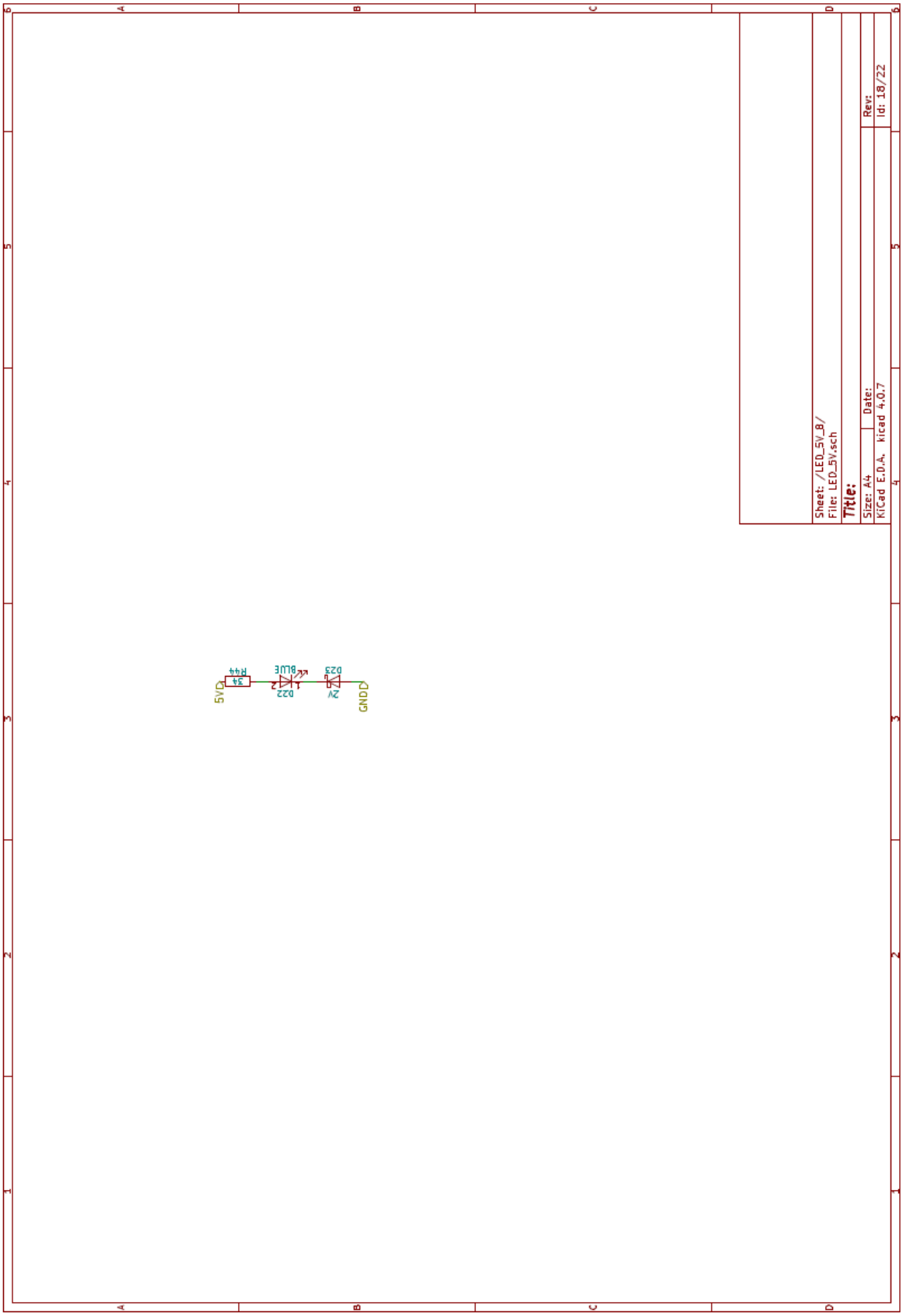
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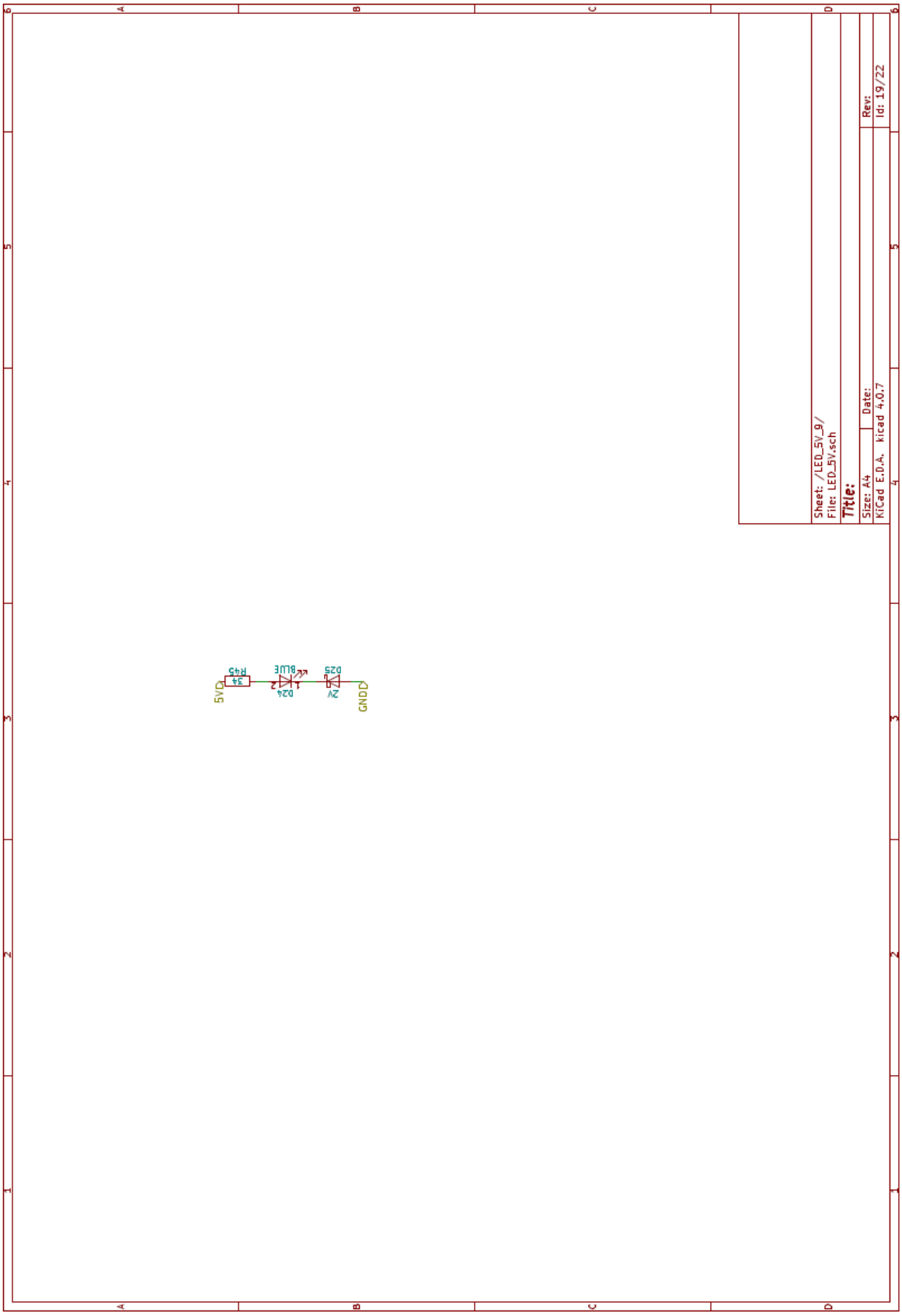
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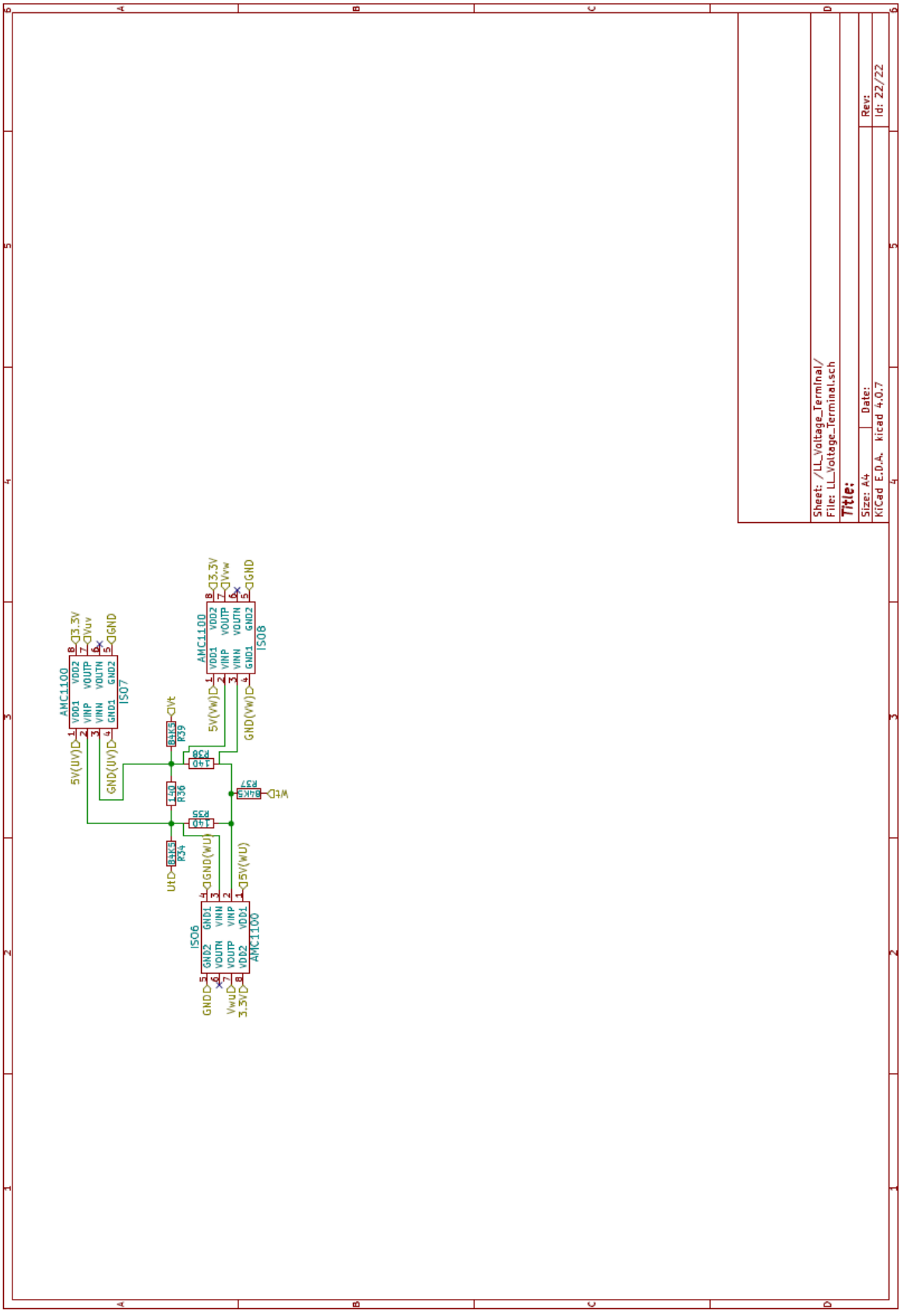
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