Integrity Issues & Simulation of Microelectronic Power Distribution Network

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Sharmin Islam

Major Professor: Aicha Elshabini, P.E., Ph.D.

Committee Members: Mohsen Guizani, Ph.D., Feng Li, Ph.D., and Fred Barlow, Ph.D.

Department Administrator: Mohsen Guizani, Ph.D.

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AUTHORIZATION TO SUBMIT THESIS

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Major Professor _____ Date_____
Aicha Elshabini, P.E., Ph.D.

Committee Members _____ Date_____
Feng Li, Ph.D.

_____ Date_____
Mohsen Guizani, Ph.D.

_____ Date_____
Fred Barlow, Ph.D.

Department Administrator _____ Date_____
Mohsen Guizani, Ph.D.

ABSTRACT

High speed, high densities and system-in-packages play an important role in microelectronics. Taking advantage of process technology improvements, semiconductor vendors are increasing device densities which increases demand on total current delivery. In this case, electrical integrity which includes signal integrity, power integrity and electromagnetic interference, is a major issue. Signal integrity assures acceptable quality of signals within the system, such as transmission line effects, cross talk, impedance mismatch. Power integrity assures acceptable quality of power delivery within the system, such as voltage drop, high impedance, parasitic via inductances, noise coupling are the most significant challenges for a semiconductor device designer. The increasingly rigorous noise requirements and timing issues require more predictive signal integrity and power integrity analysis to meet the market demand.

A robust power distribution network (PDN) is fundamental to the enhanced performance and reliable operation of high-speed and dense microelectronics. The designer must consider proper fabrication and advanced packaging system along with the design techniques to address signal and power integrity issues. Efficient design of the microelectronic system is a multi-variate optimization problem across numerous parameters such as, voltage tolerance, AC current demand, impedance profiles, and package parasitics. In addition, simulation is important to achieve the optimal solution. Simulation can reduce the cost and production time significantly, especially for new product development. Therefore, signal and power integrity simulation is becoming an integral and essential part of the package design and development flow.

In this thesis, three PCB boards included (1) no trace, (2) with trace, and (3) with trace and vias, were designed to characterize the simplest versions of power distribution network (PDN) using differential S parameters. Since PDNs can be extremely complex, that requires advanced

levels of laboratory setups and high performance computational capabilities which were not in the scope of this work. These three designs were fabricated and measured using Network Analyzer N5225A. The three PDN designs were modeled and simulations were conducted using Ansys HFSS. Ansys HFSS is a full wave electromagnetic field simulator for 3D volumetric modeling of passive devices. Ansys HFSS utilizes adaptive iterative solution process using finite element method and provides highly accurate solutions. From the simulations, S parameters and Z parameters of the three PDN models were obtained and differential S parameters were calculated. The results obtained from the simulations were compared with the measured S parameters, Z parameters and differential S parameters. The simulation and measurement data of the three models agreed well up to 1.5 GHz. But with the increasing frequency over 1.5 GHz, a discrepancy between the simulation and measurement data were observed. This may be due to calibration issues with the increasing frequency during measurements. Since the simulation was validated with the measurement data up to 1.5 GHz, these simulation models can further be used with added complex features such as VRM, decoupling capacitors and other elements. and can predict the more complex signal and power integrity characteristics.

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DEDICATION

To my parents,

Late Md. Aminul Islam and Momotaz Begum,

And

My husband,

Shams Ul Arifeen

for their support, affection, and inspiration

TABLE OF CONTENTS

LIST OF FIGURES

LIST OF TABLES

CHAPTER 1

INTRODUCTION

The modern CMOS technology is scaling down to provide a smaller and faster transistor. So, the power supply voltage continues to decrease and the power supply current continues to increase; which creates the signal integrity and the power integrity issues in semiconductors. The objective of signal integrity is to ensure the timing and the signal of high speed data transmission, whereas the objective of power integrity is to meet the DC power requirement and reduce the power fluctuation caused by the AC current switch [1],[2]. Decreasing trace widths, high I/O pin counts, low power supply voltages, and high power supply currents create signal integrity problems. Many signal integrity problems are electromagnetic phenomena in nature and hence related to the Electromagnetic Interference (EMI). Due to the signal integrity, losses and reflections in interconnecting traces, crosstalk between signal lines, or between signal and clock lines, DC "ground bounce", and timing errors arise. In **Figure 1**, arrows are indicating static, quasi-static electric or magnetic fields, and propagation of electromagnetic fields which are produced by electronic circuits and cause the failure of other nearby circuits.

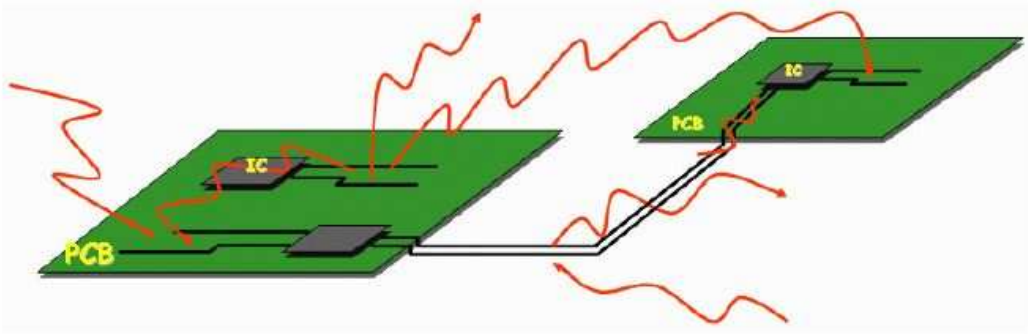


Figure 1: Electromagnetic Interference (EMI)

Higher device densities and faster switching frequencies induce large switching currents that flow in the power and ground networks and cause degradation of performance and reliability. The excessive voltage drops can reduce switching speeds and noise margins of circuits, and may induce noise which can contribute to functional failures. The signal integrity analysis of high-speed electronic designs requires the interconnect models be valid over a wide bandwidth and, for that, scattering parameters (S parameters) are used for signal integrity analysis. On the other hand, power integrity is the sub-division of signal integrity. At higher-frequency, energy is distributed through transmission planes and is dependent on signal integrity issues, so power integrity is more complex than signal integrity [3]. In power integrity analysis, at DC, modeling is relatively simple in that the series resistance of traces, plane shapes, and vias needs to be calculated. But for high frequencies, analyzing the impedance between power and ground at various locations on the PDN requires complex calculations. The PDN must provide rigorous voltage regulation at numerous load points, and maintaining low power consumption is becoming more challenging due to reduction of chip area and increasing metal layers. The intrinsic capacitors between parallel plates of power and ground distribution networks work as local charge storage and help to reduce the voltage drop

at load points; however, these capacitors are not sufficient to mitigate the voltage drop within safe bounds and often designers need to add explicit decoupling capacitors (de-cap) on-package or on-die at strategic locations.

To design an optimal semiconductor device and to get better performance, geometry and material selection, solution of signal integrity and power integrity issues is of the essence. The objective of this research was to analysis signal integrity and power integrity issues for high speed transmissions. Then, high speed IC fabrication, advanced packaging system, transmission line and different network parameters of transmission line, simulation of customized three PDN board measurements and simulations using Ansys have been analyzed. The challenges of IC fabrication advanced packaging system and design challenges of PDN, measurement of three simplified PDN and their simulations, comparison of results and conclusions are described in Chapter 3 to Chapter 7.

CHAPTER 2

BACKGROUND AND LITERATURE REVIEW

Michael Faraday discovered that electrical conduction of silver sulfide crystals increases with temperature, which is not usual in copper and other metals in 1833. Since that time, the semiconductor industry started [4]. After that in 1947, the invention of transistor helped the semiconductor industry to evolve [5]. Later in 1959, the Integrated Circuit (IC) was invented [6] and in 1965, Intel co-founder Gordon Moore formulized that "transistor density doubled every 18 months," which is known as Moore's law [7]. **Figure 2** shows Moore's law [8].

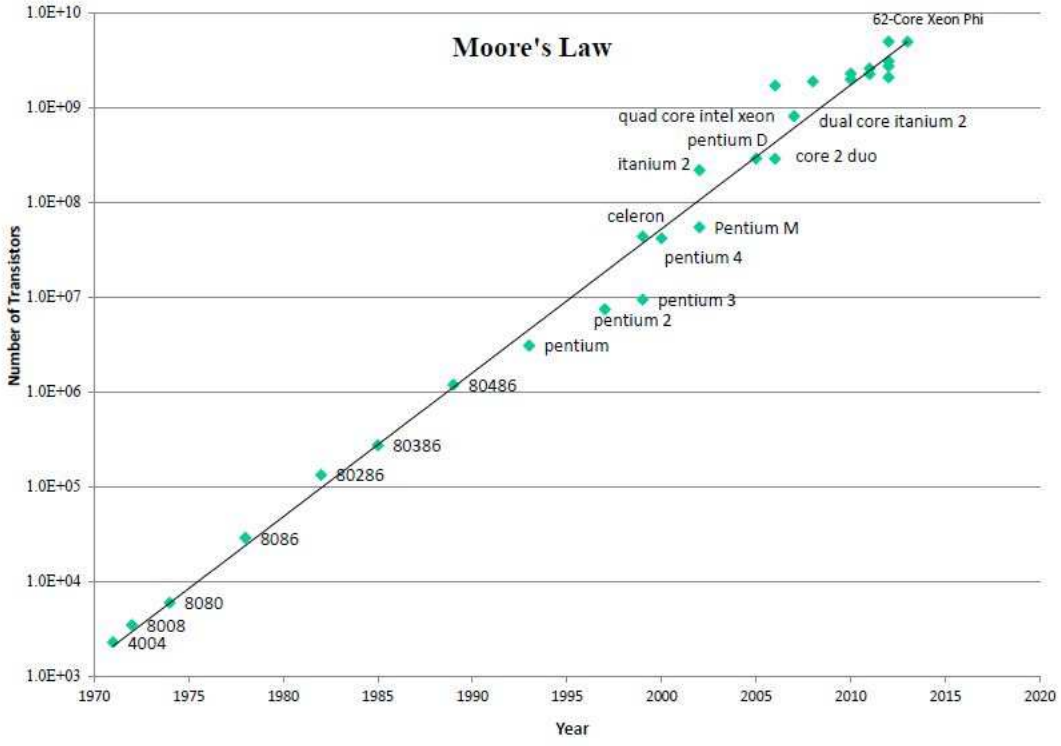


Figure 2: Moore's Law (1970 - 2020)

But, now-a-days, in the semiconductor industry remarkable challenges like Technology Challenge, Power Challenge and Design productivity challenges [9] are threatening for the

continuation of Moore's Law. For technology challenges, IC fabrication and advanced packaging system are significant. Power distribution network (PDN) is fundamental for power challenge of the microprocessor and signal integrity-power integrity is the design productivity challenges.

2.1 High Speed IC Fabrication:

High-speed connectivity needs fabrication of packages that support very fast, varying, broadband signals with good signal integrity (SI). Fabrication is a multiple-step process to create an integrated circuit (IC) on wafer-made semiconductor materials. The electrical properties of a semiconductor material rely on its band gap energy. Usually, Si and GaAs are used as semiconductor materials. Some commonly used semiconductors and their band gap energy at room temperature are given in Table 1:

Table 1. Some commonly used semiconductors and their band gap energy

Semiconductor Material	Band Gap Energy (eV) @ 300K
Silicon (Si)	1.11
Silicon Carbide (SiC)	2.86
Gallium Arsenide (GaAs)	1.43
Gallium Nitride (GaN)	3.40

With extreme temperature due to heat generated during operation and atmospheric temperature, the typical silicon based devices and components are no longer functional for

high efficiency microwave transistors, thus, silicon carbide (SiC)/ gallium nitride (GaN) are potential solutions to have excellent performance in high speed devices [9]. General IC fabrication process for a Si wafer is:

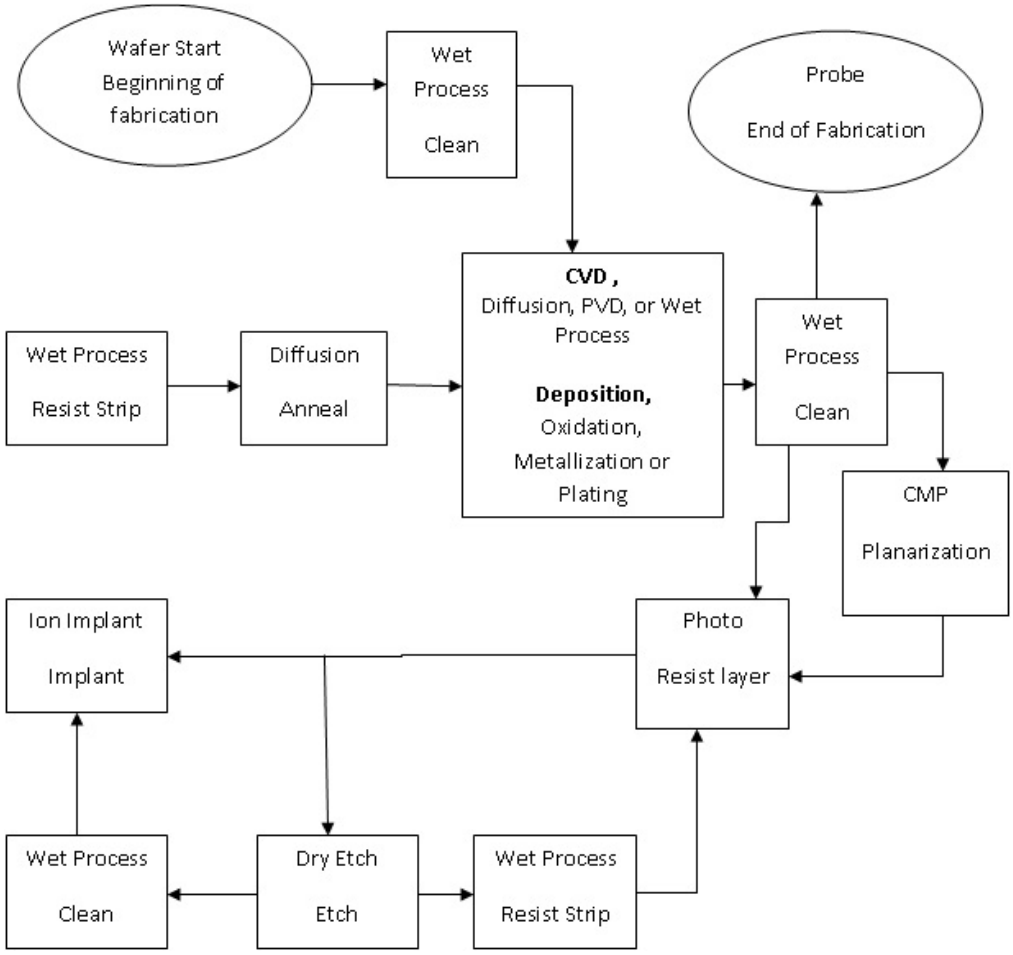


Figure 3: Flow Chart of IC Fabrication Process

2.2 Integrity Issues in Electronic Packaging:

The electronic package is divided into two spheres: the top/bottom domain and the inner domain. The inner domain is the part of the package enclosed by the top and bottom power-ground planes. These two spheres are self-contained multiport networks, and they are associated at the farthermost anti-pad domain of the plate-through vias [10]. With shrinking geometry size, packaging spaces are getting smaller. So, circuit boards and increasing clock frequencies, packaging issues and system-level performance issues (such as crosstalk and transmission lines) are becoming increasingly significant. Thus, integrity of signal transmission becomes critical at high frequencies in IC packaging.

Specifically, High package inductance, inappropriate routing, mismatched traces and placement, inadequate safety for critical paths, and inappropriate return current paths are principal issues for electronic packaging [11].

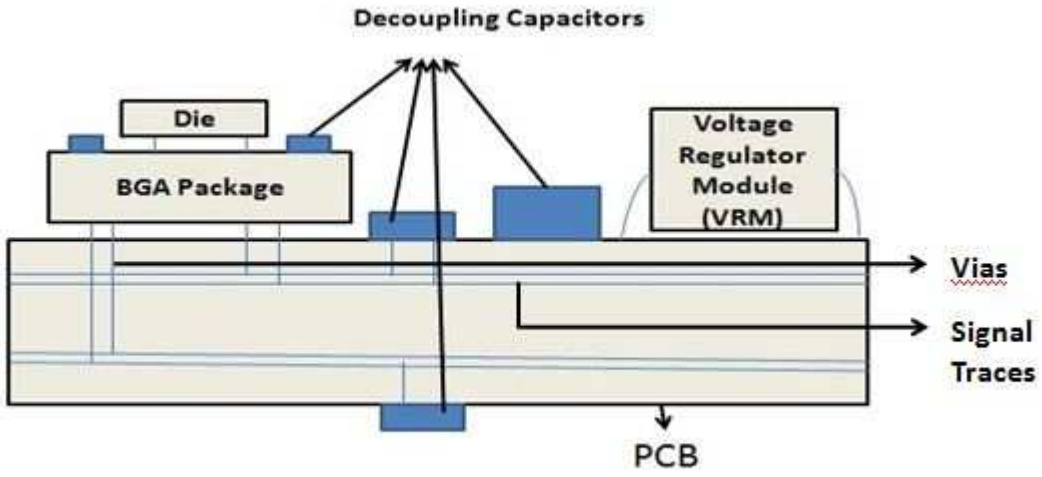


Figure 4: Integrity Challenges in IC Packages

2.3 Transmission Line:

Electrical signals transmitted through metal conductors are called transmission lines. In IC chips and packages, transmission lines are used for connecting the output of on-chip drivers to other transistor circuits. The transmission line is designed as a distributed circuit and the equations are derived by utilizing circuit theory. A circuit model of a trace with transmission line effects is presented in **Figure 5**:

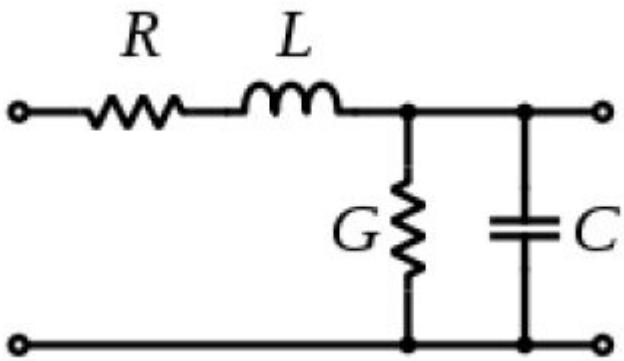


Figure 5: Circuit model of a Transmission Line

In chip packages or printed circuit boards, various transmission lines (like microstrip lines as well as striplines) play a substantial role for SI analysis. Microstrip line (**Figure 6**-a) is used for transmitting microwave-frequency signals and can be assembled using printed circuit board technology, where signals need to be routed from one part of the assembly to another with minimal distortion, and avoiding high cross-talk and radiation. On the other hand, a stripline (**Figure 6**-b) circuit utilizes a flat strip of metal which is sandwiched between two parallel ground planes. Stripline is much harder to assemble than microstrip, because of the second ground plane, narrower widths for given impedance, and board thickness [12].

Figure 6: Different types of transmission line structures in packages and PCB

2.4 Power Distribution Network:

A robust power distribution network (PDN) is fundamental to the enhanced performance and reliable operation of high-speed and dense microelectronics, such as microprocessors. As the modern CMOS technology is scaled to provide a smaller and faster transistor, the power supply voltage continues to decrease and the PDN design becomes more challenging. The PDN must provide rigorous voltage regulation at numerous load points, and maintaining low power consumption is becoming more challenging due to the reduction of chip area and increasing metal layers. Presently, there are two significant power distribution network types: 1) core and 2) input/output; these two are increasingly implemented as filtered supply rails [13]. Higher device densities and faster switching frequencies induce large switching currents that flow in the power and ground networks and cause degradation of performance and reliability. The excessive voltage drops in PDN can reduce switching speeds and noise margins of circuits, and may induce noise which can contribute to functional failures. Due to electro-migration, the high current densities that are common in these products lead to the unwanted wearing out of metal traces [14]. There is also a voltage drop across the network due to the resistance, which is commonly referred as *IR drop*. The intrinsic capacitors between parallel plates of power and ground distribution networks work as local charge

storage and help to reduce the voltage drop at load points; however, these capacitors are not sufficient to mitigate the voltage drop within safe bounds and, often, designers need to add explicit decoupling capacitors (de-cap) on-package or on-die at *strategic* locations. These de-caps increase the required design area and the leakage-power consumption of the chip.

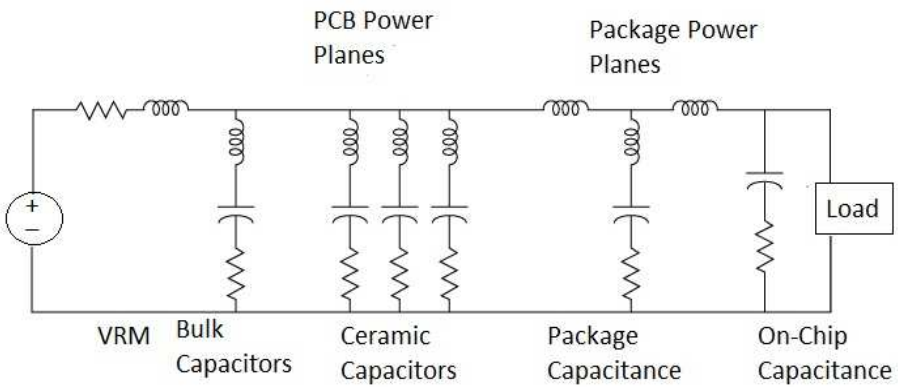


Figure 7: Power Distribution Network Schematic

In **Figure 7**, the voltage regulator module is mounted on the motherboard (MB) to supply voltage to the die through wire-bond pads or C4 bumps. To design an optimal PDN, geometry and material selection is of the essence. The PCB stack-up and PDN planes, the design of AC/DC sources, and the values and locations of de-caps, all must be of certain shape, size, and placement to provide optimal system performance [15].

2.5 Different Network Parameters:

A general circuit can be represented by a multi-port network, where the "ports" are defined as connected terminals at which voltages and currents can be described. Z (Impedance) parameters, Y (Admittance) parameters, S (Scattering) parameters, T parameters, H (Hybrid) parameters, and ABCD (Transfer) parameters are used to represent multi-port networks. Among these network parameters, only S parameters are measureable at high

frequency, but with open or short circuits other parameters (Z parameters, Y parameters, T parameters, ABCD parameters, etc.) are measurable at low frequency.

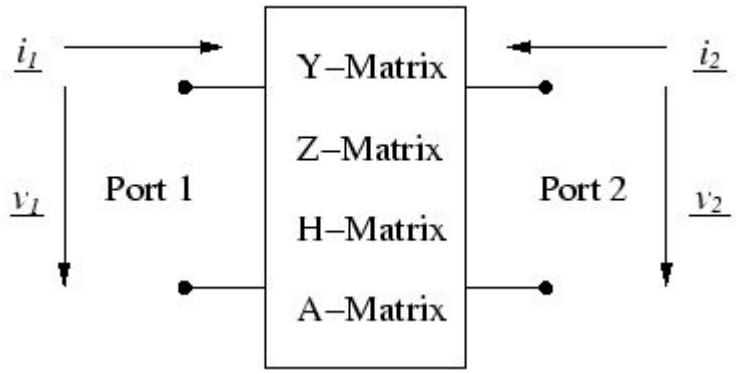


Figure 8: Voltages and Currents of a two port low frequency network [16]

These parameters are beneficial because through the inverse discrete Fourier transform (IDFT) they can be converted to the time domain response, and used to estimate the switching noise.

2.5.1 S-Parameters:

Scattering parameters, or S-parameters, are a measure of how much power or voltage can be transmitted by a port from the chip to the board. S-parameters play a substantial role in high-frequency technology. At high frequencies, true open and short terminations of the device are hard to achieve and it is very difficult to measure currents and voltages. However, what can be measured is the wave entering a port or being reflected by a port. S-parameters are the complex ratio between reflected wave and incident wave and it is complex because both the magnitude and phase of the input signal are changed by the network. S parameters mainly depends on four (4) things-

i. Network

ii. Frequency

iii. Load Impedance (Output Impedance)

iv. Source impedance (Input impedance)

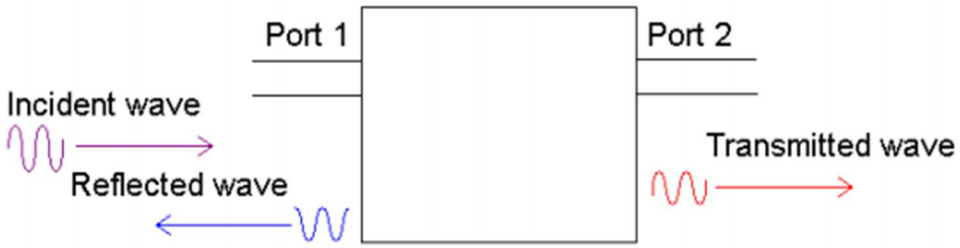


Figure 9: Waves of two ports network

The advantage of S-parameters does not only lie in the complete device performance at microwave frequencies but also the ability to convert to other parameters, which is described in section 2.5.1.2 and section 2.5.2.1.

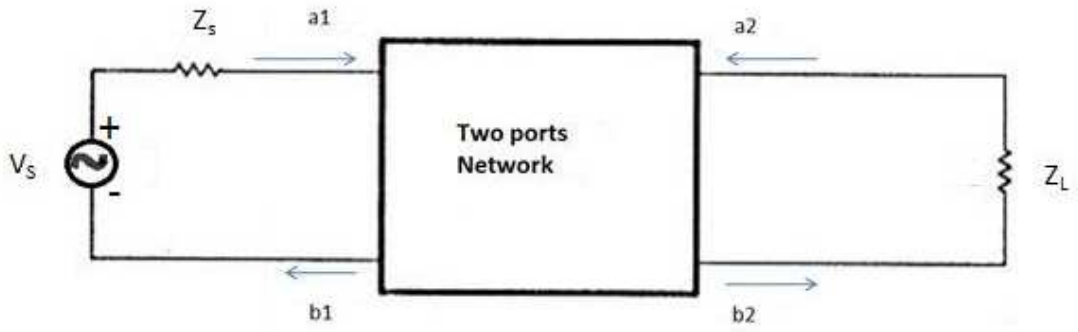


Figure 10: Two port networks for S parameters definition

In **Figure 10**, a1 and a2 are incidents waves which can be described as normalized form:

$$a1 = \frac{Voltage\ wave\ incident\ on\ port\ 1}{\sqrt{Z_0}}$$

$$a1 = \frac{V_1 + I_1 Z_0}{2\sqrt{Z_0}} \qquad (1)$$

$$a1 = \frac{V_{i1}}{\sqrt{Z_0}} \qquad (2)$$

and,

$$a2 = \frac{V_{i2}}{\sqrt{Z_0}} \qquad (3)$$

b1 and b2 are incidents waves which can be described as normalized form:

$$b1 = \frac{Voltage\ wave\ reflected\ on\ port\ 1}{\sqrt{Z_0}}$$

$$b1 = \frac{V_1 - I_1 Z_0}{2\sqrt{Z_0}} \qquad (4)$$

$$b1 = \frac{V_{r1}}{\sqrt{Z_0}} \qquad (5)$$

and,

$$b2 = \frac{V_{r2}}{\sqrt{Z_0}} \qquad (6)$$

Here,

$S_{11} = \frac{b1}{a1}$ with a2 = 0 is a measure of input impedance where input reflection coefficient with the output port terminated by a matched load ($Z_L = Z_0$)

$S_{12} = \frac{b1}{a2}$ with a1 = 0 where reverse transmission with the input port terminated by a matched load ($Z_s = Z_0$)

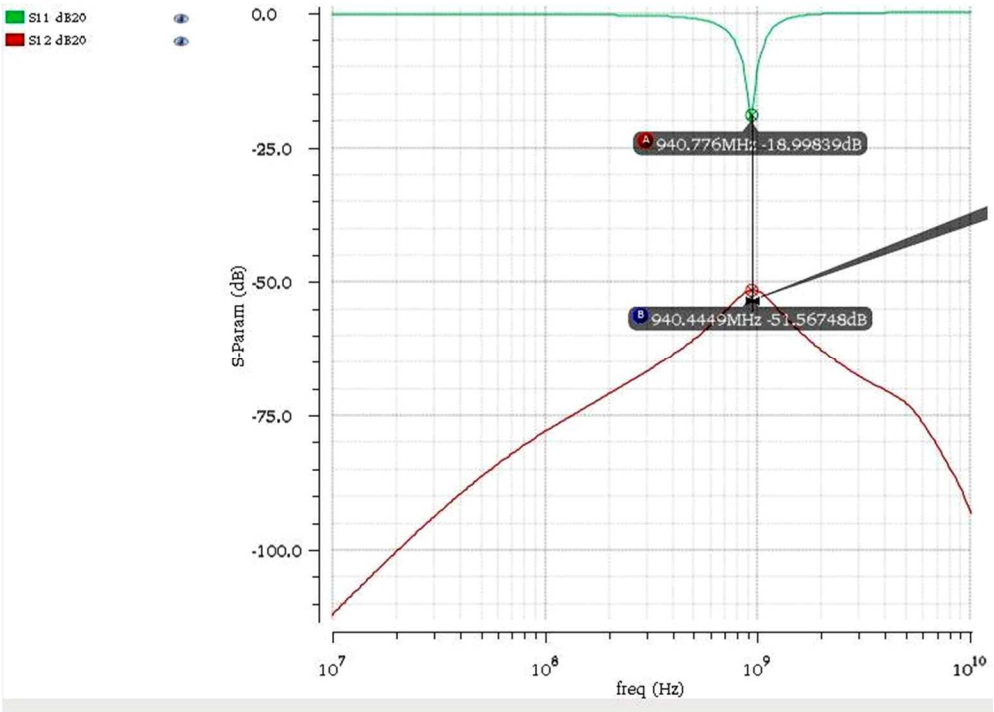


Figure 11: S11 and S12 for 940 MHz low noise amplifier

$S_{22} = \frac{b2}{a2}$ with a1 = 0 is a measure of output impedance where output reflection coefficient with the input port terminated by a matched load ($Z_s = Z_0$)

$S_{21} = \frac{b2}{a1}$ with a2 = 0 where forward transmission gain with the output port terminated by a matched load ($Z_L = Z_0$)

The S matrix for an n port contains n^2 coefficients and the number of rows and columns in a S parameter matrix is equal to the number of ports. A full matrix version of NxN S parameters is:

$$\begin{bmatrix} b_1 \\ b_2 \\ . \\ . \\ . \\ b_N \end{bmatrix} = \begin{bmatrix} S_{11} & S_{12} & . & . & . & S_{1N} \\ S_{21} & S_{22} & . & . & . & S_{2N} \\ . & . & . & . & . & . \\ . & . & . & . & . & . \\ . & . & . & . & . & . \\ S_{N1} & S_{N2} & . & . & . & S_{NN} \end{bmatrix} \begin{bmatrix} a_1 \\ a_2 \\ . \\ . \\ . \\ a_N \end{bmatrix}$$

Or,

$$[b] = [S]\,[a]$$

Here, [b] is the reflected wave; [S] is the Scattering matrix and [a] is the incident wave.

2.5.1.1Mixed mode S- Parameters:

Traditional S-parameters are useful for single ended devices. But mixed-mode S-parameters have the proficiency of testing and anticipating differential (balanced) lines and devices of modern high-speed digital systems. The measurement of Mixed-mode S-parameters offer ideal symmetry transmission across a wide frequency ranges (up to several GHz). Mixed mode S parameters consist of Differential and Common mode S parameters. The common mode is also known as even mode and the differential mode known as odd mode. Odd mode (**Figure 12**-b) impedance is defined as impedance of a single transmission line when the two lines in a pair are driven with signals of the same amplitude and opposite polarity. For odd mode,

$$V_1 = - V_2$$

Even mode (**Figure 12**-a) impedance is defined as impedance of a single transmission line when the two lines in a pair are driven with the same amplitude and the same polarity. For even mode,

$$V_1 = V_2$$

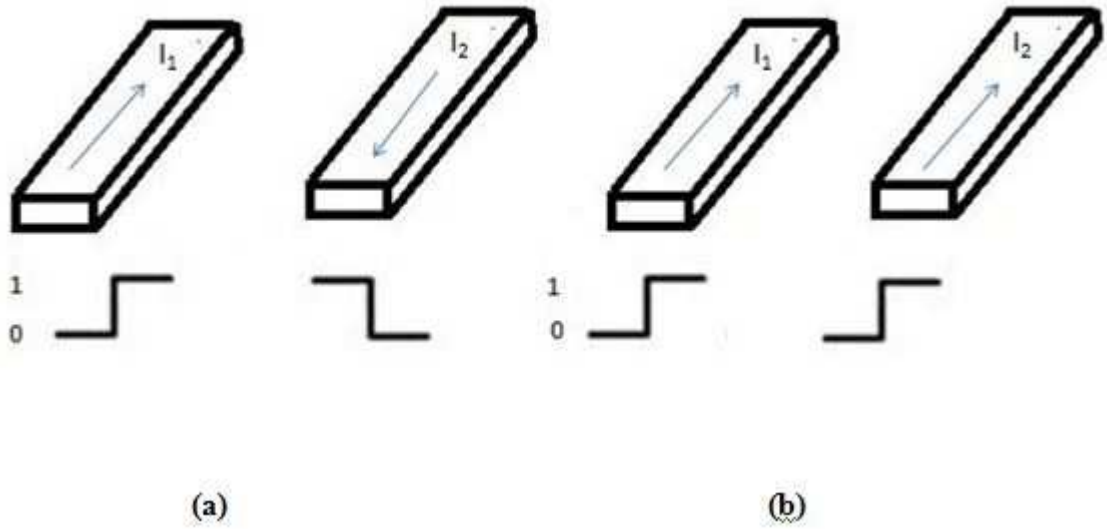


Figure 12: Odd mode and even mode in a microstrip line

A full matrix form of mixed mode S parameters is:

$$\begin{bmatrix} b_{D1} \\ b_{D2} \\ b_{C1} \\ b_{C2} \end{bmatrix} = \begin{bmatrix} S_{D1D1} & S_{D1D2} & S_{D1C1} & S_{D1C2} \\ S_{D2D1} & S_{D2D2} & S_{D2C1} & S_{D2C2} \\ S_{C1D1} & S_{C1D2} & S_{C1C1} & S_{C1C2} \\ S_{C2D1} & S_{C2D2} & S_{C2C1} & S_{C2C2} \end{bmatrix} \begin{bmatrix} a_{D1} \\ a_{D2} \\ a_{C1} \\ a_{C2} \end{bmatrix}$$

Here, for S_{YZ} , Y = response port and Z = stimulus port

S_{DD} implies that both response port and stimulus port are in differential mode

S_{CC} implies that both response port and stimulus port are in common mode

S_{DC} is called common to differential mode and it implies that response port is in differential mode and stimulus port is in common mode

S_{CD} is called differential to common mode and it implies that response port is in common mode and stimulus port is in differential mode

2.5.1.2 Conversion to single-ended S parameters to mixed mode S-parameters

Single ended S parameters can be converted into mixed mode S parameters. In a single-ended ground-referenced device, the input voltage is the difference between the voltage on the node and ground, and the current is the current flowing into the input node; the ground current does not consider when determining the input current [17].

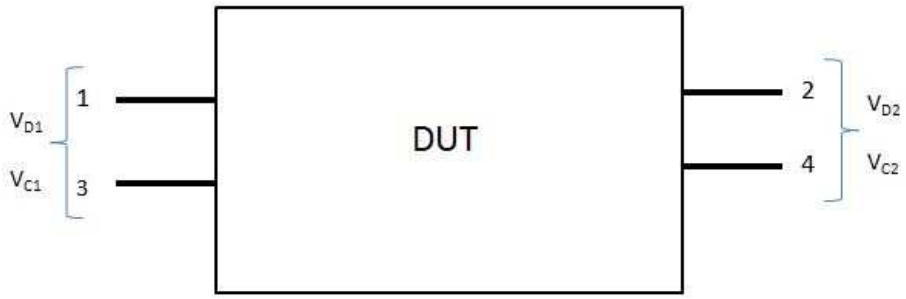


Figure 13: Differential Mode Voltage and Common Mode Voltage

From **Figure 13**, if voltage is V_D and the differential input voltage is the difference between the two inputs, then the differential input voltage will be,

$$V_{D1} = V_1 + (-)V_3 = V_1 - V_3 \qquad (7)$$

And differential output voltage and current will be,

$$V_{D2} = V_2 - V_4 \qquad (8)$$

The differential current is the average of the current flowing into port 1 and out of port 3. The "left-over" is due to common mode current flowing into the network and out of the actual ground node. Thus, one-half of the current flowing into port 1 is differential, and one half is

common; and the different current out of port 3 is the same as $-I_3$, so the average differential current is:

$$I_{D1} = \frac{1}{2}(I_1 - I_3) \quad (9)$$

$$I_{D2} = \frac{1}{2}(I_2 - I_4) \quad (10)$$

For balanced devices, differential input waves and differential output waves are accordingly known as the differential incident (or forward) waves and scattered (or reflected) waves. So, the differential mode forward and reverse voltages are:

$$V_D^F = \frac{1}{2}(V_D + I_D Z_D) \quad (11)$$

$$V_D^R = \frac{1}{2}(V_D - I_D Z_D) \quad (12)$$

Like the differential mode, the common-mode current into the network is the sum of the currents going into ports 1 and the return current flows returning at port 3, and the common-mode voltage into the network is the average of the voltage on ports 1 and 3. So,

$$V_{C1} = \frac{1}{2}(V_1 + V_3) \quad (13)$$

$$V_{C2} = \frac{1}{2}(V_2 + V_4) \quad (14)$$

And common current,

$$I_{C1} = I_1 + I_3 \quad (15)$$

$$I_{C2} = I_2 + I_4 \quad (16)$$

So, the forward and reverse voltage for common mode is:

$$V_C^F = \frac{1}{2}(V_C + I_C Z_C) \quad (17)$$

$$V_C^R = \frac{1}{2}(V_C - I_C Z_C) \quad (18)$$

For electrical impedance,

$$Z = \frac{V}{I}$$

So, at differential mode the impedance will be,

$$Z_D = \frac{V_{D1}}{I_{D1}} \qquad (19)$$

Applying equation (7) & (8) into equation (19),

$$Z_D = \frac{V_1 - V_3}{\frac{1}{2}(I_1 - I_3)} = 2Z_0 \qquad (20)\ ,$$

Where Z_0 is the characteristic impedance. Similarly as equation (19),

$$Z_C = \frac{V_{C1}}{I_{C1}} \qquad (21)$$

Applying equation (13) & (15) to equation (21),

$$Z_C = \frac{\frac{1}{2}(V_1 + V_3)}{I_1 + I_3} = \frac{Z_0}{2} \qquad (22)$$

Now as a and b are accordingly forward power wave and reverse power wave, so

$$a_{D1} = \frac{V_D^F}{\sqrt{Z_D}} \qquad (23)$$

$$a_{D1} = \frac{\frac{1}{2}(V_D + I_D Z_D)}{\sqrt{2Z_0}} \qquad (24), \qquad [From\ equation\ 11\ \&\ 20]$$

$$= \frac{1}{\sqrt{2}}\left[\left(\frac{V_1 + I_1}{Z_0}\right) - \left(\frac{V_3 + I_3}{Z_0}\right)\right]$$

$$= \frac{1}{\sqrt{2}}\,(a_1 - a_3) \qquad (25)$$

Similarly,

$$b_D = \frac{V_D^R}{\sqrt{Z_D}} \qquad (26)$$

$$a_C = \frac{V_C^F}{\sqrt{Z_C}} \qquad (27)$$

$$b_C = \frac{V_C^R}{\sqrt{Z_C}} \qquad (28)$$

From these (23), (26) - (28) equations of port 1 and 2,

$$a_{D2} = \frac{1}{\sqrt{2}}(a_2 - a_4) \qquad b_{D1} = \frac{1}{\sqrt{2}}(b_1 - b_3) \qquad b_{D2} = \frac{1}{\sqrt{2}}(b_2 - b_4)$$

$$a_{C1} = \frac{1}{\sqrt{2}}(a_1 + a_3) \qquad a_{C2} = \frac{1}{\sqrt{2}}(a_2 + a_4) \qquad b_{C1} = \frac{1}{\sqrt{2}}(b_1 + b_3)$$

$$b_{C2} = \frac{1}{\sqrt{2}}(b_2 + b_4)$$

Applying these equations we get,

For forward waves,

$$\begin{bmatrix} a_{D1} \\ a_{D2} \\ a_{C1} \\ a_{C2} \end{bmatrix} = \frac{1}{\sqrt{2}} \begin{bmatrix} 1 & 0 & -1 & 0 \\ 0 & 1 & 0 & -1 \\ 1 & 0 & 1 & 0 \\ 0 & 1 & 0 & 1 \end{bmatrix} \begin{bmatrix} a_1 \\ a_2 \\ a_3 \\ a_4 \end{bmatrix}$$

For reverse waves,

$$\begin{bmatrix} b_{D1} \\ b_{D2} \\ b_{C1} \\ b_{C2} \end{bmatrix} = \frac{1}{\sqrt{2}} \begin{bmatrix} 1 & 0 & -1 & 0 \\ 0 & 1 & 0 & -1 \\ 1 & 0 & 1 & 0 \\ 0 & 1 & 0 & 1 \end{bmatrix} \begin{bmatrix} b_1 \\ b_2 \\ b_3 \\ b_4 \end{bmatrix}$$

If common portion of these waves is M, then,

$$M = \frac{1}{\sqrt{2}} \begin{bmatrix} 1 & 0 & -1 & 0 \\ 0 & 1 & 0 & -1 \\ 1 & 0 & 1 & 0 \\ 0 & 1 & 0 & 1 \end{bmatrix}$$

and,

$$M^{-1} = \frac{1}{\sqrt{2}} \begin{bmatrix} 1 & 0 & 1 & 0 \\ 0 & 1 & 0 & 1 \\ -1 & 0 & 1 & 0 \\ 0 & -1 & 0 & 1 \end{bmatrix}$$

So, the Mixed mode S parameters of single ended S parameters will be:

$$S_{mixed\_mode} = M * M^{-1} * S_{Single\_ended}$$

$$S_{mixed-mode} = \frac{1}{\sqrt{2}} \begin{bmatrix} 1 & 0 & -1 & 0 \\ 0 & 1 & 0 & -1 \\ 1 & 0 & 1 & 0 \\ 0 & 1 & 0 & 1 \end{bmatrix} * \frac{1}{\sqrt{2}} \begin{bmatrix} 1 & 0 & 1 & 0 \\ 0 & 1 & 0 & 1 \\ -1 & 0 & 1 & 0 \\ 0 & -1 & 0 & 1 \end{bmatrix} * \begin{bmatrix} S_{11} & S_{12} & S_{13} & S_{14} \\ S_{21} & S_{22} & S_{23} & S_{24} \\ S_{31} & S_{32} & S_{33} & S_{34} \\ S_{41} & S_{42} & S_{43} & S_{44} \end{bmatrix}$$

So, Single ended S parameters can be converted into mixed mode S parameters:

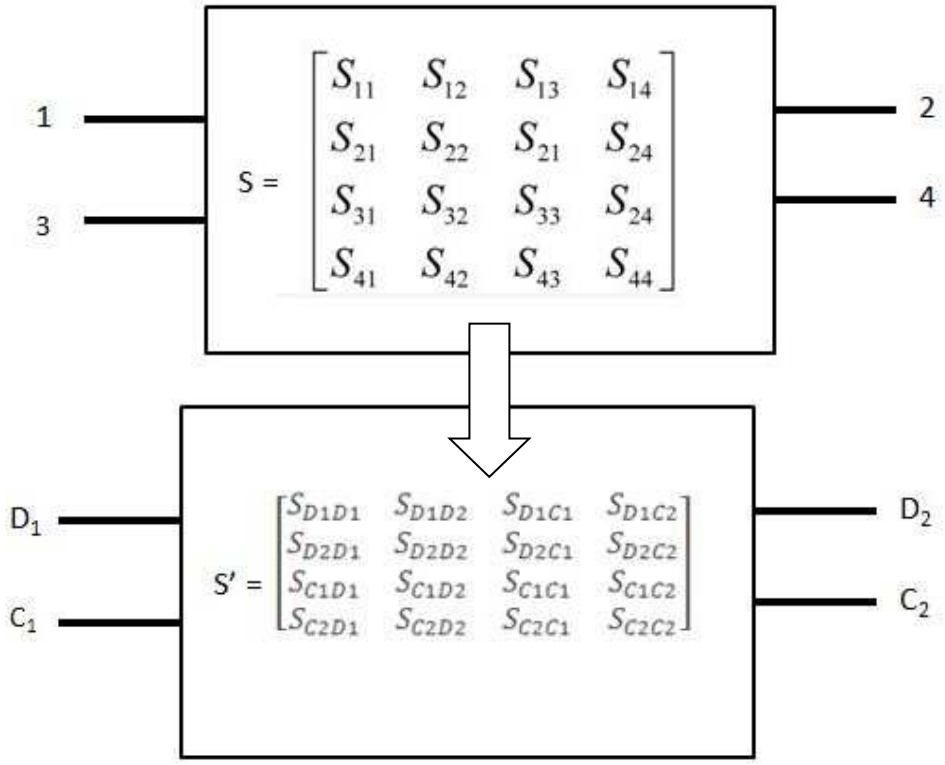


Figure 14: Single ended S parameters to Mixed-mode S parameters

2.5.2 Z-Parameters:

Z parameters or impedance parameters are the complex ratio of voltage to current. In every case, one port of this parameter remains open, so this parameter is also known as open circuit impedance.

$$[V] = [Z][I]$$

Or,

$$\begin{bmatrix} V_1 \\ V_2 \end{bmatrix} = \begin{bmatrix} Z_{11} & Z_{12} \\ Z_{21} & Z_{22} \end{bmatrix} \begin{bmatrix} I_1 \\ I_2 \end{bmatrix}$$

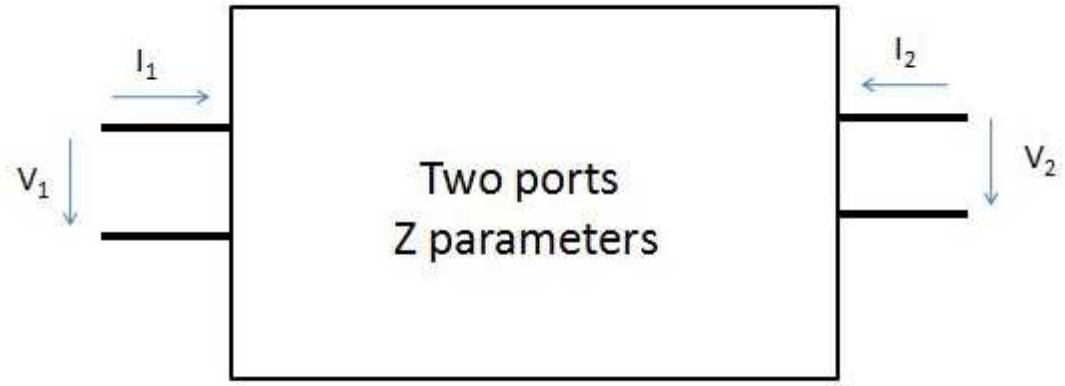


Figure 15: Two port Z parameters

For two ports Z parameters,

$Z_{11} = \frac{V_1}{I_1}$ with $I_2 = 0$ is a measure of input impedance where port 2 is open circuit

$Z_{12} = \frac{V_1}{I_2}$ with $I_1 = 0$ is a measure of transfer impedance where port 1 is open circuit

$Z_{21} = \frac{V_2}{I_1}$ with $I_2 = 0$ is a measure of transfer impedance where port 2 is open circuit

$Z_{22} = \frac{V_2}{I_2}$ with $I_1 = 0$ is a measure of output impedance where port 1 is open circuit

2.5.2.1 Conversion to single-ended S parameters to Z-parameters:

The relationship between reflection coefficient and impedance is the basis of the Smith Chart transmission-line calculator [18]. For S parameters,

$$S_{11} = \frac{b1}{a1}$$

$$S_{11} = \frac{\frac{V_1}{I_1} - Z_0}{\frac{V_1}{I_1} + Z_0}$$

$$= \frac{Z_1 - Z_0}{Z_1 + Z_0}$$

and

$$Z_1 = Z_0 \frac{1 + S_{11}}{1 - S_{11}}$$

Where,

$$Z_1 = \frac{V_1}{I_1}$$

CHAPTER 3

IC FABRICATION & PACKAGING CHALLENGES

Technology towards higher densities and speeds are making the IC fabrication process more complicated than ever before. Nowadays, the chip design and fabrication technology have undergone a tremendous evolution; gate lengths have been scaled from 50 μm in the 1960s to 0.18 μm, and are projected to reach 0.1 μm in the next few years [1].

The major challenges for packaging of high speed semiconductor devices are the die attaches, the substrate design, and the selection of wire bonding.

3.1 Substrates Issues:

For electronic packaging, the substrates contribute to the base for the entire package and maintain an extraction of its power/ground model. Due to the increase of signal transmission speed and the decrease of performing voltage, packaging substrate requires higher density of circuits with thinner materials to assure signal integrity. On the other hand, poor substrate connection causes IC power establishment problems. Generally, the space between the electron die and the substrate is very precise, so during the operation it allows the transfer of the heat generated by the die to the substrate. For this reason, the thermal characteristics of the substrates play a significant role in heat dissipation of package and make the substrate an important component in the thermal management of the overall package. It is a difficult challenge, not only for packaging substrate manufacturers but also materials suppliers, to assure required electrical performance such as signal integrity and power integrity together with mechanical strength and thermal management.

There are various types of substrates and among them the laminated substrates (printed wiring boards) are usually lower power and higher I/O density devices. Conventional laminated substrates materials are not rated to higher temperatures, but the cost is relatively cheap and usually used for multichip and flip chip applications. These laminated substrates are non-uniform structures composed of three elements: a core, build-up layers, and finishing layers. Each element has to develop to meet the demands of packaging applications. For buildup structure substrate, to assure signal integrity and power integrity, thicker core layers evolve into thinner core layer materials and/or change to coreless buildup structure to decrease the loop inductance [19]. Coreless thin substrates (wire bond and flip chip) with reduced metal layers support thin packages and also used for stacked die packages. Substrates with selected solder precoating and thin NiAu plating areas are another alternative [20].

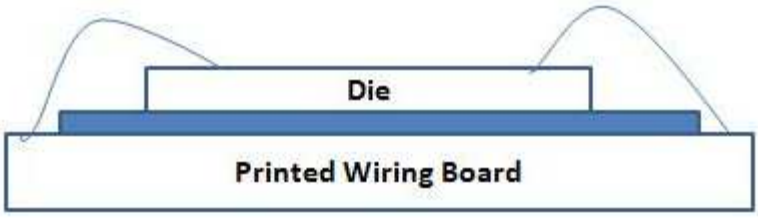


Figure 16: Packaging of High Speed Semiconductor Devices

The key aspect of laminate package technologies is that the electrical performance of the sub-assembly are highly electrically conductive metallurgy to minimize resistive voltage drops (IR drops). According to the Semiconductor Industry Association and NEMI roadmaps current, voltage and power trends will continue for the foreseeable future [21].

Table 2. Roadmap of Current, Voltage & Power Trends

SIA ROADMAP	'01	'02	'03	'04	'05	'06	'07	'10	'13	'16
Power Supply Voltage (V) V_{dd} (High Performance)	1.1	1.0	1.0	1.0	0.9	0.9	0.7	0.6	0.5	0.4
Allowable Maximum Power High Performance with heatsink	130	140	150	160	170	180	190	218	251	288
NEMI ROADMAP	'01	'02	'03	'04	'05	'06	'07	'10	'13	'16
Max. Power/Device (W) Large Business Machine Products			200		225		225	240	280	300
Max. Current/Device (W) Large Business Machine Products			200		250		280	300	350	375

In laminate substrate technology, to effectively deliver power to the chip: low-inductance connections to scale down simultaneous switching noise (SSN); low-dielectric constant insulator materials to better match board impedances and to diminish undesirable parasitic capacitances; and advanced thermal interface materials to maintain high power densities on the chip and to get improve performance are the accountable aspects. The use of thinner, high dielectric constant (k) dielectrics can significantly increase the effectiveness of

this approach. Standard FR-4 technology is limited to 2 mils thickness, a k value of approximately 4 and a capacitance density of only 0.5 nF/in^2. Nowadays, thinner (< 25 μm) dielectric materials, especially those filled with high dielectric ceramic particles, are used for the high frequency power distribution issues. Microprocessor applications represent the significant challenge for laminate substrate technologies. High chip power values lead to increasing current densities that will exceed allowable limits if the design of the laminate is not analyzed and adjusted very carefully. Moreover, higher power values together with fragile low-k dielectric layers on the chip accelerate the critical coefficient of thermal expansion (CTE) mismatch problem between the underfill and chip. In this case, new underfill materials require balancing the thermal expansion between the chip and the laminate substrate [22].

3.2 Die Attach and Die related other issues:

Die attach contributes to interconnects between the perpendicular devices and the substrate. It also provides path for thermal conduction and mechanical supports of the die. In die attach procedure,

- The die is first selected from a classified wafer or waffle tray
- Then the die conforms to a target pad on the carrier or substrate
- Then the die permanently adheres, generally by means of a solder, flip chip bonding, DAF, epoxy bond or taping.

The two most common methods of die attachment are: wire bond attachment (Figure 17-a) and flip chip attachment (Figure 17-b) [[23]-[24]].

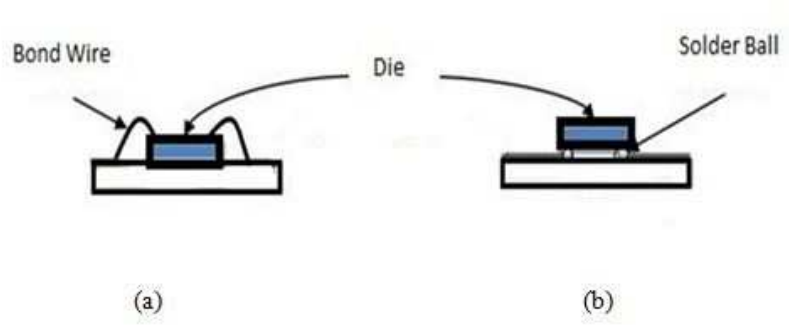


Figure 17: Common methods of Die attachment

Taping process adheres to the surface of the die with the lead fingers on top of the die and develops the die to package density, and increases accuracy and performance by using no epoxy and scaling down wire length to improve speed. During epoxy or taping, the good die evacuates from the wafer using push pins and vacuum tip.

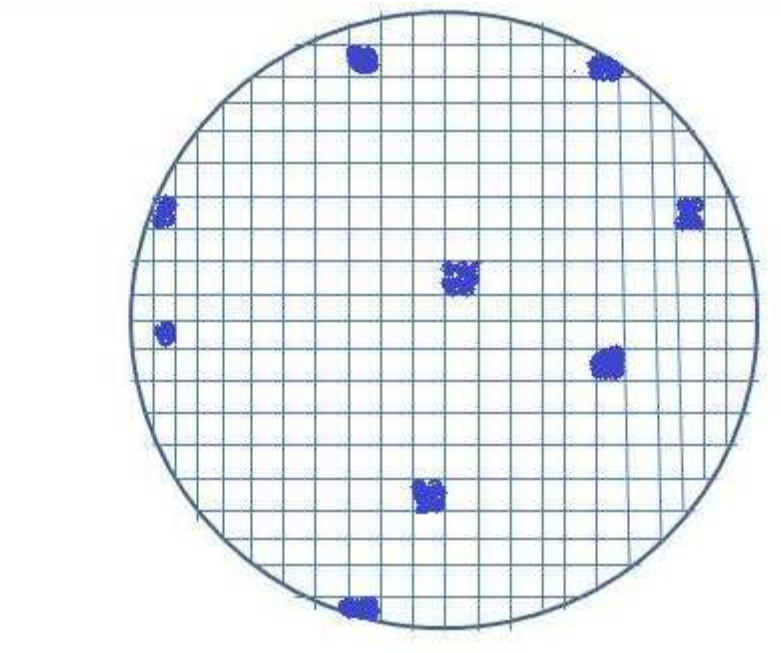


Figure 18: Wafer map at die attach

Void fraction is a challenging issue in die attach. It is important to have minimum void fraction since void fraction can increase the resistance for electric and thermal conduction and become the cause for the failure of the die attach. Typically, for power and high-power applications, utmost void ratio granted is 5% [25]. The requisites [9] for the die attach are,

- Not to transmit destructive tension to the delicate chip (matching coefficient of thermal expansion (CTE)). In general, engineering materials expand with the increase of temperature. The thermal expansion varies in different materials with respect to temperature, and this is called the coefficient of thermal expansion (CTE).
- To create intimate contact between the chip and substrate materials, with no voids.
- To adhere well to both surfaces of chip and substrate material.
- To take out heat generation inside the chip, it should demonstrate high thermal conductivity.
- High melting point.
- Depending on the applications, the die should be either a good electrical conductor or a good insulator.

Heat generation is another major issue in advanced high performance ICs, especially in die attaches procedure. It is anticipated to become more complicated as performance increases and environments become more challenging. With the decreasing heat conductivity of low k dielectrics expected in future generations of ICs, the impact of interconnect self-heating and desirable degeneration is a greater extent of consideration. Die attach done with die backside to the board. Bonding material conditions consists of high adhesion, high

electrical conductivity and high thermal conductivity. Solders with low young's modulus can reduce the stress in the die due to thermal expansion and the thermal expansion is one of the reasons of mechanical stress [26].

For lead frame based packages, where the lead count is typically less than 200, there is a growing problem due to the shrinking die size. The inner lead pitch of the leadframe is limited to a mechanical stamping process. The tightest pitch leadframe inner lead pitch is about 8mils, based on a leadframe thickness of 4mils, but is more typically 10mils. As a rule of thumb, the longest wirebond length should be kept to less than 100x the wire diameter. Otherwise, there is the danger of wirebonds sagging or shorting during the molding process. As die size shrinks, this problem will get worse. One solution is to use an interposer in the cavity, fabricated with a lithographic process that has a fine pitch to match the chip, and fans out to a coarser pitch to match the leadframe [27].

3.3 Packaging Technologies:

Wafer Level Packaging Technology is a developing interconnection technology for the IC packaging for small form factor, high density and/or low-inductance. This technology attributes to a technique in which bumps are applied precisely to a wafer, and after that the wafer is diced into singular ICs. In the semiconductor packaging industry, costing of a semiconductor device packaging is a big issue. So according to accumulative acceptance costs of preferred packaging technologies is usually considered to be:

(1) Wirebonding

(2) Wafer Level Packaging & Flip Chip

(3) Tape Automated Bonding (TAB), already faded out

(4) Through-Silicon-Via (TSV)

Wire bonding is a technique of developing interconnections between an integrated circuit (IC) or other semiconductor device and its packaging during semiconductor device fabrication. Usually aluminum, copper, platinum, nickel and gold are used for wire bonding a die to a package. It is one of the main fail-prone aspects in microelectronic packages. In a harsh environment especially the technique requires a high quality of bond procedures and passive substantial combinations [[28], [29], [30], [31]]. The fundamental impact of the bond wire is its supplementary series inductance. If the length of a bond wire is 100mils, which is important at the performing frequencies, then it shows transmission line behavior. Moreover, wire bonds also produce considerable amount of crosstalk, which restrict the adjacency of signal nets to each other on the wire bonds [23, 24].

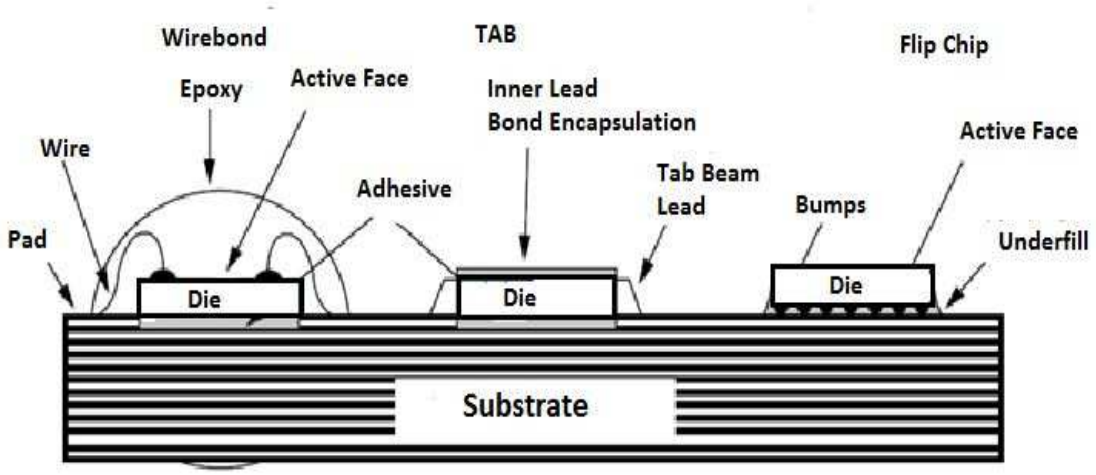


Figure 19: Different Packaging Technologies

On the other hand, flip chip packaging is essentially an excellent form of packaging in regard to electrical perspective. A flip-chip connection is achieved by locating small balls of solder on the pads of the die and then placing the die upside down on the package substrate. If

the series inductance of the flip-chip connection is 0.1 nH, then it is an order of magnitude less than that of a usual wire bond [32]. Other advantages are that the solder ball connections can probably be placed over the entire die, not just on the periphery, so the effect of crosstalk in the solder balls (also called Controlled-Collapsed-Chip-Connector or C4) is minimal, and the I/O count on the flip-chip package is larger. However, flip-chip packaging is not advised due to its thermal and mechanical issues. The thermal coefficient of expansion (CTE) must be comparable between the die and the substrate so that heating of the chip does not motivate the solder balls to be strained. Additionally, cooling of the chip is more demanding and needs expensive procedures as the whole side of the die is wrapped with solder balls and this procedure cut down heat transfer. For these reasons, flip-chip packaging is more expensive than wire bonding and is usually used for high performance applications. Other advantages include higher potential pad count for power and ground pads and flexible positioning over the surface of the die will decrease the impedance of the power and ground distribution network.

From the perspective of device manufacturing cost, wire bond packaging may develop to be a better option, but from an SI and system reliability point of view, flip-chip mounting is more advantagious than wirebonding. It allows for abundant power and ground connections, even for a high signal count package. Moreover in this case, power and ground bumps can be used to surround sensitive I/O bumps.

Tap Automated Bonding (TAB) is for high frequency and high density signal lines. This technique primarily established on mounting and interconnecting ICs on metalized pliable polymer tapes. One edge completely automated bonding of an etched copper beam lead to an IC, and other edge of the lead to a PWB. The primary purpose of the TAB is for

high I/O counts density, so that it can increase electrical performance. It eliminates large wire loops between the chip and substrate and gives support to cut down the impedance and signal delays, and the low profile interconnection structures help to produce thin packages. But the main problem associated with this technique is insufficient production manufacturing, complications in assembly modification, and system testability.

Table 3. Electrical Properties of Various Interconnects

Packaging Technologies	**Resistance Per Length**	**Inductance Per Length**	**Typical Lengths**	**Typical Resistances**	**Typical Inductances**
Wirebond	1 Ohm/inch	25nH/inch	50-100mils	50-100mOhms	1.2-2.5nH
Flip Chip	0.08 Ohm/inch	18nH/inch	3-6mils	<1mOhm	<0.1nH
TAB	0.25 Ohm/inch	21nH/inch	100-300mils	25-75mOhms	2.1-6.3nH

Through-Silicon Via (TSV) is another wafer packaging technology which facilitates the advantages of three dimensional (3D) integrated circuits (3DIC) and conforms with the ongoing challenges for smaller and faster electronics. Higher performance, higher operation speed and volume shrinkage need high 3D interconnect densities [[32],[33], [34], [35]]. Nowadays, wire bonding is restricted in density and performances. So, 3D stacking with micro-vias or TSV, appeared as an unavoidable technology in the future. This technology is important for miniaturization first and growing performances after. Semiconductor

manufacturers are accepting 2.5-D and 3-D technologies to raise the performance and density of their devices through the use of silicon substrates and Through-Silicon Vias (TSVs).

There are two traditional signaling approaches for TSVs:

1. Single-ended
2. Differential signaling

Between these two signaling approaches in high speed system, differential signaling is much more preferrable than single ended signaling due to the doubled voltage margin and virtual ground effect [[36], [37], [32]]. Channel loss for high-speed signaling can be an important issue due to TSV. So, the modeling and analysis of the signalings with TSVs are significantly important for designing high performance TSV channel in 3D IC.

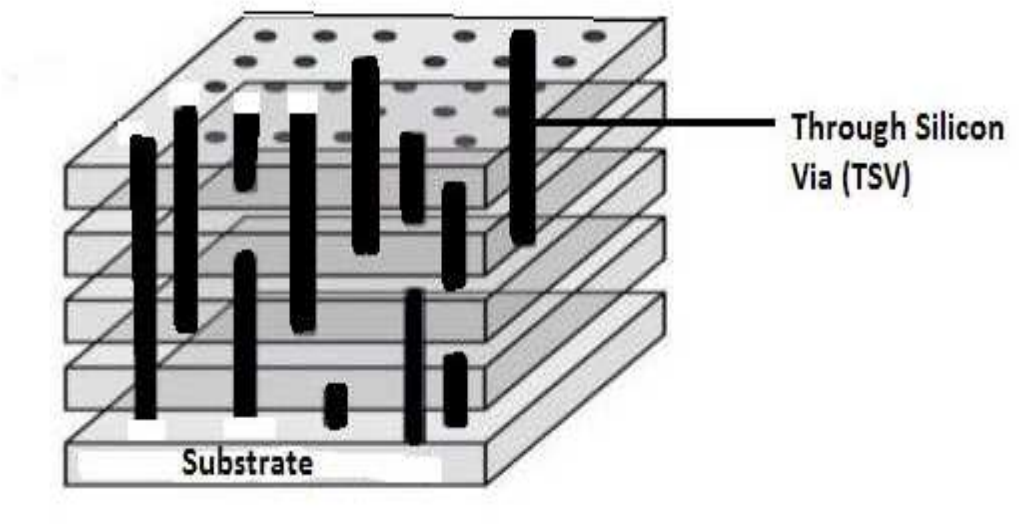


Figure 20: Through Silicon Via (TSV) Technology

Three-dimensional system in-package (3-D SIP) stacks dice in the upright direction, so it reduces the package size and length of the interconnection design significantly. Due to the shortest and vertical interconnection, the TSV designs have excellent electrical

performance with smaller package size and higher I/O density than the wire bonding design. Thermal issue is one of the biggest challenges in die stacking due to thermal hot spot. Another challenge of TSV is due to CTE mismatches in between metal vias and Silicon die stack. That is why the design rules need a keep-out area with no effective devices around the TSV. The design tools are also required to design in such a way that the heat can flow through TSV stacks as some DRAMs cannot accept the feasible temperatures if they are stacked directly on logic layers [38]. TSV with Cu filling has aroused as the procedure of choice of interconnecting stacked and thinned 2-D circuits. Image sensors, flash, DRAM, processors, FPGA, and power amplifiers are some of the remarkable applications of TSV [39, 40]. However, signal integrity (SI) is another key challenge generated by the advance nano-scale interconnects technologies. Coupling noise one of the major signal integrity issues in Through-Silicon-Vias (TSVs) [41].

As package structures of semiconductor devices change significantly due to heat dissipations and IC performance, so considering that, the accepting technique for connecting package to the PCB is ball grid array (BGA). BGA packages use substrates rather than lead frame to get the possible significant improvements in performance. The substrate power and ground connections can be placed adjacent to the die to reduce inductance and resistance. Data and control connections can be laid out to reduce pin-to-pin capacitive coupling and to eradicate any line length variations to reduce the skew. In this case of high speed application, the routing of the signals in the package is done in an impedance controlled mode. BGA utilizes large number of solder balls for acquaintance between the chip and its package and a large fraction between 20% to 30%, of the balls are used as power feeds. This way power is delivered at utmost number of nodes to minimize the current [42, 43, 44].

BGA solder connects BGA package and circuit board and all the signals are transmitted through the BGA solder joints. But the BGA solder joints cause big signal integrity issues in high speed system. As when two solder joints, the transmission performance are impacted significantly. So, Signal Integrity (SI) problems of BGA solder joint cannot be overlooked in high-speed circuit design. Based on height, maximum outside diameter and solder port diameter, BGA creates an impact on signal integrity of solder joints. The return loss of the system increases as the height and maximum outside diameter of solder joints increases in the range of the high frequency. At low frequency, the height and maximum outside diameter of solder have insufficient influence on return loss. However, the impact increases along with the rise of the frequency.

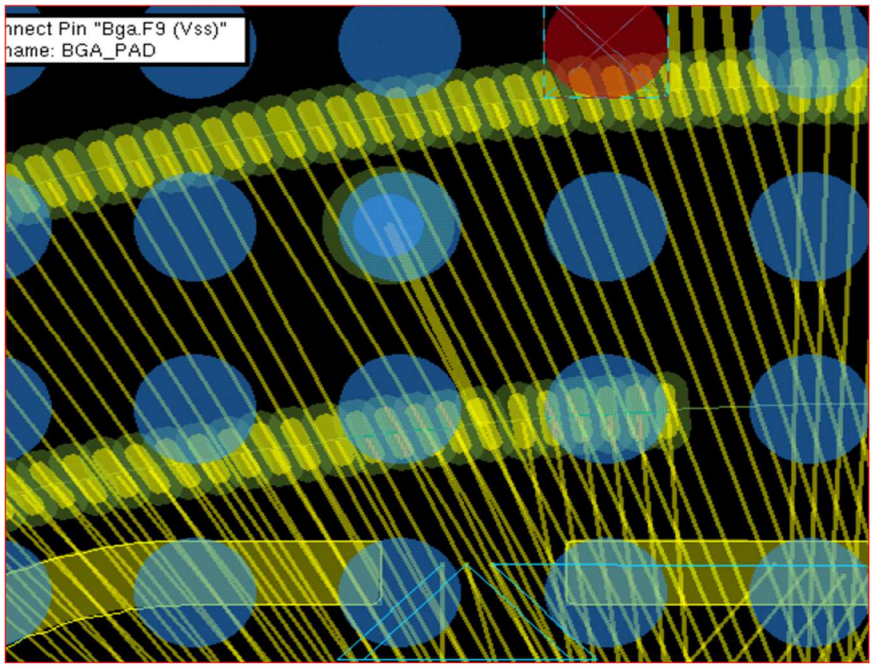


Figure 21: Ball Grid Array (BGA) routing

A perfectly designed package that reduces parasitics is one of the first considerations in semiconductor syetem and for that the positioning of power and ground pin is very

important. So, for BGA routing (**Figure 21**) at first it requires to create power or ground ring. If the power or ground ring does not have the same power like die pins, then it requires to match the power or ground pin with the die pins. For an example, if die pins have only V_{SS}, V_{CC} and VCCIO. But three rings may have V_{SS}, V_{DD} and VCCIO**.** Then it need to change the V_{DD} ring into V_{CC}. So, that the wire bond connection from die pin to ring can not be wrong.

In BGA, vias are expensive in undesirable inductance and abandoned capacitance. So, it is better to keep the vias as minimum as possible. Generally, two vias per trace is the utmost acceptable in addition to the BGA pads. Using a BGA package allows the signal and ground connections to be infuse in a "checkerboard" arrangement, to efficiently shield the signal lines from interfering with each other and in this case, Flip-chip BGA packaging gives much lower parasitics than wire bonding.

CHAPTER 4

DESIGN CHALLENGES

As system performance is increasing, so the designers' challenges are also getting more difficult. The impact of higher performance on the system means the designers have to deal with not only the digital properties, but also the analogue development within the system. As speed increases, the system adopts high-frequency and the shortest lines experience various problems; such as ringing, crosstalk, reflections and ground bounce, electromigration and IR drop. These mentioned problems affect the response of the signal which is the causes of signal integrity. On the other hand, due to smaller and faster transistor, the power supply voltage continues to decrease and the PDN design becomes more challenging. PDN is the major source of power integrity problems. The signal integrity and power integrity issues of high performance semiconductor devices can be overcome by acceptable design technique and by following uncomplicated layout guidance. Some of the common design challenges of high performance semiconductor devices and common strategies to resolve these issues have been discussed in this chapter.

4.1 Power Integrity Design Challenges:

Power integrity attributes are designed to execute the power supply noise across the voltage and ground terminals of the transistors in such a way so they can operate at specific speed. The chip, package, and PCB all contribute towards the generation of power supply noise and the core and I/O circuits required to be powered through the power distribution network (PDN). Therefore, individual designs and communications between chip, package and PCB, play a significant role in determining power supply noise. There are several challenges in the practical design of PDN. The key items are summarized below.

4.1.1 Voltage Regulator:

The voltage regulator is a power supply that keeps the voltage across a load constant as much as possible, by adjusting the amount of current supplied to the load. The challenge of designing a PDN is in accomplishing low voltage at load (0.8 V to 2.5 V) over a large varying current range (up to 100A) [45]. A voltage drop across the network due to the resistance and inductance is of the form [46]:

$$V_{drop} = R\ I + L\ \frac{dI}{dt} \qquad (29)$$

where R is resistance and L is inductor of the channel.

To overcome the voltage drop, designing several supply voltages and placing de-caps in the PDN is very common.

4.1.2 Bypass Capacitors:

Capacitors between the power and the ground distribution network (de-caps) work as charge storage and help to reduce the voltage drop at load points. However, constant de-cap on board and package is not sufficient to mitigate the voltage drop within secure bounds, and designers have to generally add sufficient de-caps on the die at strategic locations. Most designers recommend placing capacitors near the active devices' supply pins; but these capacitors increase the area and leakage power consumption of the chip. Parasitic connections of decoupling capacitors, resistors, and inductors with high-power area-connection packages (PGA, BGA, LGA) produce a complicated RLC structure. Such structures have its unique resonance frequencies [47, 48].

If the resonance frequencies lie near the functioning frequency of the design, large voltage drops due to resistance can develop in the grid [49]. Resonance frequency of a non-ideal capacitor is given by the following relationship

$$f = \frac{1}{2\pi\sqrt{LC}} \qquad (30)$$

where L is the parasitic inductance of the capacitor in henrys, and C is the capacitance in farads.

For the above equation, the impedance of the capacitor is Z=R, where R is the equivalent series resistance (ESR) of the capacitor; thus, the minimum impedance is R. To maximize charge delivery, PDN requires low ESL de-caps. The impedance vs. frequency of an actual electrolytic capacitor (47 μF) is measured using an impedance network analyzer, as shown in **Figure 22**. Here, the impedance initially drops to the 118 Ohms at 1st resonant frequency, then increases due to ESL, but drops beyond 2nd resonant frequency (320 MHz) and finally oscillates until 500 MHz. This behavior highlights the challenge in modeling a realistic capacitor with a simple RLC model, and the practical challenges in selecting the optimal capacitor. In **Figure 22**, the x-axis is frequency (Hz) and the y-axis is impedance (Ω), with the top plot showing the magnitude and the bottom plot showing the phase.

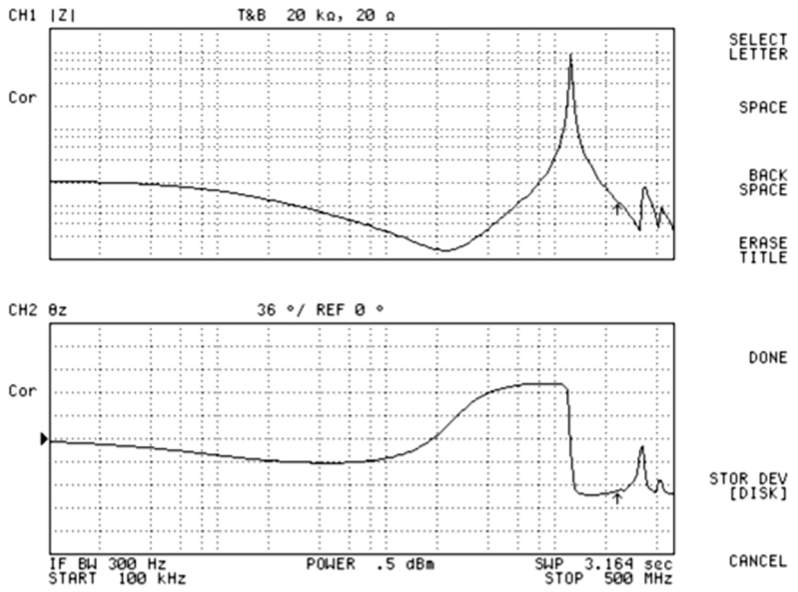


Figure 22: Impedance of an Electrolytic Capacitor

Choosing the values and location of capacitors is very important to achieve the optimal impedance profile, especially because parallel resonances can develop between de-caps and develop into very high impedance. If this high impedance takes place at a frequency in which current transients exist, the noise problem gets worse due to resonance [50].

4.1.3 Noise Coupling:

In the PDN design, the switching noise caused by a digital chip can be closely coupled to near signal traces, and the characteristics of the noise coupling depends on the clock frequency. As the layout density increases in extremely integrated structures, the noise in the power/ground networks becomes increasingly coupled to the signal traces [51], and an accurate modeling and simulations methodology is required to quantify the coupling to the signal traces.

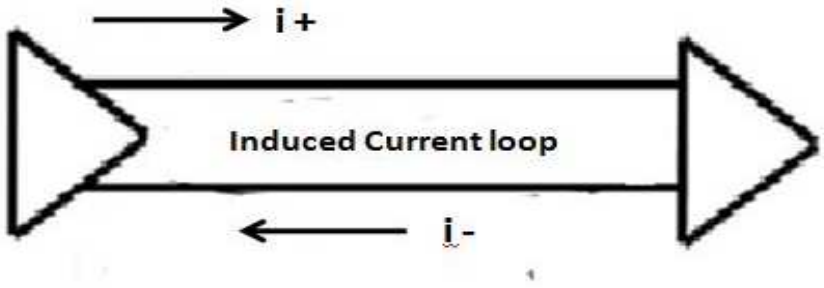


Figure 23: Differential Signaling with closed loop current [52]

Noise coupling is most common near vias at layer transitions, and at partial plane edges. It is expected that the switching noise coupling to signal traces can be reduced by using the differential signaling strategy [51]. Differential signaling is a way of carrying electrical signals with two traces; one of the trace carries positive signal and another carries equal valued negative signal. Due to its high noise immunity, differential signaling can contain extremely high data rates (10 Gb/s) compared to single-ended signaling. Differential signaling induces current flow in a closed loop on the plane under the traces, as shown in **Figure 23**. This type of closed-loop current flow helps to reduce PDN inductance through opposing magnetic flux densities, which is very desirable for a PDN design.

4.1.4 Parasitic Via Inductances:

In the PDN, understanding the parasitic inductance of vias is important for signal/power integrity and electromagnetic intervention analysis, the reason why multiple vias carrying currents in the same way should not be located close to each other [53]. To minimize the separation between via pairs, it is very important to use vias as abruptly as possible to mitigate via inductance.

4.1.5 Mid to Low Frequency:

In PDN, for mid to low frequency, a continuing objection in the DC to kHz frequency range is to evaluate the extremely small impedances of DC-DC converters, or shorted conductor structures that lead to sub-milliohm values. The two main determining aspects of these frequency ranges are the cable-braid ground loop that provides an inaccurate floor in two-port shunt-through networks, and undesirable noise of instrument which is known as instrument noise floor [54].

4.1.6 Package and Board Planes:

A major challenge with design of power/ground planes is their performance as electromagnetic resonant cavities, where dielectric constant of the insulator and the dimensions of the cavity influence the resonance frequency. At resonance frequency, the planes turn into a substantial source of noise in the package and the board [55].

In PDN, the power plane behaves like two-dimensional transmission lines [56] and the impedance is given by [57], where Z_p is power plane impedance in Ω, ε_r is the relative permittivity of the dielectric layer, h is the distance between the planes in mils and p is the plane periphery in mils.

$$Z_p = \frac{532}{\sqrt{\varepsilon_r}} \frac{h}{p} \qquad (31)$$

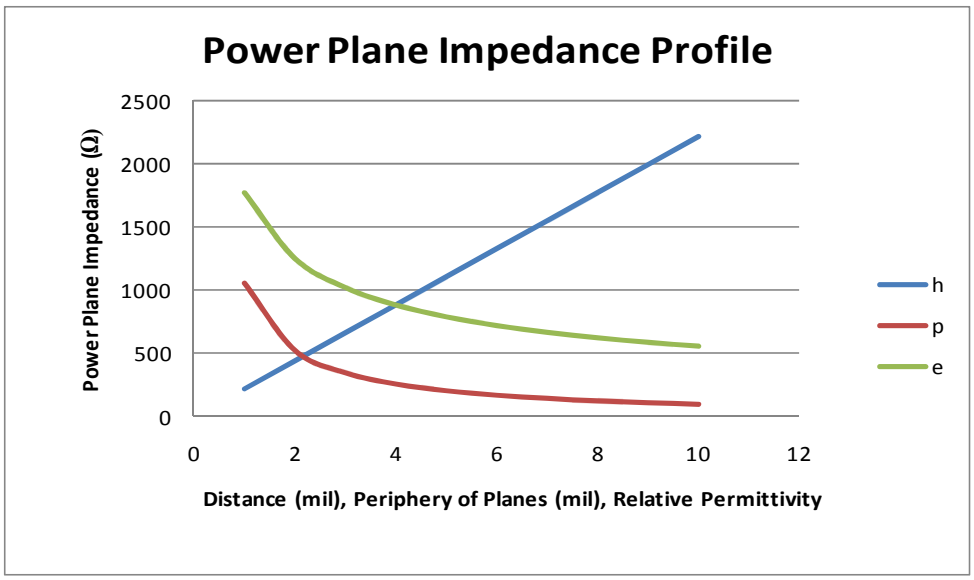


Figure 24: Power Plane Impedance

In **Figure 24**, the power plane impedance is determined according to plate separation (h) when it was 4 mils, the periphery of plane (p) when it was 1.2 mils and the relative permittivity (ε_r) of dielectric between plates when it was 4.

4.1.7 Low Impedance:

Measuring low impedance is another challenge in practical PDN design and due to the options of equipment, and setup it is difficult to measure low impedances [58].

4.2 Signal Integrity Design Challenges:

Signal Integrity (SI) mainly has two concerns regarding the electrical design aspects. One is the timing and another is the quality of the signal. Most of the SI issues are precisely connected to dV/dt or source-drain current transition (dI/dt). Faster rise times negatively affect SI consequences like reflection noise, transmission line effect, impedance mismatch, crosstalk noise, and power/ground switching noise [58]. In the past, when the processor speed

was low, then designers' major concern was routing the signals. At that time, the designers did not require to care about the electrical performance of interconnects. But now with the increase of clock speed, the rise time has also been reduced a lot. So nowadays the designers are more interested on the electrical performance of the interconnects, transmission line and jitter performance. There are several signal integrity challenges in the practical design of high speed semiconductor devices. The key items are summarized, as follows.

4.2.1 Transmission line effects:

When the lengths of a PCB trace or any other cable or conductor carrying signals are long enough that the signals delay back and forward down the trace evolve into longer than signals' rise or fall time, then transmission line effects occurs. These effects rely upon the signal edge rate, not the signal frequency. So, the transmission line effects required to be considered in the design when there is an increasing speed in the system, especially systems that consider fast (edge rate) signals. Fast edge rates produce enormous ringing and overshooting at the load [59].

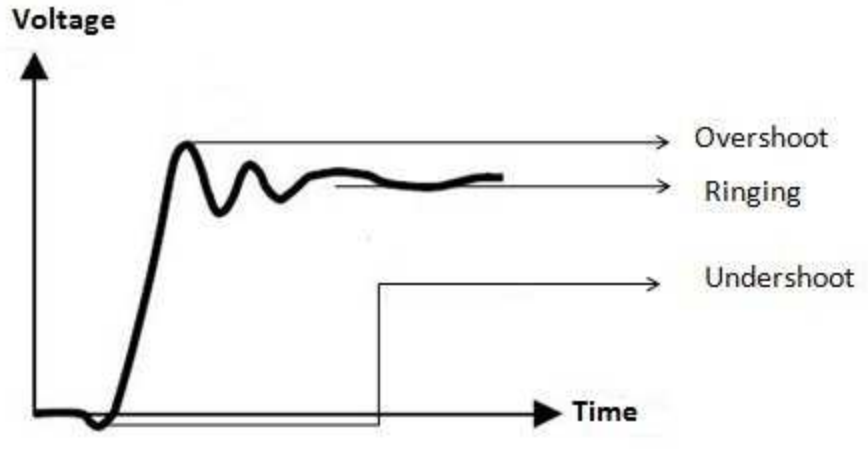


Figure 25: Transmission Line Effects

Temporary ringing occurs when a high-speed signal transition on an interconnection behaves as an improperly terminated transmission line that generates reflections. Ringing is the voltage oscillations above and below the eventual steady-state level. One of the ways to reduce the consequences of ringing is to delay for the reflections to subside before allowing the system to develop new data. By adding one or more clock cycles to each operation, it is possible to reduce the system's clock frequency and get the extra delay.

Overshoot is the measure of the peak amount that how much a pulse voltage swings above its quiescent high voltage and undershoot is the measure of the peak amount by how much a pulse voltage swings below its quiescent low voltage. The undershoot or overshoot can be the reason of damaging the ICs by damaging input protection circuitry. Such as when the enormous voltage continues for more than a negligible amount of time then the IC is overstressed and may latch up (functional chip failure) [60].

4.2.2 Crosstalk:

Whenever a signal is guided along a wire, a magnetic field establishes around the wire. If two wires are located close to each other, then the two magnetic fields connect causing a cross-coupling of energy between signals known as crosstalk. The two energy coupling types are the most important reasons of crosstalk:

1. Mutual Inductance
2. Mutual Capacitance

Mutual Inductance:

Mutual Inductance appears when a current in one path creates a magnetic field. Changes in the magnetic field then induce a current in an adjacent path. Mutual inductance is the purpose of positive waves to appear on the near end of the line which is closest to the transmitter causing near-end inductance. On the other hand, negative waves appear at the far end of the transmission line which is nearer to the receiver, causing far end cross-talk. Leakage from the transmitter end of the Aggressor to interfere with the transmitter end of the line is called near-end crosstalk (NEXT). Interference with the receiver end is called far-end crosstalk (FEXT).

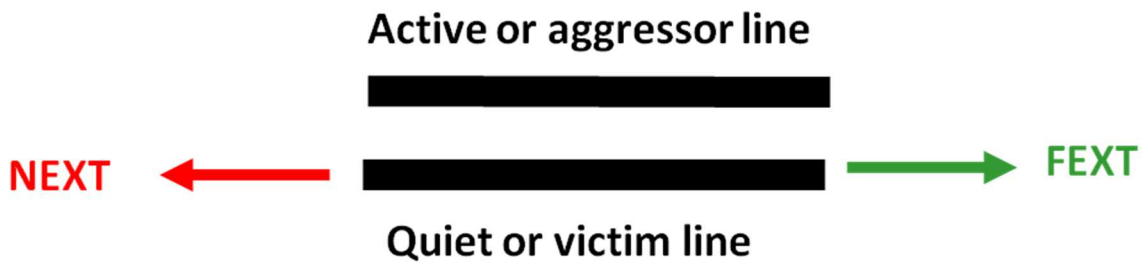


Figure 26: Crosstalk of High Speed Digital Design

The circuit element of mutual inductance can be characterized as follows,

$$V_m = L_m \frac{dI}{dt}$$

Mutual Capacitance:

The coupling of two electric fields when current is introduced in the quiet line proportional to the ratio of change of voltage in the driver,

$$I_m = C_m \frac{dV}{dt}$$

Cross-talk can be remarkably reduced by precise PCB design. Cross-talk can be decreased by designing the transmission line in such a way that the conductor is as adjacent to the ground plane as possible and micro-strip or strip-line layouts by widen spacing between signal lines as much as routing conditions will be granted. Conductor adjacent to the ground plane supports to couple the transmission line of the ground plane and help decouple it from close signals. Differential routing procedures uses especially for complicated PCB traces, and route with short parallel sections also helps to minimize long coupled sections between nets [61].

4.2.3 Impedance Mismatch:

Impedance is defined as the increasing reactance and resistance of a circuit element shows to a circuit. It is generally characterized as the level of obstruction a component presents to an electric current. Connecting a signal source or generator to a load is required for transferring the electromagnetic signal. If the source and load impedances vary from each other, then it is called impedance mismatch. This means the transmitted signal is not completely absorbed within the receiver and the excess energy will be reflected back to the transmitter. That would unavoidably develop in reflections and signal losses. This technique will keep going back and forth until all of the energy is absorbed. A rule of thumb for choosing an interconnect is to restrict the minimum or maximum impedance values to no more than 10% deviation from the system impedance level at the rise time. At high data rates, impedance mismatch has critical effects on the signal, causing overshoot, undershoot, ringing, and stair-step waveforms, all of these issues produce errors in signaling. A designer can

minimize these reflections and assure the proper signal quality by adjusting the impedances of different part of the system.

Along with the return loss, an approach of characterizing the effects of impedance mismatch in the frequency domain is Voltage Standing Wave Ratio (VSWR). VSWR is the ratio between the steady state Voltage measured at either side of an impedance mismatch. Since VSWR and Return Loss are both impedance related, they are precisely proportional. VSWR can give fast insight into the amount of power that is reflected back into a transmitter from an interconnect. Return loss provides comparable insight into the conditional level of a signal that is transmitted through the same interconnect. To solve the impedance mismatch issue, the transceiver buffers can be matched to the transmission media. In the case of a PCB, this can be accomplished by accurate selection of medium and by the use of the appropriate termination strategy [61, 62].

CHAPTER 5

MODELING AND MEASUREMENTS OF PDN

Three PCB boards have been made for testing. First and second PCB were made for Z-probe probing. Because of unpredictable calibration parameters, the measurements were done with inaccurate results, so the last one was made using SMA connector (**Figure 27**).

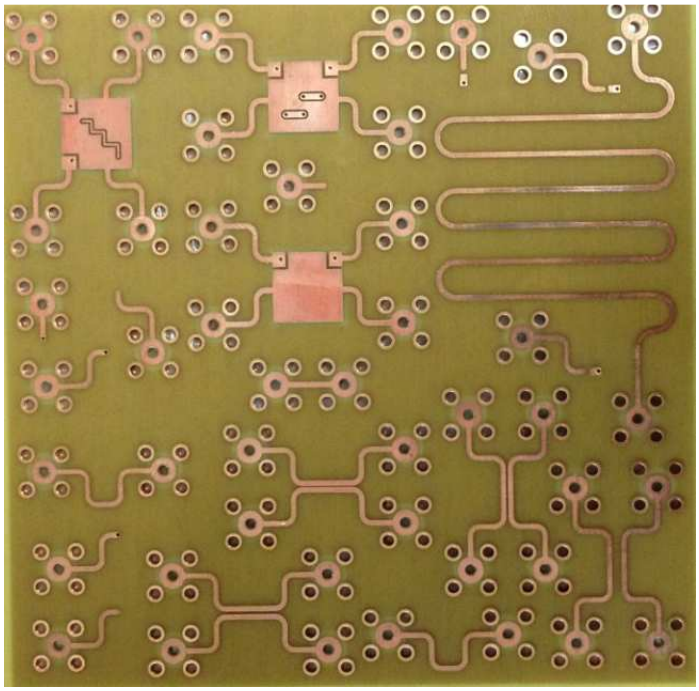


Figure 27: Third PCB design with SMA connector

5.1 Modeling and Measurement of PDN:

The PDN of a system is formed by a combination of multiple level networks forming a hierarchical interconnection structure. PCB level PDN has been observed for the research. The first PDN does not have any traces, including only vias. Via inductance is about 75%~80% of the total loop inductance. As the Power-Ground pair space and location changed, the via inductance of capacitor may vary. The second PDN has very simple traces

and the third PDN has little bit complex traces than the second PDN. S parameters and mixed mode S parameters of three different PDN model was measured [63] to observe how the parameters differ from each other.

5.1.1 PNA Network Analyzer N5225A:

For the PDN measurements, PNA N5225A network analyzer from Agilent or Keysight has been used for this research. The PNA has four ports with two internal signal sources from 10MHz to 50GHz and integrated true-mode stimulus application (iTMSA). The iTMSA provides true differential and true common stimulus and enables balanced measurements under real operating conditions. The iTMSA also has the proficiency to do forward-only sweep, reverse-only sweep, and frequency or power sweep with arbitrary phase for balanced measurements. According to Agilent N5224A and N5225A PNA Microwave Network Analyzers Service Guide, all the measurement includes unpredictable errors (e.g. Directivity, Source match, Load match, Reflection and transmission frequency tracking, Isolation (crosstalk), Noise, Drift, Connector repeatability, and Test cable stability).

5.1.2 Probes, connectors, and calibration substrates:

For this research, GS-500 Z-Probe has been used for one port measurement, and SG-500 Z-Probe has been used for two port measurement. Those probes were used for PCB, IC pins and ceramic substrate probing.

The connector for those Z-probes is 2.4mm to 2.92 mm. The 2.4 mm is to connect to cable, and 2.92 mm is for probe.

The calibration substrate used is called CSR-5, and is made especially for Z-probes. The CSR-5 has following characteristics.

Table 4. Calibration Substrate CSR-5 Characteristic [63]

Material	Alumina
Size	16 x 13.7mm
Thickness	635um
Dielectric Constant	ε = 10.2
Effective Permittivity	5.73
Effective Velocity	0.43
Phase Velocity	7.36 ps/m
THRU Impedance	nominally 50 Ω
DC accuracy (LOAD)	50 Ω +/- 0.15 Ω
Temperature	between –263°C and +150°C
Maximum Power	0.3W

5.1.3 Measurement Procedures and Equipment:

Prior of doing any measurement, pure alcohol was used to clean up the entire connectors and adaptors. After cleaning, it requires to apply gage kit calibration to test all the connectors and adaptors to have the correct contact. One is 2.92 mm/3.5 mm manual gage kit and the other one is 1.85 mm/ 2.4 mm digital gage kit. The gage kits need to be calibrated with standard connector and to apply 4 lb. wrench and set to zero. Next it needs to apply gage kit to adaptors and connectors. To make the correct contact, it is necessary to turn the screw in one end and hold it tight in other end. This can avoid the connections get grind each other and

damage the center pin. After gage kit connects to adaptors or connectors, it is expected to use the correct wrench with certain force. If the value is negative in gauge kits, then the connection is good. But if the values turn to positive, the adaptors or connectors would have been damaged. After that it requires to place Z-probe to the station, and connect with 2.4mm/2.92mm adaptor, and connect 2.4 mm cable to PNA and adaptor [63].

CHAPTER 6

ANALYSIS OF THREE DIMENTIONAL (3D) PDN

6.1 Simulation with ANSYS HFSS

Ansys HFSS is a High Frequency Structure Simulator. It is a full wave electromagnetic field simulator for 3D volumetric modeling of passive devices and uses finite element method to solve Maxwell's Equations. Structure is subdivided into finite elements and electromagnetic fields are found within each element. The subdivided structure is called mesh and tetrahedron mesh elements are typically used to discretize the model to conform to arbitrary geometry. In practice, to calculate the fields and S-matrix associated with a structure with ports, HFSS derives the electric and magnetic field equations in matrix form for each element. These matrices then combine to form a global matrix and the field solution is obtained by using an iterative process. HFSS employs an adaptive meshing algorithm which continually searches for the largest gradients in the E-field or error and subdivides the mesh to provide most refined and efficient mesh which is essential to obtain accurate and mesh independent solutions. Ansys HFSS FEM flow chart is illustrated in **Figure 28.**

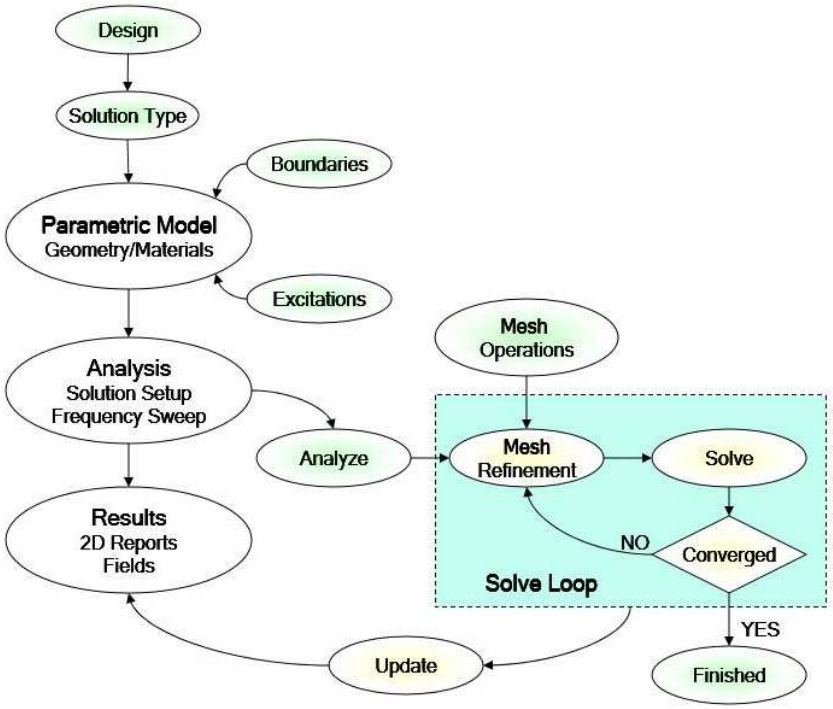


Figure 28: ANSYS HFSS FEM Flowchart

The general processes for an adaptive meshing are as follows:

1. HFSS generates an initial, geometrically conformal, mesh.

2. Using the initial mesh, HFSS calculates the electromagnetic fields that exist inside the structure when it is excited at the solution frequency and an adaptive solution is executed only at the specified solution frequency.

3. Based on the current finite element solution, HFSS determines the regions of the problem domain where the exact solution has a high degree of error. Tetrahedron elements are refined by creating a number of smaller tetrahedron elements that replace the original larger elements.

4. HFSS generates another solution using the refined mesh.

5. HFSS uses iterative process (solve => error analysis => refine) and repeats until the convergence criteria are satisfied or the requested number of adaptive passes is completed.

6. If a frequency sweep is being performed, HFSS then solves the problem at the other frequency points without further refining the mesh.

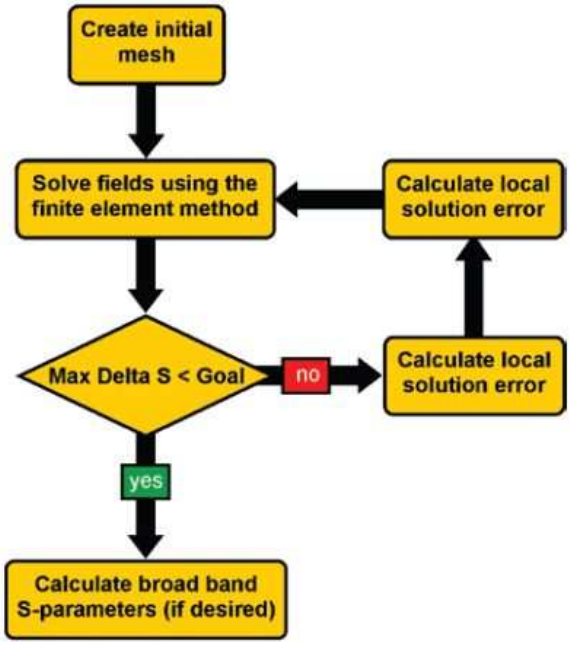


Figure 29: HFSS's Accuracy Chart [64]

6.1.1 *Simulation Procedures:*

This section illustrates the simulation techniques that had been used with ANSYS HFSS. Six steps have been followed for the proper HFSS simulation. The steps include the following,

1. Create model/geometry

2. Assign boundaries
3. Assign excitations
4. Set up the solution
5. Solve
6. Post-process the results

The PDN models have been created within HFSS using the 3D modeler. 3D modeler creates structures that are variable with regard to geometric dimensions and material properties. To create the structures, 'Driven Terminal' has been used as it solves S matrix based on voltages and currents. 'Mils' was selected as the unit of the models. The copper ground plane dimensions were 400 mil × 400 mil × 1.4 mil and connected to a small square-shaped pad on the top layer. Between the ground and the top layer, 18 mils FR4 epoxy dielectric has been used. The ports of the models are selected in such a way that their size agrees with the actual size of the Z-Probe used in PNA which is 40 μm of widths.

The boundary was set to be radiation for all of the size of the air box except for the bottom side since the Device Under Test (DUT) is placed on a metal (Perfect E) surface in the clean room.

After assigning the boundaries, the excitations (or port) have been applied. In this case, lumped ports have been applied for the simulations. The excitation is applied at a point/cell as a voltage or current in the lumped port. The proper uses of the excitations help to get the most accurate HFSS results.

At first, the frequency type has been chosen to be linear and interpolating sweep for the solution setup. The interpolating sweep utilizes rational polynomial fit to the S Parameters versus frequency. This kind of sweep does not have bandwidth limitations and well improved for DC extrapolation. Frequency ranges of the models were set to be 0 to 5 GHz.

6.1.2 Simulations of Z parameters:

In this section, three power distribution network models have been discussed. The S parameters and Z parameters of these three models and the comparison of simulated and measured data of Z parameters and differential S parameters also been discussed.

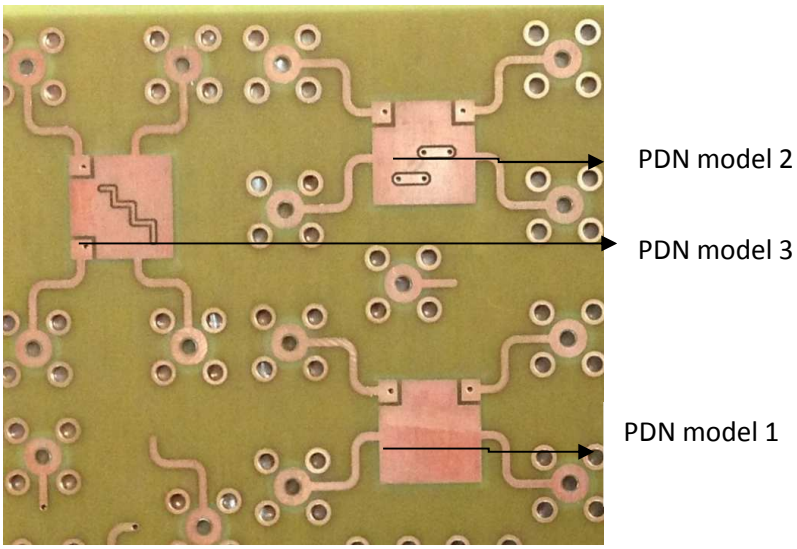


Figure 30: PCB with three simplified power distribution network (PDN) models

6.1.2.1 Power Distribution Model (PDN) with no traces:

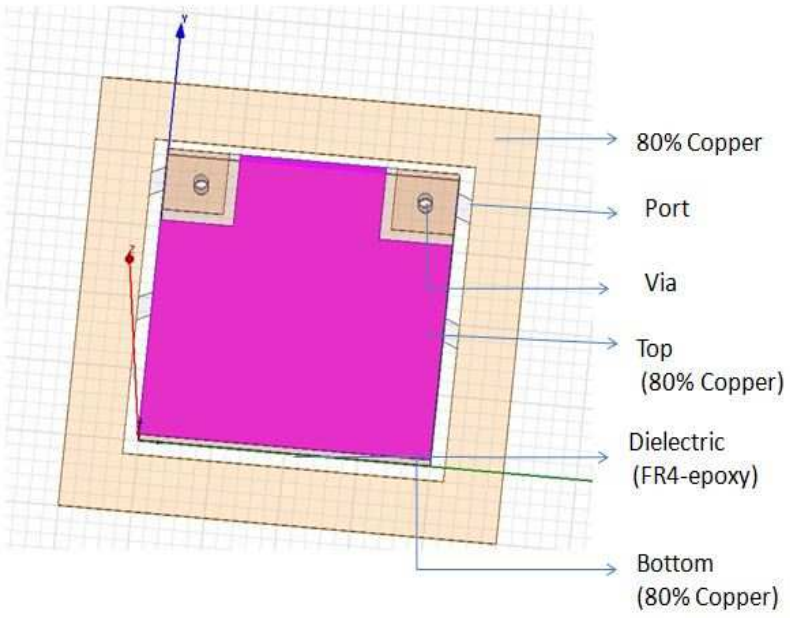


Figure 31: PDN with no traces

PDN with no traces, as shown in **Figure 31**, was simulated in Ansys HFSS to obtain single ended S parameters. Simulated S parameter results were compared with the measured S parameter results for validation. The comparisons between the simulated and measured S parameters demonstrated excellent agreement up to 1.5 GHz and have been showed in the Appendix A.

S parameters were used to analyze the board and provide design guideline and corrections since they can be measured at high frequencies. Generating Z-parameters at high frequencies can be difficult due to not achieving strict termination conditions such as open and short. Simulation of S parameters and then converting to Z parameters helped in quick analysis and determined if the three of the models were correct.

The Z parameters are properties to describe behavior of a linear electrical network such as PDN. So, the Z parameters simulation in Ansys HFSS is a useful tool to test frequency response of models like capacitor. $Z_{11} = Z_{33}$, and $Z_{22} = Z_{44}$ due to the symmetric design of the PCB with no traces.

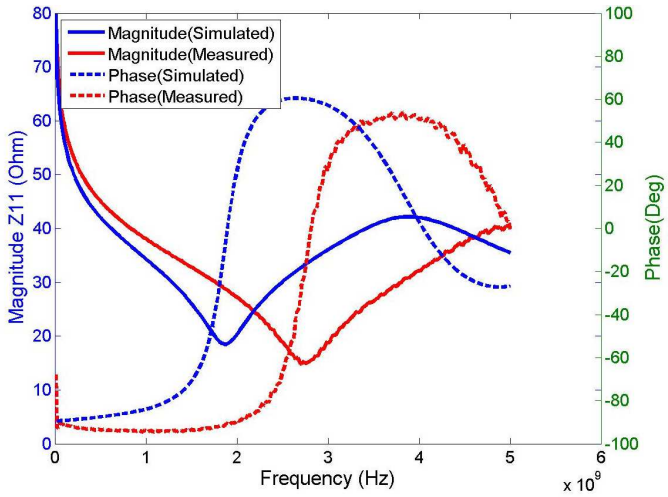


Figure 32: Comparison (Sim Vs Mea) of Z11

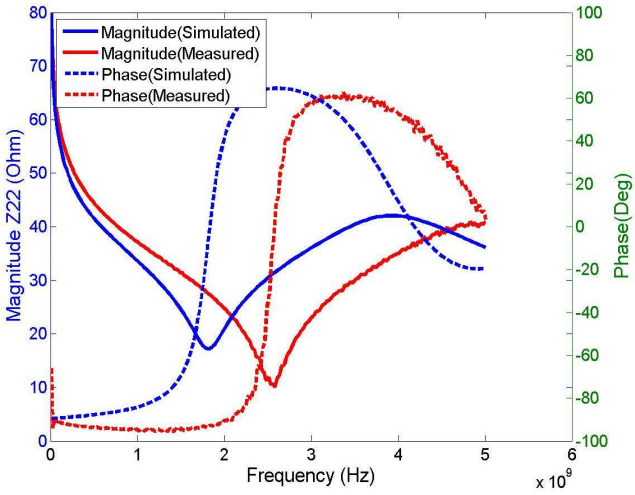


Figure 33: Comparison (Sim Vs Mea) of Z22

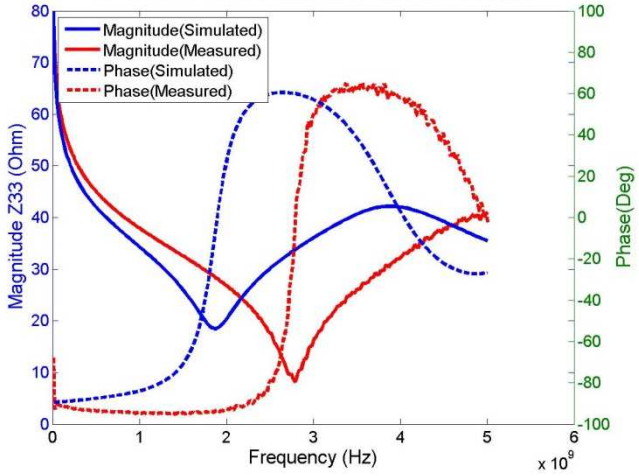


Figure 34: Comparison (Sim Vs Mea) of Z33

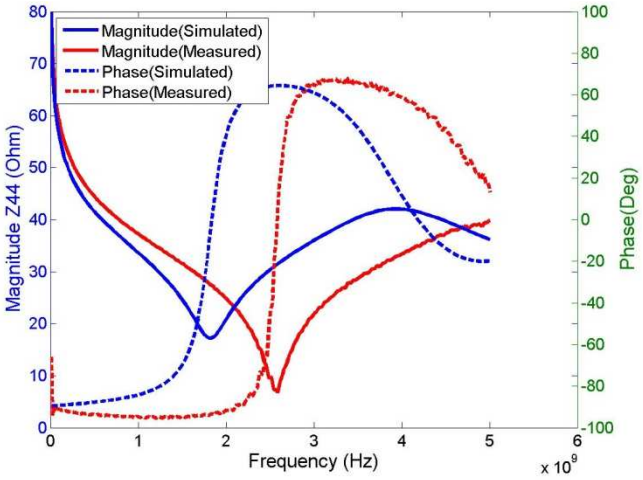
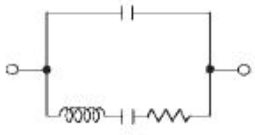


Figure 35: Comparison (Sim Vs Mea) of Z44

The comparison of Z parameters between simulation and measurement is shown in **Figure 32, Figure 33, Figure 34**, and **Figure 35**. The simulated frequency response curve partially fits with the measurement results. But both of the graphs are showing same characteristics. The characteristics of the Z parameter curves of the above figures suggested that the circuit mode looks like,  and fits for resonator (ceramic) type

DUT. In these figures, 1.9 GHz is the self resonant frequency (SRF) and 3.8 GHz is the anti resonant frequency. From 0-1.9 GHz, the graphs are behaving like capacitor. From 1.9 GHz to 3.8 GHz, the graphs are showing characteristics of inductance. After 3.8 GHz, the graph again started to behave like a capacitor.

On the other hand, due to the symmetrical design, $Z_{13} = Z_{31}$ and $Z_{24}=Z_{42}$.

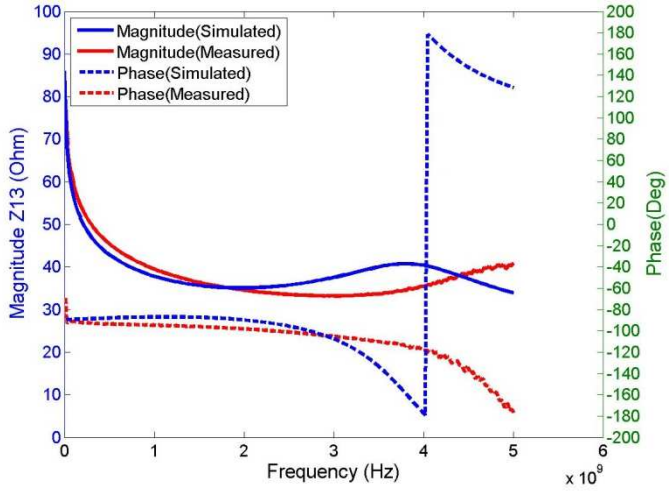


Figure 36: Comparison (Sim Vs Mea) of Z13

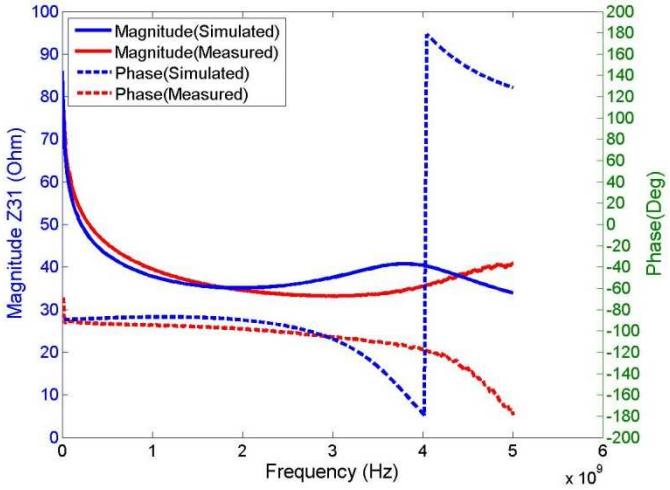


Figure 37: Comparison (Sim Vs Mea) of Z31

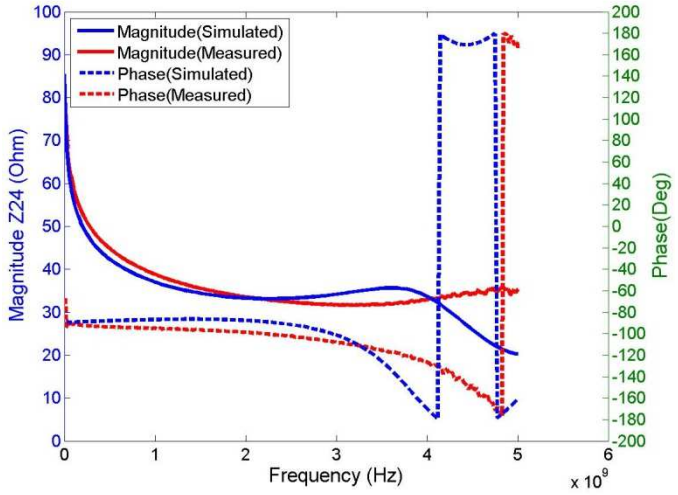


Figure 38: Comparison (Sim Vs Mea) of Z24

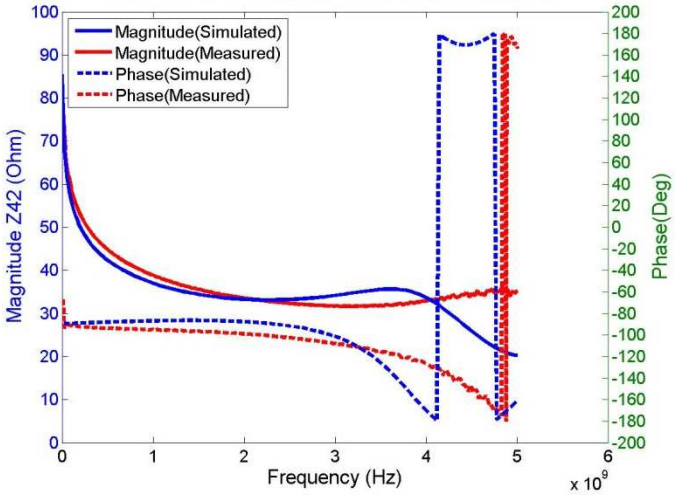


Figure 39: Comparison (Sim Vs Mea) of Z42

In **Figure 36, Figure 37, Figure 38**, and **Figure 39**, impedance characteristics are reflecting that there is high core loss in the system. At 4 GHz, one can observe that graphs are showing undershoot and overshoot of the phase response (turquoise curve) and the phase is from -180 degree to 180 degree, which is indicating that the inductor and capacitor is out of phase. So the model is good up to 3 GHz.

6.1.1.2 Power Distribution Model (PDN) with vias:

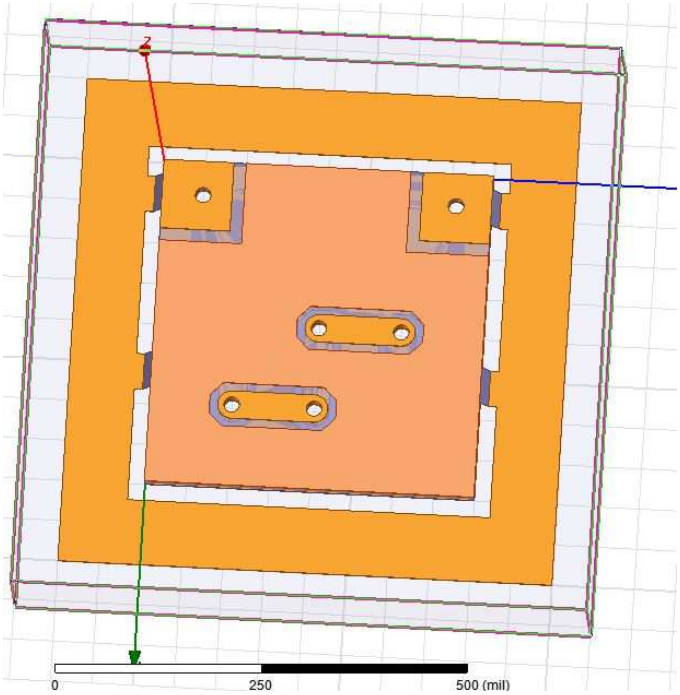


Figure 40: PDN with vias

The Z parameters of PDN with vias were simulated to compare with the measurement data. In this model, due to symmetric design, $Z_{11} = Z_{22}$, and $Z_{33} = Z_{44}$.

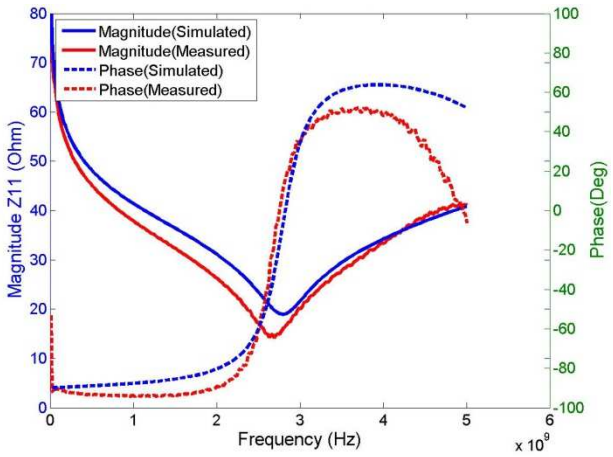


Figure 41: Comparison (Sim Vs Mea) of Z11

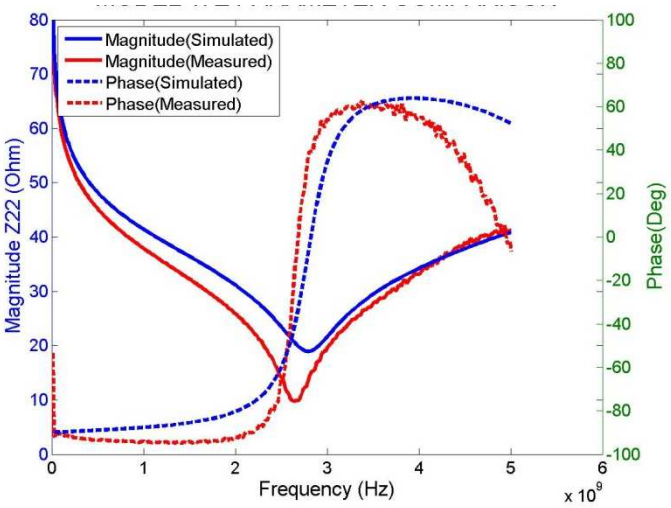


Figure 42: Comparison (Sim Vs Mea) of Z22

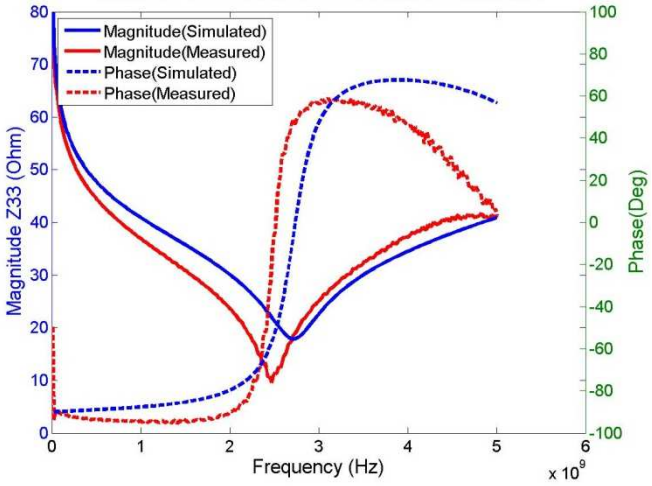


Figure 43: Comparison (Sim Vs Mea) of Z33

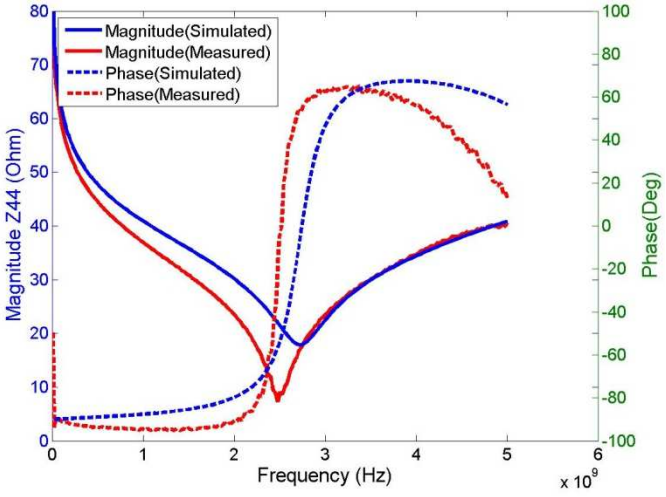


Figure 44: Comparison (Sim Vs Mea) of Z44

In **Figure 41, Figure 42, Figure 43**, and **Figure 44,** the simulated and measurement results are very close to each other. But measured data was shifted left than the simulated data and the Z parameters are behaving as resonators. Ideally, inductors and capacitors have +/-90 degree phase differences between voltage and current. But, neither the simulation, nor the measurement is in ideal situation. So, the phase differences are not exactly +/- 90 degree. Also, these phase characteristics are indicating that there is substrate imperfection and dielectric loss in the board. But due to the uses of vias, the model's curve is showing better correlation than the first model (PDN with no traces).

Again, due to symmetrical design in this model, $Z_{12} = Z_{21}$ and $Z_{34} = Z_{43}$.

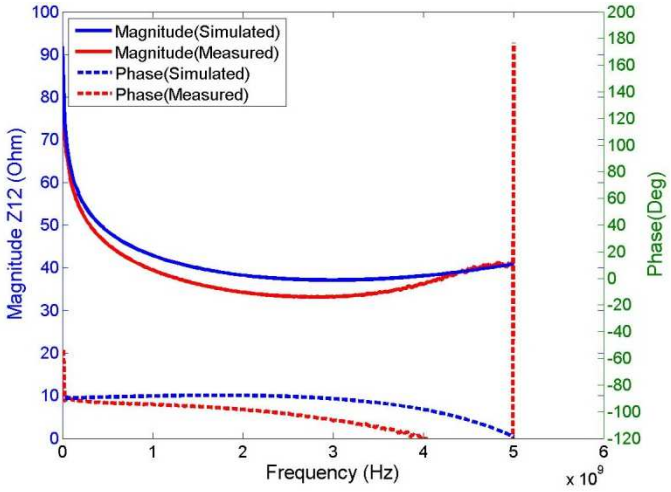


Figure 45: Comparison (Sim Vs Mea) of Z12

In **Figure 45, Figure 46, Figure 47,** and **Figure 48,** simulation and measurement results are very close to each other. In these curves, the impedance with a low frequency decreases inversely with frequency, similar to the ideal capacitor. ESR (loss due to dielectric substances, electrodes or other components) shows a value equivalent to dielectric loss from delay of polarization in the dielectric substance.

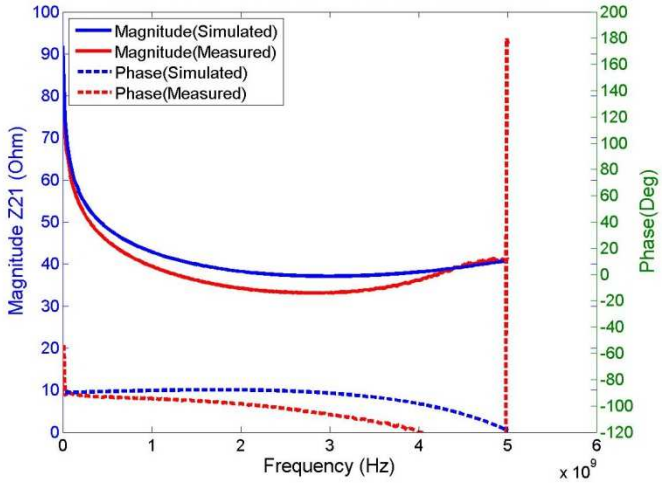


Figure 46: Comparison (Sim Vs Mea) of Z21

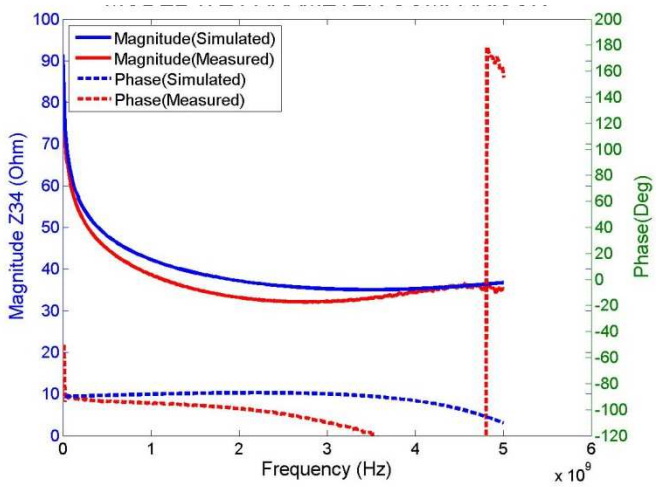


Figure 47: Comparison (Sim Vs Mea) of Z34

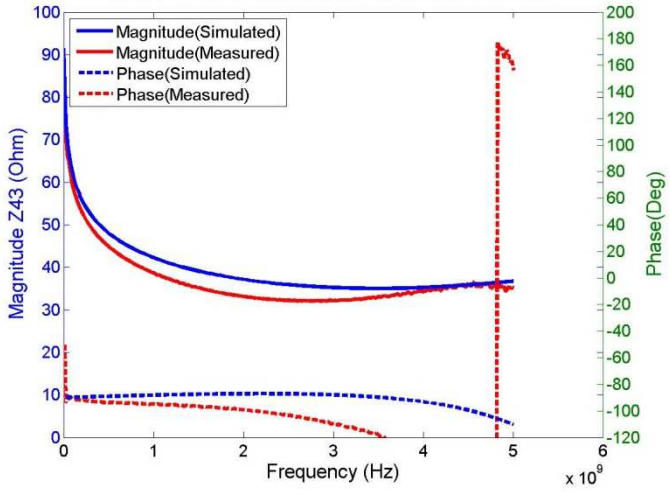


Figure 48: Comparison (Sim Vs Mea) of Z43

6.1.1.3 Power Distribution Model (PDN) with traces:

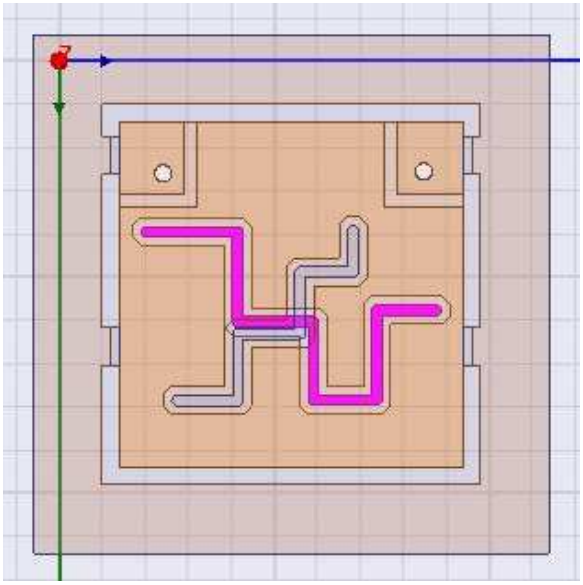


Figure 49: PDN with traces

The port assignments for model 2(PDN with vias) and model 3 (PDN with traces) are exacltly the same. So, the Z parameters of PDN with traces has, $Z_{11} = Z_{22}$, and $Z_{33} = Z_{44}$.

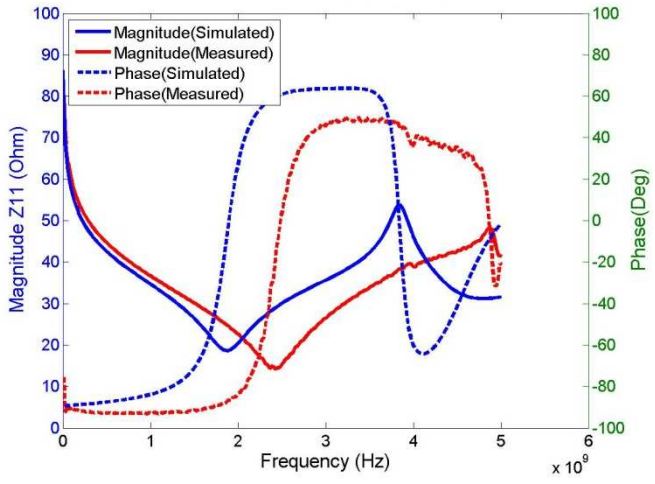


Figure 50: Comparison (Sim Vs Mea) of Z11

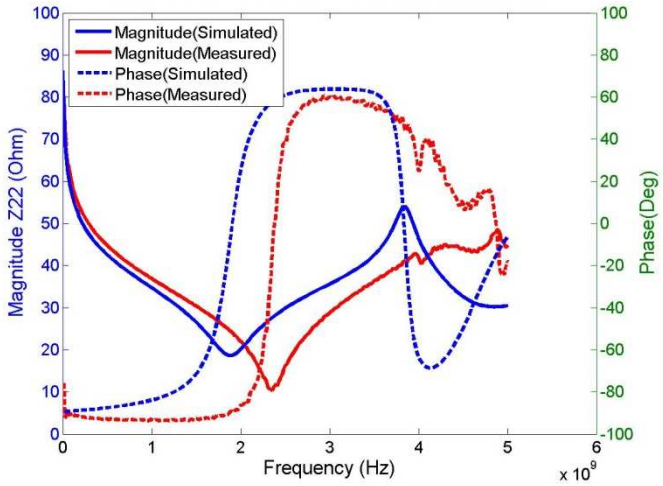


Figure 51: Comparison (Sim Vs Mea) of Z22

In **Figure 50, Figure 51** the self resonant frequency is at 1.9 GHz and the anti resonant frequency is at 3.9 GHz. Before 1.9 GHz the graph is behaving as capacitor, from 1.9 GHz to 3.9 GHz the graph is behaving as inductor and after 3.9 GHz again it is showing capacitive characteristics. The Z curves of measured result and the simulated results are behaving like a series parallel resonators.

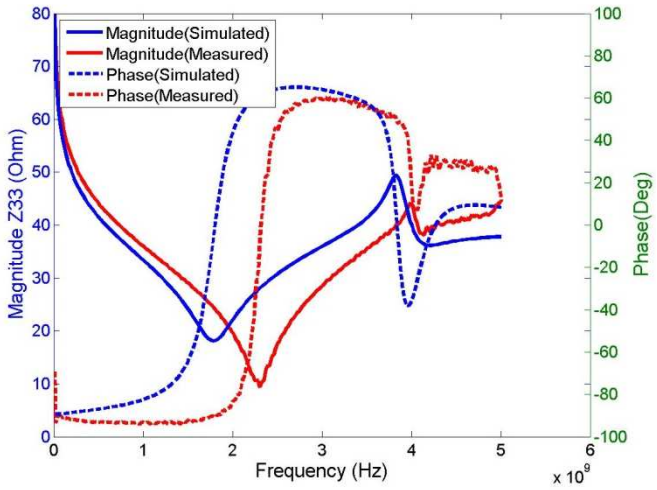


Figure 52: Comparison (Sim Vs Mea) of Z33

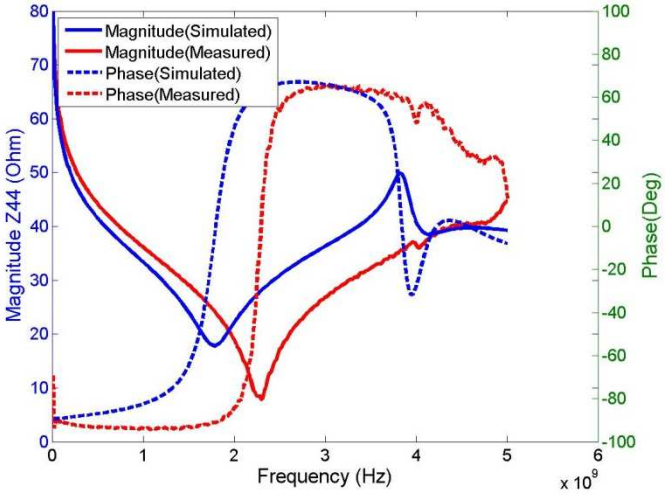


Figure 53: Comparison (Sim Vs Mea) of Z44

Figure 52, and **Figure 53,** the simulated and measurement results did not correlate to each other. But the Z curves of measured result and the simulated result are behaving as resonators. Before, 1.9 GHz the graph is behaving as capacitor, from 1.9 GHz to 3.9 GHz the graph is behaving as inductor, and after 3.9 GHz again it is showing capacitive characteristics.

On the other hand, in this model, due to symmetrical design, $Z_{12} = Z_{21}$ and $Z_{34}=Z_{43}$.

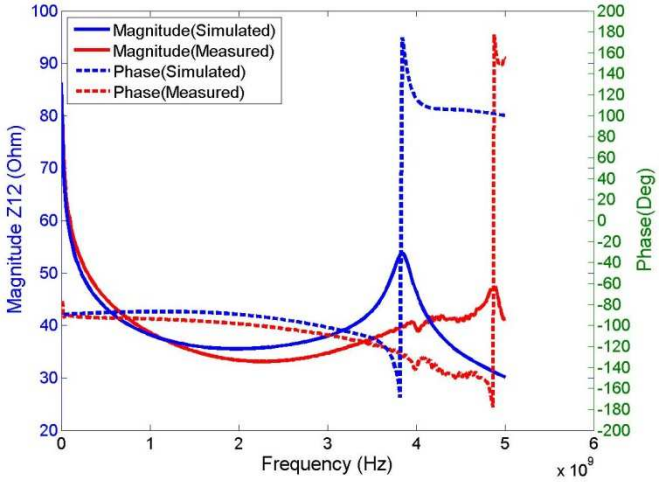


Figure 54: Comparison (Sim Vs Mea) of Z12

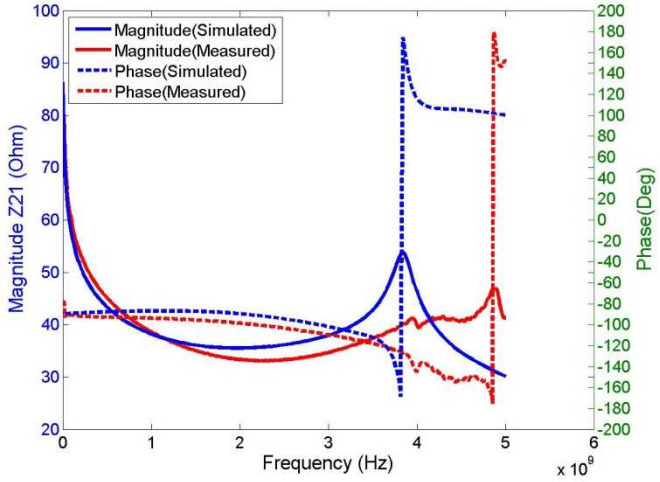


Figure 55: Comparison (Sim Vs Mea) of Z21

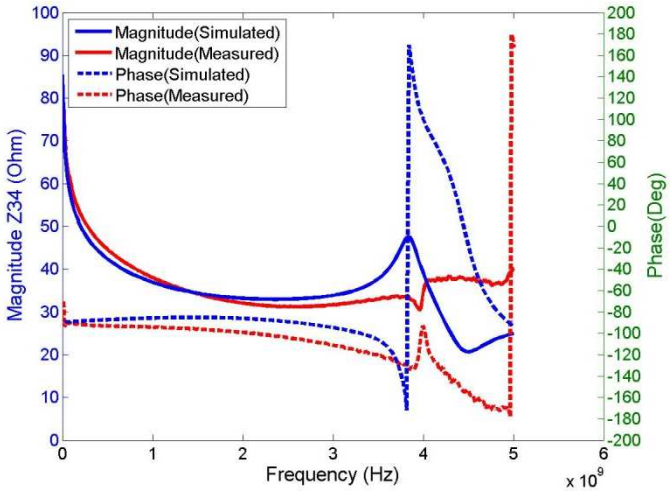


Figure 56: Comparison (Sim Vs Mea) of Z34

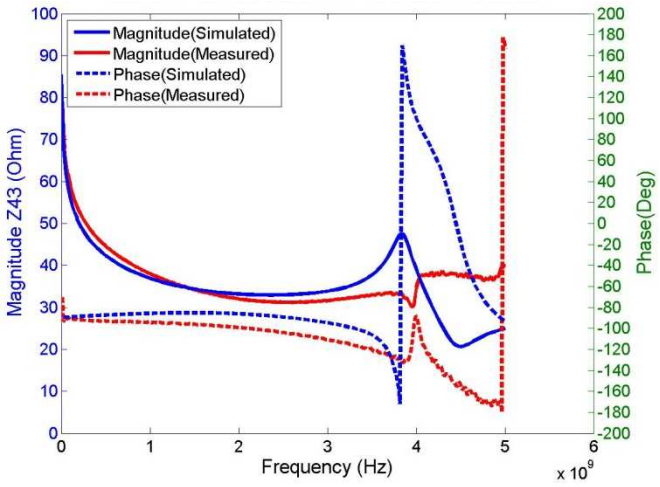


Figure 57: Comparison (Sim Vs Mea) of Z43

In **Figure 54**, **Figure 55**, **Figure 56**, and **Figure 57**, the curves at lower frequency are behaving like a capacitor. As the frequency increases above series resonance point, the curves behave like an inductor until the frequency reaches its parallel resonant frequency. Therefore, the above curves suggest that they are combinations of series and parallel tuned resonance circuits. Parallel resonant frequency or the anti-resonance frequencies peaks are not limited to

parallel-connected discrete capacitors: it occurs when at a particular frequency some of the parallel-connected impedances are inductive and some are capacitive.

The simulation and measurement curves of the three models looked agreeable to each other. The measurement and simulation curves are not exactly the same due to the imperfect simulations. Dielectric and conductivity of the boards are frequency dependent, but in simulation one frequency has been used for the simplicity. In the second model (PDN with vias), due to the uses of vias, the curves show better correlation with the measurement data than the first model (PDN) with no traces and third model (PDN) with traces. In the second model, due to uses of four extra vias, there is high impedance which transformed into a short circuit (or very low impedance) to provide an effective low-resistance path for current flow across the joint. Moreover, the short circuit terminated parallel open ended electromagnetic waves, so the simulation results of second model (PDN with vias) is better than the first model (PDN with no traces) and the third model (PDN with traces).

6.1.3 Simulations of differential S Parameters:

Differential S parameters were determined in this research since they are usually used for effective reduction of EMI and to improve the signal quality. The measured differential S parameter results were compared with the simulation results. However, in Ansys HFSS 13, it is not possible to obtain differential S parameters directly from the simulation models. Therefore, simulated differential S parameters have been calculated by transforming the simulated S parameters as described by Fan et al. **[65]**.

6.1.3.1 Power Distribution Model (PDN) with no traces:

For the first model of PDN, $S_{DD11} = S_{DD22}$ and $S_{DD12} = S_{DD21}$.

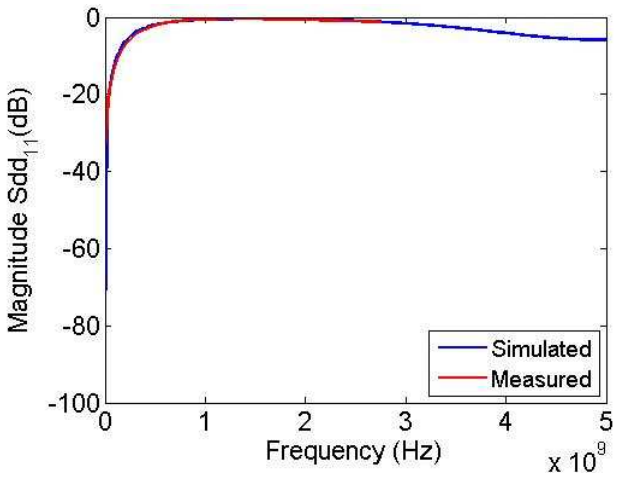


Figure 58: Comparison (Sim Vs Mea) of Differential S parameter, SDD11

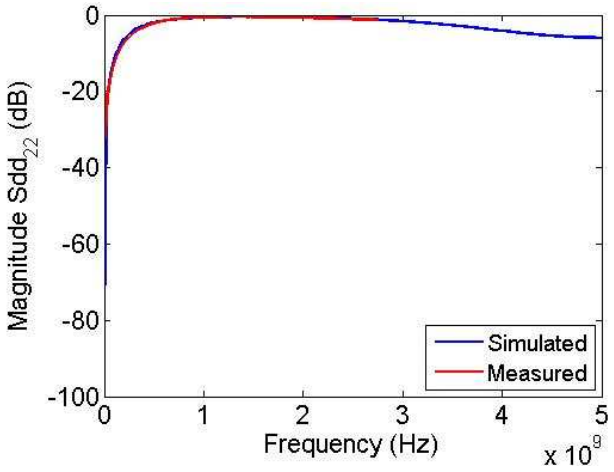


Figure 59: Comparison (Sim Vs Mea) of Differential S parameter, SDD22

In **Figure 58**, and **Figure 59,** the differential return loss SDD11 and SDD22 of measurement results and simulation results are identical to each other as expected.

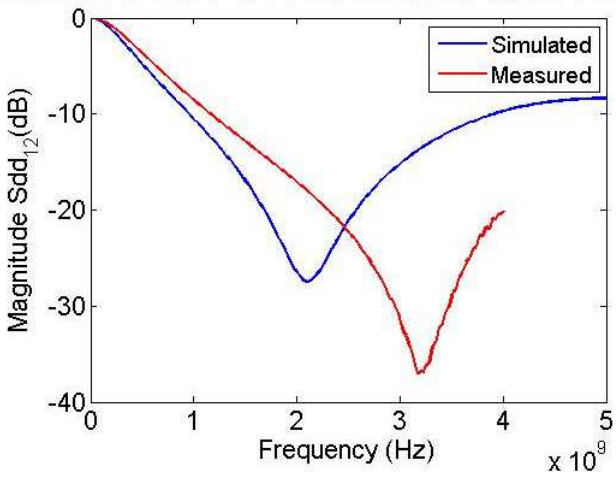


Figure 60: Comparison (Sim Vs Mea) of Differential S parameter, SDD12

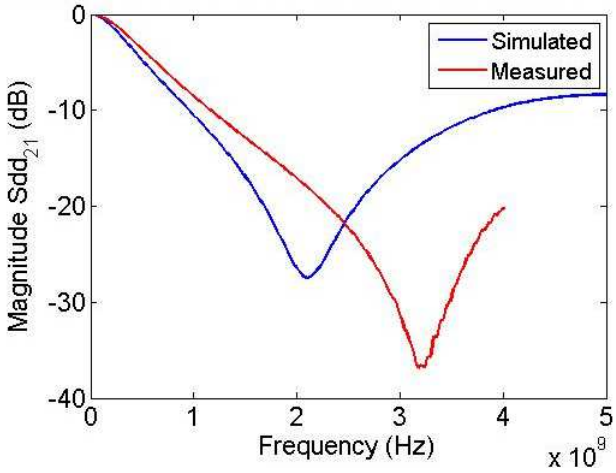


Figure 61: Comparison (Sim Vs Mea) of Differential S parameter, SDD21

In **Figure 60,** and **Figure 61,** the differential transmission loss, SDD12 and SDD21 were not identical. There were not any components on the PCB model. Therefore, only passive components such as parasitic capacitance were measured in this case. Moreover, there is loss and error for connectors and SMA, which makes the simulation and measurement curves different from each other. The resonant frequency of the simulation is 37.5 % within the measurement and the magnitude of the simulation is 23.69%.

CHAPTER 7

CONCLUSIONS

The increasing physical complexities of the system (i.e., various supply rails, continuously increasing currents, diminishing supply voltages, discontinuous return paths, impedance mismatch and higher chip leakage) make the semiconductor devices design even more complicated due to signal integrity and power integrity issues. To overcome these issues not only the semiconductor fabrications are important but also the packaging of semiconductor devices. Package substrates require considerable development and improvement for packaging the high speed devices. Heat generation is also a big issue in advanced high performance ICs, especially in die attaches procedure. Solders with low young's modulus can reduce the stress in the die due to thermal coefficient expansion (CTE) mismatch. Flip chip packaging with BGA is essentially excellent form of packaging in regard to electrical perspective for power and ground connections with high signal count package.

Due to the modern CMOS technology scaling, the transistors require faster rise time. But, faster rise times causes negative SI effects (i.e. reflection noise, transmission line effect, impedance mismatch, crosstalk noise and power/ground switching noise). To decrease these effects, selecting termination values and controlling characteristic impedance is important. Moreover constraining routing and board stack up can lessen signal integrity. On the contrary, the PDN must be carefully designed to decrease the PI issues. Maintaining a constant voltage and low impedance over a wide frequency is a major challenge in PDN design. Simulations of large PDN system with complex designs and additional features can be challenging to the PDN designers. To overcome such modeling and simulation challenges, designers need more advanced tools which can handle complicated PDN design.

In addition to discussing the signal integrity and power integrity challenges, modeling of three different PDN designs using FEM were discussed in this document. The S parameters, Z parameters and differential S parameters of PDN designs were measured using PNA N5225A network analyzer and compared with the simulations conducted using Ansys HFSS. Most of the simulations and measurements curves of the three models looked very agreeable to each other up to 1.5 GHz. Some deviations were observed between the measurement and simulation results possibly due to some error from not only the device but also the machine, cable, connector, probe and calibration error. Since the simulation was validated with the measurement data up to 1.5 GHz, so these models can further be used with added complex features such as VRM, decoupling capacitors, among other factors and can predict more complex signal and power integrity characteristics.

REFERENCES

[1] R. Y. Chen, "Signal Integrity," Sigrity Inc., Santa Clara, California.

[2] "Power Integrity Simulation for High Speed Board using CST PCBs," Computer Simulation Technology, 2015. [Online]. Available: http:/www.cst.com.

[3] P. Carrier, "Signal Integrity and Power Integrity in High-speed Design," *EDN Network,* 26 August 2014.

[4] "Computer History Timeline," [Online]. Available: http://www.computerhistory.org/semiconductor/timeline.html. [Accessed 3 February 2015].

[5] "The Theory of p-n Junctions and p-n Junction Transistors," [Online]. Available: http://bit.ly/17yWtPE. [Accessed 3 February 2015].

[6] "Semiconductor Device and Lead Architecture," [Online]. Available: http://bit.ly/178vY00;. [Accessed 3 February 2015].

[7] G. E. Moore, "Cramming More Components onto Integrated Circuits," *Electronics,* vol. 38, no. 8, April 1965.

[8] "Intel Corporation Inc.," [Online]. Available: http://www.intel.com/content/www/us/en/history/museum-gordon-moore-law.html.

[9] A. Elshabini, F. Barlow, S. Islam and P. Wang, "Advanced Devices and Electronic Packaging for Harsh Environment," in *46th IMAPS International Conference & Exhibition of Symposium on Microelectronics*, Orlando, Florida, 2013.

[10] Z. Z. Oo, Writer, *Efficient Modeling of Power and Signal Integrity for semiconductors and Advanced Electronic Package Systems.* [Performance]. Phd Thesis, National University of Singapore, 2008.

[11] L. Chi-Un, "VLSI Macromodeling and Signal Integrity Analysis via Digital Signal Processing Techniques," University of Hong Kong, 2011.

[12] S. Peddada, "Signal Integrity Analysis of Transmission Lines in Anisotropic Substrates for High-Speed Data Transmission," Dissertation of Masters of Science, Auburn University, August 2013.

[13] I. Novak, "A New Dawn in R&D," *IEEE Microwave Magazine,* vol. 12, no. 5, pp. 51-60, 2011.

[14] J. R. Black, "Electromigration Failure Modes in Aluminum Metallization for Semiconductor Devices," *Proceedings of the IEEE,* vol. 57, no. 9, pp. 1587-1594, Sept 1969.

[15] L. Smith, R. Anderson, T. Pelc and T. Roy, "Power Distribution System Design Methodology and Capacitor Selection for Modern CMOS Technology," *IEEE Transaction on Advanced Packaging,* vol. 22, no. 3, pp. 284-291, August 1999.

[16] S. WAGNER, "Small-Signal Device and Circuit Simulation," Small-Signal Device and Circuit Simulation, April 2005. [Online]. Available: http://www.iue.tuwien.ac.at/phd/wagner/node20.html. [Accessed 4 February 2015].

[17] "Differential and Balanced S parameters," [Online]. Available: http://www.keysight.com/owc_discussions/servlet/JiveServlet/download/72-15557-48373-2432/BalancedS. [Accessed 6 February 2015].

[18] "S parameters techniques for faster, more accurate network design," Hewlett Packard, California, 1967.

[19] H. H. Utsunomiya, "Challenge on Packaging Substrate Technologies Towards Next Decade," in *IEEE 3rd International Microsystems, Packaging, Assembly & Circuit Technology*, Taipei, 2008.

[20] M. A. Bolanos, "Semiconductor IC Packaging Technology Challenges: The Next Five Years," Texas Instruments, May 2006.

[21] J. S. Peiffer, "Using Embedded Capacitance to Improve Electrical Performance, Eliminate Capacitors and Reduce Board Size in High Speed Digital and RF Applications," 3M Company, St. Paul, MN, 2006.

[22] E. D. Blackshear, M. C. E. Klink, S. R. Engle, R. S. Malfatt, D. N. d. Araujo, S. Oggioni, L. D. LaCroix, J. A. Wakil, G. G. Hougham, N. H. Pham and D. J. Russell, "The Evolution of Build-up Package Technology and its Design Challenges," *International Business Machines Corporation (IBM),* vol. 49, no. 4/5, pp. 641-661, July/September 2005.

[23] D. Zwitter, N. Nal, M. Arseneault, K. Yonehara, H. Hu, M. Bailey and T. Cannon, "Competitiveness and Technical Challenges of Low Cost Wirebond Packaging for High Speed SerDes Applications in ASICs," in *IEEE Electronic Components and Technology Conference*, Reno, NV, 2007.

[24] N. Na, J. Audee and D. Zwitter, "Discontinuity Impacts and Design Considerations of High Speed Differential Signals in FC-PBGA Packages with High Wiring Density," in *IEEE Electrical Performance of Electronic Packaging*, Oct 2005.

[25] M. Thomas, "Die Attach Material Processes," Solid State Technology, [Online]. Available: http://electroiq.com/blog/2007/04/die-attach-materials-and-processes/. [Accessed 10 February

2015].

[26] A. Dhakal, "Transient Liquid Phase Bonding for Die Attach," University of Idaho, Moscow, Idaho, 2012.

[27] E. Bogatin, "Roadmaps pf Packaging Technology," Integrated Circuit Engineering Corporation , 1997.

[28] R. Lyn and W. Crockett, "Assembly Using X-Wire™ Insulated Bonding Wire Technology," Microbonds Inc., Canada, 2007.

[29] G. Harman, Wirebonding in Microelectronics, New York: McGraw Hill, 2010.

[30] X. Zhang and T. Y. Tee, "Numerical and Experimental Correlation of High Temperature Reliability of Gold Wire Bonding to Intermetallics Uniformity," *Thin Solid Films,* vol. 504, no. 1–2, pp. 355-361, 10 May 2006.

[31] S. Hunter, Writer, *Recent Development Work in IC Bond Pad Structure and Circuit Under Pad.* [Performance]. University of Idaho, 2011.

[32] S. H. Hall, G. W. Hall and J. A. McCall, High-Speed Digital System Design: A Handbook of Interconnect Theory and Design Practices, Wiley-IEEE Press, August 25, 2000.

[33] E. Beyne, "Solving Technical and Economical Barriers to the Adoption of Through-Si-Via 3D Integration," in *IEEE Electronics Packaging Technology Conference*, Belgium, Dec 2008.

[34] N. Magen, A. Kolodny, U. Weiser and N. Shamir, "Interconnect-Power Dissipation in a Microprocessor," in *International Workshop on System Level Interconnect Prediction*, New York, 2004.

[35] R. Hoofman, G. Verheijden, J. Michelon, F. Iacopi, Y. Travaly, M. Baklanov, Z. Tökei and G. Beyer, "Challenges in the implementation of low-k dielectrics in the back-end of line," *Microelectronic Engineering,* vol. 80, pp. 337-344, June 2005.

[36] H. Johnson and M. Graham, High Speed Signal Propagation: Advanced Black Magic, Prentice Hall, 2003.

[37] E. Bogatin, Signal and Power Integrity - Simplified (2nd Edition), Prentice Hall, 2009.

[38] "Addressing Interposer and TSV Quality Challenges," Evaluation Engineering, [Online]. Available: http://www.evaluationengineering.com/articles/201202/addressing-interposer-and-tsv-quality-challenges.php. [Accessed 10 February 2015].

[39] T. Mitsuhashi, Y. Egawa, O. Kato, Y. Saeki, H. Kikuchi, S. Uchiyama, K. Shibata, J. Yamada and M. Ishino, "Development of 3D-Packaging Process Technology for Stacked Memory Chips," *Material Research Society (MRS) Proceedings,* vol. 970, 2007.

[40] P. Morrowa, B. Blacka, M. J. Kobrinskya, S. Muthukumara, D. Nelsona, C.-M. Parka and C. Webba, "Design and Fabrication of 3D Microprocessors," *Material Research Society (MRS) Proceedings,* vol. 970, 2006.

[41] C. Liu and S. K. Lim, "A Study of Signal Integrity Issues in Through-Silicon-Via-based 3D ICs," in *International Interconnect Technology Conference (IITC)*, Burlingame, CA, June 2010.

[42] S. Clark, "IC Package Design's Effects on Signal Integrity," *DesignCon ,* 2003.

[43] S. P. Raghavan, "Signal Integrity Analysis of Package and PCB for High Speed Data link Application," Texas Instruments, Sweden.

[44] "Intel 2000 packaging databook," Intel Corp., [Online]. Available: http://www.intel.com/content/dam/www/public/us/en/documents/packaging-databooks/packaging-chapter-14-databook.pdf. [Accessed 10 February 2015].

[45] M. Swaminathan, J. Kim, I. Novak and J. P. Libous, "Power Distribution Networks for System-on-Package:Status and Challenges," *Advanced Packaging, IEEE Transactions on,* vol. 27, no. 2, pp. 286-300, May 2004.

[46] F. Carrió, V. González and E. Sanchis, "Basic Concepts of Power Distribution Network Design for High-Speed Transmission," *The Open Optics Journal,* vol. 5, pp. 51-61, 2011.

[47] P. Larsson, "Resonance and damping in CMOS circuits with on-chip decoupling capacitance," *Transactions on Circuits and Systems-I: Fundamental Theory and Applications,* vol. 45, no. 8, pp. 849-858, Aug. 1998.

[48] M. Pant, P. Pant and D. Wills, "On-chip decoupling capacitor optimization using architecture level prediction," *IEEE Transactions on Very Large Integration (VLSI) Systems,* vol. 10, p. 319–326, June 2002.

[49] S. Pant, "Design and analysis of power distribution networks in vlsi circuits," The University of Michigan, 2008.

[50] K. Bharath, E. Engin and M. Swaminathan, "Automatic package and board decoupling capacitor placement using genetic algorithms and M-FDM," in *Design Automation Conference, 2008. DAC 2008. 45th ACM/IEEE*, Anaheim, CA, June 2008.

[51] J. Kim, M. D. Rotaru, S. Baek, J. Park, M. K. Iyer and J. Kim, "Analysis of Noise Coupling From a

Power Distribution Network to Signal Traces in High-Speed Multilayer Printed Circuit Boards," *IEEE Transactions on Electromagnetic Compatibility,* vol. 48, no. 2, pp. 319-330, May 2006.

[52] D. Brooks, " Differential Signals," CMP Media publication, October 2001.

[53] J. Kim, L. Ren and J. Fan, "Physics-Based Inductance Extraction for Via Arrays in Parallel Planes for Power Distribution Network Design," *IEEE Transactions on Microwave Theory and Techniques,* vol. 58, no. 9, pp. 2434 - 2447, September 2010.

[54] I. Novak, Y. Mori and M. Resso, "Accuracy Improvements of PDN Impedance Measurements in the Low to Middle Frequency Range," *DesignCon2010,* pp. 1-26.

[55] J. S. Pak, J. Lee, H. Kim and J. Kim, "Prediction and verification of power/ground plane edge radiation excited by through-hole signal via based on balanced TLM and via coupling model," in *IEEE Proc. Topical Meeting on Electrical Performance*, Princeton, NJ, USA, 2003.

[56] M.-S. Zhang, Y.-S. Li, L.-P. Li, C. Jia, J. Pan, J.-M. Lu, S. Gao and D.-C. Jiang, "An efficient power delivery method for the design of the power distribution networks for high-speed digital systems," *IEEE Transactions On Microwave Theory and Techniques,* vol. 57, no. 3, pp. 693-707, March 2009.

[57] I. Novak, Power Distribution Network Methodology, International Engineering Consortium, 2008.

[58] N. Rao, "FPGA Packaging and Signal Integrity: A Connectivity Perspective," Xilinx, Inc., May 29, 2007 .

[59] J. Keinänen, "High Speed Rules - Part 1 Signal Integrity Is Here," Chili Devices International, 2006.

[60] J. Sutherland, "As edge speeds increase, wires become transmission lines," California Micro Devices, October 1999.

[61] "The Basics of Signal Integrity, Part I-II," Altera, [Online]. Available: http://www.altera.com/technology/signal/fundamentals/basics/sgl-basics-cont.html. [Accessed 10 February 2015].

[62] "Interconnect Signal Integrity Handbook, ,," Samtec, Inc., 2007.

[63] P. J. Wang, "Mixed-Mode S-Parameter Measurements of Power Distribution Networks," University of Idaho, Moscow, ID, 2015.

[64] "An Introduction to HFSS: Fundamental Principles, Concepts, and Use," Ansys, Inc., Canonsburg, USA, 2013.

[65] A. L. L. L. W. B. K. L. W. Fan, "Mixed-Mode S-Parameter Characterization of Differential Structures," in *Electronics Packaging Technology, 2003 5th Conference IEEE*, 2003.

[66] S. M. B. R. K. G. W. R. G Subhash, "Fatigue crack propagation in aluminum nitride ceramics under cyclic compression," *Journal of Materials Research,* vol. 34, no. 19, pp. 4645-4652, 1999.

[67] [Online]. Available: http://www.matweb.com.

[68] S. P. S. L. S. P. S. Pietranico, "Thermal fatigue and failure of electronic power device substrates," *International Journal of Fatigue,* vol. 31, no. 11-12, 2009.

[69] C. Selvanayagam, "Nonlinear thermal stress/strain analyses of copper filled TSV (through silicon via) and their flip-chip microbumps," in *Electronic Components and Technology Conference*, 2008.

[70] Y. O. N. S. M. O. Hiroshi Yamagata, "Effect of Temperature on the Continuous Dynamic Recrystallization of 99.99 mass% Aluminum," *MATERIALS TRANSACTIONS,* vol. 42, no. 11, pp. 2440-2445, 2001.

APPENDIX A

Model 1 (PDN with no traces)

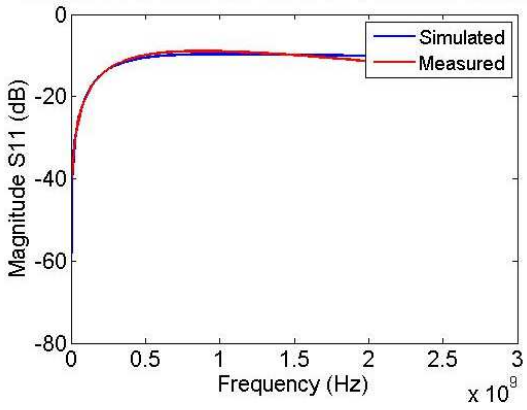


Figure 62: Comparison (Sim Vs Mea) of S11

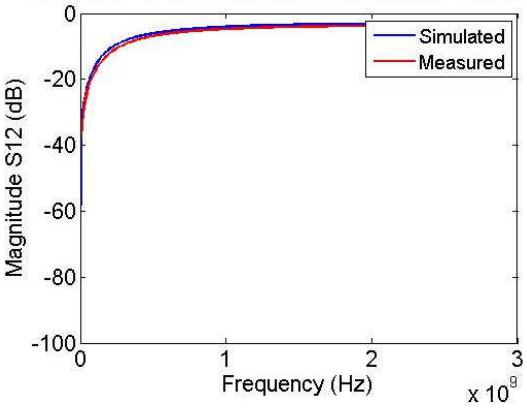


Figure 63: Comparison (Sim Vs Mea) of S12

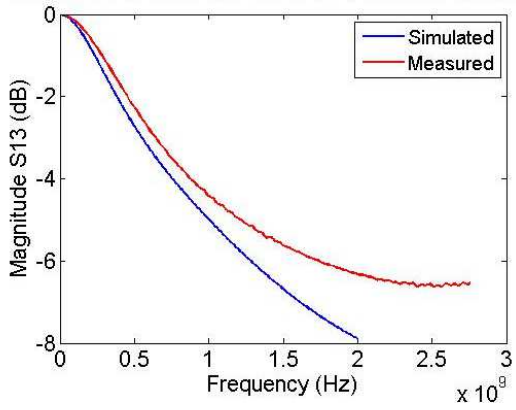


Figure 64: Comparison (Sim Vs Mea) of S13

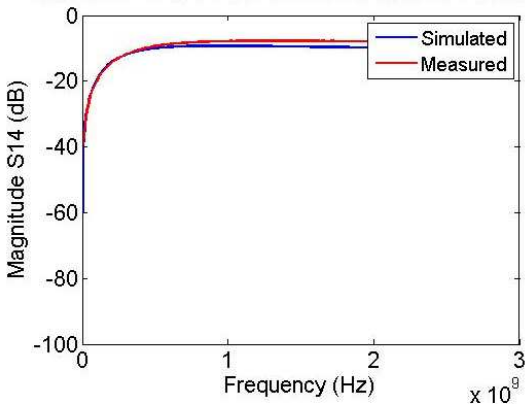


Figure 65: Comparison (Sim Vs Mea) of S14

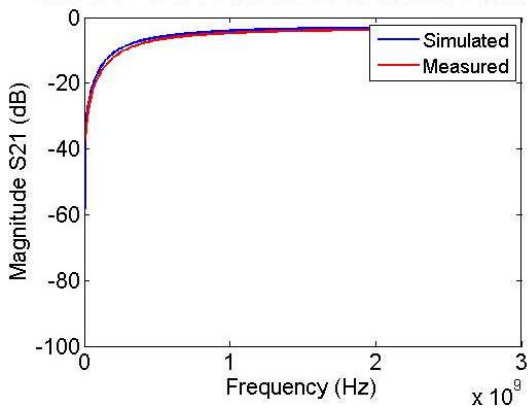


Figure 66: Comparison (Sim Vs Mea) of S21

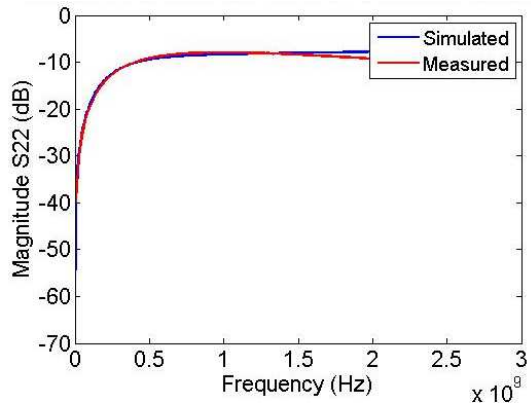


Figure 67: Comparison (Sim Vs Mea) of S22

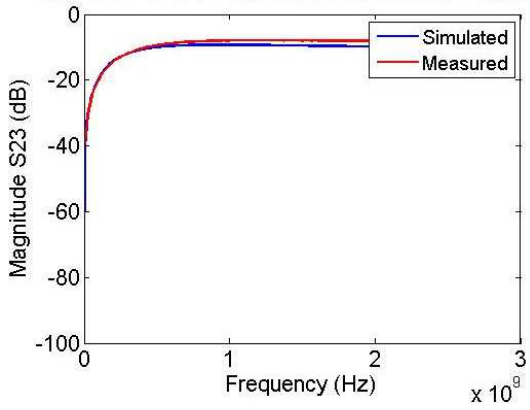


Figure 68: Comparison (Sim Vs Mea) of S23

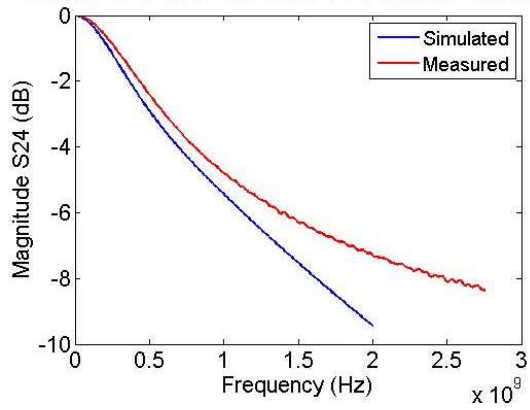


Figure 69: Comparison (Sim Vs Mea) of S24

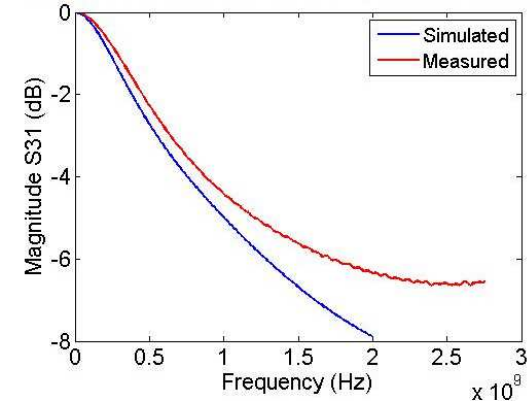


Figure 70: Comparison (Sim Vs Mea) of S31

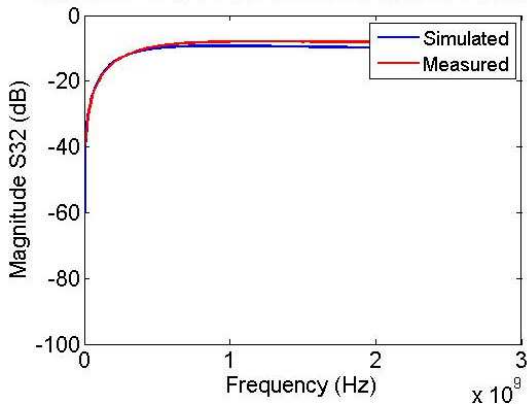


Figure 71: Comparison (Sim Vs Mea) of S32

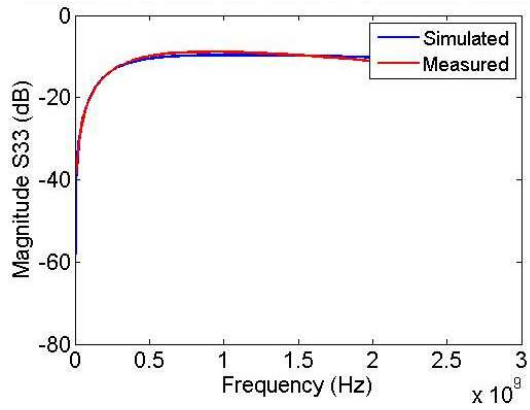


Figure 72: Comparison (Sim Vs Mea) of S33

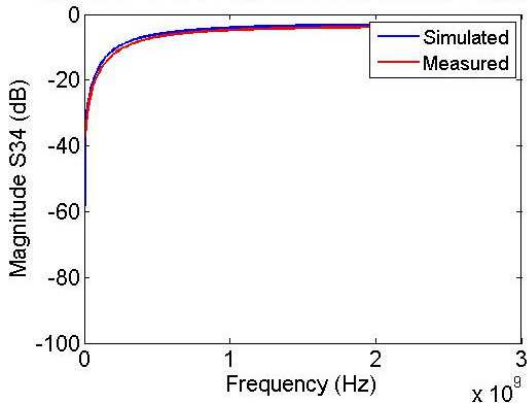


Figure 73: Comparison (Sim Vs Mea) of S34

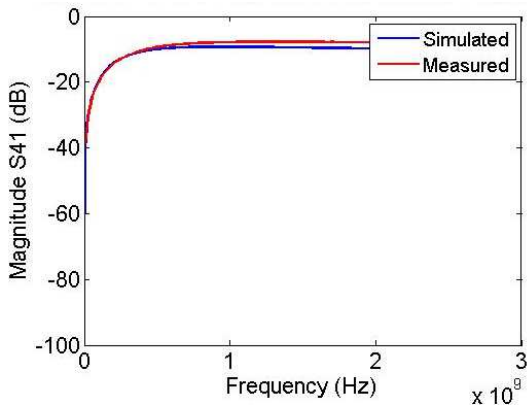


Figure 74: Comparison (Sim Vs Mea) of S41

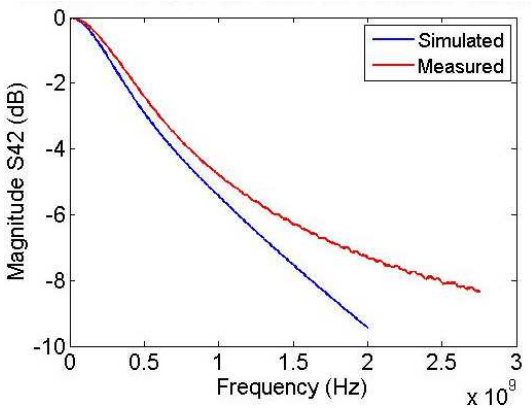


Figure 75: Comparison (Sim Vs Mea) of S42

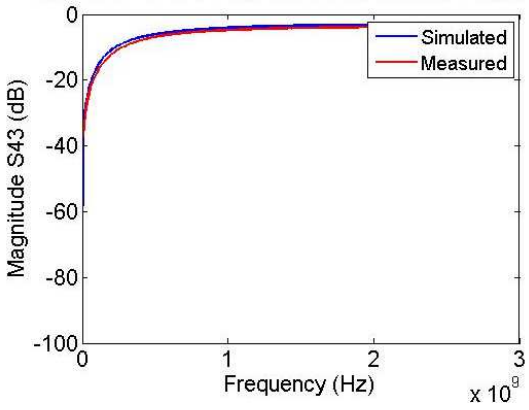


Figure 76: Comparison (Sim Vs Mea) of S43

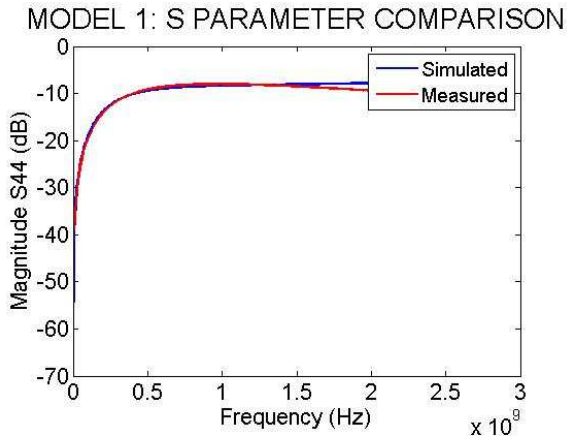


Figure 77: Comparison (Sim Vs Mea) of S44

Model 2 (PDN with vias)

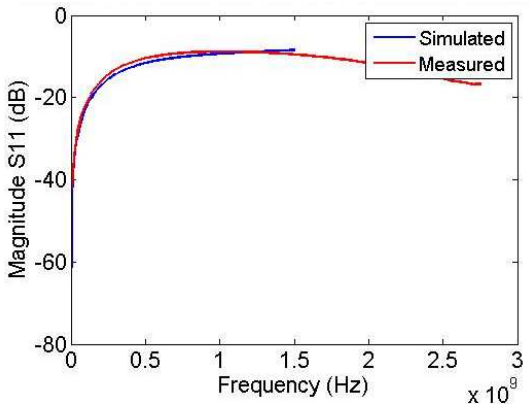


Figure 78: Comparison (Sim Vs Mea) of S11

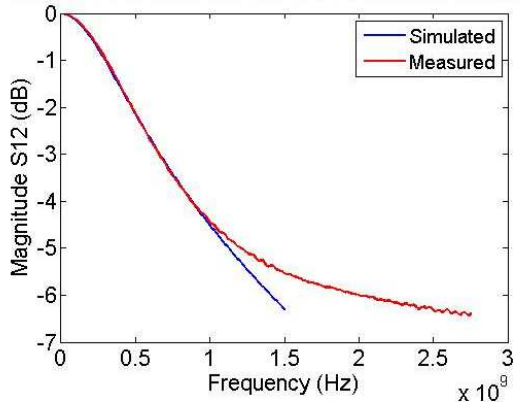


Figure 79: Comparison (Sim Vs Mea) of S12

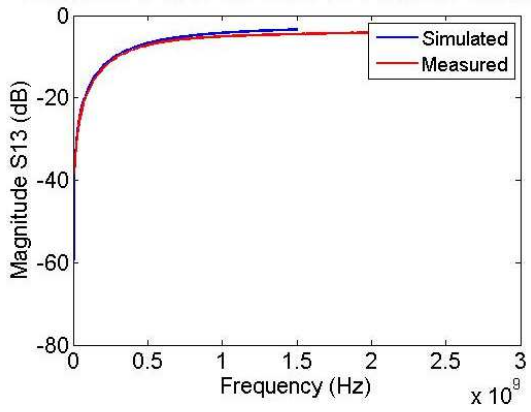


Figure 80: Comparison (Sim Vs Mea) of S13

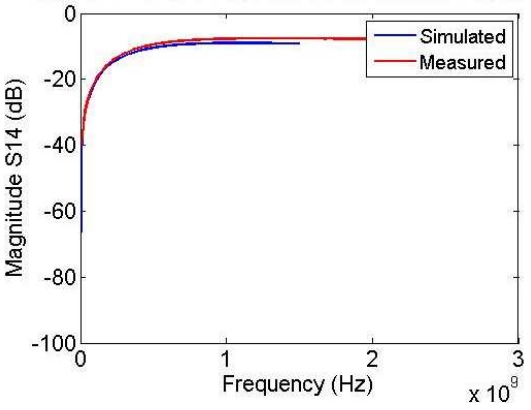


Figure 81: Comparison (Sim Vs Mea) of S14

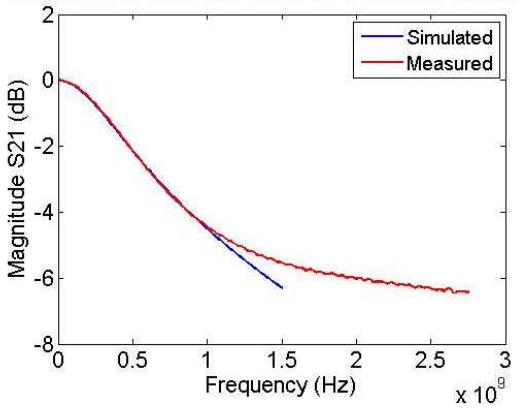


Figure 82: Comparison (Sim Vs Mea) of S21

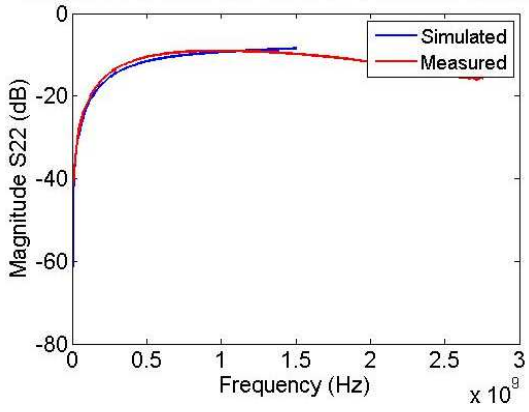


Figure 83: Comparison (Sim Vs Mea) of S22

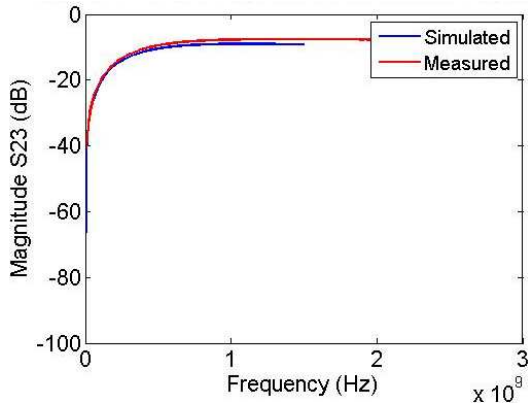


Figure 84: Comparison (Sim Vs Mea) of S23

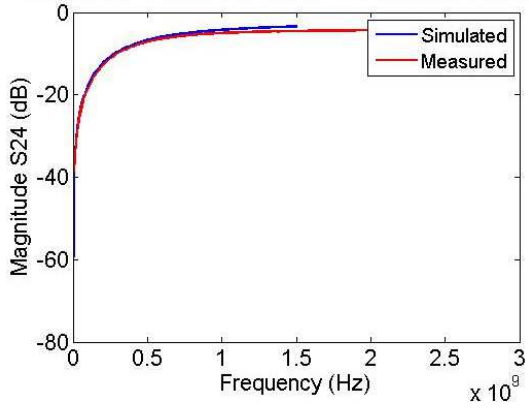


Figure 85: Comparison (Sim Vs Mea) of S24

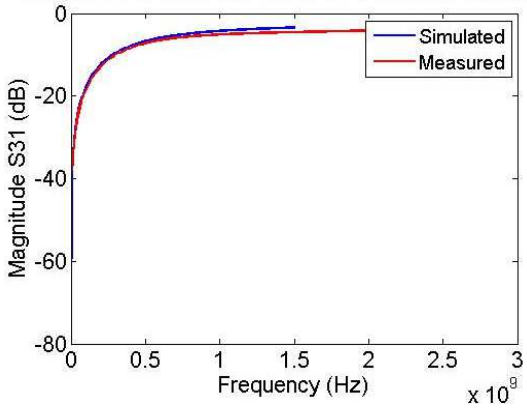


Figure 86: Comparison (Sim Vs Mea) of S31

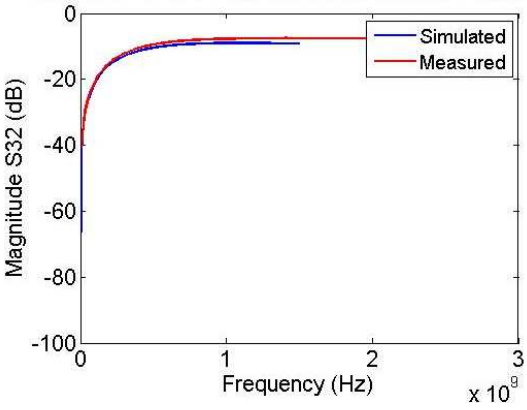


Figure 87: Comparison (Sim Vs Mea) of S32

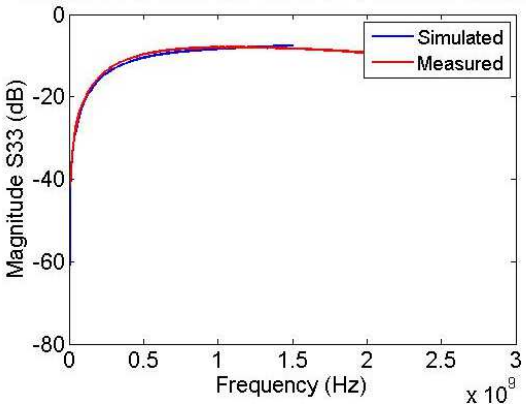


Figure 88: Comparison (Sim Vs Mea) of S33

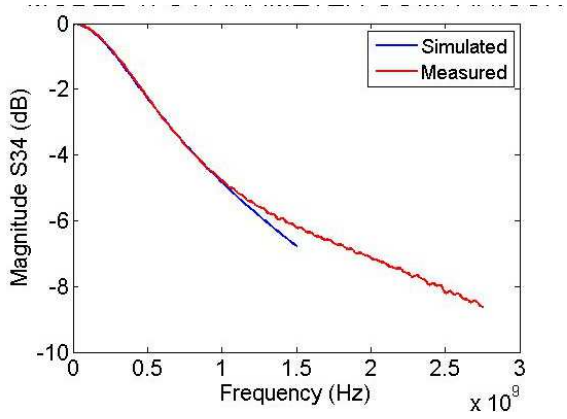


Figure 89: Comparison (Sim Vs Mea) of S34

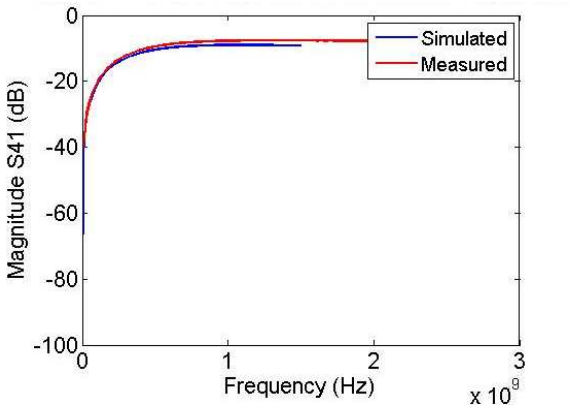


Figure 90: Comparison (Sim Vs Mea) of S41

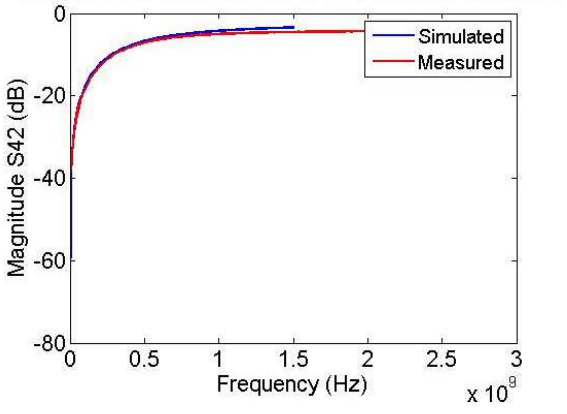


Figure 91: Comparison (Sim Vs Mea) of S42

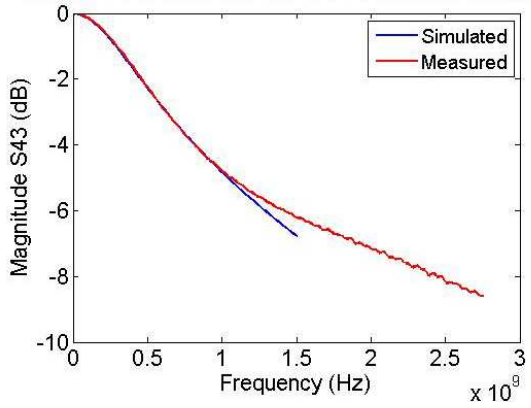


Figure 92: Comparison (Sim Vs Mea) of S43

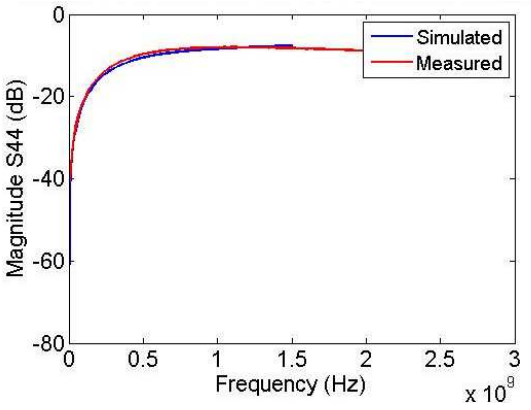


Figure 93: Comparison (Sim Vs Mea) of S44

Model 3 (PDN with no vias)

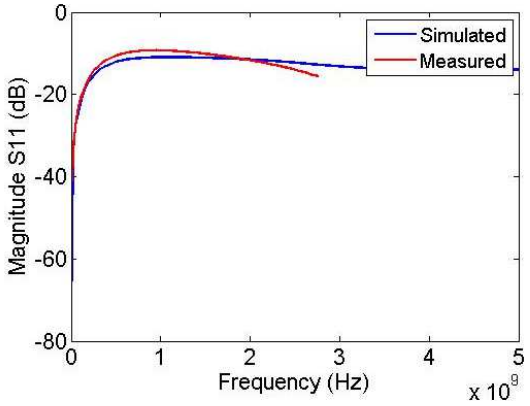


Figure 94: Comparison (Sim Vs Mea) of S11

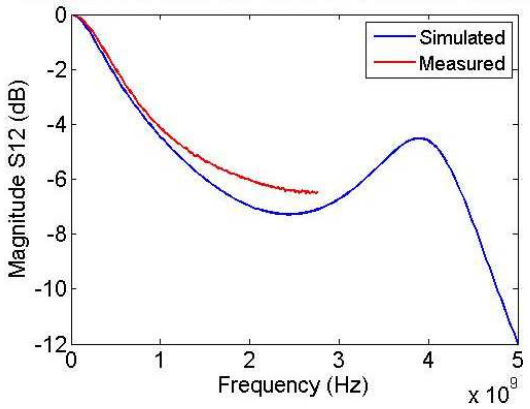


Figure 95: Comparison (Sim Vs Mea) of S12

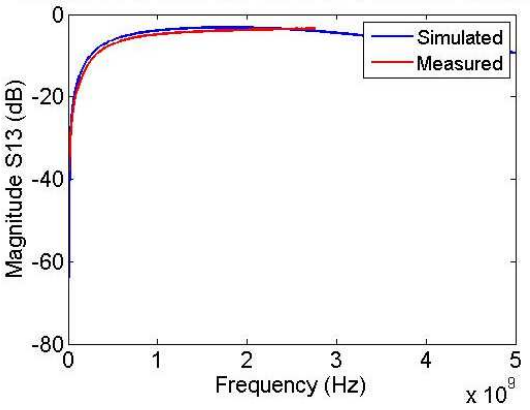


Figure 96: Comparison (Sim Vs Mea) of S13

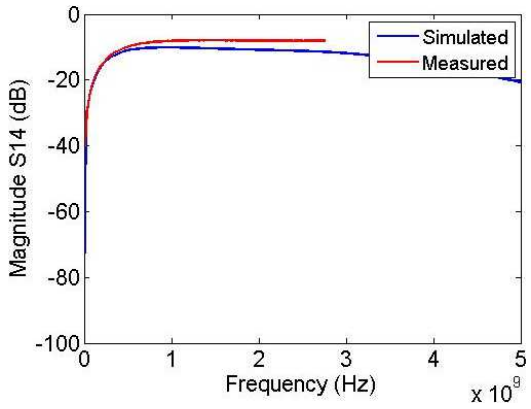


Figure 97: Comparison (Sim Vs Mea) of S14

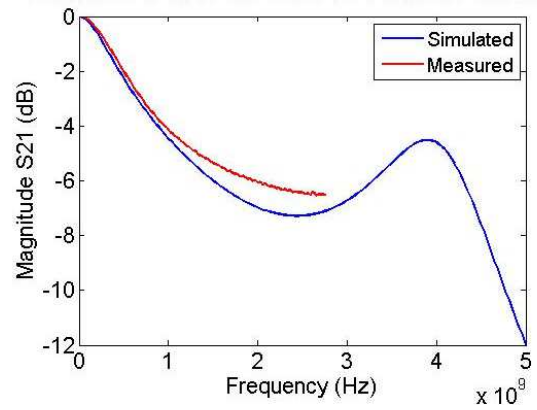


Figure 98: Comparison (Sim Vs Mea) of S21

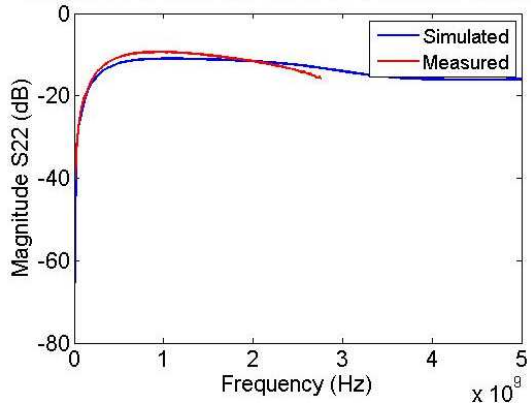


Figure 99: Comparison (Sim Vs Mea) of S22

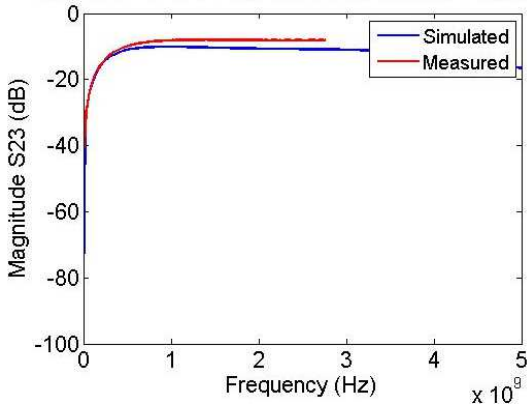


Figure 100: Comparison (Sim Vs Mea) of S23

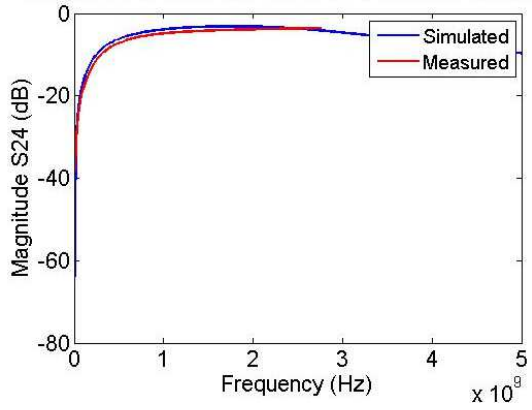


Figure 101: Comparison (Sim Vs Mea) of S24

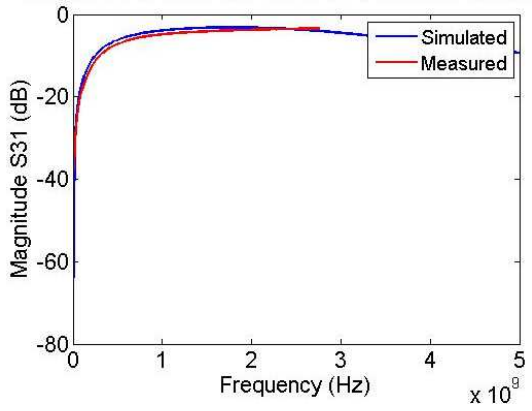


Figure 102: Comparison (Sim Vs Mea) of S31

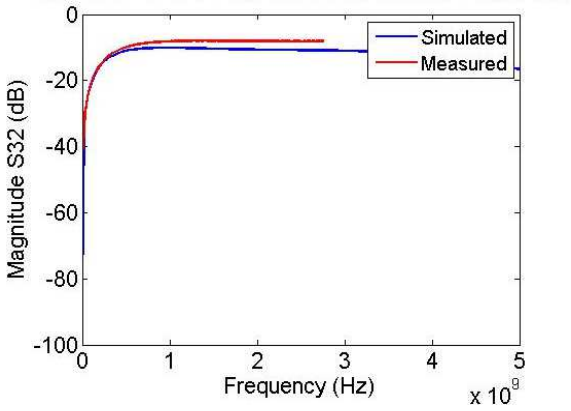


Figure 103: Comparison (Sim Vs Mea) of S32

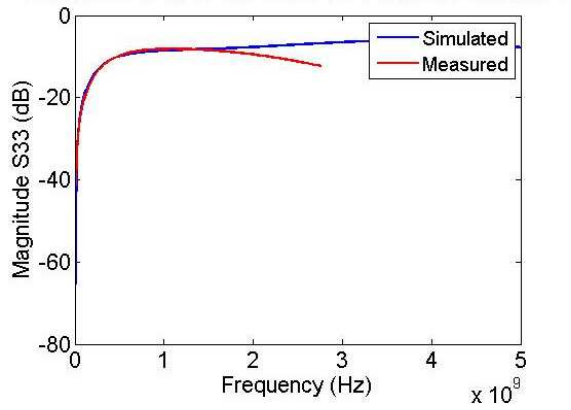


Figure 104: Comparison (Sim Vs Mea) of S33

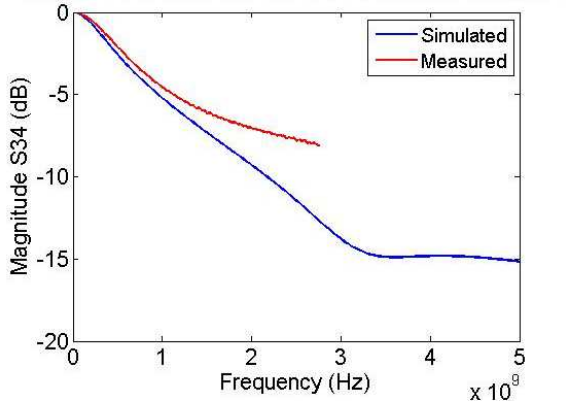


Figure 105: Comparison (Sim Vs Mea) of S34

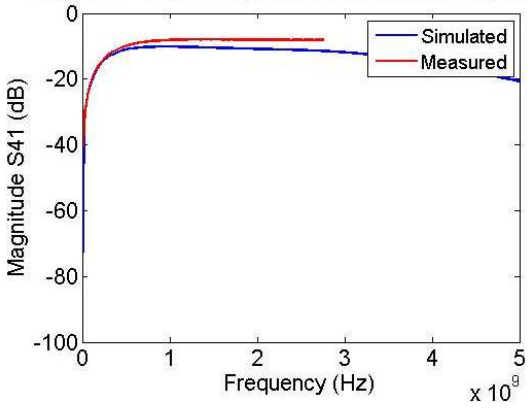


Figure 106: Comparison (Sim Vs Mea) of S41

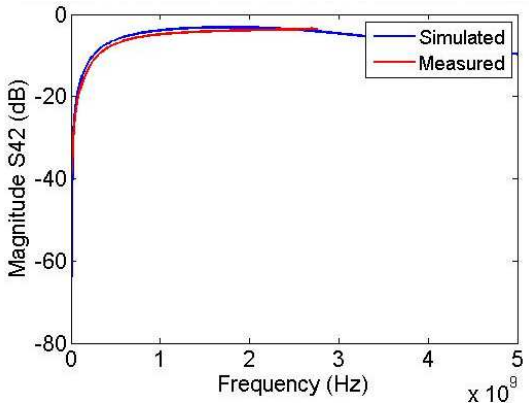


Figure 107: Comparison (Sim Vs Mea) of S42

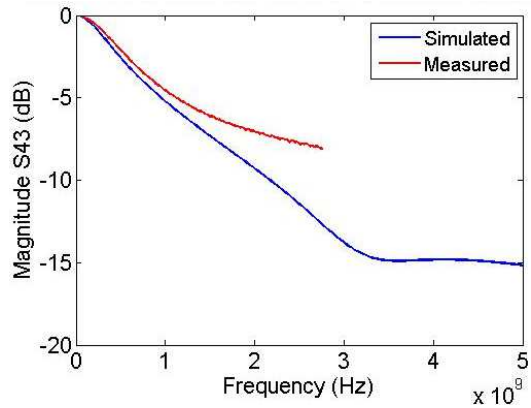


Figure 108: Comparison (Sim Vs Mea) of S43

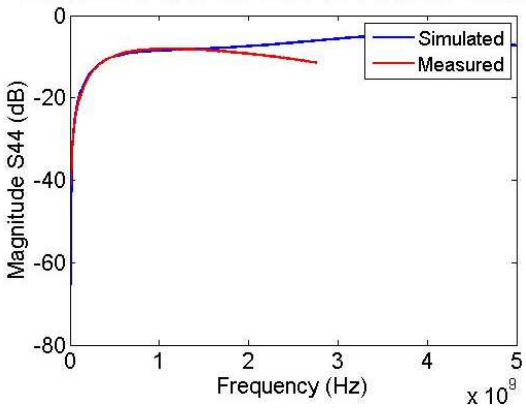


Figure 109: Comparison (Sim Vs Mea) of S44