MODELING AND SIMULATION OF A STATIC SYNCHRONOUS COMPENSATOR (STATCOM) FOR THE UI ANALOG MODEL POWER SYSTEM

A Thesis

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Authorization to Submit Thesis

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Abstract

Fast, efficient dynamic reactive power compensation is important for maintaining voltage stability on the electric power grid as a whole as well as maintaining local voltage regulation to the customer. Dynamic reactive compensation is discussed in several courses in the ECE program. In this presentation, the design and modeling of a static synchronous compensator (STATCOM) that can be connected the Analog Model Power System (AMPS) at the University of Idaho for classroom instruction will be presented. Detailed averaged and switching models of a STATCOM will be presented. The goal of the modeling is to replicate the real world behavior of a STATCOM interfaced with the AMPS which will provide a basis for class projects and studies demonstrating concepts of dynamic reactive power compensation. After developing the model of the STATCOM interfaced with the AMPS, simulations were conducting to verify the STATCOM works as intended. The results from the simulations lay the foundations for a hardware implementation of the STATCOM in the lab.

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Chapter 1

Introduction

In this thesis, modeling of a static synchronous compensator (STATCOM) for the Analog Model Power System (AMPS) at the University of Idaho will be presented. Detailed averaged and switching models of a STATCOM will be developed and presented. Open loop and closed loop control schemes for the STATCOM will be discussed. The goal of the modeling is to replicate the real world behavior of hardware based STATCOM that will be interfaced with the AMPS to provide a basis for studies related to the reactive compensation using the AMPS. After the modeling of the STATCOM, the simulations will be run to verify the STATCOM works as intended.

A STATCOM is a voltage sourced converter system whose primary function is to exchange reactive power with the host AC system. In an electric power system, the STATCOM can be used to increase the line power transmission capacity, to enhance the voltage/angle stability, or to damp the system oscillatory modes [1]. In a distribution system, the STATCOM is mainly used for voltage regulation; however it can also temporarily supply real power to the loads in the case of a service interruption if it is augmented with an energy storage device, for example, a battery storage system. Moreover, the STATCOM may also be employed to balance phase currents a distribution network by compensating for load imbalances [2].

1.1 Objectives

The goals of this research work are to:

a) Create three phase models for the STATCOM-both averaged and switching for the use with the UI Analog Model Power System.

b) Develop the models to be used as the part of the lab experiments. Dynamic reactive compensation is discussed in several courses in the ECE program.

c) Determine the parameters for the hardware implementation of the STATCOM, so that they may be used to develop the hardware model.

d) Use the models for different studies in future related to the reactive compensation and voltage support for the analog model power system.

In this chapter, we will look at why we need reactive compensation, different kinds of compensation techniques available, and provide a brief introduction to the STATCOM.

1.2 Need for Reactive Compensation

In general, the problem of dynamic reactive power compensation is viewed from the two aspects: load compensation and voltage support. In load compensation, the objectives are to increase the value of the system power factor, to balance per phase real power drawn from the ac supply, provide voltage regulation and to eliminate voltage flicker produced by large and fluctuating nonlinear industrial loads. In voltage support, dynamic reactive compensation is used to reduce voltage fluctuation at a given terminal of a transmission or distribution line. Reactive power compensation in transmission systems helps in improving the stability of the ac system by increasing the maximum active power that can be transmitted. It also helps to maintain a substantially flat voltage profile at all levels of power transmission and distribution; in addition, it improves HVDC conversion terminal performance, increases transmission efficiency, controls steady-state and temporary overvoltages, and can help avoid disastrous blackouts [3]. Some of the other advantages of using dynamic reactive power compensation are: limiting rapid voltage increase or decline, limiting slow voltage increase or decline, and limiting fast wave-front overvoltages due to switching transients [4]. The power electronic based devices used for dynamic reactive power compensation fall under the family of FACTS devices which will be discussed next.

1.3 Basic types of FACTS Controllers

FACTS is defined by the IEEE Power Engineering Society (PES) as alternating current transmission system devices incorporating power electronic based and other static controllers to enhance controllability and enhance power transfer capability. A FACTS controller is defined as a power electronic based system or other static equipment that provides control of one or more AC transmission system parameters [1].

In general, the FACTS controllers can be divided into the following four categories,

i) Series controllers: The series controller could be a variable impedance, such as thyristor switched capacitor, reactor, or a power electronics based variable source of main frequency that injects a voltage in series with the line as can be seen in Figure 1.1(b) [1]. The series voltage in the line can be represented by a variable impedance multiplied by the current flow through it. The series controller supplies or absorbs variable reactive power when the voltage is plus or minus 90 degrees out of phase with the line current, and any other phase relationship involve with the transfer of real power as well and requires either an external energy source or energy storage.

ii) Shunt controllers: As in the case of series controllers, the shunt controllers may be variable impedance, variable voltage or current source, or a combination of these as seen in Figure 1.1(c) [1]. The shunt controllers effectively inject current into the system at the point of connection. The shunt controller supplies or absorbs variable reactive power when the

injected current is plus or minus 90 degrees out of phase with the line voltage, and any other phase relationship involves the transfer of real power as well.

iii) Combined series-series controllers: These controllers are the combination of two or more separate series controllers, which are controlled in a coordinated manner in a multiline transmission system as seen in Figure 1.1(d) [1]. The device could be also be a unified controller, in which series controllers provide independent series reactive compensation for each line while transferring real power between the lines via the dc link. The real power transfer capability of the unified series-series controller makes it possible to balance both the real and reactive power flow in parallel lines and therefore maximize the utilization of the transmission system.

iv) Combined series-shunt controllers: These controllers are a combination of separate shunt and series controllers, which are controlled in a coordinated manner. An example is a Unified Power Flow Controller (UPFC) with series and shunt elements joined through a common dc bus. The combined shunt and series controllers inject current into the system with the shunt part of the controller and voltage in series in the line with the series part of the controller. When the shunt and the series controllers are unified, there can be a real power exchange between the series and shunt controllers via the power link as seen in the Figure 1.1(f) [1].

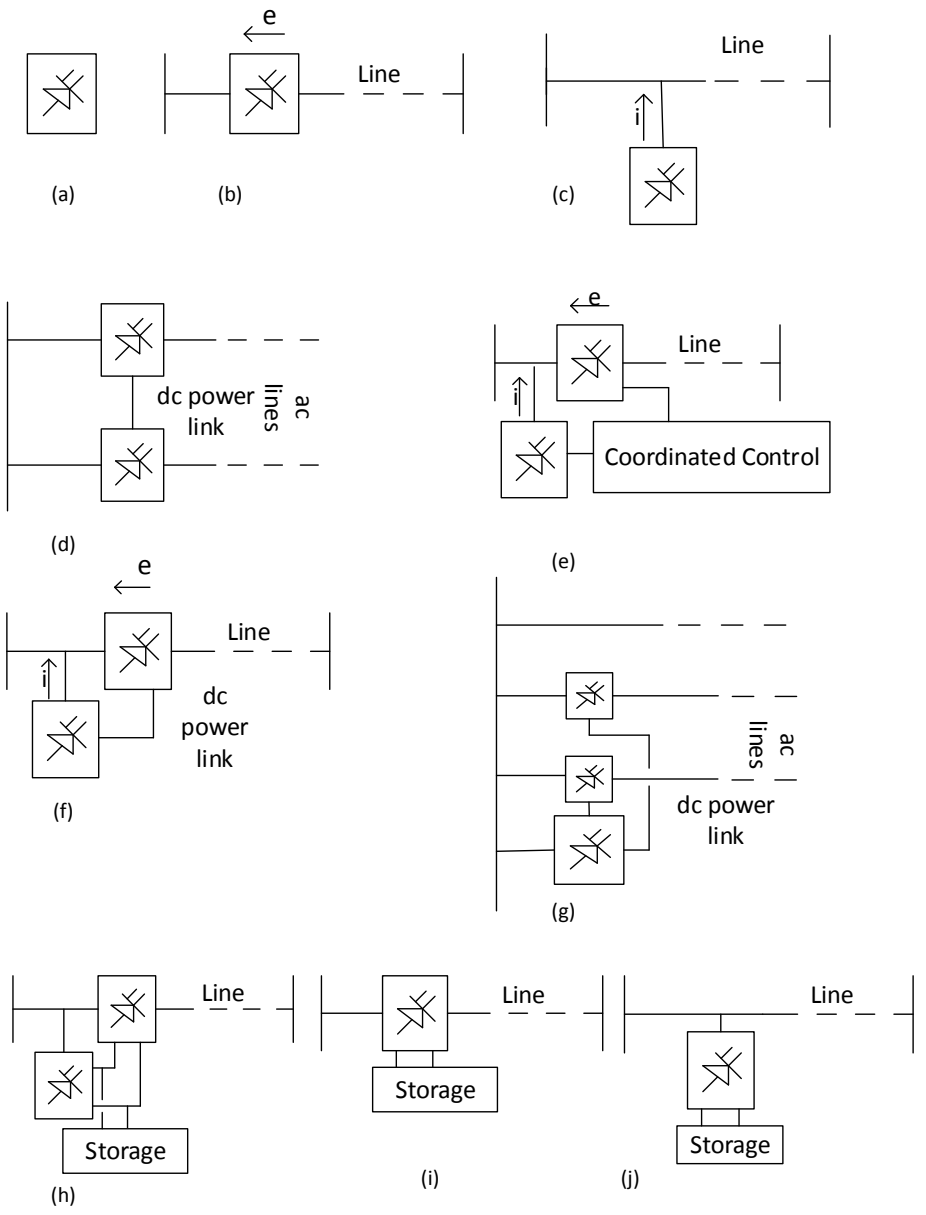

Figure 1.1: Basic types of FACTS Controllers: a) general symbol for FACTS controller; b) series controller; c) shunt controller; d) unified series-series controller e) coordinated series and shunt controller; f) unified series-shunt controller g) unified controller for multiple lines; h) series controller with storage; i) shunt controller with storage ; j) unified series-shunt controller with storage [1].

1.4 Shunt Connected Controllers

Among the different categories of the FACTS controllers, the two devices considered for the purpose of this research are the STATCOM and the SVC. These devices fall under the category of shunt connected controllers.

1.4.1 Static VAR Compensator (SVC)

A SVC is a shunt-connected static var generator or absorber whose output is adjusted to exchange capacitive or inductive current to maintain or control specific parameters of the electrical power system. This is a general term for a thyristor-controlled or thyristor-switched reactor, and/or thyristor-switched capacitor or combination as seen in Figure 1.2. A SVC is based on thyristors without gate turn-off capability. A SVC typically includes separate devices to provide leading and lagging vars: the thyristor-controlled reactor, possibly a thyristor-switched reactor for absorbing reactive power with minimal harmonic generation, and a combination of mechanically or thyristor-switched capacitors for supplying reactive power. A SVC can also be considered as a lower cost alternative to the STATCOM, although this may not be the case if the comparison is made based on the certain performance requirements or need for a minimal substation footprint, and not just the MVA capacity [1].

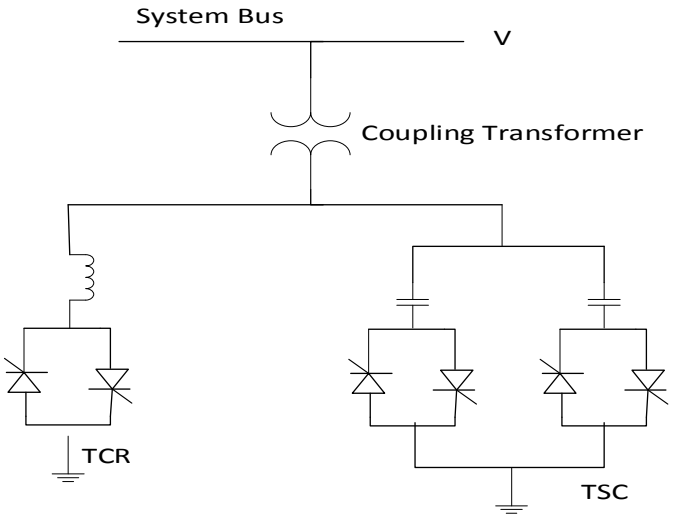

Figure 1.2: Static VAR Compensator (SVC)

1.4.2 Static Synchronous Compensator (STATCOM)

A STATCOM can be viewed as a static voltage source operated as a shunt-connected static var compensator whose capacitive or inductive output current can be controlled independent of the ac system voltage [1]. A STATCOM is based on a voltage-sourced converter or a current-sourced converter (although none have been implemented in practice). The voltage sourced converters are preferred from overall cost point of view, and are the most commonly applied converter-based FACTS controllers. In the voltage-sourced converter based STATCOM, the ac output voltage is controlled such that the required reactive current flows for a given ac bus voltage as seen in Figure 1.3. The dc capacitor voltage is adjusted as required to serve as a voltage source for the converter. The STATCOM can be controlled to also act as an active filter to absorb system harmonics, but that is limited to low voltage, low MVA applications. A STATCOM as defined by IEEE is a subset of the broad based family of shunt connected controllers which includes the possibility the

addition of an active power source or energy storage on the dc side of the converter so that the injected current may include active power. The STATCOM operating principles will be described in detail later in this thesis.

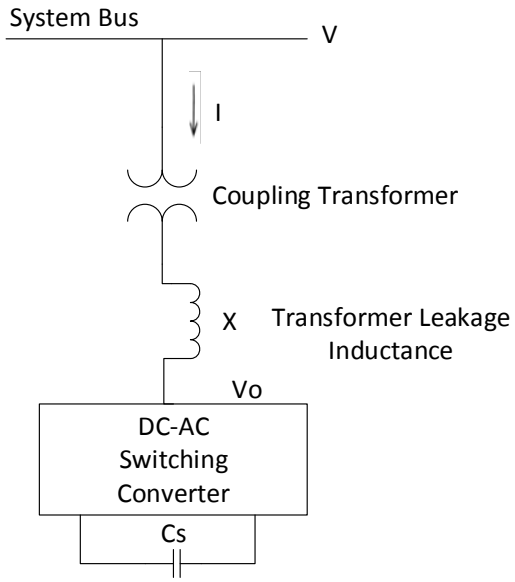

Figure 1.4: Static Synchronous Compensator (STATCOM)

1.5 Organization of the thesis

The thesis is organized as follows:

This chapter introduced the objectives of the research, reactive compensation techniques, and different types of FACTS devices, with a brief introduction to the STATCOM.

Chapter 2 describes the basics of STATCOM operation, and the associated control system. The chapter discusses the circuit topology of the STATCOM, and looks into when the switching model of the STATCOM can be replaced with an averaged model. It also looks into

the equations describing the averaged models and the switching models. Furthermore, some options for closed loop control of the STATCOM are described.

Chapter 3 provides the information about the Analog Model Power System (AMPS) and the ATPDraw model of the AMPS. It also introduces the software used for the simulation, which is ATP (Alternate Transients Program), which uses ATPDraw as a graphical user interface.

Chapter 4 describes the modeling of the STATCOM component blocks and the implementation of the associated controls. In this chapter the ATPDraw implementations of the averaged and the switching models for the STATCOM are discussed. It also describes the control model used in the simulations.

Chapter 5 shows the results of simulations using the STATCOM with the AMPS. Different types of simulation scenarios, such changing the load impedances, changing the line lengths, and including faults in the AMPS system are presented. The reactive power support provided by the STATCOM in different simulation scenarios is discussed in detail.

And finally, Chapter 6 presents the conclusions from the thesis and the future work associated with the STATCOM modeling and simulation. The chapter discusses how the simulation model can be used in future courses and for research purposes, and the ratings for the devices for the hardware implementation are discussed as well.

Chapter 2

Static Synchronous Compensator (STATCOM) Operation and Characteristics

In this chapter, the basic circuit configuration for the STATCOM and its operation and control characteristics are discussed. An equivalent circuit for the STATCOM system will be described. The differences between STATCOM and SVC will be explored, and the benefits associated with choosing the STATCOM system compared to the SVC system for the model power system application will be discussed as well.

2.1 Basic Operating Principle

The basic operating principle for reactive power generation from a voltage-sourced converter is similar to that of the conventional rotating synchronous machine as seen in Figure 2.1.

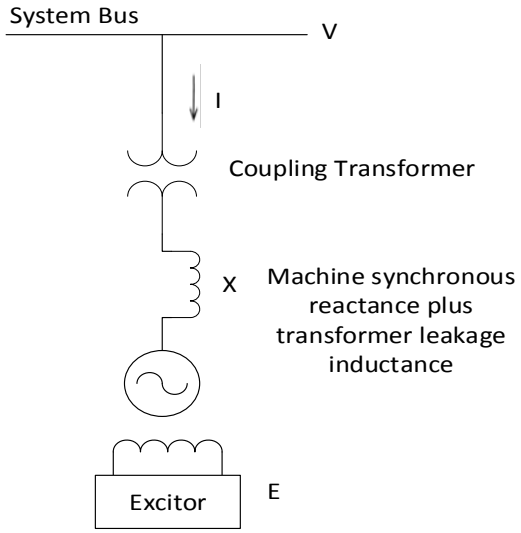

Figure 2.1: Equivalent Circuit of a Rotating Synchronous Machine [1]

The current drawn by the synchronous compensator is determined by the system voltage V, the internal voltage E, and the total circuit reactance X as shown in equation (2.1) for the case when V and E are in phase with each other, and no real power flows.

$$I = \frac{|V| - |E|}{X} \tag{2.1}$$

The corresponding reactive power Q exchanged can be expressed as follows,

$$Q = \frac{1 - \frac{|E|}{|V|}}{X} \cdot (|V|)^2 \tag{2.2}$$

Note than equations (2-1) and (2-2) assume the angle of E is equal to the angle of V. The reactive power flow can be controlled by varying the excitation of the machine, and thus the amplitude |E| of its internal voltage relative to the amplitude |V| of the system voltage. Increasing |E| above |V|, or operating overexcited results in a leading current, that is, the machine appears capacitive to the system. When |E| is below |V|, or operating underexcited, the machine produces a lagging current, which means the machine is seen as inductive by the ac system. Under both operating conditions, a small amount of real power flows from the ac system to the machine to supply its mechanical and electrical losses which are not represented above. If the excitation of the machine is controlled so that the corresponding reactive output maintains or varies a specific parameter of the ac system, then the machine functions as a rotating synchronous compensator [1].

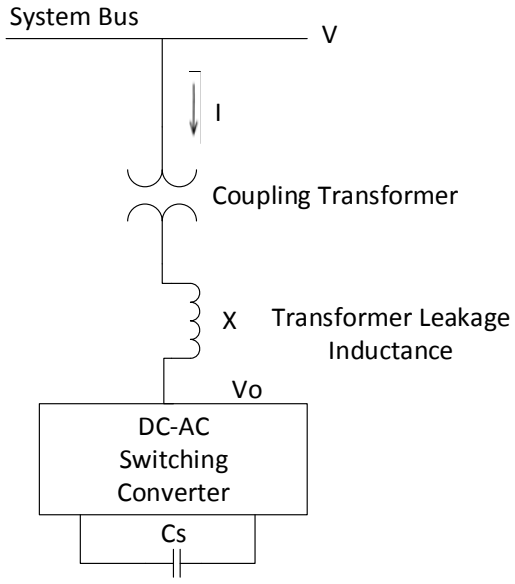

Figure 2.2: Reactive Power Generation by a Static VSC [1]

The basic voltage-sourced converter scheme for reactive power generation is shown in Figure 2.2. The converter produces a set of controllable three-phase output voltages with the frequency of the ac power system tracked from the input voltage source, provided by the charged capacitor Cs. The output voltage, Vo, which is in phase with the ac system voltage, is coupled to the corresponding ac system voltage through a relatively small reactance. The reactive power exchange between the converter and the ac system can be controlled by varying the amplitude of the output voltages produced similar to the effect of varying the excitation of the rotating synchronous machine. If the amplitude of the fundamental component of the converter output voltage is increased above that of the ac system, then the current flows through the reactance from the converter to the ac system, and the converter generates reactive (capacitive) power for the ac system. If the amplitude of the output voltage is decreased below that of the ac system, then the reactive current

flows from the ac system to the converter, and the converter absorbs reactive (inductive) power. If the amplitude of the output voltage is equal to that of the ac system voltage, the reactive power exchange is zero [1].

2.2 Basic control approaches

2.2.1 Inner Control Loop

The control system of the voltage source converter in a STATCOM is often based on an inner and outer control loop structure. The inner current control loop generates the commands for the switching, and the reference current for the inner loop is provided by the outer loop. The commands generated from the inner control are used to send the signals to the gate drivers for power semiconductor devices. In most cases we are controlling the ac current. As seen in Figure 2.3, in an inner control loop, the measured three phase currents are transformed to the synchronous reference frame using the Park's transformation resulting in Id measured and Iq measured. The measured currents are compared to current references: Iqref and Idref. Typically the error from the reference terms will go through a proportional integral inner controller. The outputs from the controller are modulating functions md(t) and mq(t), which are converted back to the abc reference frame.

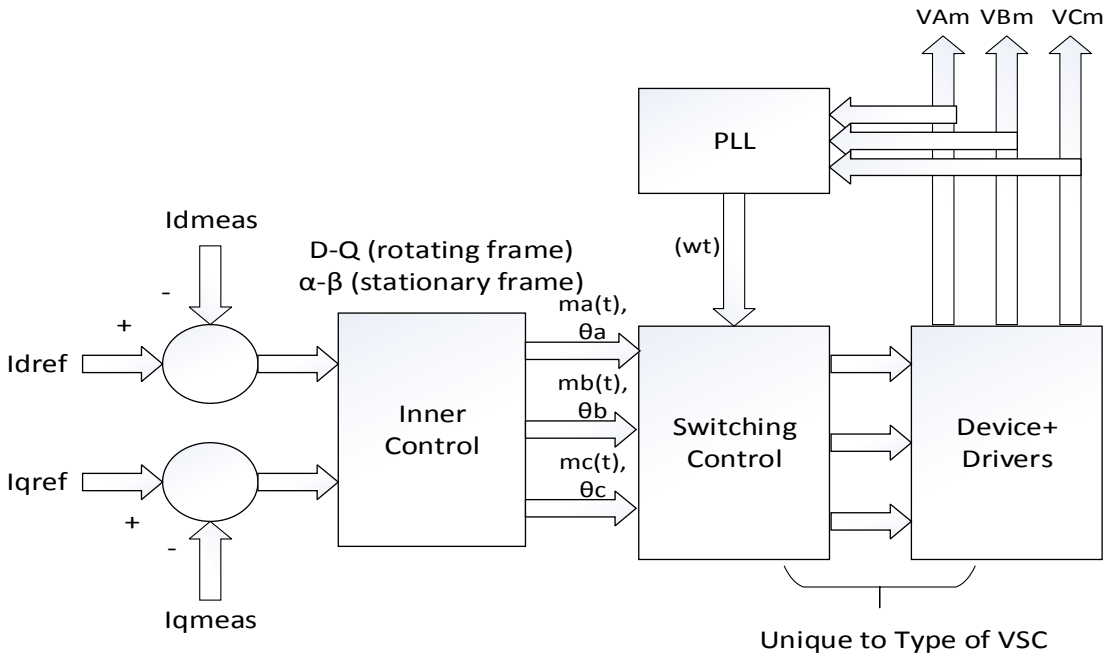

Figure 2.3: Inner Control Scheme for the VSC

The inner control loop has a fast response to regulate current. The bandwidth of the control increases towards inner control from the outer control. Because of this, the design of the controller is simplified too, since control is decoupled by the Park's transformation. Transformation to the synchronous reference frame simplifies control design by slowing the variation of the signals. It is assumed that controlled only responds to transients that are slowly varying and the measured quantities maybe low pass filtered to support this. The advantage of a synchronous reference frame is that it makes decoupling, or separating the 60 Hz steady state component from other components easier in the computations, allowing simple PI controllers to be used. The amplitude of each feedback variable is limited by clamping the pertinent reference. This approach also simplifies the field work because the control loops can be put into operation and tested one after another. Another major

advantage is that a disturbance in the system affects inner loop first before reaching the outer controls; and since the inner loop is faster it results in a better disturbance rejection. The inner controller used for the STATCOM will be described further in Chapter 4.

2.2.2 Outer Control Loop

The outputs of the outer control are Idref, Iqref in the synchronous reference frame. If the controller operates in the stationary reference, they would be Ialpha and Ibeta. The possible inputs for the outer control loop are: magnitude V_{ac} vs. V_{acref}, V_{dc} vs. V_{dcref}, P vs. P_{ref}, or Q vs. Q_{ref}. The most common used controls for STATCOM application are either regulating ac voltage or regulating reactive power with one variable and regulating the dc bus voltage with the other. The outer control loop is more application specific, whereas most of the applications have the similar inner control loops.

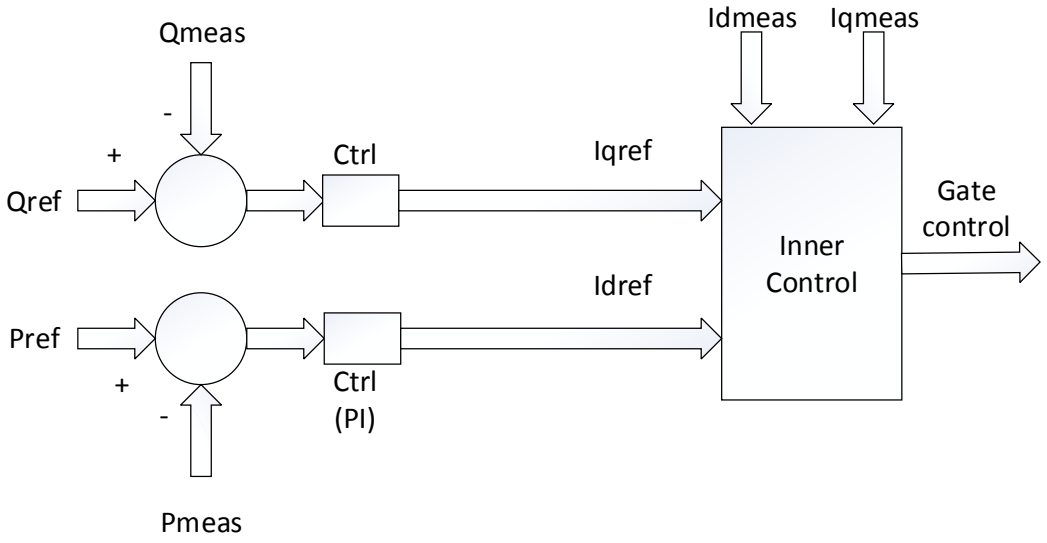

Figure 2.4: Outer Control Loop for the VSC

One can use algebraic equations or a proportional integral (PI) control to determine Idref from error between Pref and Pmeas, or Iqref from Qref and Qmeas. If the VSC is implemented with a direct voltage control scheme, it is possible to control two separate quantities simultaneously. Usually dc voltage or injected real power are used to set either Idref or Iqref, and the other current reference is set by an outer control loop regulating |Vac|. The control diagram for the outer controller is shown in Figure 2.4. Besides a PI controller, there are other ways to implement this controller described in the literature as well.

2.2.3 Phase Locked Loop

A phase locked loop (PLL) is used to synchronize the converter control with the ac line voltage. It is also used to compute the transformation angle used in the dq transformation to the synchronous reference frame. A phase locked loop block measures the system frequency and it provides the synchronous reference phase angle θ(t) for the dq transformations block. An ideal PLL can provide the fast and accurate synchronization information with a high degree of immunity and insensitivity to disturbances, harmonics, unbalances, sags/swells, notches and other types of distortions in the input signal [2].

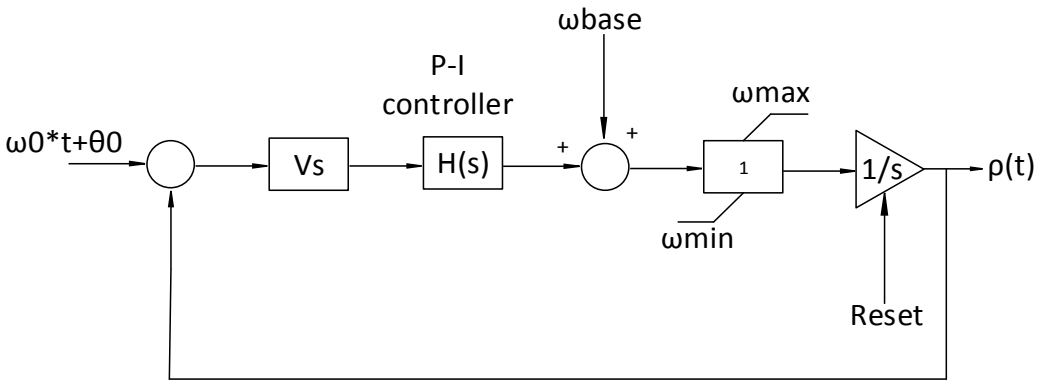

Figure 2.5: Basic Control Diagram of the PLL

The output of the phase locked loop is the phase angle as a function of time of the grid voltage which is used to synchronize the output current of the converter with the voltage at the point of common coupling (PCC) with the system. One can easily monitor the grid voltage parameters such as amplitude and frequency using the PLL. As seen in Figure 2.5, the PLL is composed of a phase comparator that provides an error signal to the PI controller. A base frequency value is then added to the output of the PI controller biasing the estimated frequency of the grid voltage. The advantage of adding the base frequency to the output of the PI controller is a better dynamic performance every time the intergrator is reset to track the system frequency.

A three phase PLL can be implemented to work with the Park's transformation. The estimated phase angle of the Figure 2.6 shows a three phase PLL utilizing the Park's transformation to the synchronous reference frame. The objective of this is to regulate Vsq, the q-axis component of the voltage at the PCC transformed to the synchronous reference

frame, to zero when synchronized. The PLL synchronizes Vsd to align with the phase A voltage at the point of connection with the grid. This is the type of PLL used in this work.

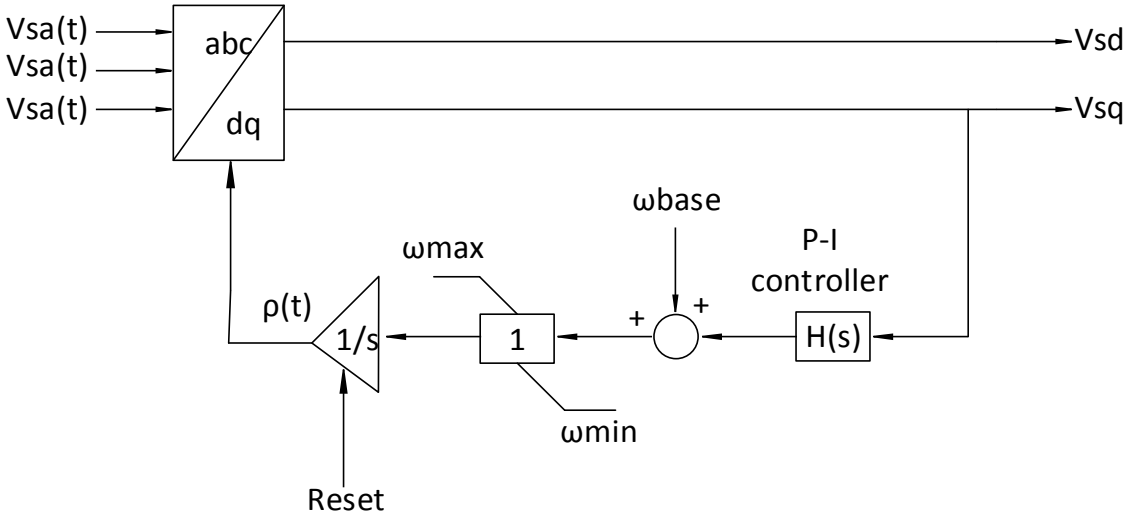

Figure 2.6: Three Phase Implementation of the PLL

2.3 Equivalent Circuit Diagram of the STATCOM

A STATCOM is a VSC (voltage sourced converter) system whose purpose is to exchange the reactive power with the host AC system. For the voltage sourced converter, a single phase bridge (H-bridge) or a three phase bridge (6-pulse or 6-step converter) topologies can be selected. It can be controlled in either the αβ-frame or the dq-frame. The control in this work is implemented in the dq-frame because it is widely used, and a three-phase phase-locked loop (PLL) is used for synchronization with the power system in dq-frame as seen in the Figure 2.7.

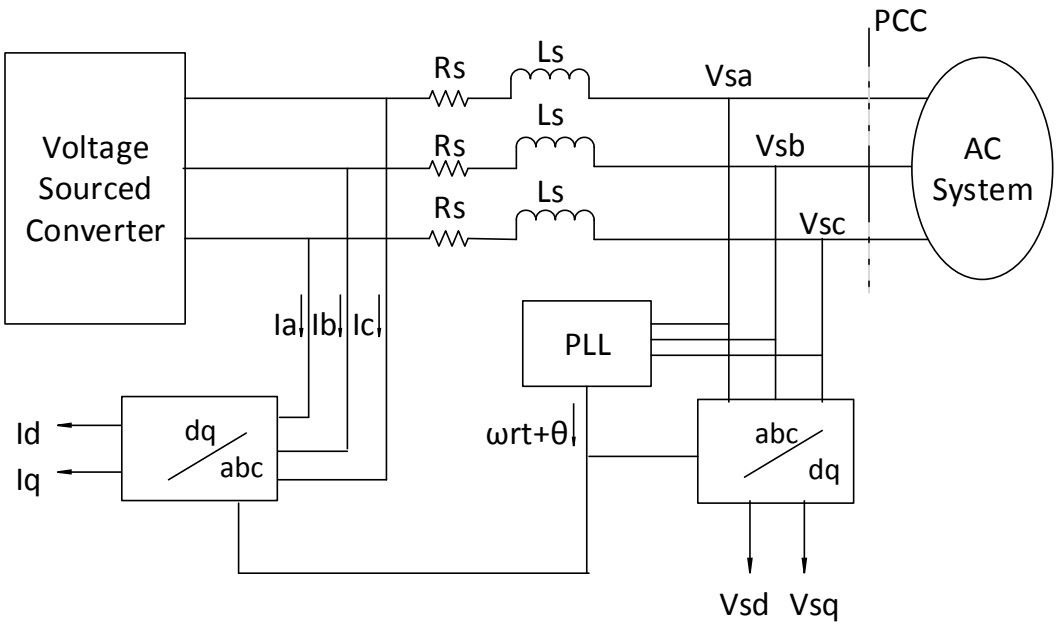

Figure 2.7: Equivalent Circuit Diagram of the STATCOM System

The voltage sourced converter is connected to the AC system through a combined inductance of the line and the interface transformer which is represented by L_s. In Figure 2.7, the STATCOM can be seen as a special case of the controlled DC voltage power port

from [2], where the STATCOM DC-bus voltage, V_{dc} is regulated by controlling the real power exchanged with the rest of the system [2]. In the figure, the electrical node where the STATCOM three ac-side phases are connected to the corresponding phases of the ac system is called the point of common coupling (PCC). It can be seen that the VSC synchronization signals, that is, the PLL inputs, are obtained from the PCC. The reference current and voltage values (Id, Iq, Vsd, and Vsq) are fed back to the controller for the STATCOM. Since the VSC AC side terminal voltages are modulated waveforms and L_s is relatively large, V_{sabc} may include large harmonic voltage distortions that distort both the load voltage and the feedback signals V_{sd} and V_{sq}. Therefore, a three phase series RLC filter can be connected in parallel with the STATCOM at the PCC (not shown in the figure). Each RLC branch is usually tuned to the dominant pulse-width modulation (PWM) side-band harmonic, but the filter also exhibits large impedance at the grid frequency. Therefore, the VSC current harmonics flow through the RLC filter and do not penetrate the grid [2].

2.4 Comparison with SVC

Another option for the reactive power compensation considered for implementation with the AMPS was a Static VAR Compensator (SVC). In the linear operating range, the V-I characteristic and functional compensation capability of the STATCOM and the SVC are similar. But, the basic operating principles of the STATCOM and SVC are different. The STATCOM works as a shunt-connected synchronous voltage source due to the converter based var generator. This is different from the SVC which functions as a shunt-connected, controlled reactive admittance based on thyristor-controlled reactors. Because of the

application flexibility provided by the voltage sourced converter, the STATCOM has superior functional characteristics and better performance at low voltages [1].

The comparisons can be done using various parameters described below,

i) Operating regions of the SVC and STATCOM

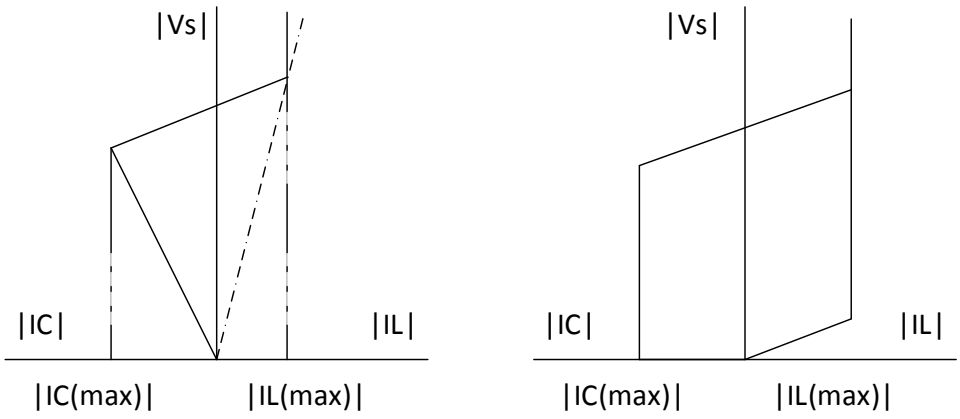

Figure 2.8: Operating Areas of SVC and STATCOM

The typical operating areas of SVC and STATCOM can be seen in Figure 2.8. Note that the maximum reactive current of the SVC in either inductive or capacitive operation is proportional to the network voltage because the SVC is based on passive components once the firing angle limits are reached. The reactive current of the STATCOM is determined by the voltage difference between the network and converter voltages. Also, the maximum reactive current is only limited by the converter device capability and it is independent of the network voltage variation [6]. This is significant in extreme cases, especially during low voltage conditions.

ii) Transient Stability

The ability of the STATCOM to maintain full capacitive output current at low system voltage makes it more effective than SVC in improving the transient stability. The STATCOM is better than SVC in providing voltage support under large system disturbances. The STATCOM has an increased transient rating in both the inductive and capacitive operating regions [1].

iii) Response Time

The STATCOM has better response time than the SVC and better bandwidth of the closed loop voltage regulation as well. This is important for applications requiring fast response, although such applications are relatively rare. This is also the case for typical transmission applications as well. The STATCOM can provide stable operation with better response over a much wider variation of the transmission network impedance than is possible with an SVC [1].

iv) Capability to Temporarily Exchange Real Power

A STATCOM can be used for the applications requiring short term real power compensation, because it can interface dc energy storage with the ac system for real power exchange. The STATCOM is capable of drawing controlled real power from an energy source at its dc terminal and delivering it as ac power to the system. It can also control energy absorption from the ac system to keep the storage device charged. This helps in enhancing the dynamic compensation, improving power system efficiency in the case of steady state generation,

and preventing the power outages [1]. In effect, it provides a STATCOM some ability to provide inertia to the power system, based on the ability to store energy.

v) Operation with unbalanced ac system

The operation of the STATCOM under unbalanced system conditions is different from that of the SVC. If the ac system voltages become unbalanced, then an alternating power component at twice the fundamental frequency will appear at the ac terminals of the STATCOM converter due to the negative sequence voltage and current components, and this will be matched by an alternating second harmonic charging current in the dc terminals, producing in turn an associated alternating voltage component of the same frequency across the capacitor shunting the dc terminals. As a result, the STATCOM will, in general, draw a negative sequence fundamental current component, as well as a third harmonic current component. This is one of the disadvantages of using the STATCOM [1].

vi) Harmonics

We can expect harmonics from both the SVCs and STATCOMs. Network harmonic current distortion occurs from the TCR of an SVC which is harmonic current source. In the case of STATCOM which is a harmonic voltage source, the network voltage harmonic distortion occurs from the voltage division between the STATCOM phase impedance and the network impedance. The major harmonic generation in SVCs is at low frequencies, whereas the STATCOMs have their major harmonic generation at higher frequencies. However, the low

frequency current harmonics from the SVC are easier to filter than high frequency voltage harmonics from the STATCOM [7].

vii) Losses

The losses in the STATCOM are due to the converter bridges which are usually greater than those from the SVC, because the self-commutating semiconductor devices usually have higher conduction losses and switching losses than the thyristors. With advances in the semiconductor industry, STATCOMs are expected to have reduced losses in the future, but will still have lower efficiency that a comparable SVC.

Usually, the most utilities operate SVCs and STATCOMs at close to zero steady-state MVAR output under normal conditions to have the SVCs and STATCOMs available for dynamic voltage support. In these cases, both these devices operate well below 0.5% losses. But, the losses will increase if the operating point is offset from zero. STATCOM manufacturers are moving toward using the modular multilevel converter (MMC) based VSCs, which have lower losses than present designs, although still somewhat more than the SVC [7].

viii) Footprint

The STATCOM is usually preferred for applications with limited substation space, based on the smaller footprint for application because the passive reactive elements are replaced with semiconductor components. The VSCs are built with converter modules in series. Because of this, the STATCOM has a smaller substation footprint than the SVC [7].

ix) Cost

The investment cost of SVCs is lower than that of the STATCOMs. Even though SVC takes more space in a substation compared to STATCOM, the cost of SVC is 70-80% less than that of STATCOM. This is one of the reasons that most new orders are still SVCs and not STATCOMs. The cost of the semiconductor devices used in VSC schemes must come down for the overall cost of the STATCOM to become lower [7].

This project will use a STATCOM to provide more flexibility for classroom and research applications. In addition, at lab scale voltage and current ratings, a STATCOM is less expensive than a SVC.

Chapter 3

Lab Applications of the STATCOM

3.1 The UI Analog Model Power System

The Analog Model Power System (AMPS), which is located at the University of Idaho, is a controlled hardware environment with which engineers can intentionally create and observe real electrical faults on a scale model power distribution system. Power electronic converter based FACTS devices, custom power devices and energy storage devices can be interfaced with the AMPS. The AMPS includes the main elements of a commercial electrical grid, such as lines, sources, transformers, loads, instrumentation, and protection. It was designed and built by Idaho Power Company to enable its protection engineers to analyze portions of its grid for protection scheme development, and later donated to the University of Idaho [8].

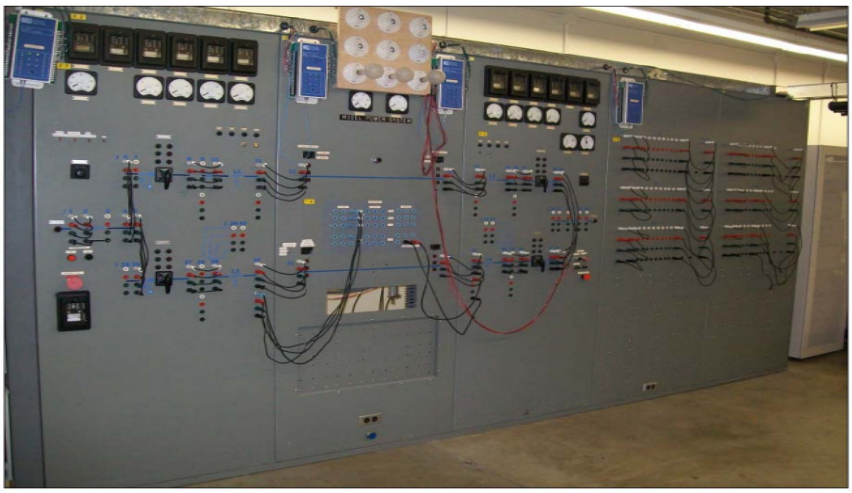

Figure 3.1: The UI Analog Model Power System

As seen in Figure 3.2, there are four line sections in the AMPS. These lines can be connected in various configurations to create different power system models. Each of the four lines on AMPS has separate 3 pole circuit breaker, current transformer and potential transformer. Each line has total line impedance of 1+j10 ohms. The line impedance can be varied with steps of 10% by changing the position of the tap 3 connections on panels 5F and 6F of the AMPS. Each of the four current transformers (CT) has current transformation ratios of 2:1. The voltage transformation ratios for the potential transformers (PT) on lines L2 and L4 are 2:1, while the potential transformers (PT) on lines L1 and L3 have transformation ratios of 1.732:1 [9].

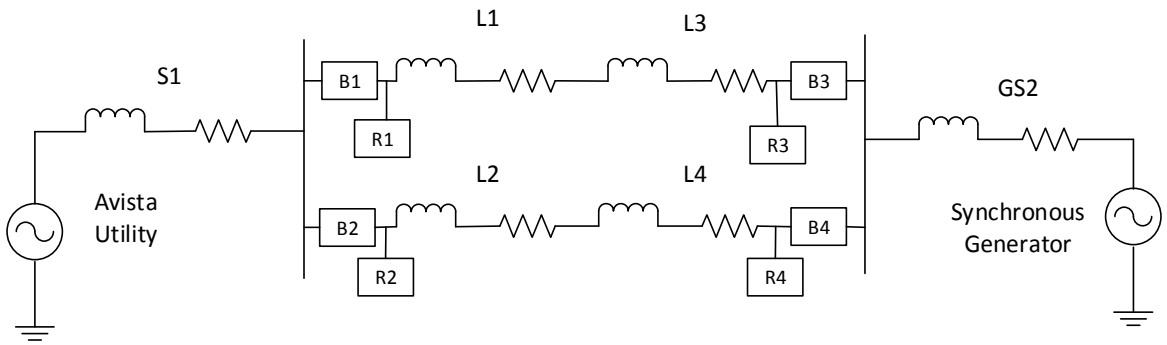

Figure 3.2: Analog Model Power System Circuit Diagram

3.2 Alternate Transients Program

The Alternate Transients Program (ATP) is a universal program system for digital simulation of transient phenomena of electromagnetic as well as electromechanical nature. With this digital program, complex networks and control systems of arbitrary structure can be simulated. ATP has extensive modeling capabilities and additional important features besides the computation of transients [10].

ATP was developed by Dr. W Scott Meyer and Tsu-huei Liu, the co-Chairmen of the Canadian/American EMTP User Group. ATP dates back to 1984 when Dr. Meyer and Dr. Liu did not approve of the proposed commercialization of the BPA (Bonneville Power Administration) EMTP by EPRI (Electric Power Research Institute) DCG (development coordination group). Dr. Liu resigned as DCG Chairman, and Dr. Meyer, using his personal time, started a new program from a copy of BPA's public domain EMTP. ATP is not in public domain, and therefore licensing is required to use it [10].

ATPDraw is a graphical preprocessor for ATP on the MS Windows platform. The program handles node names and creates the ATP input file based on “what you see is what you get”. It has all types of editing operations and has more than 100 standard components and 40 TACS objects are available, and in addition the user can create new objects based on MODELS. The main windows are main menu, toolbar, side bar, header, circuit windows, circuit map, and component selection menu. The file types in ATPDraw are the project file (with file extension acp) which contains all circuit data, support file (sup) which contains component definitions, data file (alc/bct/xfm) which contains special data, and help file (sup/txt) which contains user specified help text. The project is stored in a single binary file (*.acp). Under the ATP options, the settings such as simulation time step, unit specification options for capacitances and inductances, setting for frequency scans and output format, load flow output settings can be specified. The user can inspect the .atp and .lis files to see how the program performed and check for the errors if the program did not run successfully [11].

3.3 ATP Model of the UI AMPS

An ATP Model for the UI Analog Model Power System, shown in Figure 3.3, was developed by Mike Staihar in his master's thesis. To run this model, make sure that the punch (.pch) files associated with each block are placed in the appropriate path specified in each of the corresponding blocks. These pch files can be found in the usp folder of the ATPDraw directory. Figure 3.3 shows an example configuration of the AMPS.

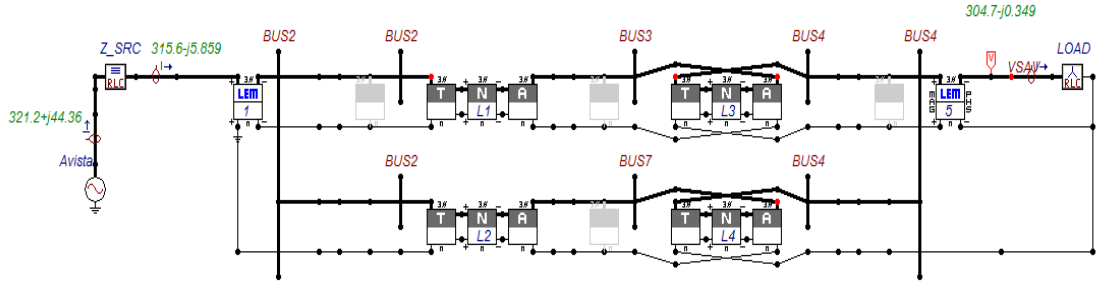

Figure 3.3: ATP Model of the UI AMPS

In this model of the AMPS, the Avista power supply is modeled as the ideal 3 phase AC voltage source, and the motor generator set is modeled the same as well. Each transmission line is modeled using the three sections, T, N, and A. The T section models fixed capacitors connected in A, B, and C phases to represent the coupled capacitances at one end of the pi section, the resistance in the leads connecting line section T to the panel jacks and the series capacitors, which can be bypassed when not needed. The N section models the resistance of the 10-tap position inductors in phases A, B, C, and the neutral, the series inductance of the 10-tap inductors in phases A, B, C, and the neutral, and the shunt capacitor bank adjacent to the 10-tap inductors for the other end of the pi section. Line section A is used to model the four winding transformer that provides phase to phase

mutual coupling. The AMPS transmission line model uses a multi-ratio current transformer (CT) to provide inductive coupling between phases A, B, C, and neutral [12].

The AMPS data acquisition system in the lab has an option to obtain voltage and current data from one to three instrumentation units which use components manufactured by LEM Instruments Inc. Each instrumentation unit is referred to as a LEM. A LEM is used to monitor system currents and voltages at a specific location of interest, and it can be moved and reconnected to another location as well. A unique number is assigned to each instrumentation module added to the network via the ATPDraw data window. This module number is used to distinguish output variables in a PL4 file, from different modules. A six character TACS variable name is assigned to voltage and current output from an ATP instrumentation module. The first three characters are 'LEM', the fourth character is a user defined LEM number, and the fifth and sixth characters identify phases for LL voltages. For currents, the fifth character is 'I', and the sixth character is the phase [12].

For simulating the faults in the AMPS, phase fault simulator with data output can be used to provide an ATP model for a 3-phase shunt fault simulator. The AMPS has a switch and resistor network used to simulate faults on the four 3-phase transmission/distribution lines. The phase fault simulator can be used to simulate phase-to-phase (AB, BC, CA), phase-to-neutral (NA, NB, NC), and phase-to-ground faults (GA, GB, GC) on a transmission line. These faults can be initiated individually or in a combination to produce three phase, line-to-line, double-line-to-ground, or single line to ground faults. The fault initiation time is specified by the user, and any combination of faults can be initiated or cleared at any given time during

the simulation. The fault resistances are constant in time and user specified, and fault currents for this device can be saved to a PL4 file [12].

Chapter 4

Modeling of the STATCOM

The approach for modeling the STATCOM was to start simple, then add more pieces, and test them at each step. The first step for the modeling was to create an AC system equivalent of the STATCOM interfaced to the AMPS model and verify against the known conditions. The initial power converter model is a simple, non-switching version which employs open-loop controls with predetermined inputs having known impacts on system. The next phase was to start adding more detail to the controls.

Once the controls were tested, the next part of the modeling was to build a switching model for the converter. Again, this starts with open loop controls with very simple AC/DC systems. Then the results are compared to results for the non-switched converter. It is important to make sure the system reaches steady state before applying any disturbances. Once the switching model is validated, the next step is to add more complexity in controls and synchronization.

4.1 Averaged Models of the STATCOM

Even though, the switched model may accurately describe the steady-state and dynamic behavior of the converter, the relationships between the modulating signal (which is the main control variable), and the current and voltage variables cannot be easily understood from the switched model. Also, for the dynamic analysis and control design purposes, knowledge about the high frequency details of variables is often not necessary. This is

because the compensators and filters in a closed-loop control system usually exhibit low-pass characteristics and they do not react significantly to high-frequency components. In addition, the high frequency behavior does not propagate very far into the system. For these reasons, the dynamics of the average values of variables are of more interest, rather than in the dynamics of the instantaneous values. Also, an averaged model enables description of the converter dynamics as a function of the modulating signal. The averaged model for a single phase STATCOM as implemented in ATPDraw is shown in the Figure 4.1 [2].

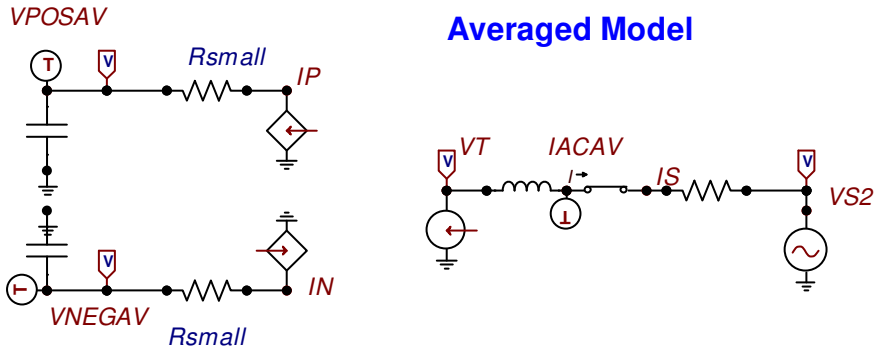

Figure 4.1: Averaged Model of the Single Phase STATCOM Implemented in ATP

For the averaged model, the switching is replaced with the dc side controlled current sources IP and IN such that,

$$i_n = \left(\frac{1-m}{2}\right)\cdot i \qquad (4.1)$$

$$i_p = \left(\frac{1+m}{2}\right)\cdot i \tag{4.2}$$

In equations (4.1) and (4.2), i_p and i_n represent IP and IN in Figure 4.1 and i is the current flowing in the AC side of the STATCOM. The modulating function, m, can be a constant, quasi dc value or a sinusoidal reference such that,

$$m = \sqrt{2}\cdot|V|\cos(\omega t + \delta) \tag{4.3}$$

The ac equivalent for the converter is a controlled voltage source as shown in Figure 4.1. The equation driving this source will be described below. More information on this can be found in [2].

The single phase averaged model can be expanded to the three phase as shown in Figure 4.2. In this case there are three half bridges in which the switches are modeled by three sets of current sources.

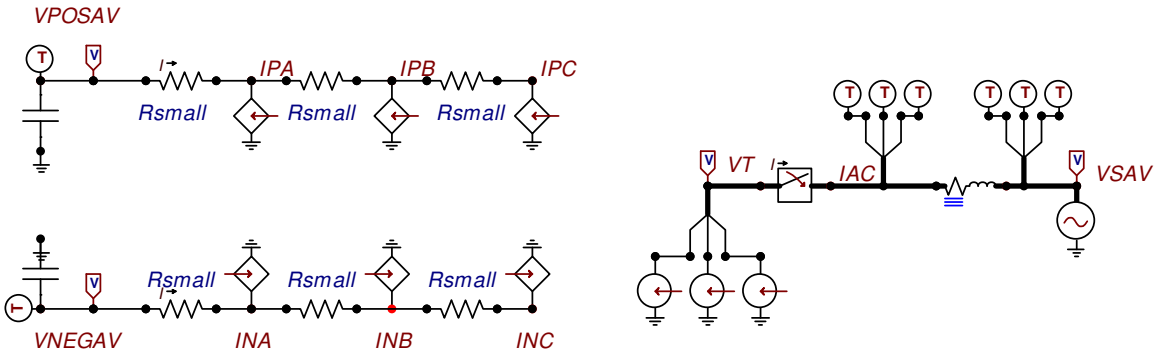

Figure 4.2: Averaged Model of the Three Phase STATCOM Implemented in ATP

4.1.1 Generating Modulating Functions

The open loop modulating functions, m_a, m_b, and m_c are calculated as shown in the Figure 4.3. Equation (4.4) shows the calculation for phase A. Similar equations will be used for phases B and C, with appropriate phase shifts.

$$MA(t) = MAGM \cdot \cos(\omega \cdot t - \delta) \tag{4.4}$$

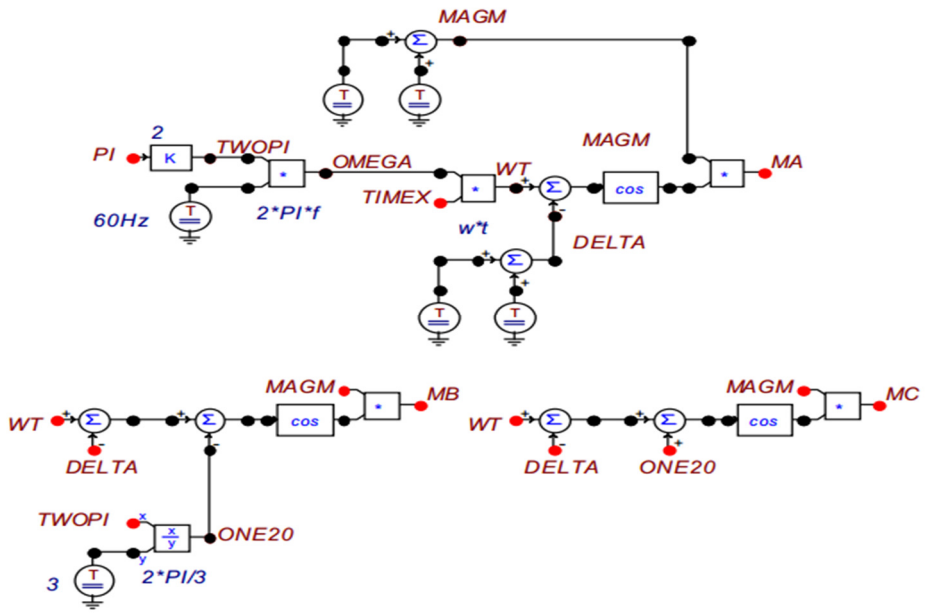

Figure 4.3: Generation of the Modulating Functions for the Open Loop Control.

The circuit in Figure 4.3 has two sets of sources for the magnitude and two for the angle. The first source for the magnitude specifies the initial magnitude of MA. The second source specifies the change in the magnitude after 0.05 seconds. For determining the angular frequency, omega, the built in constant PI is used and it is multiplied with the frequency, and then multiplied with current simulation runtime function TIMEX. After that the delta

value is subtracted which is specified in radians. Then it is multiplied with the cosine and multiplied with the magnitude to get the MA function.

4.1.2 Three Phase Model Voltage and Current Commands

As seen in Figure 4.4, the open loop modulating controls commands were developed for controlling the voltages and the currents. The currents Ip and In are found as described by equations (4.1) and (4.2). Similarly, the terminal voltages for each phase are found using equation (4-5).

$$V_T = \frac{m \cdot V_{DC}}{2} \tag{4.5}$$

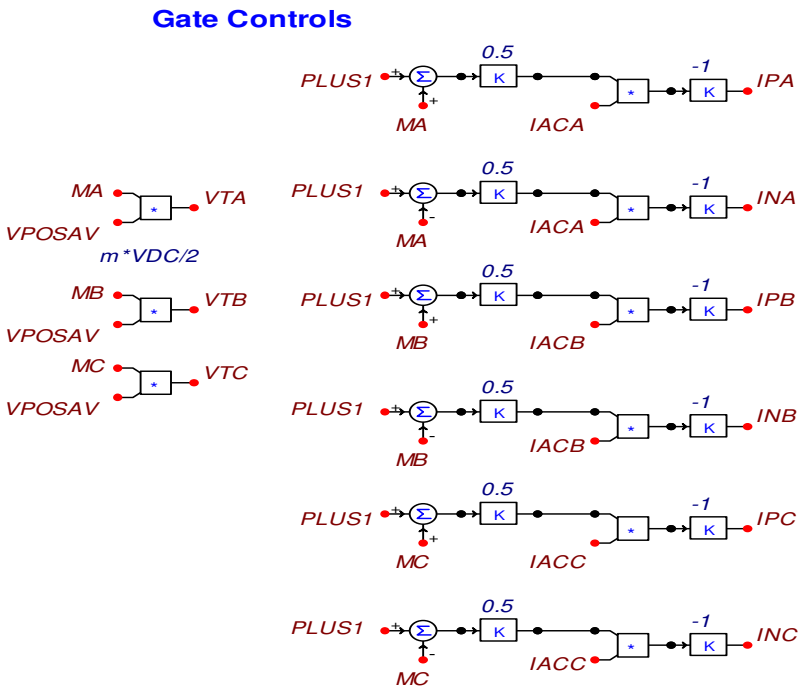

Figure 4.4: Open Loop Control Commands for the STATCOM in ATP

4.2 Switching Models of the STATCOM

A switching model of the single leg dc power pole is implemented in the ATP as shown in Figure 4.5. The switches/IGBTs are represented with the controlled switches in the ATP. The capacitors are represented with the DC voltage sources for now, and the switched DC port is connected to the system through a resistance, and inductance values as shown in the circuit.

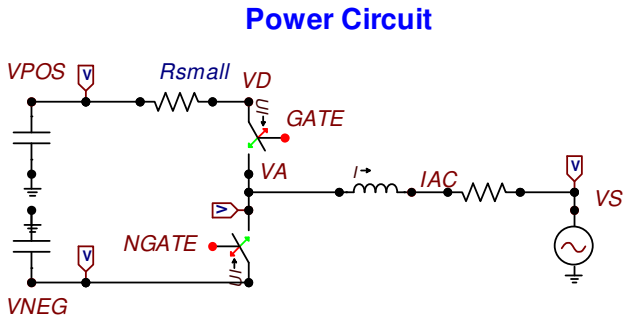

Figure 4.5: Single Phase VSC Switching Model in ATP

As in the case of the averaged models, the single phase switching model can be extended to three phase models, with three sets of the switches working together as shown in Figure 4.6.

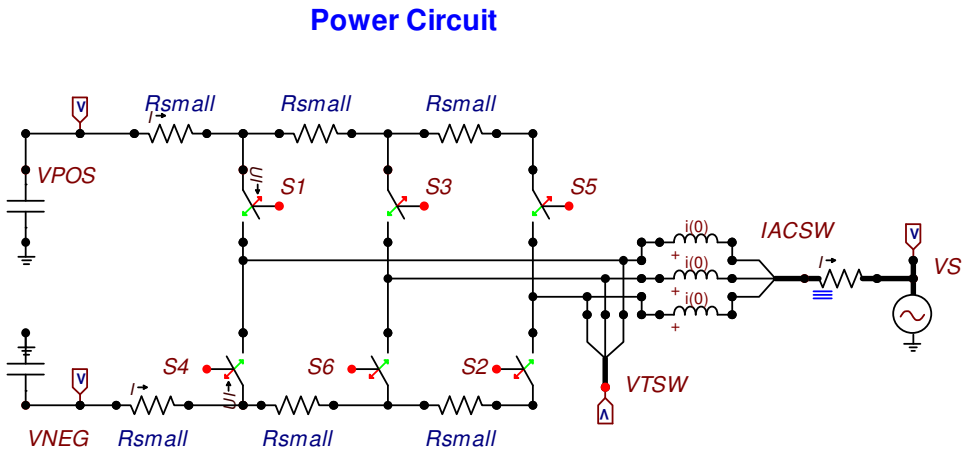

Fig 4.6: Three Phase VSC Switching Model Implemented in ATP

4.2.1 Sine Triangle Comparator for the Switching Models

To control the switching devices, a sine triangle comparator was used, as seen in Figure 4.7. A triangle wave was generated at the carrier frequency which varies in amplitude from -1 to 1. Then the comparator compares the triangle wave to the modulating function. The comparator will output +1 or -1 depending upon whether the modulating function or the triangle wave is bigger. Then the output will turn on the gate pulse of the upper device and the output is inverted to turn on the lower device in the switching model.

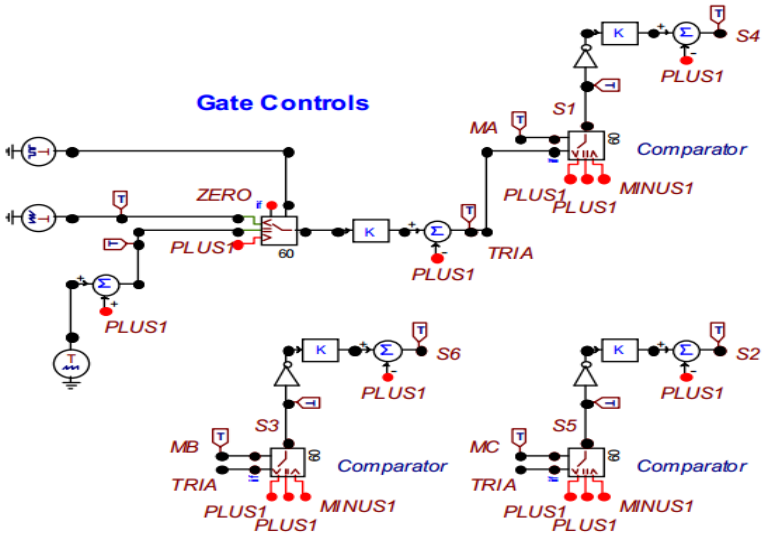

Figure 4.7: Sine Triangle Comparator for the Switching Model in ATP

4.3 Closed Loop Control of the STATCOM

The closed loop control in the dq reference frame uses I_{dref} and I_{qref} as inputs to the PI controller as seen in Figure 4.8. First, the three phase real power is calculated in the synchronous reference frame in (4.6). Since the converter is ungrounded on the ac side, i_0=0.

$$P = \frac{3}{2}\cdot\left(V_{sd}\cdot i_q + V_{sq}\cdot i_q + V_o\cdot i_o\right) \tag{4.6}$$

The reference from PLL is chosen such that the V_{sq} = 0. So i_{dref} can be calculated as,,

$$i_{dref} = \frac{2}{3}\cdot\frac{P_{ref}}{V_{sd}} \tag{4.7}$$

Similarly, reactive power can be calculated as,

$$Q = \frac{3}{2}\cdot\left(V_{sq}\cdot i_d - V_{sd}\cdot i_q\right) \tag{4.8}$$

Again, $V_{sq}*i_d=0$ so this gives,

$$i_{qref} = \frac{-2}{3}\cdot\frac{Q_{ref}}{V_{sd}} \tag{4.9}$$

There are two parts separate PI controller loops, one for the direct axis current and one for the quadrature axis current. The output of each PI controller goes to a summing junction. One of the inputs to the summing junction is a cross-coupling term that multiplies the current from the other axis component times w0*L. This term corrects an inherent cross-coupling term from the system. The other part is the voltage feed forward term provided by the d and q axis voltages which helps in tracking the current. The proportional gain and integral gain constants (k_p and k_i) are specific to the system. From this closed loop control scheme the modulating functions in the dq reference frame can be found which can be converted to αβ and finally to ABC reference frame. The values k_p and k_i can be found as shown in the equations (4.10) and (4.11), where T_i is the time constant of the resultant closed-loop system.

$$k_p = \frac{L}{T_i} \tag{4.10}$$

$$k_i = \frac{R + r_{on}}{T_i} \tag{4.11}$$

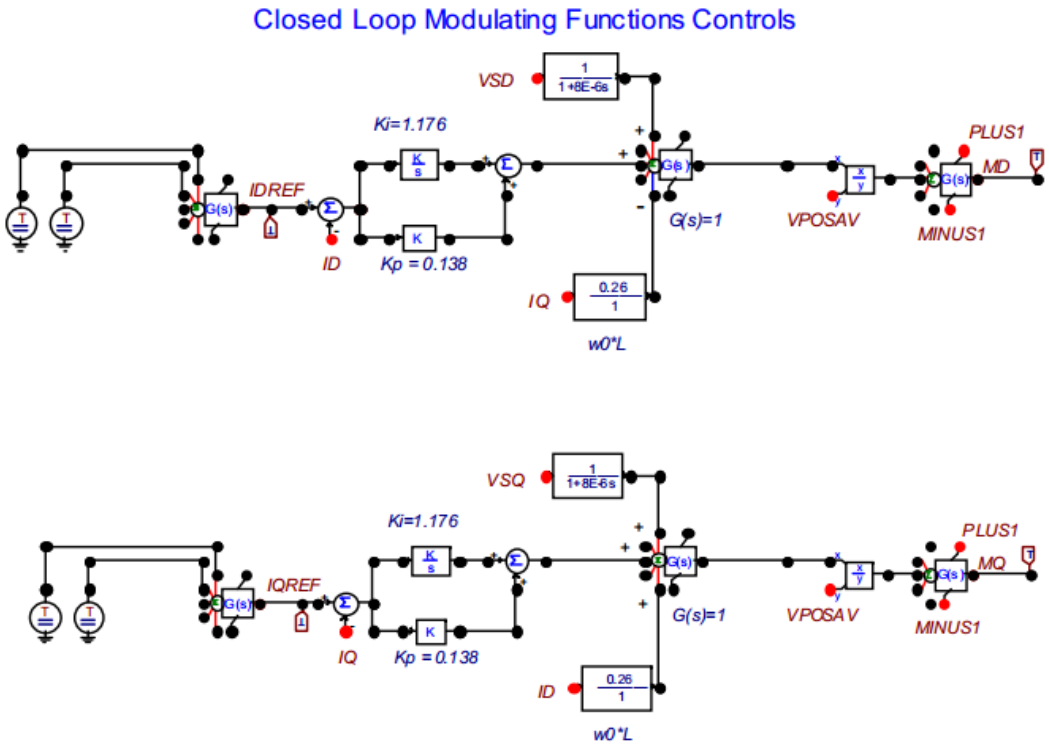

Figure 4.8: Closed Loop Control Diagram for the STATCOM

4.3.1 Outer control loop for the STATCOM

The outer control loop for the STATCOM consists of a reactive power controller and a DC voltage controller as seen from Figure 4.9. The outputs of the outer control loop are Iqref and Idref which is then used in the inner controls.

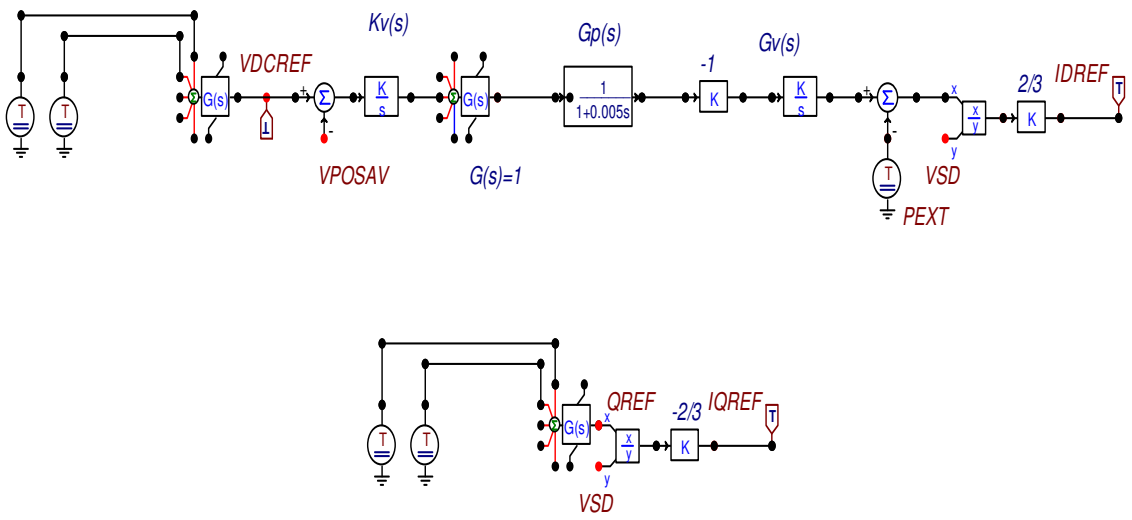

Figure 4.9: Outer Control Loop for the STATCOM

The DC voltage controller is used to regulate the DC bus voltage. As shown in Figure 4.9, VDCREF is compared with the VDC, then the error signal is processed by the compensator Kv(S), and the command IDREF is issued for the real power controller. The closed-loop system is composed of the compensator Kv(s), real power controller Gp(s), and control plant Gv(s) and the loop gain can be found from equation (4.12). More information about the compensator design can be found in [2].

$$l(s) = -K_v(s)\cdot G_p(s)\cdot G_v(s) \tag{4.12}$$

where,

$$K_v(s) = N(s)\cdot\frac{k_0}{s} \tag{4.13}$$

$$G_p(s) = G_i(s) = \frac{1}{\tau_i\cdot s + 1} \tag{4.14}$$

$$G_V(s) = \frac{-2}{C} \cdot \frac{\tau \cdot s + 1}{s} \tag{4.15}$$

Since, we are regulating the output real power of the STATCOM to be zero, this research focuses more on the reactive power controller. As can be seen from Figure 4.9, the reference value for the output reactive power is provided to the outer control loop. Then the value for Iqref is calculated using equation (4.9), which is then sent as an input to the inner control loop of the STATCOM. Therefore, we can decide the amount of the reactive power to be supplied to or from the system by the STATCOM. This can also be replaced by an ac voltage magnitude regulator.

4.4 Measurement of the output power

For calculating the converter output power, first the voltages and currents are changed to the alpha beta domain, and then changed to the synchronous dq domain as shown. The abc reference frame quantities are transferred to the alpha-beta reference frame using equation (4.12).

$$\begin{pmatrix} V_\alpha \\ V_\beta \\ V_0 \end{pmatrix} = \sqrt{\frac{2}{3}} \cdot \begin{pmatrix} 1 & \frac{-1}{2} & \frac{-1}{2} \\ 0 & \frac{\sqrt{3}}{2} & \frac{-\sqrt{3}}{2} \\ \frac{1}{\sqrt{2}} & \frac{1}{\sqrt{2}} & \frac{1}{\sqrt{2}} \end{pmatrix} \cdot \begin{pmatrix} V_a \\ V_b \\ V_c \end{pmatrix} \tag{4.12}$$

The alpha beta reference frame quantities are then changed in the dq reference frame using equation (4.13).

$$\begin{pmatrix} V_d \\ V_q \\ V_0 \end{pmatrix} = \begin{pmatrix} \cos(\theta) & \sin(\theta) & 0 \\ -\sin(\theta) & \cos(\theta) & 0 \\ 0 & 0 & 1 \end{pmatrix} \cdot \begin{pmatrix} V_\alpha \\ V_\beta \\ V_0 \end{pmatrix} \tag{4.13}$$

The transformation from the abc reference frame to the dq reference frame can be seen in equation (4.14).

$$\begin{pmatrix} V_d \\ V_q \\ V_0 \end{pmatrix} = \sqrt{\frac{2}{3}} \cdot \begin{pmatrix} \cos(\theta) & \cos\left(\theta - \frac{2\cdot\pi}{3}\right) & \cos\left(\theta + \frac{2\cdot\pi}{3}\right) \\ -\sin(\theta) & -\sin\left(\theta - \frac{2\cdot\pi}{3}\right) & -\sin\left(\theta + \frac{2\cdot\pi}{3}\right) \\ \frac{1}{\sqrt{2}} & \frac{1}{\sqrt{2}} & \frac{1}{\sqrt{2}} \end{pmatrix} \cdot \begin{pmatrix} V_a \\ V_b \\ V_c \end{pmatrix} \tag{4.14}$$

These equations for transferring the abc reference frame quantities to the dq reference frame are implemented in ATP as seen in the Figure 4.10.

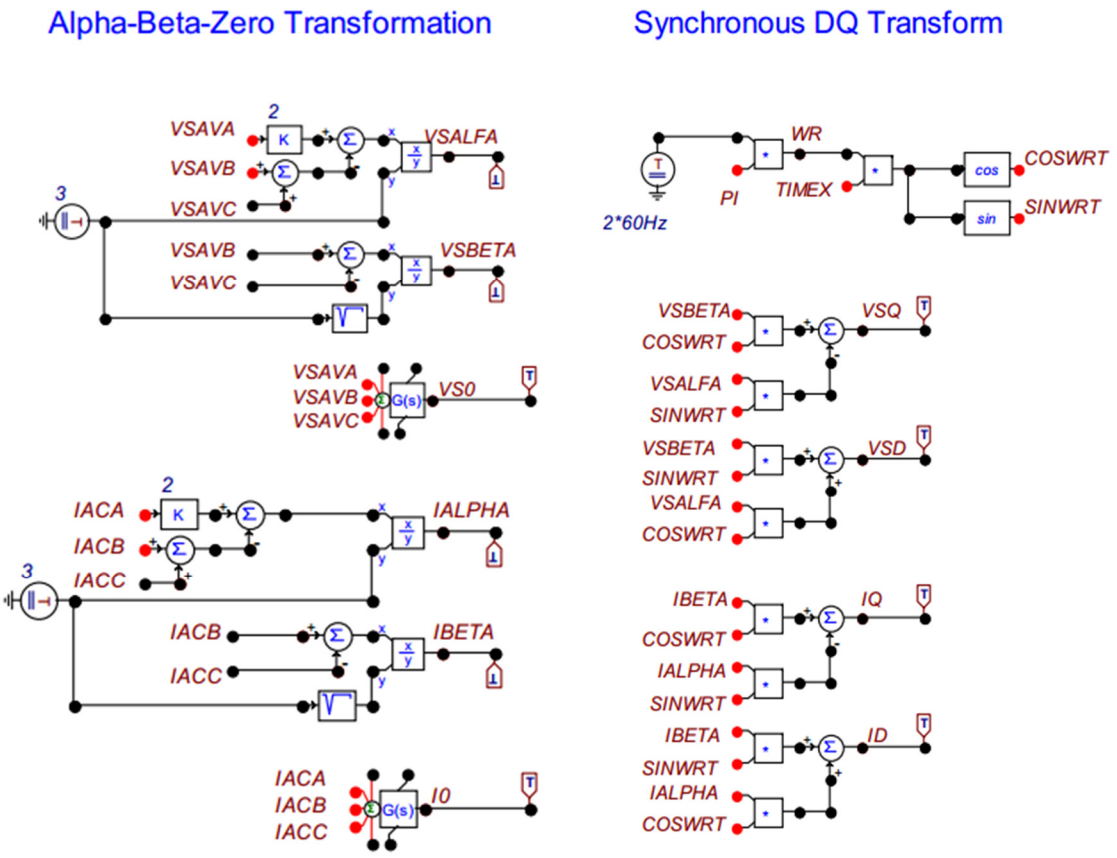

Figure 4.10: a) Alpha-Beta Transformation b) Synchronous dq Transformation

4.4.1 Calculations of P and Q at PCC

After calculating the Vsd and Vsq values from the synchronous dq transformation, equations (4.6) and (4.8) are used to calculate the output power P and Q at the point of common coupling, as shown in Figure 4.11.

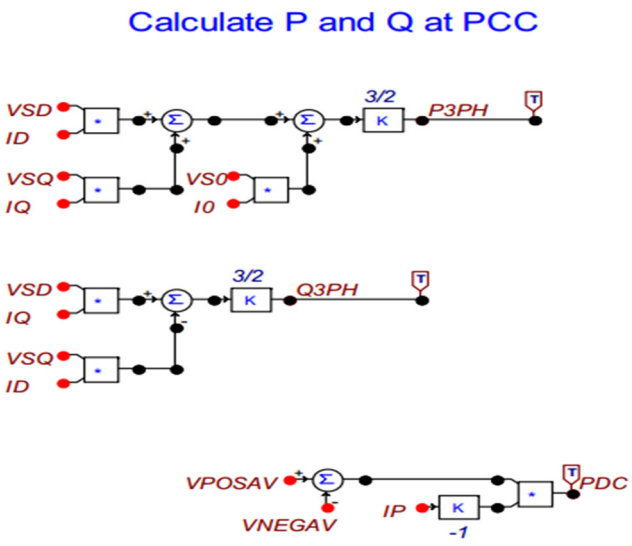

Figure 4.11: Calculations of the Real and Reactive Power in the Synchronous Reference Frame

4.5 Phase Locked Loop

The phase locked loop circuit shown in the Figure 4.12 is used to synchronize the STATCOM with the power system voltages. The phase locked loop keeps the track of the power system currents and voltages and is used to keep the STATCOM voltages in phase with the system voltages. The phase locked loop plays important role in grid connected power electronics system. A good PLL system can detect the grid phase angle and frequency fast and accurately, and additionally it can extract the positive sequence exactly [13]. As described in Figure 2.5 and Figure 2.6, the output of the PLL is the phase angle as a function of time. The PLL is composed of a phase comparator that provides an error signal to the PI controller. A base frequency value is then added to the output of the PI controller resulting in the estimated frequency of the grid voltage.

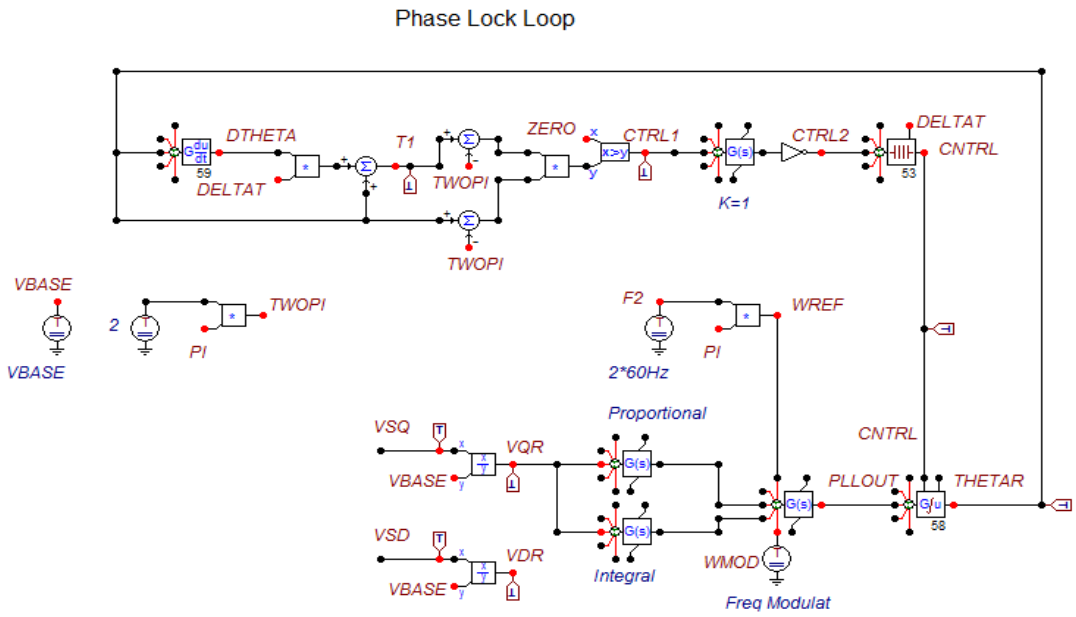

Figure 4.12: Phase Locked loop to Synchronize the System and STATCOM Voltages as Implemented in ATP.

Chapter 5

Simulation Results

Different control scenarios were used to test the STATCOM with the AMPS model. These scenarios were based on the ones that could be done with a hardware implementation of a STATCOM on the AMPS. The first scenario used open loop control and was conducted with the averaged converter models. The goal for the simulation was to vary the reactive power provided by the STATCOM from -200VAR to 300VAR. The modulating functions ma, mb, and mc values calculated from the power flow calculations were used in the open loop controls. The open loop model was simulated and results were analyzed in comparison to the required reactive power values.

The second set of simulations used a closed loop control scheme and tried to vary the reactive power from -200VAR to 300VAR, as was done in the open loop tests. The performance of the closed loop control was compared to the open loop control in getting the required reactive power to the system. The values for the Qref and Iqref to provide the required amount of the reactive power were determined as well.

In the third case, the load impedances were varied using different resistances, capacitances, and inductances values, which matched the values of the resistive, capacitive, and inductive load banks available in the lab. From the simulation results, the controller was able to maintain the phase voltages at the required level, and it was possible to determine the required reactive power.

In the fourth case, the line length was varied and the STATCOM was controlled to provide reactive support to the AC system to support the power transfer to maintain the voltage. The line impedances were varied from 10% to 100% for all the lines in the analog model power system. The amount of reactive power compensation required provided by STATCOM to maintain the voltage at the point-of-interconnect as the line lengths were varied was analyzed.

Several fault cases that can be implemented in the AMPS were simulated in the fifth case, and the STATCOM was used to provide the reactive power support to the point-of-interconnection with AMPS using the closed loop controls. Again the goal was to find the necessary parameters for the STATCOM control system to provide reactive compensation to maintain |V| for different fault scenarios.

Finally, the ability of the STATCOM to provide voltage support in a case with imbalances in the power system was tested. To create the imbalances, unbalanced loads were applied, and the STATCOM was used to provide the reactive power to the system. The effect of the variation of the Qref values in the voltages and currents in the unbalanced system were analyzed in this case.

The parameters used for the simulation in ATP can be seen in Table 5.1.

Table 5.1: ATP Parameters Used in the Simulations

Parameter	Values
Fundamental Frequency	60 Hz
Switching Frequency	5 kHz
AMPS Source Voltage	173.6 V
STATCOM DC Capacitors	81.19 uF
STATCOM AC Line Resistance	0.096 ohms
STATCOM AC Inductance	10.133 mH
STATCOM DC Side Resistance	1E-8 ohms

5.1 Case I Open Loop Tests

The first test case used the averaged model of the STATCOM utilizing the open loop control strategies discussed in the modeling of the STATCOM in Section 4. The results should not be as clean as will be seen with the closed loop controls. As seen in Figure 5.1, the STATCOM was set to provide 100VAR of the reactive power, but actually produced 94.39 VAR from the open loop control. The output voltage and the output current of the STATCOM at the PCC can be seen from Figure 5.2 and 5.3. The phase A voltage was measured to be 121.9V and the phase A current was measured to be 2.421 A.

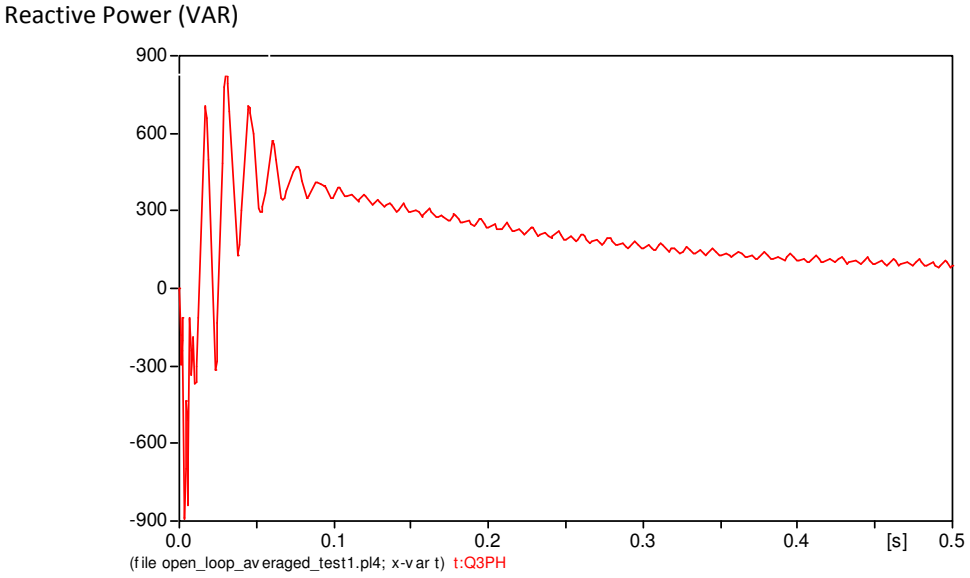

Figure 5.1: Output Reactive Power from the Open Loop Test

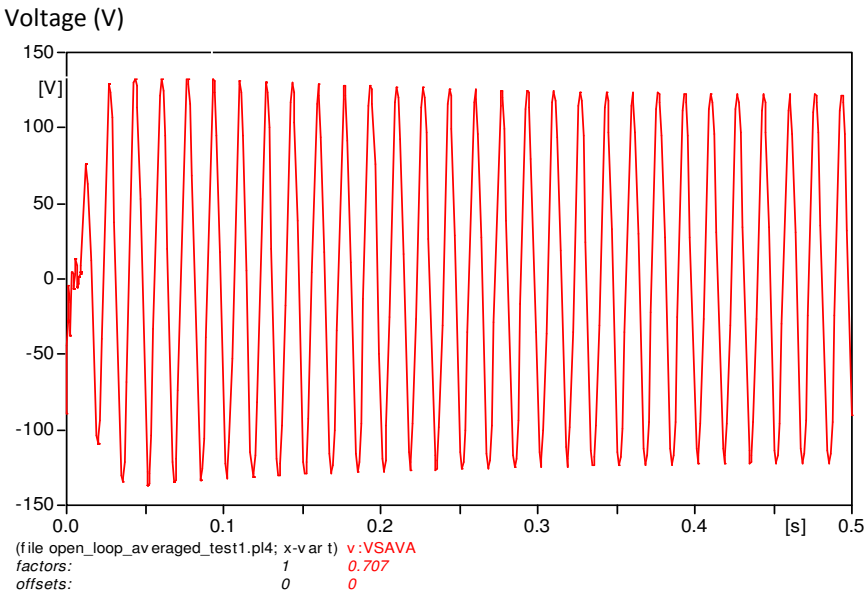

Figure 5.2: Output Voltage from the Open Loop Test

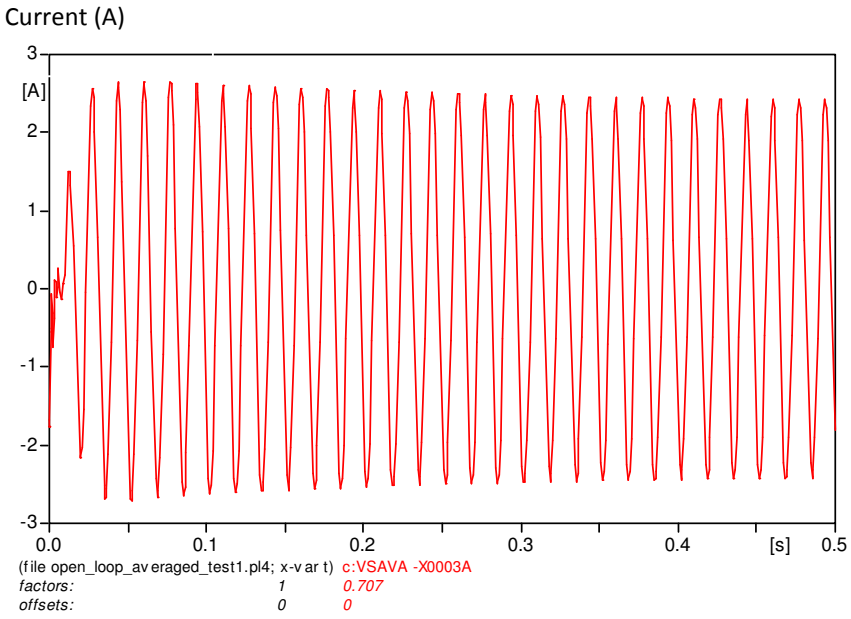

Figure 5.3: Output Current from the Open Loop Test

Similarly, the ability of the STATCOM to provide 100VAR was tested with the switching model as well. The switching frequency of the STATCOM was set to 5kHz. After simulating the switching model, the output reactive power of the STATCOM was measured to be

97.54VAR and the output voltage was measured to be 122.5V which was close to the values from the averaged model. The reactive power supplied and the output voltage from the switching model can be seen from Figure 5.4 and Figure 5.5 respectively.

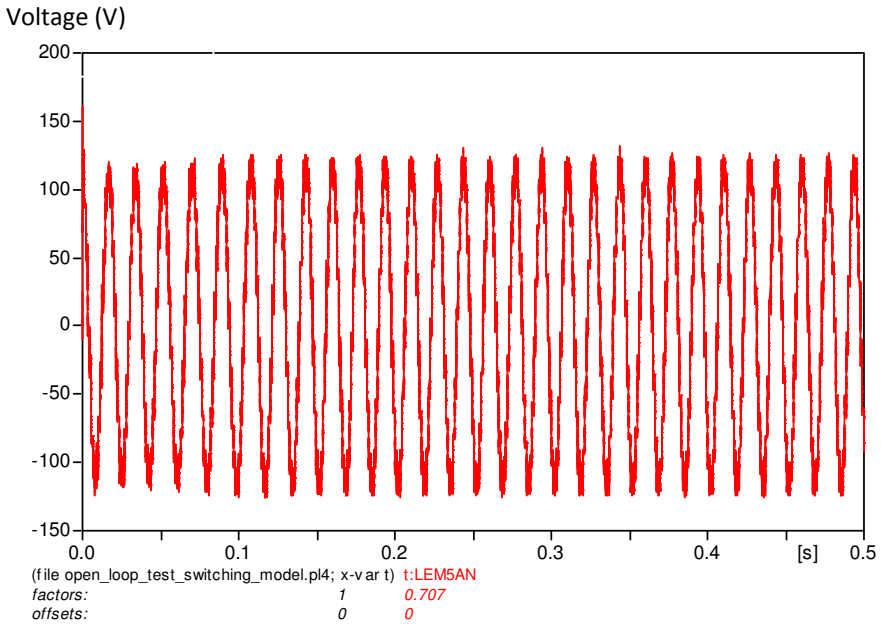

Figure 5.4: Output Voltage from the Switching Model

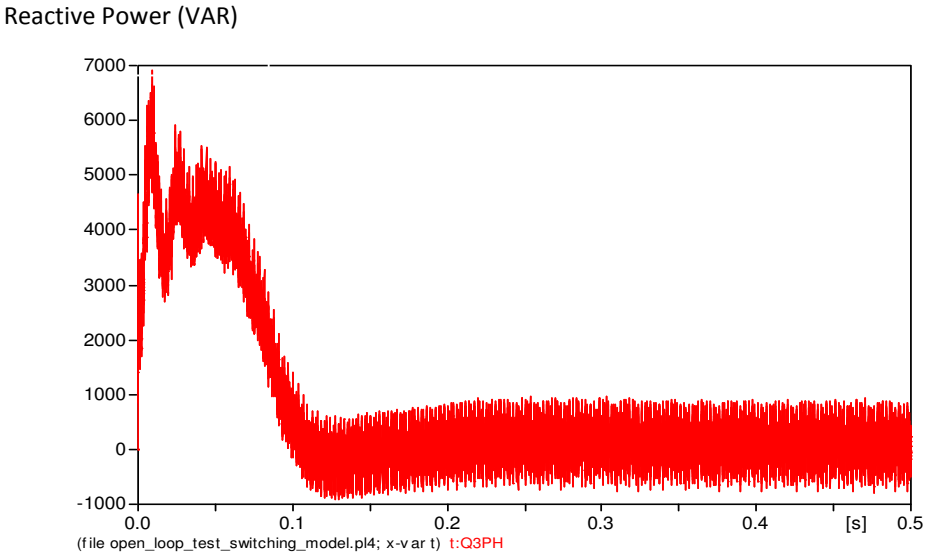

Figure 5.5: Output Reactive Power from the Switching Model

The results from the variation of the reactive power from -200VAR to 300VAR are shown in Table 5.2. The modulating function values were calculated from the power flow calculations, and the output voltages and currents were measured at the point of interconnection. Figure 5.6 shows how well the results from the open loop test performed to the expected values. Although, there was some increase in the reactive power supplied with the increase in the modulating function values, the supplied reactive power was not close to the required values because of the lack of the closed loop that would track the changes in the |V|. The closed loop control is expected to produce better results.

Table 5.2: Case I Open Loop Test Results

Required reactive power (VAR)	Modulating function |Ma|	Output Currents (A)	Output Voltages (V)	Reactive Power Supplied (VAR)
-200	0.783	2.225	112.2	-135.6
-100	0.789	2.296	115.7	-56.9
100	0.8	2.421	121.9	94.39
200	0.806	2.474	124.5	166.9
300	0.811	2.534	127.6	246.1

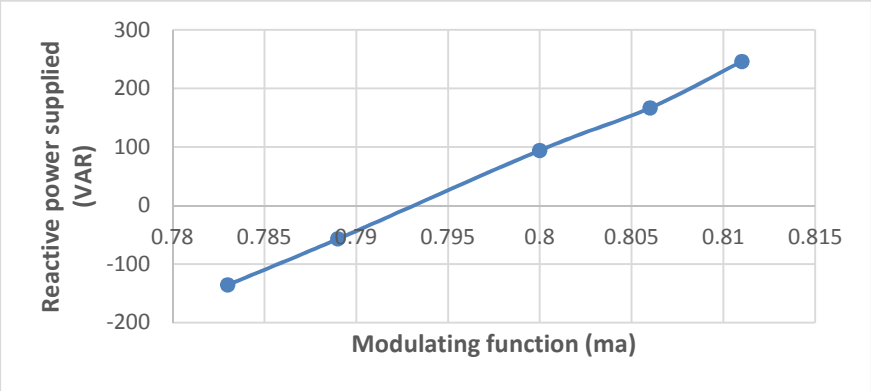

Figure 5.6: Open Loop Control Results

5.2 Case II Closed Loop Simulation Regulating Reactive Power Injection

As discussed in Chapter 2 of this thesis, a closed loop control scheme was designed and implemented for the STATCOM. The closed loop control consists of an inner control loop and an outer control loop. For performing the closed simulation, a value for the Qref was provided to the control scheme. Later simulations will calculate Qref based on the difference between the ac voltage set point and the magnitude of the ac voltage at the point-of-interconnection. Then Iqref was next calculated using equation (4-10). Using these values in the closed loop simulation, the reactive power supplied was measured to be 100.4VAR as seen in Figure 5.7 which was close to the expected value of 100VAR. The first part of Figure 5.7 is a start-up transient and the STATCOM is not started as a real one would start in practice. The phase A voltage was measured to be 121.76V and the phase A current was 2.418A as seen in Figure 5.8 and Figure 5.9 respectively. The Vsq value from the PLL was regulated to 0 and Vsd value was regulated to the amplitude necessary to support the reactive power transfer.

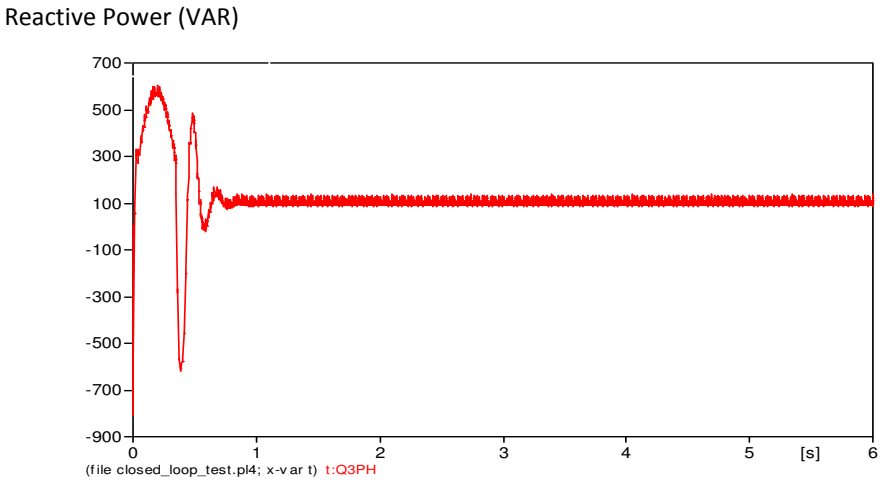

Figure 5.7: Output Reactive Power from the First Closed Loop Test

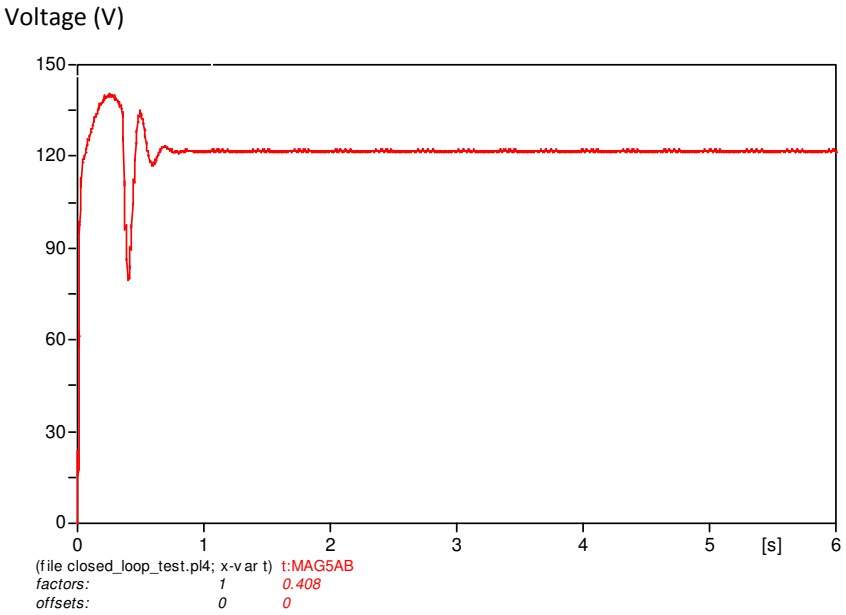

Figure 5.8: Output Voltage from the First Closed Loop Test

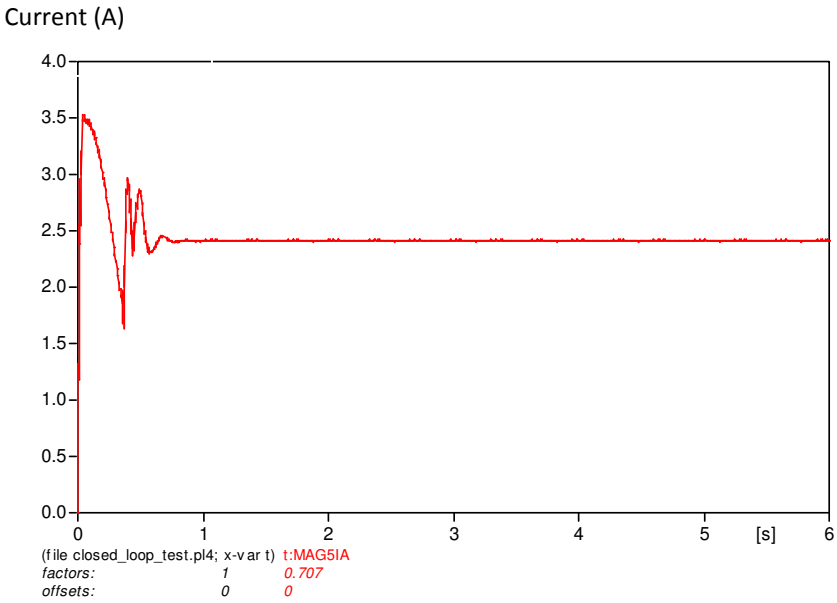

Figure 5.9: Output Current from the First Closed Loop Test

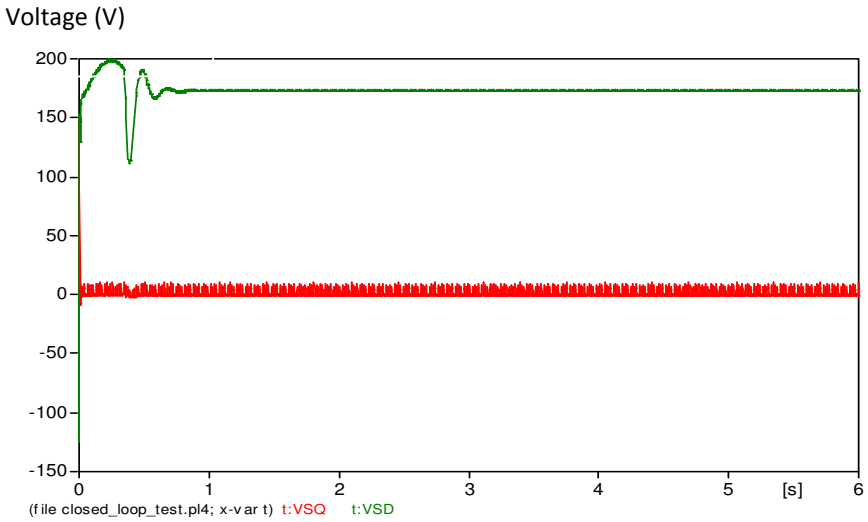

Figure 5.10: Vsq and Vsd from the First Closed Loop Test

As can be seen from Table 5.3 and Figure 5.11, the closed loop control system was able to perform better as compared to the open loop controls. The closed loop control tracked the required reactive power more closely as it was varied from -200VAR to 300VAR demonstrating the advantage of using a closed loop control scheme, and setting the state for the other simulations.

Table 5.3: Case II Closed Loop Test Results

Qref (VAR)	Iqref (A)	Output Currents (A)	Output Voltages (V)	Reactive Power Supplied (VAR)
-200	0.6117	2.154	108.61	-200.1
-100	0.2931	2.25	113.42	-100.1
100	-0.273	2.418	121.76	100.4
200	-0.53	2.494	125.511	200.2
300	-0.774	2.565	129.047	300.4

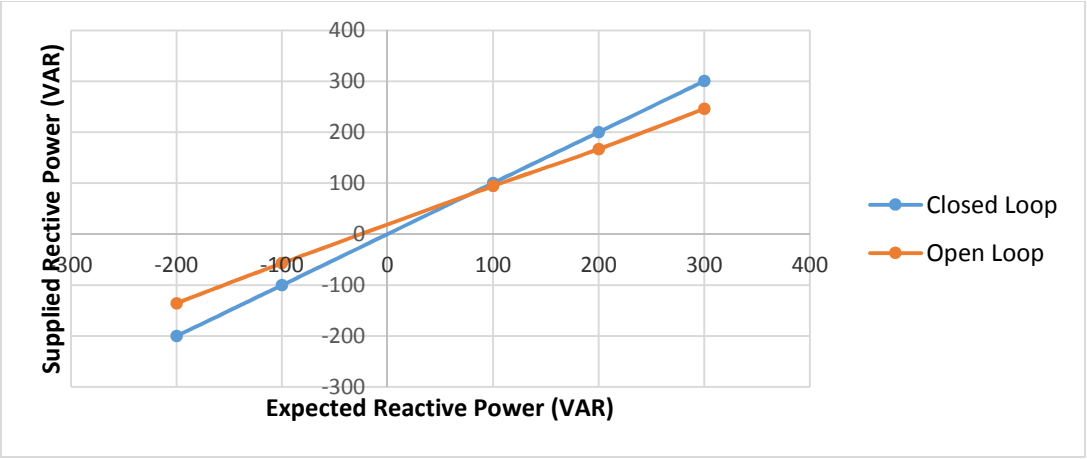

Figure 5.11: Open Loop Control vs Closed Loop Control (case II)

5.3 Case III Closed Loop AC Voltage Regulation with Load Impedance Variation

In this case, the load impedances were changed in steps that match the values for the load impedances in the lab. The goal was to see how the STATCOM would react to the changes in the load impedances to maintain the voltage. The simulation cases used resistive loads, resistive plus inductive loads, and capacitively compensated loads (which would be the case if the STATCOM is used primarily for dynamic compensation). From the simulation, it was possible to find the value of the Qref and Iqref that would provide the required reactive compensation to maintain the voltage level.

As can be seen in Table 5.4 and Figure 5.12, it was found that as the load impedances decreases in the case of the resistive loads, the real and reactive power required increased respectively. When the loads were replaced with the inductive loads, there was even more required reactive power to maintain the voltage. Finally, a negative value for the Qref had

to be used to decrease the voltage level due to the reactive compensation provided by the overly capacitively compensated loads.

Table 5.4: Case III Load Impedances Variation Results

Load Impedances (Ohms)	Output Voltages (V)	Output Currents (A)	|Iqref| (A)	Qref (VAR)
Resistive				
50.325	125	2.48	0.6963	185
43.7	125	2.859	0.7183	270
35.561	125	3.512	1.184	445
Inductive + Resistive				
31.972+53.622	125	2.008	1.132	425
21.878+45.632	125	2.477	1.406	528
14.278+37.05	125	3.155	1.877	705
Capacitive + Resistive				
48.25-11.969	125	0.001504	0.3513	-132
41.351-11.178	125	0.001404	0.3513	-132
33.356-9.4	125	0.001181	0.3513	-132

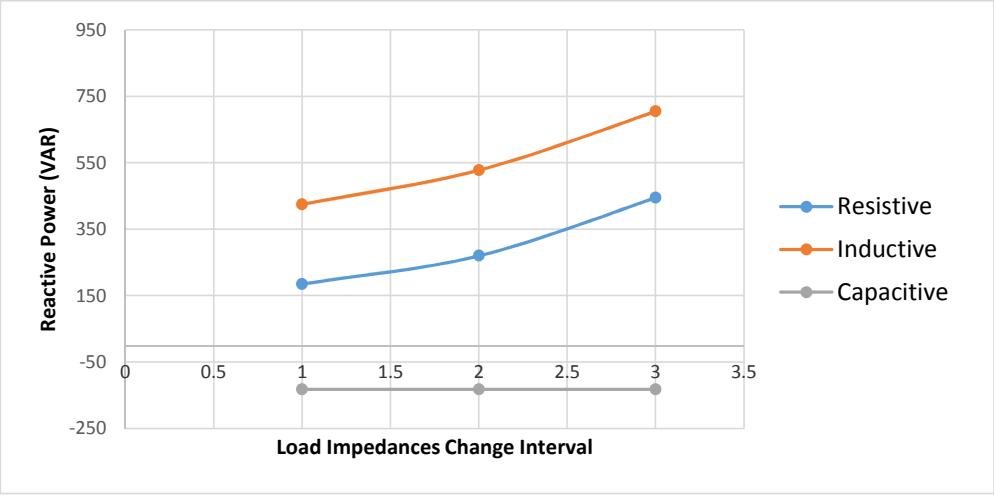

Figure 5.12: Reactive Power Injection from STATCOM for Changes in Load Impedances

For the capacitively compensated loads, the ability of the STATCOM to provide better response in comparison to the mechanically switched capacitors can be simulated. The problem with the mechanically switched capacitors is that when the load increases or decreases, the capacitor control does not react fast enough and the STATCOM provides this ability to react according to the load changes. As can be seen from Figure 5.13 and Figure 5.14, the voltage with the capacitively compensated load was 131.78V. After 1.5 sec, -132VAR was injected to the system to reduce the voltage level to 125V. Finally, to bring the voltage level to 120V, -78VAR was injected to the system after 2.5 sec.

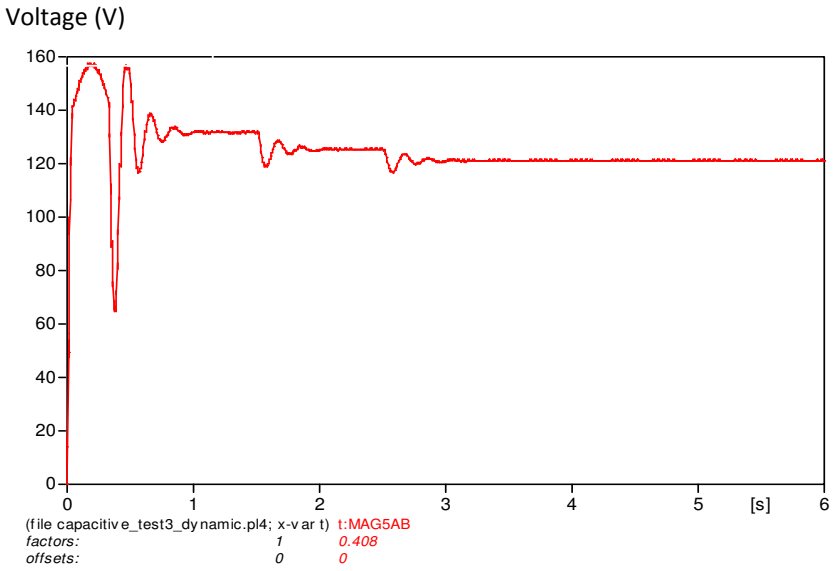

Figure 5.13: Output Voltages for the Capacitively Compensated Loads

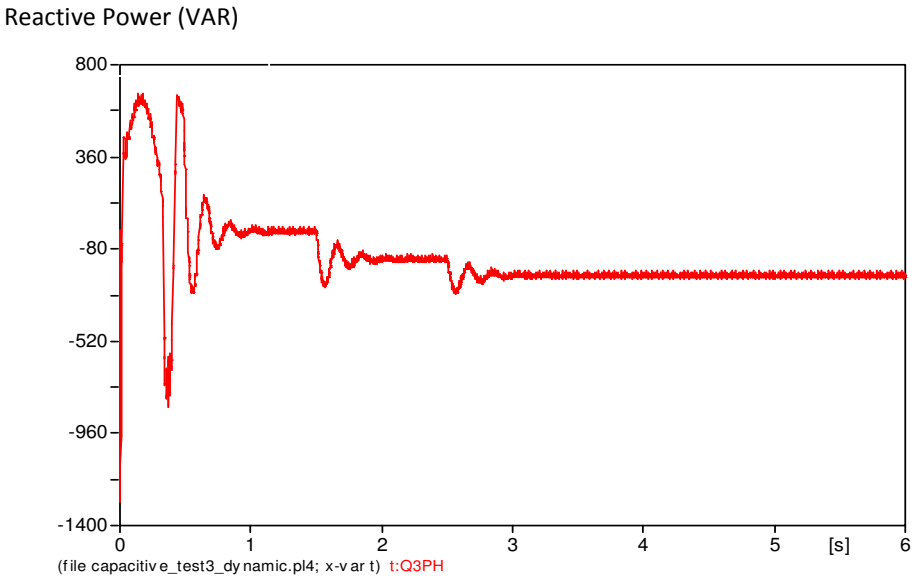

Figure 5.14: Output Reactive Power for the Capacitively Compensated Loads

5.4 Case IV Voltage Regulation with Line Length Variation

In this case, the lengths for the lines in the AMPS were varied and the response of the STATCOM to the line length variation was analyzed. The goal was to see how the changes in line length would the affect the reactive support provided by the STATCOM to maintain the voltage at the point-of-interconnection at a given value. For this purpose the values of Qinjected required to maintain the voltage at 125V were measured when the line length was varied from 10% to 100%. This could be used for a lab in a course.

As can be seen from Table 5.5, as the line length values are increased, there was an increase in the required reactive power to support the voltage as well. There was not much variation in the output currents and the Iqref values increased with the increase in the line length as expected. Figure 5.15 shows the required reactive power increased for 10% to 30% increase in line length and from 80% to 100% variation, while it stayed almost the same in the

middle. This might be due to the line impedances variation in the middle steps are not as big as in comparison the beginning and the later stages of the lines.

Table 5.5: Case IV Line Length Variation Results

Line Impedances	Output Voltages (V)	Output Currents (A)	Iqref (A)	Qref (VAR)
10%	125	2.486	0.4418	166
20%	125	2.485	0.4527	170
30%	125	2.486	0.4632	174
40%	125	2.486	0.4656	175
50%	125	2.486	0.4656	175
60%	125	2.487	0.4677	176
70%	125	2.488	0.4677	176
80%	125	2.483	0.4705	177
90%	125	2.485	0.4787	180
100%	125	2.482	0.4923	185

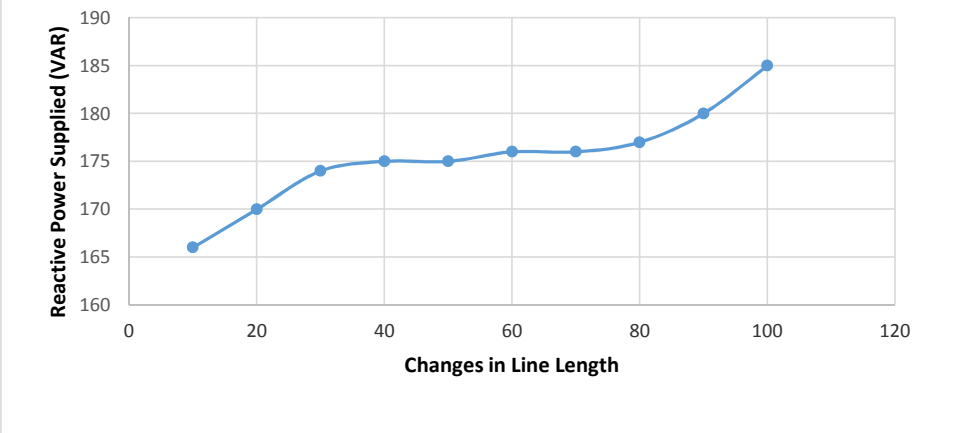

Figure 5.15: Changes in Line Length

5.5 Case V STATCOM Response to Faults in the System

In this part, the response of the STATCOM to the faults applied in the system was analyzed. The faults can be created in the AMPS using the fault simulator. For creating the faults in the ATP model, the fault switches were closed. The parameters that need to be changed to

implement a fault are the “Nxx_GO” values. For example, to do a SLG fault on phase A occurring 50 milliseconds (3 cycles) into the simulation, NA_GO should be changed to 0.05. To implement a LL fault between phases B and C occurring 50 milliseconds into the simulation, BC_GO should be changed to 0.05. To do a DLG fault from B to C to ground NB_GO and NC_GO need to be set to both turn on. Similarly, to perform a three phase fault, NA_GO, NB_GO, and NC_GO should all be turned on. It is important to turn off any previous faults before we create a new one [14].

In this case a three phase fault was applied at the location between line 1 and line 2 as seen in Figure 5.16.

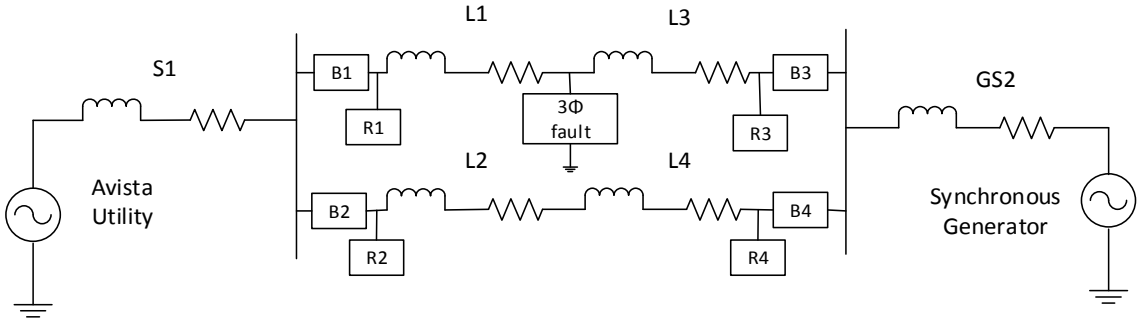

Fig 5.16: Three Phase Fault Applied in the AMPS

The three phase fault was applied at the location between line 1 and line 2 after 2 sec. After the fault was applied, the voltage value went down from 117.9V to 99.4V. Then the reactive power support from the STATCOM was provided 0.5 sec after the fault is applied. The value for Qref was 578VAR so that it would bring the voltage level to the previous value before the fault was applied which was 117.9V. The fault was cleared after 3.5 sec and again the STATCOM was able to maintain the voltage at the previous level after the fault was cleared as can be seen from Figure 5.17 and Figure 5.18. From Figure 5.19, the reactive power

supplied from the STATCOM during the fault can be seen. Note that the case had an unrealistically long duration. In practice, the protective relays would respond open breakers within 5-8 cycles. The long fault duration is added in the case to provide allow the users to better observe the behavior of the STATCOM.

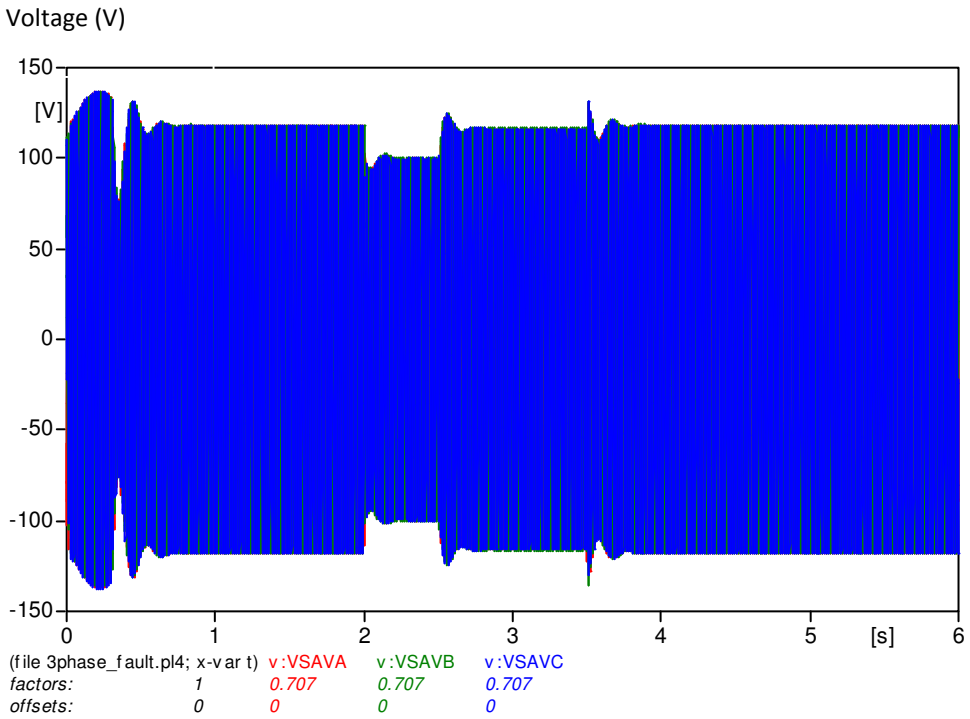

Figure 5.17: Output Voltages for a Three Phase Fault

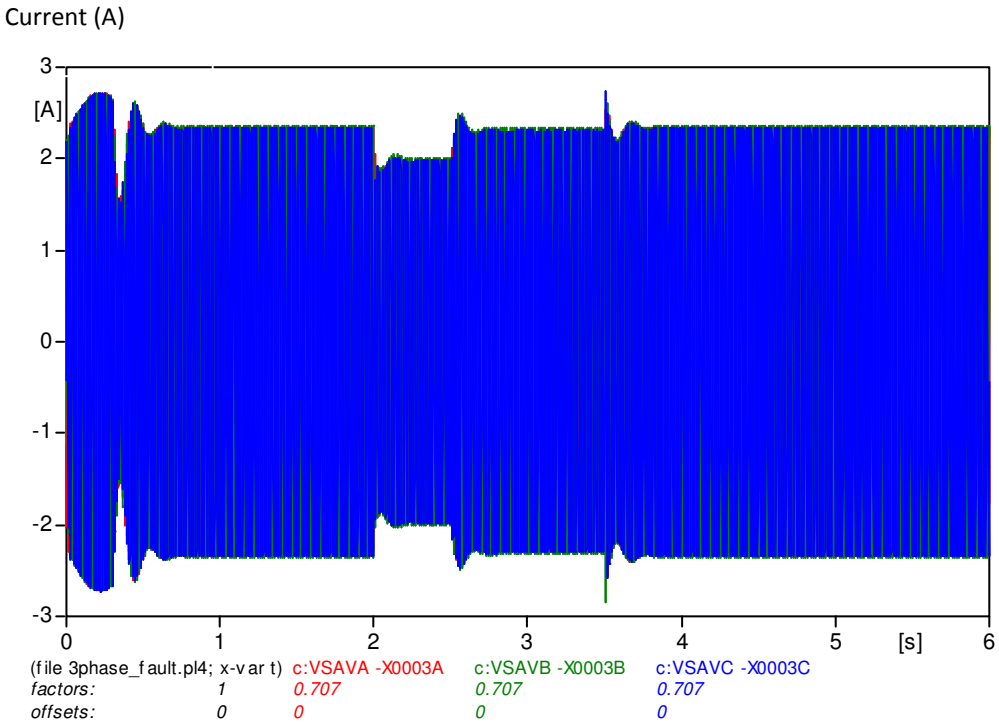

Figure 5.18: Output Currents for a Three Phase Fault

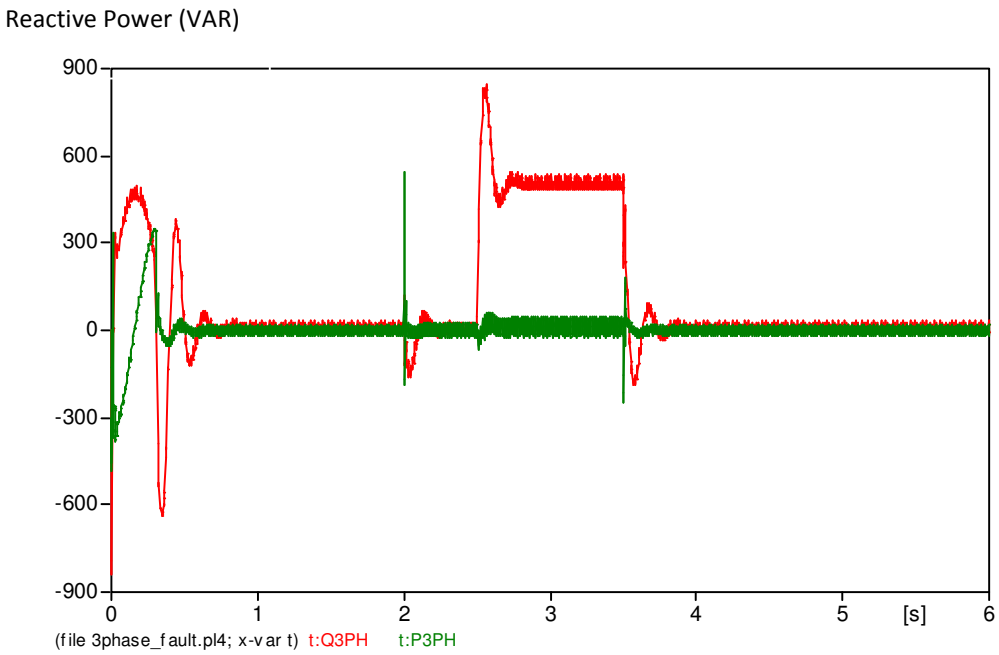

Figure 5.19: Output Real and Reactive Power during a Three Phase Fault

Chapter 6

Hardware Implementation

6.1 Selection of the Components

A senior design team worked on a hardware implementation of a STATCOM in parallel with this work. The author was a mentor for this team. The senior design team's goal was a hardware implementation of a STATCOM so that it could be used with the Analog Model Power System. The switching devices suggested were IGBT's (FGP5N60 from Mouser Electronics). The capacitor sizing was calculated based on the rated DC voltage to be 81.79 uF. For measuring the currents and voltages to the STATCOM, the team used the LEM voltage sensors and LEM current sensors available in the lab.

Initially a Pinguino microcontroller was suggested, which is the least expensive, but potentially the most difficult platform to use. When the Pinguino microcontroller proved insufficient, the Microchip microcontroller was suggested. The Microchip was a more expensive option because of the development board. The Microchip also has other useful features such as a built in PLL, which will be difficult to implement on any other controller. The Phase-Locked Loop is the main stumbling block faced by the coders. Furthermore, a plug-in module for the Microchip, DSPic 33 FJ256 was suggested for future.

Finally, the Cerebot MX3cK microcontroller was suggested, which is the platform on which the senior design team was trained on. This made the programming problem less significant

MX3cK than the Pinguino's, but the group need the processing power for implementing a dq transformation and a Phase-Locked Loop algorithm.

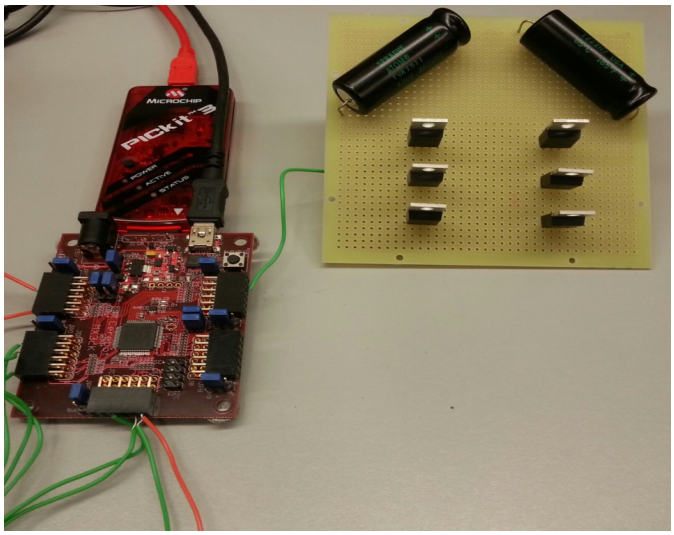

Figure 6.1: STATCOM Circuit Implementation Board Developed by the Students

6.2 Control Development

Initially, the control system of the STATCOM device was to be a Parks-Transform based three-phase system. Three analog voltage signals and three current readings were to be taken synchronously by the LEM modules. These devices output a voltage from -2.5VDC to +2.5VDC; which is out of the readable range for the MX3CK board's inputs, which only read from 0VDC to +3.3VDC. A voltage divider and DC offset had to be applied in order to take the sine wave inputs to the readable range.

Testing for the controls was done in the Microcontrollers lab using a function generator and Agilent Oscilloscope. A 60Hz Sine wave from 0VDC to 1.9VDC was applied to a common

point attached to 6 ADC inputs, and the equation (6.1) was used to sample each ADC in an interrupt.

VxG = (float)ReadADC10(n)*(3.3/1023); (6.1)

where **x** is the phase voltage, and **n** is the ADC number.

The multiplication at the end of the VxG code converts the Analog signal from an unsigned integer to a readable voltage between 0VDC and 3.3VDC. When each ADC was read at the fastest possible timing configuration, each input differed by up to a full volt. This indicated that the analog to digital conversions taking place were not fast enough. Though there are 10 ADC inputs on the MX3CK, there aren't 10 Analog to Digital Converters; the inputs are multiplexed into a single module, so a conversion takes up to 60us to complete, and completing a full six conversions took up to a quarter of the input sine wave's period.

6.2.1 Configuring the Built-In ADC

The main obstacle to the progress of the control design was configuring the ADC module. The definition provided by the equation (6.2) is the most important line of the code for this purpose. Changing the two parameters in bold to higher or lower values adjusts the amount of time taken between ADC samples. The project utilized the fastest setting, but was unable to meet specifications for three-phase sampling.

#define PARAM3 ADC_CONV_CLK_PB | **ADC_SAMPLE_TIME_31** | ADC_CONV_CLK_SYSTEM | **ADC_CONV_CLK_2Tcy** (6.2)

6.3 Timing Testing

To ensure that the Peripheral Bus Clock and System clock were optimally configured, a latch inversion was performed on every compare call. This revealed seemingly arbitrary slowdowns periodically, caused by the ADC interrupt; however, the delays were longer than predicted. A new latch invert was performed on every triangle wave peak, and this revealed that the clocking was being inexplicably blocked. The line of code described by equation (6.3) was added to the configuration files for this purposes.

SYSTEMConfig(SYS_FREQ, SYS_CFG_WAIT_STATES | SYS_CFG_PCACHE); (6.3)

Immediately afterwards, the triangle wave reached expected frequency, and compares happened at a rate of 6-8kHz. This code must be included in any STATCOM implementation in the initialization block for the clocking of any MXxK model to function optimally. If this line is omitted, both the Peripheral Bus and System Clocks will have arbitrary slowdowns and glitches.

6.4 Single-Phase (Current implementation)

The current implementation that the STATCOM runs uses only one ADC. The port is sampled at the highest frequency possible, then is compared to a high-frequency, internally generated triangle wave 20% larger than the highest ADC signal. When the ADC signal (referred to as VA) is higher than the triangle wave's amplitude at the point of sampling, IGBT B (the negative switch) turns off, and IGBT A turns on. When VA is lower than the triangle wave's amplitude at the point of sampling, IGBT A turns off, and IGBT B comes on.

The interrupt-read sequence is disabled during comparison, and IGBTs A and B are never on at the same time, preventing the shock in the dc bus capacitor.

This control scheme creates a wave that is exactly the same frequency as the input signal, modulates based on its amplitude, and crosses zero at the same time as the input. This is undesirable for sourcing reactive power, but the DC offset circuit causes a delay in the signal received by the ADC, creating a phase shift that forces the STATCOM to supply reactive power.

6.5 Future Implementation and Design Notes

Although, the team was not able to implement to have the complete setup of the hardware for the STATCOM and perform the testing of the hardware, the circuitry design is available for future students who may take up the project, and the code has been heavily commented for their use. In order to change to a three-phase setup, the controller must be fed external ADC signals via the I2C interface. This will allow for the fastest possible data acquisition, reading all six ADC modules almost simultaneously. Also, PWM cores can be considered which can do the PWM without burdening the main control. A Parks Transform will finish the conversion, and the clock can be run as fast as needed without any ADC configuration.

Chapter 7

Conclusion and Future Work

7.1 Summary

An ATPDraw model of a STATCOM was developed and simulated with a model of the analog model power system. Open loop and closed loop control models were developed for controlling the STATCOM, and averaged and switching models were developed and tested as well. The closed loop control yields better results than the open loop controls as expected. The STATCOM performances were simulated with different scenarios that could be used in classes such as changing the load impedances, changing the line lengths, and applying the faults to the system.

A single phase hardware implementation for the STACOM was developed by a senior design team. The simulation results can be used in conjunction with the lab experiments in different power classes. Also, these results can be used for developing the three phase hardware implementation of the STATCOM for future students.

7.2 Future Work

Some of the future work possible building on this research work includes:

1. Hardware Implementation

Three phase hardware models can be created for the STATCOM for interfacing with the analog model power system. The IGBTs and the capacitors from the senior design team can

be used for further expansion. The parameters found from the simulation for the closed loop control of the STATCOM can be a basis for the models. Also, the choices of the microcontroller and IGBTs can be taken into consideration while developing the hardware models.

2. Use the simulation cases for the lab experiments

The simulation cases can be used for the lab experiments for various courses in the ECE program related to the reactive power compensation techniques. This would be specific to courses like Utility Applications of Power Electronics, and Transmission and Distribution Applications of Voltage Sourced Converters. Students can use the models to study the reactive power compensation provided when there is the changes in the load impedances values, line length variation, applications of the faults, and the imbalances in the power system. First, the students can compute the values for the modulating function and the reference current values for the closed loop control, and they can be used to see how the STATCOM would react to the specified changes in the system in simulations and then in the lab.

3. Improvement in the control system

The control system of the STATCOM can be fine-tuned to produce even better results in the future. Signification improvement can be made to the open loop controls to produce the desired results. Also, the closed loop control can be improved to produce even better results such as tracking the point of common coupling voltage and providing dynamic

compensation according to the PCC voltage changes. The real power controller can also be made more robust if the exchange for real power is desired in future. The microcontroller program can be improved so that it can be more robust in detecting the voltage and currents in the system and providing the required amount of the reactive power accordingly.

4. Use the models for different studies

The models developed can be used for various different studies related to the reactive power compensation in future. These models can be used with research related to other FACTS devices as well which use voltage sourced converters. Some of the features of the models such as inner and outer control loop and phase locked loop for the synchronization can be used in developing the models for other FACTS devices. After the models for other devices are developed, the models from this research can be used to perform comparison between different devices used for reactive power compensation.

5. Visual effects of VSCs on power system

The improvements in the hardware implementation of the STATCOM can be used by the students to visualize the effects of the voltage sourced converters in the power system. The students can visually see how the increase in reactive power in the AMPS would enhance the voltage in the system by observing the light bulb loads, and the effect of the decrease in the reactive power in the system as well. It would be a more practical approach to the concepts learned in the classes.

Bibliography

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Appendix A

A.1 Calculation of the modulating functions

The values for the modulating functions and the DC voltages can be found as follows,

If R << X or XoverR > 10, we can approximate that,

$$S_{ST} = \frac{\left(\left|V_S\right|\right)^2 \cdot \text{ang}(90\text{deg}) - \left|V_s\right| \cdot \left|V_T\right| \cdot \text{ang}(0 - \delta + 90\text{deg})}{X}$$

$$P_{ST} = \text{Re}\left(S_{ST}\right)$$

$$P_{ST} = \frac{\left|V_S\right| \cdot \left|V_T\right| \cdot \sin(0 - \delta)}{X}$$

$$P_{out} = -P_{ST}$$

$$P_{out} = \frac{\left|V_S\right| \cdot \left|V_T\right| \cdot \sin(\delta - 0)}{X}$$

$P_{TS} = -P_{ST}$ since R=0

$$Q_{ST} = \text{Im}\left(S_{ST}\right)$$

$$Q_{ST} = \frac{\left|V_S\right| - \left|V_S\right| \cdot \left|V_T\right| \cdot \cos(0 - \delta)}{X}$$

$$Q_{out} = -Q_{ST}$$

$$Q_{out} = \frac{-\left(\left|V_S\right|\right)^2}{X} + \frac{V_S \cdot V_T \cdot \cos(0 - \delta)}{X}$$

$$Q_{TS} = \frac{\left(\left|V_T\right|\right)^2 - V_T \cdot V_S \cdot \cos(\delta - 0)}{X}$$

For P=0W, δ should be zero.

This gives,

$$Q_{out} = \frac{-(|V_S|)^2}{X} + \frac{|V_S| \cdot |V_T|}{X}$$

$$V_T := \frac{\left[Q_{out} + \frac{(|V_S|)^2}{X}\right] \cdot X}{|V_S|} = 144.603V$$

$$V_{DC} := \frac{2 \cdot V_T}{m} = 361.507V$$

$$\frac{V_{DC}}{2} = 180.754V$$

After, we find the DC voltage, we can find the values of the m for the required amount of the reactive power. For example, if the required reactive power is 200VAR, the modulating function can be found as.

Now, for Q=200VAR

$$m = \frac{2 \cdot V_T}{V_{DC}}$$

$$Q_{out} := 200VAR$$

$$V_T := \frac{\left[Q_{out} + \frac{(|V_S|)^2}{X}\right] \cdot X}{|V_S|} = 145.606V$$

$$m := \frac{2 \cdot V_T}{V_{DC}} = 0.806$$

A.2 Calculation of the idref and iqref values

The idref and iqref values for the closed loop control are calculated as follows,

$V_{sd} := 169.831V$

$P_{ref} := 0W \qquad Q_{ref} := 100VAR$

Therefore,

$$i_{dref} := \frac{2}{3} \cdot \frac{P_{ref}}{V_{sd}} = 0$$

$$i_{qref} := \frac{2}{3} \cdot \frac{Q_{ref}}{V_{sd}} = 0.393A$$

A.3 Calculation of the capacitor values

The capacitor values was calculated as follows,

$$V_{DC} := \frac{2 \cdot V_T}{m} = 361.507V$$

$$\frac{V_{DC}}{2} = 180.753V$$

$$X_{cap} := \frac{\left(\frac{V_{DC}}{2}\right)^2}{1000VAR} = 32.672\Omega$$

$$Cap := \frac{1}{\omega \cdot X_{cap}} = 81.189\mu F$$

A.4 Datasheets for the hardware components

A.4.1 Microcontroller

The microcontroller suggested by the senior design team was the Cerebot MX3cK from Mouser Electronics. The specifications for the microcontroller are provided below. More information can be found in [16].

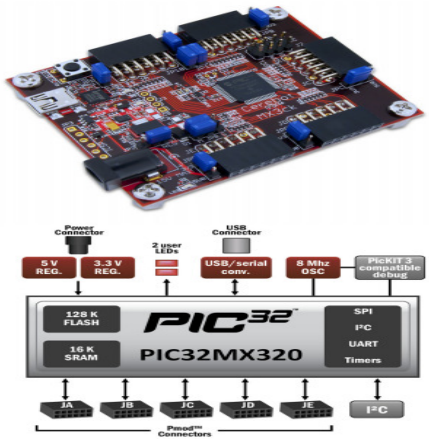

Figure A.1: Cerebot MX3cK Microcontroller

Table A.1: Specifications for the MX3cK Microcontroller

Microcontroller	PIC32MX320F128H
Flash Memory	128K
RAM Memory	16K
Operating Voltage	3.3V
Max Operating Frequency	80MHz
Typical Operating Current	75mA
Input Voltage (Recommended)	7V to 15V
Input Voltage (Maximum)	20V
I/O Pins	42 total
Analog Inputs	12
Analog input voltage range	0V to 3.3V
DC Current per pin	+/- 18mA

A.4.2 IGBTs

The IGBTs selected by the senior design team were the FGP5N60 from Mouser Electronics. The specifications for the IGBTs are provided in the table below. More information can be found in [17].

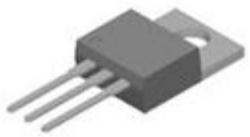

Figure A.2: IGBTs for Switching

Table A.2: Specifications for the IGBTs

Manufacturer	Fairchild Semiconductor
Product Category	IGBT Transistors
Collector – Emitter Voltage VCEO Max	600V
Collector – Emitter Saturation Voltage	1.8V
Maximum Gate Emitter Voltage	20V
Continuous Collector Current at 25C	10A
Gate-Emitter Leakage Current	400nA
Power Dissipation	83W
Maximum Operating Temperature	+125C
Package/Case	TO-220
Packaging	Tube
Minimum Operating Temperature	-55C
Mounting Style	Through Hole
Series	FGP5N60
Unit Weight	0.063493oz

A.4.3 Gate Drivers for the IGBTs

The gate drivers suggested by the senior design team were the MC34151PG from Mouser Electronics. The table below provides the specifications for the gate drivers. More information can be found in [18].

Figure A.3: Gate Drivers for the IGBTs

Table A.3 Gate Drivers for the IGBTs

Manufacturer	ON Semiconductor
Configuration	Inverting
Number of Drivers	2
Rise Time	31ns
Fall Time	32ns
Supply Voltage – Min	6.5 V
Supply Current	10.5mA
Maximum Power Dissipation	1000mW
Maximum Operating Temperature	+ 70 C
Mounting Style	Through Hole
Package/Case	PDIP-8
Type	High Speed
Brand	ON Semiconductor
Minimum Operating Temperature	0C
Number of Outputs	2
Packaging	Tube

A.4.5 Capacitors

The senior design team evaluated capacitors for the hardware STATCOM. The capacitors chosen were the P10397TB-ND from the Digi-Key, see Fig. A.4. The Table. A.4 provides the datasheet information of the capacitors. More information can be found in [19].

Figure A.4: Capacitor for the Hardware Implementation

Table A.4 Specifications of the Capacitors Used

Family	Aluminum Capacitors
Packaging	Tape and Box
Capacitance	100uF
Voltage Rating	50V
Tolerance	+/-20%
Lifetime@Temp	2000 Hrs @ 85degC
Operating Temperature	-40degC~85degC
Applications	General Purpose
Ripple Current	250mA
Lead Spacing	0.197”(5.00mm)
Size/Dimension	0.315” Dia (8.00mm)
Height – Seated (Max)	0.492” (12.50mm)
Mounting Type	Through Hole
Package/Case	Radial, Can

A.5 Line Impedances Values

The Tables A.5-A.8 show the line impedances values for the transmission lines in the AMPS. Each line has 10 taps and the tables list the variations with tap selection. More information about these impedance values can be found in [12].

Table A.5: Line 1 Impedances Values

LINE#1	SERIES INDUCTOR IMPEDANCE [OHMS @ 60 HZ] (NON-SATURATED)									
	TAPS 0-1 R [OHMS] wL [OHMS]	TAPS 0-2 R [OHMS] wL [OHMS]	TAPS 0-3 R [OHMS] wL [OHMS]	TAPS 0-4 R [OHMS] wL [OHMS]	TAPS 0-5 R [OHMS] wL [OHMS]	TAPS 0-6 R [OHMS] wL [OHMS]	TAPS 0-7 R [OHMS] wL [OHMS]	TAPS 0-8 R [OHMS] wL [OHMS]	TAPS 0-9 R [OHMS] wL [OHMS]	TAPS 0-10 R [OHMS] wL [OHMS]
PHASE A	0.0959	0.1918	0.2877	0.4243	0.5303	0.6364	0.7438	0.8500	0.9563	1.0625
	0.2110	0.4158	0.8620	1.6677	2.5844	3.6818	5.0009	6.4965	8.2059	10.1093
PHASE B	0.0842	0.1684	0.2526	0.3515	0.4393	0.5272	0.6142	0.7019	0.7896	0.8774
	0.2245	0.4513	0.9246	1.6764	2.5724	3.6847	4.9854	6.4464	8.1406	10.0284
PHASE C	0.1004	0.2007	0.3011	0.4217	0.5271	0.6325	0.7333	0.8381	0.9428	1.0476
	0.2171	0.4609	0.9350	1.7063	2.6234	3.7318	4.9995	6.4622	8.1124	9.9671
NEUTRAL	0.0847	0.1695	0.2542	0.3517	0.4397	0.5276	0.6143	0.7020	0.7898	0.8775
	0.2313	0.4644	0.9365	1.6824	2.5902	3.6943	4.9943	6.5092	8.1775	10.0304

Table A.6: Line 2 Impedances Values

TABLE 2A	ALL VALUES ARE LINKED TO WORKSHEET 3 TABLE 2C									
LINE#2	SERIES INDUCTOR IMPEDANCE [OHMS @ 60 HZ] (NON-SATURATED)									
	TAPS 0-1 R [OHMS] wL [OHMS]	TAPS 0-2 R [OHMS] wL [OHMS]	TAPS 0-3 R [OHMS] wL [OHMS]	TAPS 0-4 R [OHMS] wL [OHMS]	TAPS 0-5 R [OHMS] wL [OHMS]	TAPS 0-6 R [OHMS] wL [OHMS]	TAPS 0-7 R [OHMS] wL [OHMS]	TAPS 0-8 R [OHMS] wL [OHMS]	TAPS 0-9 R [OHMS] wL [OHMS]	TAPS 0-10 R [OHMS] wL [OHMS]
PHASE A	0.0859	0.1718	0.2577	0.3713	0.4641	0.5569	0.6497	0.7425	0.8354	0.9282
	0.2301	0.4651	0.9449	1.7719	2.7410	3.9104	5.2628	6.8178	8.6128	10.6091
PHASE B	0.0994	0.1989	0.2983	0.4369	0.5461	0.6553	0.7645	0.8737	0.9829	1.0921
	0.2182	0.4360	0.9022	1.7263	2.6712	3.8246	5.1316	6.6985	8.4193	10.3910
PHASE C	0.1069	0.2138	0.3208	0.4522	0.5653	0.6784	0.7914	0.9045	1.0176	1.1306
	0.2372	0.4904	0.9970	1.8279	2.8242	4.0031	5.3733	6.9749	8.7546	10.7571
NEUTRAL	0.1100	0.2199	0.3299	0.4355	0.5443	0.6532	0.7620	0.8709	0.9798	1.0886
	0.2604	0.4901	1.0055	1.7228	2.6661	3.8143	5.1687	6.6741	8.4397	10.3576

Table A.7: Line 3 Impedances Values

TABLE 3A	ALL VALUES ARE LINKED TO WORKSHEET 3 TABLE 3C									
LINE#3	SERIES INDUCTOR IMPEDANCE [OHMS @ 60 HZ] (NON-SATURATED)									
	TAPS 0-1 R [OHMS] wL [OHMS]	TAPS 0-2 R [OHMS] wL [OHMS]	TAPS 0-3 R [OHMS] wL [OHMS]	TAPS 0-4 R [OHMS] wL [OHMS]	TAPS 0-5 R [OHMS] wL [OHMS]	TAPS 0-6 R [OHMS] wL [OHMS]	TAPS 0-7 R [OHMS] wL [OHMS]	TAPS 0-8 R [OHMS] wL [OHMS]	TAPS 0-9 R [OHMS] wL [OHMS]	TAPS 0-10 R [OHMS] wL [OHMS]
1PHASE A	0.0658	0.1316	0.1974	0.2895	0.3618	0.4342	0.5066	0.5789	0.6513	0.7237
	0.2274	0.4410	0.8818	1.6926	2.6313	3.7737	5.1182	6.6658	8.3972	10.3488
PHASE B	0.0818	0.1636	0.2454	0.3575	0.4469	0.5363	0.6257	0.7151	0.8045	0.8939
	0.2159	0.4283	0.8666	1.6654	2.6053	3.7258	5.0601	6.5971	8.3031	10.2170
PHASE C	0.0680	0.1361	0.2041	0.2864	0.3580	0.4296	0.5013	0.5729	0.6445	0.7161
	0.2242	0.4511	0.9169	1.6892	2.6185	3.7463	5.0706	6.6151	8.3060	10.2404
NEUTRAL	0.0870	0.1740	0.2611	0.3552	0.4440	0.5328	0.6216	0.7104	0.7991	0.8879
	0.2399	0.4550	0.9235	1.6451	2.5664	3.6834	5.0141	6.4948	8.2272	10.1492

Table A.8: Line 4 Impedances Values

TABLE 4A	ALL VALUES ARE LINKED TO WORKSHEET 3 TABLE 4C									
LINE#4	SERIES INDUCTOR IMPEDANCE [OHMS @ 60 HZ] (NON-SATURATED)									
	TAPS 0-1 R [OHMS] wL [OHMS]	TAPS 0-2 R [OHMS] wL [OHMS]	TAPS 0-3 R [OHMS] wL [OHMS]	TAPS 0-4 R [OHMS] wL [OHMS]	TAPS 0-5 R [OHMS] wL [OHMS]	TAPS 0-6 R [OHMS] wL [OHMS]	TAPS 0-7 R [OHMS] wL [OHMS]	TAPS 0-8 R [OHMS] wL [OHMS]	TAPS 0-9 R [OHMS] wL [OHMS]	TAPS 0-10 R [OHMS] wL [OHMS]
PHASE A	0.0841	0.1683	0.2524	0.3658	0.4572	0.5487	0.6401	0.7316	0.8230	0.9145
	0.2303	0.4395	0.8923	1.6898	2.6357	3.7718	5.1039	6.5655	8.4637	10.4526
PHASE B	0.0806	0.1612	0.2417	0.3572	0.4465	0.5358	0.6251	0.7144	0.8037	0.8930
	0.2202	0.4162	0.8462	1.6464	2.5632	3.6850	4.9816	6.5063	8.2586	10.2074
PHASE C	0.1021	0.2043	0.3064	0.4441	0.5551	0.6662	0.7772	0.8882	0.9992	1.1103
	0.2283	0.4693	0.9494	1.7696	2.7634	3.9299	5.2788	6.8584	8.6113	10.5634
NEUTRAL	0.0755	0.1511	0.2266	0.2916	0.3646	0.4375	0.5104	0.5833	0.6562	0.7291
	0.2614	0.5006	1.0148	1.7111	2.6602	3.7951	5.1923	6.7236	8.4770	10.4266

A.6 Load Values

The load values used for the simulation load variation test is provided in Table A.9.

Table A.9: Load Values for the Load Variation Test

Light Bulbs	**Resistive Bank (Ω)**		**Inductor Bank (Ω)**		**Capacitor Bank (Ω)**	
100 W per phase	R_1	16.4	Z_{L1}	1.469 + j16.216	Z_{C1}	-j42.328
$S = \frac{V^2}{Z}$	R_2	15.2	Z_{L2}	1.215 + j13.460	Z_{C2}	-j36.378
	R_3	15.6	Z_{L3}	1.392 + j15.419	Z_{C3}	-j45.170
(where V = 208V_{LL})	R_4	15.5	Z_{L4}	1.371 + j15.177	Z_{C4}	-j42.500
Z=144.213 Ω	R_5	14.6	Z_{L5}	1.049 + j11.611	Z_{C5}	-j40.100

A.7 Program Code

The program given below for the single phase implementation of the STATCOM was written by Ori Roundtree and Kort Laughlin from the senior design team working in the project.

```
/*********************************************************************
*****/
/*
                                    */
/*   main.c                         */
/* Read ADC, compare to triangle wave, operate two switches.
 * telling the thing which Analog input is done in init_ADC.c
 *
                */
/*********************************************************************
*****/


#include <init_ADC.h>
#include <configbits.h>
#include <plib.h>
#include <math.h>
/* ------------------------------------------------------------ */
/*                    Configuration Bits
*/
/* ------------------------------------------------------------ */



#define DCOFFSET 0.94
#define VREADMAX 1.75


BOOL VwasPositive;
BOOL IwasPositive;

float frequenz;
float period;
int T1;
int T2;
float SawAmp;
float VAG;
float IA;




/* ------------------------------------------------------------ */
/*                    Forward Declarations
          */
```

```
/* ------------------------------------------------------------ */

void DeviceInit();
void DelayInit();
void DelayMs(int cms);
void GetFreqy();
void SawTooth();
void switching();


/* ------------------------------------------------------------ */
/*                      Definitions
                        */
/* ------------------------------------------------------------ */

#define    cntMsDelay 10000           //timer 1 delay for 1ms
#define cntNsDelay  1


#define SYS_FREQ (80000000L)
#define CORE_TICS_perS (SYS_FREQ/2)


/* ------------------------------------------------------------ */
/*                      Main
                */
/* ------------------------------------------------------------ */


float dataRecord[500];
float VAGlog[500];
int VAGpointer = 0;
int dataRecordPointer = 0;

int main()
{

    SYSTEMConfig(SYS_FREQ, SYS_CFG_WAIT_STATES | SYS_CFG_PCACHE);


    DeviceInit();

    while(1)
    {
       SawTooth();
    }


}
```

```
/* ------------------------------------------------------------ */

/*  DeviceInit()

/* ------------------------------------------------------------ */

void DeviceInit()
{
    //set pin JA-08 to digital out (See p18/23 of RefMan
    TRISECLR=BIT_6;
    TRISGCLR=BIT_6;
    TRISDCLR=BIT_8;

    frequenz=60;
    period=1/frequenz;
    T1=ReadCoreTimer()*CORE_TICS_perS;//was 0
    SawAmp=0;

    // DelayInit();

    initADC();
    INTEnableSystemMultiVectoredInt();

}


//interrupts and reads a voltage from the adc to the variable
//VAG and IA
//was IPL 3

void __ISR(_ADC_VECTOR, ipl3) AdcHandler(void) {//was TPS_IN_Handler


    VAG = (float)ReadADC10(1)*3.3/1023;
    /*


    //IA = (float)ReadADC10(3)*3.3/1023;

    if ((VAG <= ((0.05*VREADMAX)+DCOFFSET)) && VwasPositive)
    {
        GetFreqy();
        VwasPositive=0;
    }else{
        VwasPositive=1;
    }

   // switching();
```

```
     */

    //toggle test timer


    mPORTDToggleBits(BIT_8);



    mAD1ClearIntFlag();

}




/* ------------------------------------------------------------ */

void GetFreqy()
{
    //get Timer value in seconds
    T2=ReadCoreTimer()*CORE_TICS_perS;
    if(((float)T2-(float)T1)<(float)(1/50))
    {
        period=T2-T1;
        frequenz=1/period;
        T1=T2;
    }
}

void SawTooth()
{
    int i;
    int j;


    //moved for testing
   // mPORTESetBits(BIT_6);

    for(i=0;i<10;i++)
    {
        //set the comparator value
        SawAmp=VREADMAX*i/10;
        switching();


        TEST;//toggle JA-9

    }
```

```
    for(j=10;j>0;j--)
    {
        SawAmp=VREADMAX*j/10;
        switching();

        TEST;//toggle JA-9
    }



}

/* ------------------------------------------------------------ */

/*** DelayInit
 **
 **   Parameters:
 **         none
 **
 **   Return Value:
 **         none
 **
 **   Errors:
 **         none
 **
 **   Description:
 **         Initialized the hardware for use by delay functions. This
 **         initializes Timer 1 to count at 10Mhz.
/* ------------------------------------------------------------ */

void DelayInit()
{
    unsigned int tcfg;

    /* Configure Timer 1. This sets it up to count a 10Mhz with a
period of 0xFFFF
     */
    tcfg = T1_ON | T1_IDLE_CON | T1_SOURCE_INT | T1_PS_1_8 |
T1_GATE_OFF | T1_SYNC_EXT_OFF;
    OpenTimer1(tcfg, 0xFFFF);

}

/* ------------------------------------------------------------ */

/*** DelayMs
 **
 **   Parameters:
 **         cms             - number of milliseconds to delay
 **
```

```
 **   Return Value:
 **         none
 **
 **   Errors:
 **         none
 **
 **   Description:
 **         Delay the requested number of milliseconds. Uses Timer1.
/* ------------------------------------------------------------ */

void DelayMs(int cms)
{
    int ims;

    for (ims = 0; ims < cms; ims++)
    {
        WriteTimer1(0);
       // while (ReadTimer1() < cntMsDelay);
         while (ReadTimer1() < cntNsDelay);//to delay around 100ns
         //no_op would be great. Look at that. Ask Dr J when it goes
wrong
    }

}

void switching(void)
{
 /*

    //testing records
    if(dataRecordPointer<500)
    {
        dataRecord[dataRecordPointer++]=SawAmp;
        VAGlog[VAGpointer++]=VAG;
    }else
    {
        while(1);
    }
*/
    if(SawAmp>=VAG)
    {
        //if the measurement exceeds the triangle wave, turn off

BOFF;
        AON;


    }else{
  AOFF;
        BON;
```

```
        }


}
```