Isolated Analog Data Acquisition Using Precision Shunt Resistor and Sigma-Delta Modulator

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Abstract

The purpose of this thesis is to study the use of a current shunt and a Sigma-Delta modulator with galvanic isolation in an attempt to replace the bulky current transformers (CTs) that are currently being used in commercial protection relays. The selection of the current shunt for the application at hand is a result of a background study on variety current sensing devices. As the electrical isolation plays an important role in power system applications for safety reasons, the proposed circuit is simulated with electrical transient models to make sure the designed circuit performs safely and that it is immune from transients to ensure data integrity. The circuit simulations and hardware testing demonstrate good performance in all cases. But there are weaknesses in noise rejection.

With the advantage in small physical size and less weight, the Sigma-Delta acquisition circuit offers an excellent, simple and economical solution to CTs. However, the poor ability to reject noise and interference remains a challenge to be resolved.

Acknowledgments

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Chapter 1. Introduction

Transformers are important hardware components that are widely used in electronics and electric power applications. They are used to transfer electrical power from an alternating current (AC) source to measuring devices while providing isolation to the devices. Another characteristic of transformers is the ability to block direct current (DC) signals while allowing AC signals to pass through. In electric power systems, the voltage/potential transformers (PT) and current transformers (CT) are used to step down the power line voltages and currents from hundreds of kilovolts and thousands of amps to hundreds volts and several amps, respectively. These values are then stepped down further to usable levels for the electronics by instrument PTs and CTs inside protective relays.

Figure 1 shows the overview of the distribution power lines' high voltages and currents being acquired by PTs and CTs and stepped down to lower values, e.g. 125V AC and 5A AC. The relay internal instrument PTs and CTs interface to the external transformers and further step down to appropriate levels for the electronics which are typically 5 V AC and 50 mA AC.

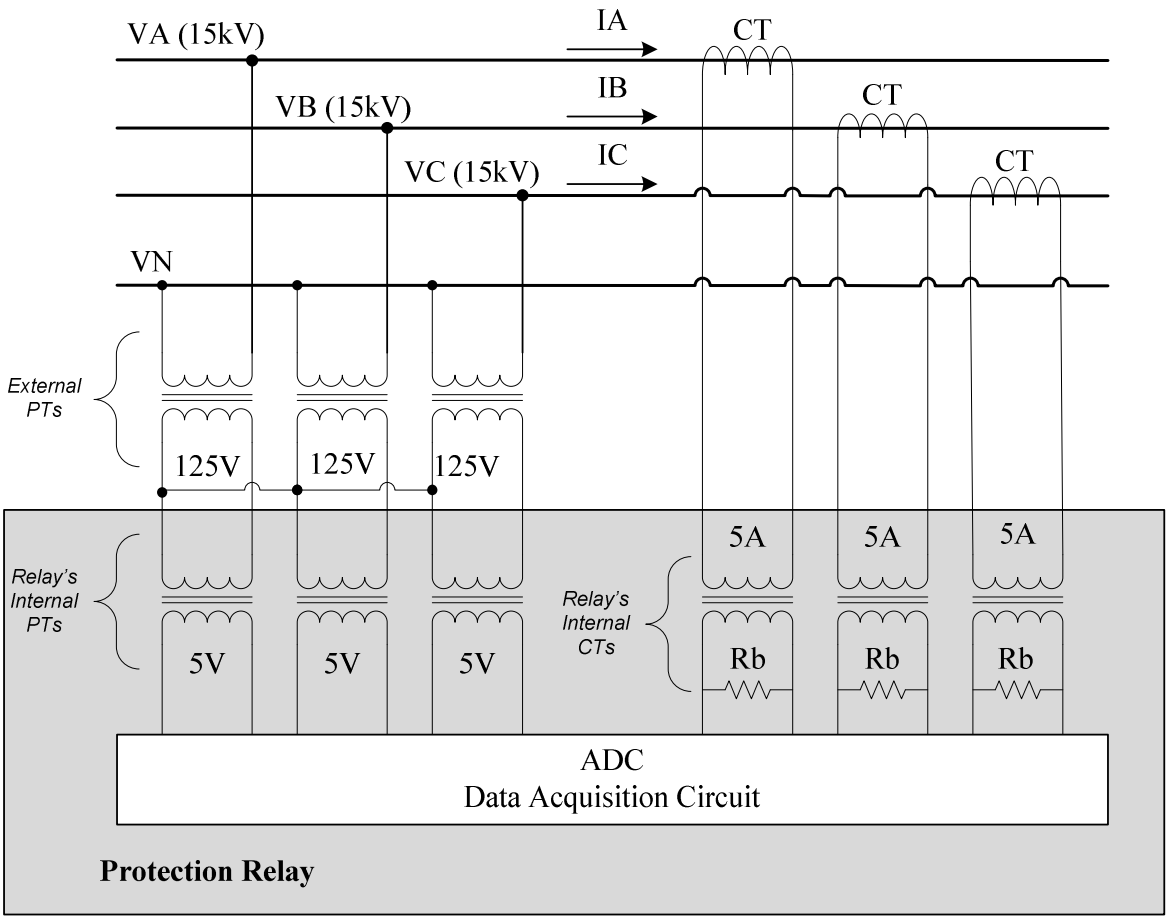


Figure 1-Protection relay being used to measure the power lines voltage and current

The current sensing circuit inside the relay typically employs a burden resistor on the CT secondary to convert the secondary winding's current into a differential voltage (shown in Figure 2). Since there are several analog channels to be measured, a Multiplexer (MUX) is used to select one channel at a time to acquire the analog voltage and feed it to the ADC for conversion. The FPGA is programmed with a digital cosine filter to recover the fundamental frequency and reject other harmonics before sending the data to the microprocessor to process the information.

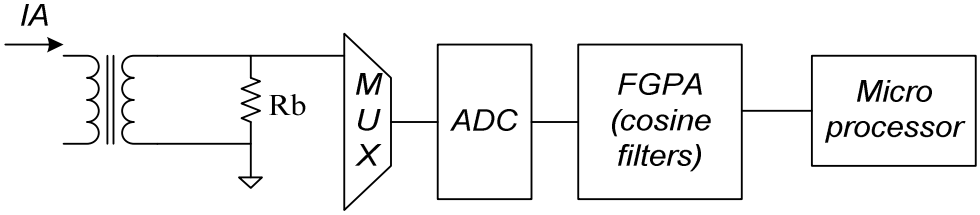


Figure 2-Typical implementation of a current sensing circuit using a CT.

In commercial relays there are two typical types of CTs depending on the application. A Type 1- CT can measure AC current from a nominal 1A up to 10 A at the primary winding. A Type 2-CT can measure AC current from a nominal 5A up to 20 A. Within the specified current range the CTs are guaranteed to operate linearly. Figure 3 shows a schematic diagram of the current measuring channel using a CT in a commercial protection relay. This circuit can measure the nominal AC current of 5A RMS up to 20A RMS. The winding turns ratio is 1:100 in order to get the desired output current at the secondary winding. For instance, when the maximum current at the primary winding is 20A RMS the secondary current will be 20A/100 = 0.2A RMS. A 2Ω burden resistor at the secondary output converts the current to 0.4V RMS voltage for use by the ADC circuit (not shown in the Figure).

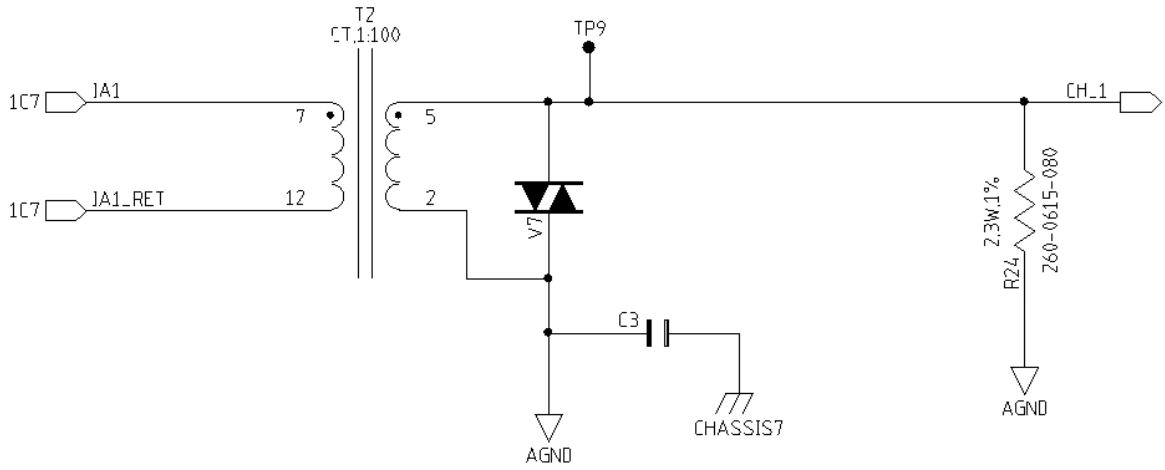


Figure 3-Schematic of a current acquisition circuit using CT.

Figure 4 shows the actual instrument CTs (left) and PTs (right) sitting side by side on the PCB board of a commercial protection relay.

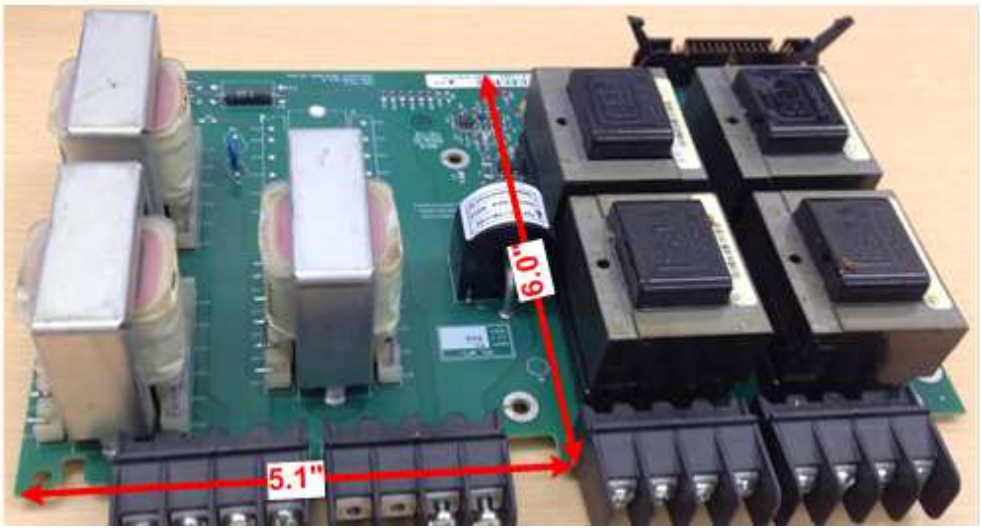


Figure 4-Current Transformers (left) in a commercial protection relay.

As of the time of this research, the majority of protection relays use instrument CTs and PTs for interfacing and providing isolation between high analog front end and digital back end [1]. However, magnetic interference (crosstalk) between adjacent transformers mounted on the same board, and non-ideal characteristics create challenges in measurement accuracy. Also, the large physical size and heavy weight of the transformers are subject to greater risk for mechanical instability, and are unfavorable for material cost control.

This paper first discusses the background and the motivation of this research which are described in Chapter 1. Chapter 2 reviews the common current sensing methods used to measure the electric current. Chapter 3 describes theory and principle operation of the Sigma-Delta acquisition circuit and its circuit design. Chapter 4 discusses the Pspice simulation of the circuit subjected to electrical transients in order to make sure the circuit is immune to the real world environmental electrical and magnetic disturbances in which the circuit operates, and that optimal operation is achieved. Chapter 5 performs functional tests of the actual circuit and compares to the performance of a data acquisition circuit using the CTs. Chapter 6 wraps up the research with conclusions on the Sigma-Delta acquisition circuit. Chapter 7 lists additional work to be done in the future to improve the circuit performance and to verify that it is immune to the actual electrical transients.

This research focuses on finding the alternatives to type 2-CTs therefore, all calculations and discussion here on evolve around type 2-CT specifications. Specifically, the Sigma-Delta acquisition circuit uses a heavy duty current shunt in place of a CT for acquiring electric

current, a passive RC filter, a Sigma-Delta modulator (SDM) and a digital filter. This circuit, when implemented will replace the CTs, offering an alternative way to acquire and measure the electric current.

The basic transformer technology hasn't been changed for more than 50 years, although transformer manufacturers continue to refine the design and process [2]. The transformer devices continue to be large, heavy and bulky due to their electromagnetic characteristics. Instrument current transformers are intensively used in power distribution system at 50 Hz and 60Hz frequency [1]. While they provide excellent efficiency up to 99.75% [7], their large physical sizes and weight pose a challenge in product mechanical integration and robustness, as well as cost effects and other disadvantages as discussed in Section 2.2.2. On the other hand, the Sigma-Delta acquisition circuit offers very high circuit integration. In addition, the Sigma-Delta modulator and the analog-to-digital converter (ADC) technologies are improving steadily with faster processing speed and higher resolution that help the relay to measure the signal more accurately. The device components continue to get faster, smaller and cheaper, which will help bring down the cost and improve the performance of the circuit over time.

Chapter 2. Literature Review: Current Sensing Techniques

The techniques available for current sensing are based on the following principles: Ohm's law of resistance, Faraday's law of induction, electric/magnetic fields, and the Faraday Effect [1].

2.1. Ohm's law based sensor

First, the current shunt, a device based on Ohm's law of resistance, is the easiest and simplest method for current measurement. Current shunts are used extensively in power electronic circuits due to their low cost, small sizes and reasonable accuracy. Current shunts can be used to acquire both AC and DC currents. The Ohm's law states that the voltage drop across the resistor is proportional to the flowing current in the resistor element.

The ideal resistor consists of only the resistance element. The non-ideal resistor consists of a resistance element plus the parasitic resistance and inductance, as illustrated in Figure 5. These parasitic elements can affect greatly on the performance of the resistor in high current applications that will be discussed later.

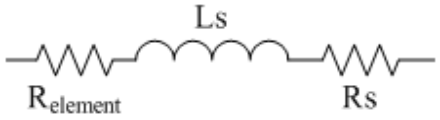


Figure 5-Equivalent shunt resistor diagram

Depending on the application, there are different types of current shunt resistors that can be applied.

2.1.1. Heavy duty coaxial shunt

In this case, the resistor can allow currents up to many thousands amperes. This type of shunt has been used to measure high current transient pulses of hundreds thousands amperes with fast rise times of nanoseconds [1]. For such applications, the high frequency behavior of the resistor is very important, and parasitic inductance and series resistance can be limiting factors for the bandwidth. There has been research on several techniques aiming at bringing the parasitic inductance in heavy duty coaxial shunt resistors down [2].

2.1.2. Surface mounted device (SMD) resistor

This resistor type offers low cost and high integration. A SMD resistor shunt can be used to measure a current up to few hundred amperes. For higher current applications the SMD resistor becomes very bulky, which may not be suitable for integration. Skin effect in the

SMD resistor is insignificant due to the small physical dimensions. Therefore, only the element's resistance and parasitic inductance affect the signal bandwidth.

The current flowing in the current shunt creates a voltage drop across it which is calculated using the formula:

$$I = \frac{V}{Z} = \frac{V}{R+j2\pi fL} \quad (1)$$

V: differential voltage across the current shunt

R: DC resistance of the shunt.

L: series parasitic inductance of the shunt.

f: signal frequency.

The impedance of the resistor is defined as:

$$Z = R+j2\pi fL \quad (2)$$

From (2), at DC level (e.g. f = 0), the impedance is purely resistive (e.g. Z = R). As signal frequency increases the reactance ($2\pi fL$) becomes significant. The corner frequency is determined when the reactance is equal to the DC resistance, or $R = 2\pi fL$, solving for f, the corner frequency is as shown in (3).

$$f_c = \frac{R}{2\pi L} \quad (3)$$

Another important characteristic of the SMD shunt resistors is their thermal drift. Ideally, given a fixed current flowing in the shunt, the differential voltage is fixed and is proportional to the R*I product (V = R*I). In reality, the current shunt resistance varies with temperature. This variation is due to the temperature coefficient resistance (TCR) and the resistor's tolerance, causing the differential voltage to fluctuate accordingly and creating a measurement error. Going with a low TCR and tolerance helps improve the accuracy with the tradeoff of higher cost.

In addition to the thermal drift, the low resistance value of the current shunt is impacted by much higher thermal drift of the PCB copper trace it is soldered to. Shown in Figure 6, by tapping two Kelvin leads between the resistor element and the copper trace it is possible to effectively eliminate the effect of thermal drift due to the PCB trace. As a result, the Kelvin sense wires effectively exclude the trace resistance, Rcu, and only measure the voltage across the resistor element.

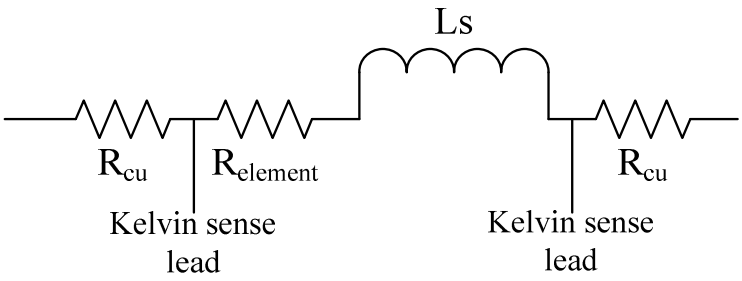


Figure 6-Equivalent shunt resistor diagram with Kelvin sense leads

2.1.3. Current shunt resistor based on the printed circuit board's trace resistance

Without the need of any additional resistor, this sensing method offers a very low cost solution for low current applications. Because no discrete resistor is needed there is no additional cost for buying and installing the resistor device. Also the power loss is limited to the copper trace's resistance. However, this method is not viable for high current or high accuracy applications such as one that is the basis of this research. For example, in order to accommodate 100A RMS AC current the copper trace has to be really thick and large. But the TCR of copper trace is relatively high (~3900 ppm/C). A large amount of current heats up the copper trace, and causes significant drift in resistance. This error can greatly degrade the measurement accuracy.

2.1.4. Other current shunt based sensing techniques

Other possible techniques include devices that use a FET's Drain-Source resistor, Rds(on), and the devices that use inductor as a sense resistor [8]. These techniques are not suitable for high accuracy applications. Specifically, in case of the FET, the Rds(on) varies depending on the gate drive threshold voltage, FET parameters, and temperature. The latter technique using an inductor has a benefit of saving power loss and reducing the cost compared to a sense resistor. Yet it has high temperature drift due to high TCR of the copper wire in the inductor.

2.1.5. Limitations in high current applications

The power dissipation due to the resistance can be substantial in high current applications, since it is proportional to the square of the current (e.g. $P = I^2*R$). The parasitic inductance in the shunt can limit the bandwidth at high frequency. These effects can limit the use of current shunts in high current applications.

The main drawback is the electrical connection from the current shunt to the sensing circuitry needs to be isolated in order to protect the electronics from the electric and magnetic transients.

2.2. Faraday's law of induction based sensors

The second current sensing technique is based on Faraday's law of induction and is employed in magnetic sensing devices such as Rogowski coils and CTs. These devices are built based on the principle that a current flowing in a conductor generates a magnetic field around it. If another conductor is placed close to the current carrying conductor, the magnetic field induces current in the second conductor. The construction of these two types of devices is generally similar. They consist of a core with the conducting wire wrapping around the core path. The current-carrying conductor to be measured is placed through the center of the core.

2.2.1. Rogowski coil

The Rogowski coil uses a core made of a nonmagnetic material. The primary current in the conductor creates a magnetic flux in the coil. The induced voltage across the coil terminal is proportional to the change in current in the conductor. The Rogowski coil requires an integrator to get a voltage proportional to the primary current. Figure 7 illustrates the schematic of the Rogowski coil with an integrator.

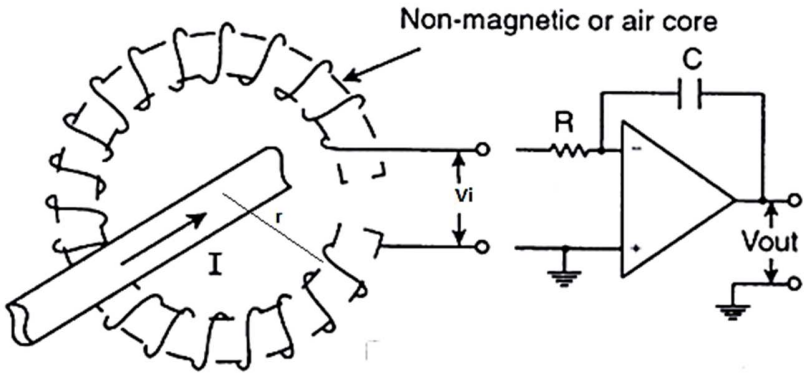


Figure 7-Rogowski coil [8]

The terminal voltage of the Rogowski coil is defined by the formula [8]:

$$V_i = \frac{-\mu_0 NA}{2\pi r}\frac{dI}{dt} \quad (4)$$

With:

μ_0: permeability of free space.

N: number of turns/length of the coil.

A: cross sectional area of the coil.

r: radius of the core.

I: current in the conductor.

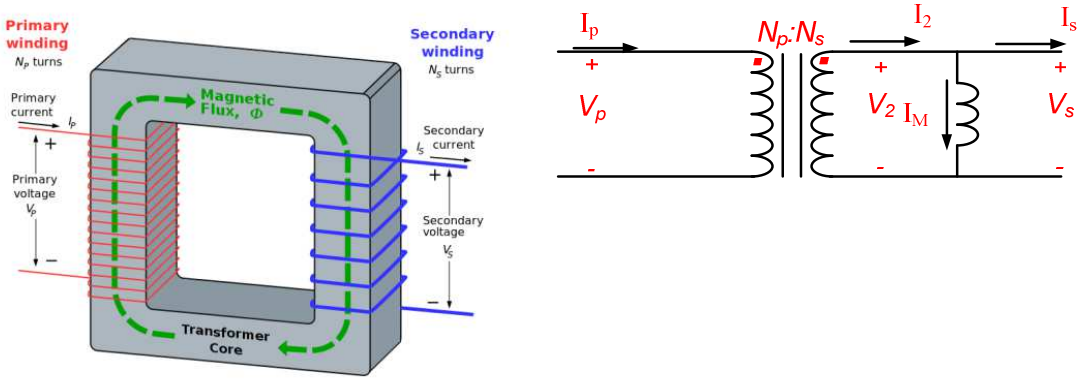
The relationship between the output voltage of the integrator and V_i is [8]:

$$V_{out} = \frac{1}{RC}\int V_i dt \quad (5)$$

The major benefit of the Rogowski coil is that the core never gets saturated since it is either non-magnetic or air. Therefore, the output remains linear and the bandwidth can extend into megahertz range [8]. The disadvantages of the Rogowski coil are the inability to measure DC current and large physical size. Also the position of the current carrying conductor inside the coil affects the measurement accuracy.

2.2.2. Instrument Current Transformer (CT)

For a CT, the core is magnetic with high relative permeability. In electric power systems, the CTs are widely used to step down the electric power line current for measurement. A CT is basically comprised of 2 separate windings called primary and secondary windings as shown in Figure 8 a).



a) Conceptual model of a CT b) Equivalent CT model representation

Figure 8-Typical Current Transformer

Figure 8 b) shows an equivalent schematic model of the CT. Notice that the CT requires a small amount of magnetizing current I_M to establish the flux in the core.

The basic operation principle of the CT is as follows. An introduction of an AC current in the primary winding creates a magnetic flux around the wire as well as in the core. The magnetizing force that creates the magnetic flux is called magnetic field strength H. The magnetic flux in the core in turn induces a current in the secondary winding. Depending on the winding turns ratio, one can control the amount of the current in the secondary to the desired level. The turns ratio of the primary and secondary windings determines the ratio of the input and output current, as shown in (6).

$$I_s = \frac{N_p}{N_s} I_p \tag{6}$$

Where:

I_p: current in the primary winding.

N_p: number of turns in the primary winding.

N_s: number of turns in the secondary winding.

The concentration of the flux in the core is called flux density B. Different magnetic materials of the core can give higher flux concentration than the others. The permeability of a material is an important characteristic of a magnetic material as it determines how well a core material can be magnetized by a certain magnetizing force H, given as

$$\mu = \frac{B}{H} \tag{7}$$

Every magnetic material is characterized by the hysteresis loop, also known as B-H loop. Figure 9 illustrates a typical hysteresis curve of a ferromagnetic core.

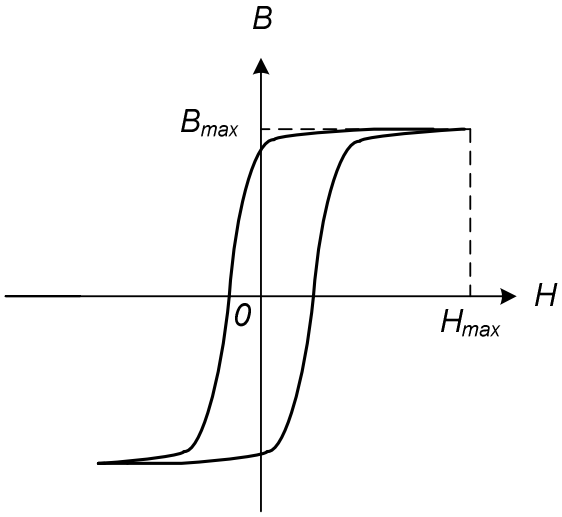


Figure 9-Hysteresis loop of a typical magnetic core.

As the driving magnetizing force H increases, the flux density B linearly increases at a rate of μ*H as given in (7). Then it increases at a slower rate at the point the core starts to saturate. When the core fully saturates the magnetizing current becomes excessive, resulting in a current error and the relationship between primary and secondary current is no longer linear. Hence, the measurement is no longer accurate [28].

Ideally, the transformers should be lossless and perfectly coupled. That means that the current in the secondary winding is linearly proportional to the current in the primary winding. In reality, transformers are non-ideal. They possess characteristics [5] that are neglected in ideal transformers such as:

1. Loss in primary and secondary windings due to wire resistances:
   The primary and secondary windings are simply wires wound around the magnetic core having some finite wire resistance. The current flowing in the windings cause undesired heat dissipation in the wire.
2. Flux loss in primary and secondary windings due to leakage flux:
   Not all of the magnetic flux is coupled into the core. This would mean that in a CT not all primary current be completely converted to secondary current.
3. Energy loss in core due to hysteresis and eddy currents:
   Eddy currents are caused by the magnetic flux flowing in the magnetic core. It circles within the core and is perpendicular to the magnetic flux line.

4. Require magnetizing current to establish magnetic flux in the transformer core: Non ideal transformer core requires a small amount of current to establish the magnetic field in the core.

These non-ideal characteristics result in a non-linear relationship between the currents in the primary and secondary winding.

Besides the disadvantages above, there are several other issues and limitations experienced on the CTs used in commercial protection relay products, such as:

- The long settling time for the current phase angle during CT calibration contributes additional error in the accuracy.
- Magnetic cross-talk between adjacent transformers that affect the signal measurement accuracy.
- Large physical size and heavy weight create greater risk for mechanical stability.
- Magnetic core material is not consistent between different batches from the same vendor, and also among different vendors.

These issues have remained constant challenges for companies when finding ways to improve the measurement accuracy and cost control.

The main advantage for using CTs is that they provide an electrical isolation barrier. The other advantage is their flexibility in AC current regulation. The desired secondary output current can be achieved by adjusting the turn ratio of primary and secondary windings.

2.3. Electric/magnetic field based sensors.

The third current sensing method uses a magnetic field sensor such as a Hall-effect sensor or a Fluxgate sensor. A Hall-effect sensor is based on Lorentz's law that a current flowing in a thin conductor sheet experiences a force if a magnetic field is applied perpendicularly through the conductor. As seen in Figure 10, when the magnetic field is absent, the charge flows upward in an approximately straight path. In the presence of a magnetic field, B, the charge is forced to follow a curve path so that the charge accumulates on one edge of the conductor sheet, resulting in a voltage potential perpendicular to both the current and the magnetic field.

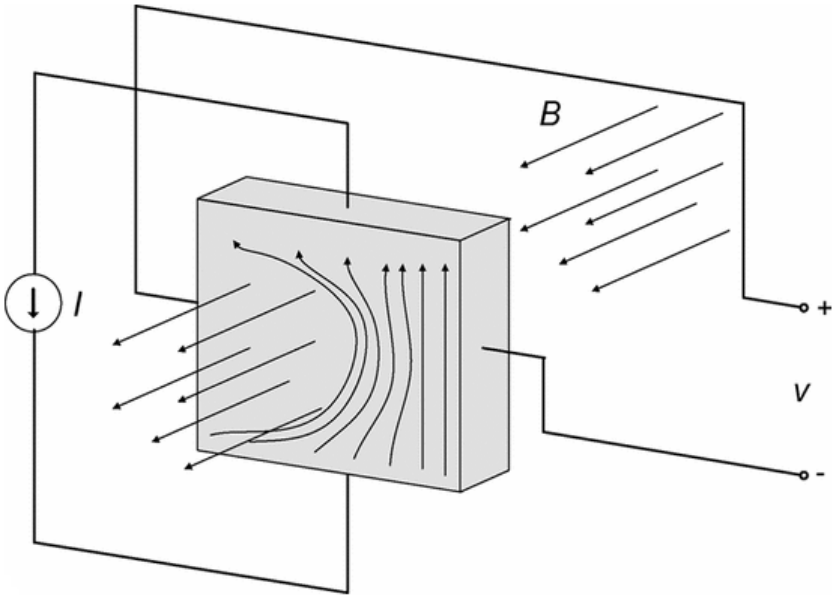


Figure 10-Hall effect sensor [1]

The generated voltage is defined by a formula:

$$v = \frac{IB}{nqd} \tag{8}$$

Where:

I: current flowing in the sheet.

B: magnetic field penetrating the sheet.

n: charge carrier density.

q: charge of the current carrier.

d: thickness of the sheet.

The sensitivity of the sensor is defined by the Hall sensor coefficient [1], [8]:

$$K_H = \frac{1}{nqd} \tag{9}$$

The resistance of the sheet is an important property of the Hall-effect sensor which determines the power dissipation.

The Hall sensor limitations include [1], [8]:

1. Low sensitivity that requires additional design to improve resolution upon which adds more cost.

2. At zero current there is an offset voltage that requires additional circuitry to compensate.
3. The frequency range is limited to 20 kHz-40 kHz.
4. The device is sensitive to mechanical stress and ambient temperature variations.

Depending on applications, there are several techniques using Hall sensor as open-loop devices and others as closed-loop devices. The simplest open-loop sensing technique is to place the Hall sensor close to the current carrying conductor, as shown in Figure 11 below.

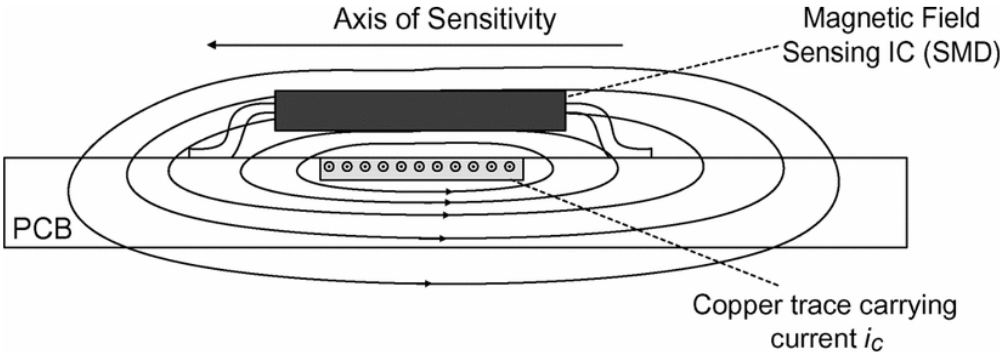


Figure 11-Simplest open-loop Hall sensor device [1].

A more complex open-loop device uses a high permeability magnetic core to concentrate the magnetic field from the current carrying conductor. There is a gap in the core that is used to place the Hall sensor, as shown in Figure 12. This technique increases the sensitivity of the sensor.

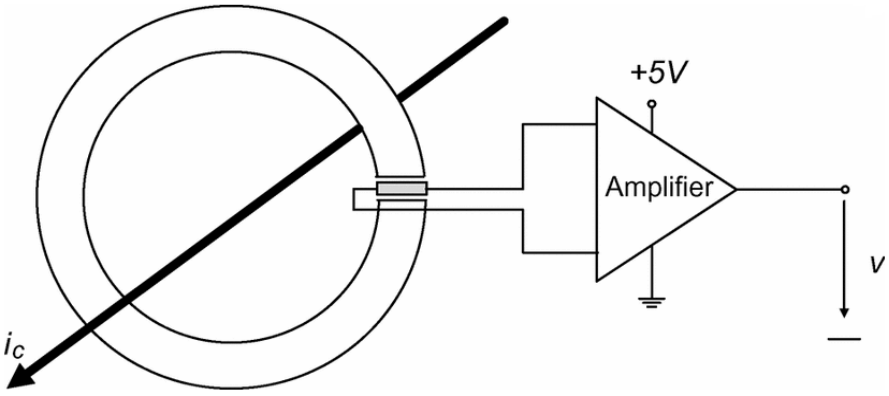


Figure 12-Open-loop using magnetic core to concentrate the flux onto the Hall sensor [1].

The open-loop methods have the advantage of being relatively simple and inexpensive. The drawback of being simple is the lack of accuracy; and the variability and non-linearity can result in significant inaccuracy in measurement. To minimize the inaccuracy, a closed-loop technique was developed in which a current is forced into an added secondary winding (see Figure 13). This current creates an opposite magnetic flux to that of the primary current in the conductor. Assuming the two magnetic fluxes perfectly cancel each other out, the secondary current is proportional to the primary current. This secondary current is passed through a resistor and can be measured to determine the primary current in the conductor.

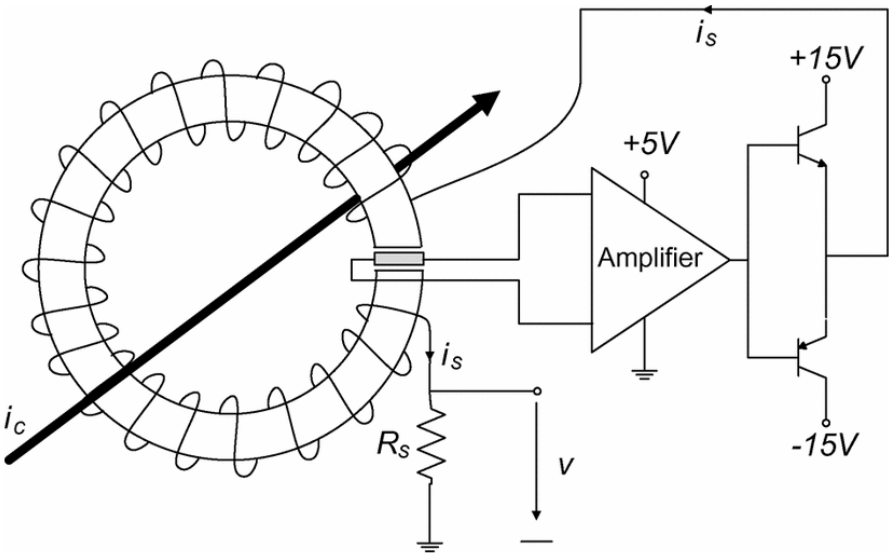


Figure 13-Closed loop Hall sensor configuration [1].

2.4. Faraday effect based current sensors

The Faraday Effect is a phenomenon that in a medium, right and left circular polarized light waves travel at different speeds if a magnetic field is applied parallel to the direction of light propagation. As a result, there will be a phase difference between the two light waves that is linearly proportional to the integral of the applied magnetic field.

The Faraday Effect can be used to measure the current as shown in Figure 14. A linear polarized light source is fed into the fiber coil with N turns that encloses a current carrying conductor to be measured. A linear polarized light wave is the superposition of a right-hand circular polarized wave and a left-hand circular polarized wave. The phase difference is linearly proportional to the current in the conductor, as shown in (10)

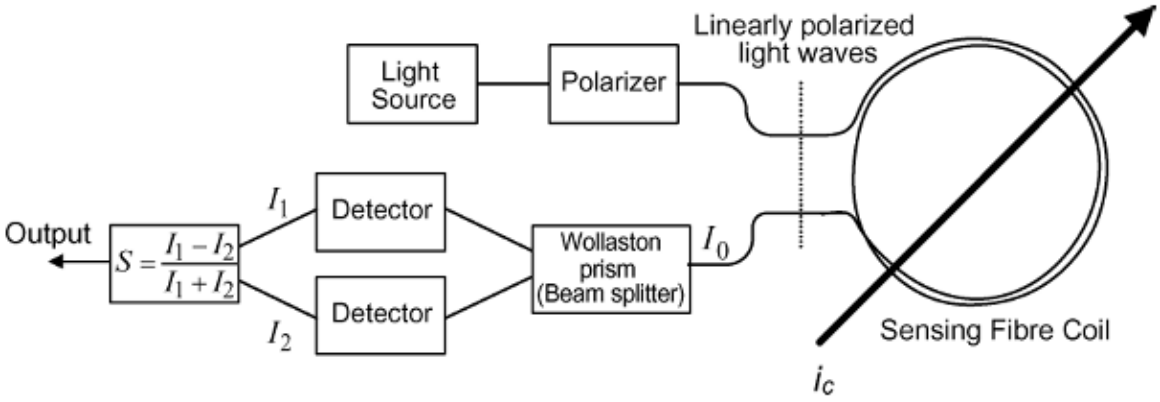


Figure 14-Optical current sensing method uses Faraday effect [1].

$$\Delta\theta = VNi_c \quad (10)$$

where:

$\Delta\theta$: phase difference between two circular polarized light waves, or the rotation angle.

V: Verdet constant, dependent on the property of the medium that describe the strength of the Faraday Effect. In this case the medium is the fiberglass.

N: number of turns of the of the fiber coil.

i_c: current in the conductor.

The rotation angle, $\Delta\theta$, is measured by injecting a light with a well-defined linear polarization state into the fiber and analyzing the polarization state of the light exiting the fiber.

The advantages of Faraday Effect based fiber-optic current sensor are that the rotation angle depends only on the current in the conductor; and that it is insensitive to stray magnetic field outside of the fiber loop, such as those caused by nearby wires or electronic components. The disadvantages include:

- The limited linearity to a small rotation angle.
- The accuracy is further reduced by birefringence due to bending the optical fiber cable. Therefore, exceptionally stable optical components are required for measuring the polarization state change.
- Mechanical vibration can yield a time-varying birefringence in the sensing fiber, which further deteriorates the accuracy.

The Faraday Effect based fiber optic current sensors are primarily used for high voltage current applications due to their superior electrical isolation characteristics. For low current applications, however, other sensing techniques are more economically attractive.

2.5. Conclusion

It is best to start with comparison tables showing different sensing techniques as discussed. Table 1 compares the performance and Table 2 compares the costs and application limitations.

		Band-width	**DC Capable**	**Accuracy**	**Thermal Drift (ppm/K)**	**Isolated**	**Range**	**Power Loss**
Shunt resistor	**Coaxial**	MHz	Yes	0.1%-2%	25-300	No	kA	W-kW
	SMD	kHz-MHz	Yes	0.1%-2%	25-300	No	mA-A	mW-W
Copper trace		kHz	Yes	0.5%-5%	50-200	No	A-kA	mW
Current Transformer		kHz-MHz	No	0.1%-1%	<100	Yes	A-kA	mW
Rogowski Coil		kHz-MHz	No	0.2%-5%	50-300	Yes	A-MA	mW
Hall Effect Sensor		kHz	Yes	0.5%-5%	50-1000	Yes	A-kA	mW
Fluxgate sensor		kHz	Yes	0.01%-0.5%	<50	Yes	A	mW-W
Fiber-Optic Current Sensor		kHz-MHz	Yes	0.1%-1%	<100	Yes	kA-MA	W

Table 1-Performance comparison among current sensing devices [1]

		Cost (USD)	Size (mm^3)	Limitation
Shunt resistor	**Shunt Resistor**	> 0.5	> 25	An overcurrent can permanently damage the shunt resistor. High power losses make it difficult to measure high currents. In high voltage applications the lack of electrical isolation is a problem
	Copper Trace	> 0.5	> 25	The accuracy is degraded by noise due to the high amplification. The bandwidth may be limited by the gain-bandwidth product of the amplifier. Measuring the trace temperature might be difficult in some applications. No electrical isolation
Current Transformer		> 0.5	> 500	A DC offset may saturate core material. For high currents a large core cross sectional area is required to avoid saturation. In high voltage applications the winding isolation becomes crucial. A high winding ratio leads to increased parasitic capacitance, which reduces the measurement bandwidth and common mode noise rejection.
Rogowski Coil		< 1	> 1000	The accuracy depends on the conductor position. Difficult to measure small currents due to poor sensitivity. A high number of turns reduces the measurement bandwidth.
Hall Effect Sensor		> 4	> 1000	AC currents with high frequency can overheat the core material. An overcurrent incident introduces a magnetic offset that can only be eliminated with a degaussing cycle. Distinct thermal drift that has to be compensated.
Fluxgate sensor		> 10	> 1000	Some variants induce notable voltage noise into the primary winding. Complicated control electronics. A high number of turns reduces the measurement bandwidth.
Fiber-Optic Current Sensor		> 1000	> 10^6	Due to high complexity the device is not suitable to measure small currents. Bending stress of the cable deteriorates the accuracy.

Table 2-Costs and application limitations of the current sensing devices [1]

For medium current sensing applications where the current ranges from milli-amperes to hundreds amperes at up to few kHz range frequency, the current shunt appears to be the best device in regard of simplicity, cost, size, and bandwidth.

Comparing the hardware between the circuitry using the shunt resistor to that using the CTs in a certain commercial protection relay product, the most obvious advantage of the current shunt over the CTs is its physical size and weight of the device. For instance, the PCB area using 4 CTs channels shown in Figure 4 requires 5.1”x 6.0” of layout area, whereas it takes 4.6”x3.1” of PCB area using the current shunts including the acquisition circuits, a 2x reduction in PCB layout area (as will be shown in Chapter 5). For these reasons the current shunts are selected to experiment their performance against that of the CTs.

Chapter 3. Circuit Design

Shown in Figure 15, the proposed circuit has four isolated and identical sub-circuits. Each of them acquires and processes one single phase analog current, namely IA, IB, IC, and IN. Depicted in Figure 15, the current in each channel is fed by a step down CT external to the current shunt. Each circuit channel is comprised of a heavy duty, and low tolerance current shunt, a passive Low Pass Filter (LPF), and a Sigma-Delta modulator which also provides isolation. A Field Programmable Gate Array (FPGA) processes the 4 modulator outputs while providing the same clock signal to all four Sigma-Delta modulators.

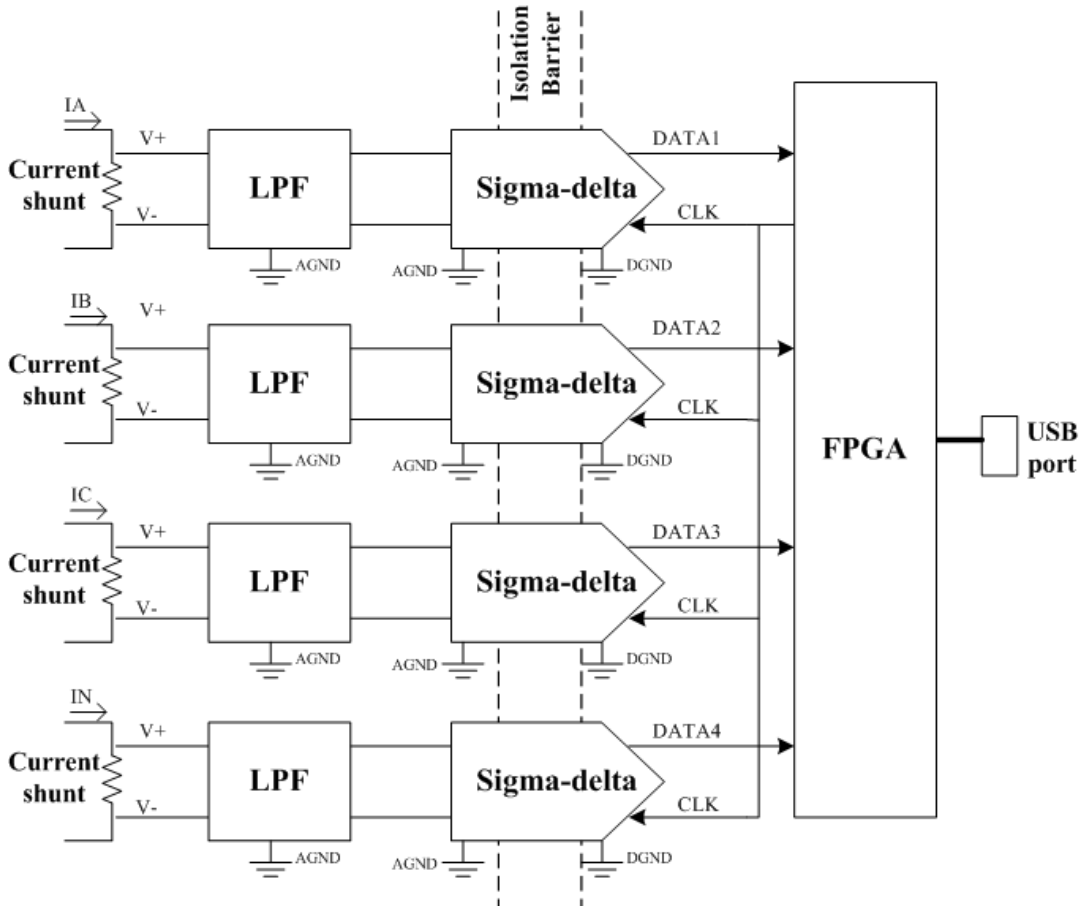


Figure 15-Top level block diagram of the SDM acquisition circuit

3.1. Circuit overview

A 60 Hz AC current flowing in the current shunt creates a differential voltage across the shunt. All electronic components in the circuit must be protected from electrical and electromagnetic transients which can cause malfunction, degradation in performance, damage to the equipment, or potential risk of electric shock to human users. The purpose of the passive RC Low Pass Filter is to slow down the rising edges of the transients that can be harmful to the Sigma-Delta modulator while allowing the signal of interest, at 60Hz and below, and up to its 16^{th} harmonic to pass through. That is, the LPF allows signals from DC level up 960Hz to pass to the isolated Sigma-Delta modulator.

The Sigma-Delta modulator serves two purposes: first, it provides the same electrical isolation as the conventional CT does; second, it samples the analog voltage at a fast rate in order to achieve higher resolution and lower quantization noise. The output of the modulator is processed by a digital filter to remove noise and reduce the sampling rate to a desired frequency usable to the processor. The Sigma-Delta modulator offers better resolution than a conventional ADC by using an oversampling method [6].

3.2. Circuit components

3.2.1. Current Shunt

The current shunt is used to convert the current into a differential voltage as described in Section 2.1.2. For the application at hand, the shunt is specified to carry a 60 Hz current ranging from minimum of 5A RMS to 20A RMS, and can be able to survive a 500A RMS inrush current for 1 second without degrading or changing its material properties. In order to carry such high current, the current shunt has to be relatively low in resistance, tolerance and TCR; because any fluctuation in the resistance can affect the measurement accuracy. However, as the resistor becomes more precise it becomes harder to manufacture, and more processes are required during manufacturing to control the resistor quality. Therefore, the associated manufacturing cost increases.

Another requirement that determines the value of the current shunt resistance is the amplitude of the differential voltage across the input of the modulator. According to the modulator's specification the full scale input range is ±320 mV peak-peak. Any value beyond this range will turn on the protection diodes of the Sigma-Delta modulator, and if too much of the

current (e.g. > 10mA) flows in the protection diode it will cause permanent damage to the device. For these reasons the current shunt was chosen to be about 1 mΩ, ±1% tolerance, ±100 ppm (parts per million), with 5nH and 1pF in parasitic inductance and capacitance typical for this size of shunt.

The actual non-ideal resistor has parasitic inductance and capacitance that can be depicted by a simple model in Figure 16.

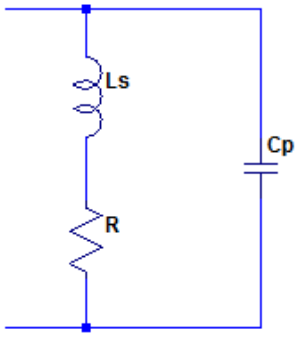


Figure 16-Simple model of a resistor.

In order to allow up to the 16th harmonic of 60Hz AC current to pass through, the current shunt has to have the cutoff frequency above 16*60 Hz = 960 Hz. With the selected shunt values, the cut off frequency can be calculated using (11):

$$f_c = \frac{1\text{m}\Omega}{2\pi * 5\text{nH}} = 32\text{kHz} \qquad (11)$$

This would mean that the shunt's cut off frequency is good up to the 530th harmonic. The resonant frequency of the non-ideal resistor shown in

Figure 16 is calculated by (12) [9]:

$$\omega_o = \sqrt{\frac{1}{L_s \cdot C_p} - \frac{R^2}{L_s^2}} \qquad (12)$$

This formula holds true for multiple identical resistors connected in parallel. In other words, the resonant frequency remains unchanged if multiple shunts are connected in parallel. With the above selected resistor (e.g. R = 1mΩ, Ls = 5nH, Cp = 1pF), using (12) the resonant frequency is calculated as 2.25GHz, which is outside the frequency of interest. The frequency band of interest is far below the cutoff and resonant frequencies. Figure 17 shows Pspice

simulation of the impedance response of the above shunt model with the mentioned parameters.

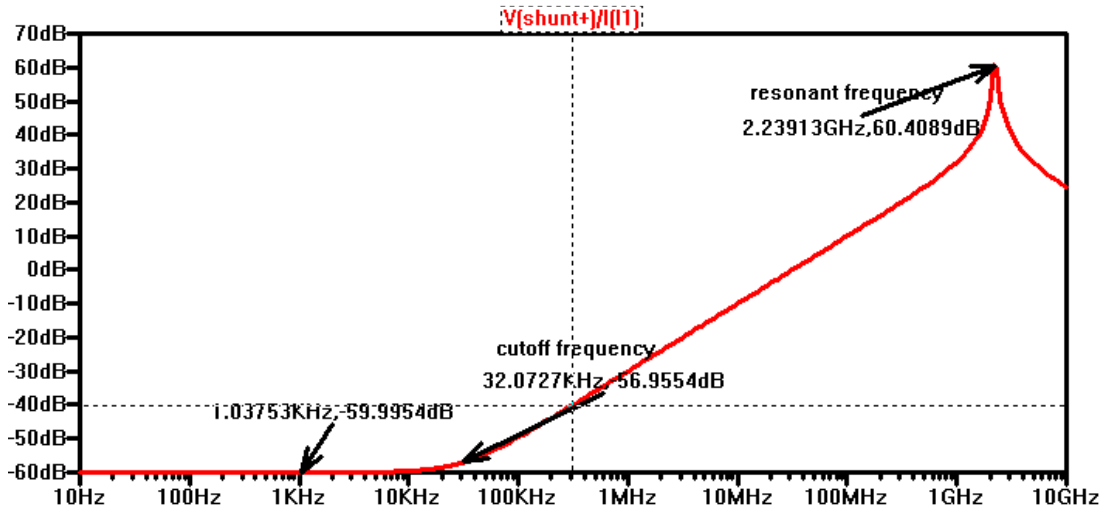


Figure 17-Current shunt impedance response.

As shown in Figure 17, at low frequency up to 10 kHz, the impedance is constant and real. As the frequency increases the above 10 kHz, the impedance becomes inductive (e.g. ωL increases). The impedance continues to increase to its peak at resonant frequency. Then it becomes capacitive and decreases beyond the resonant frequency. Any fluctuation in the impedance creates measurement error. Fortunately this occurs above 10 kHz, which is outside of the frequency of interest.

There are a few resistance models available depending on the resistor types. For the desired small resistance value (1mΩ), the proposed resistor model is deemed appropriate [9].

In order to survive 500A RMS AC current, a 1mΩ shunt has to be able to dissipate a significant amount of power as shown in (13).

$$P = I^2 * R = 500^2 * 1m\Omega = 250W \quad (13)$$

Present heavy duty SMD current shunts available in the market are rated below 10W in power rating. In order to reduce the power dissipation in the resistor, several current shunts have to be connected in parallel to share the 500A current.

3.2.2. Low Pass Filter (LPF)

The purpose of the LPF is to pass all the signals from DC level to 960 Hz and block all higher frequency signals. The second purpose of the LPF is to slow down the fast rising edge of the electrical transients coming into the circuit. These fast rising edge transients can be

overwhelming and damaging to the electronic components, such as the Sigma-Delta modulator being used in the circuit. These transients can get into the circuit via both common mode and differential mode. The passive LPF has 2 stages, each of which provide 20dB attenuation. Figure 18 shows the schematic of the LPF.

To attenuate the common mode noise, several pairs of capacitors are used, labeled as (C1, C8), (C3, C6), (C4, C7). An additional capacitor, C5, is used to attenuate the unwanted differential signal outside of the frequency band of interest. Since the LPF is used at the front end, interfacing with the transients, its ground is considered very 'noisy' and has to be isolated from the ground of the digital or data acquisition circuit, or other sensitive electronic components such as the SDM. For that reason there are two isolated grounds used for the circuit, one for the LPF and the other for the SDM. The equivalent input impedance of the SDM is also included in the simulation because it affects the dynamic impedance of the circuit (e.g. the pole locations of the LPF are affected).

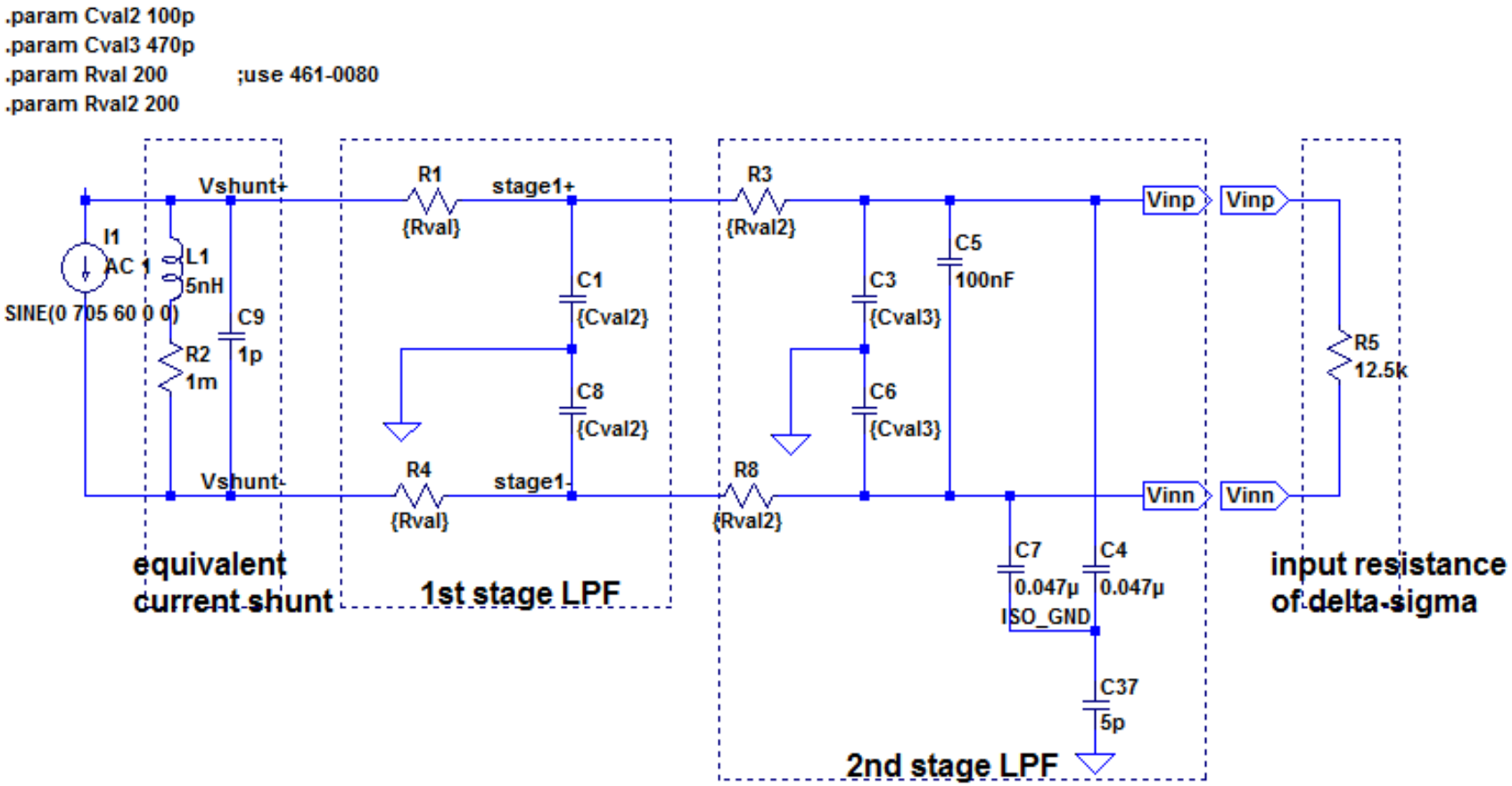


Figure 18-Complete 2nd order LPF circuit schematic

3.2.2.1. Design of First Stage LPF

Figure 19 shows the first stage of the LPF.

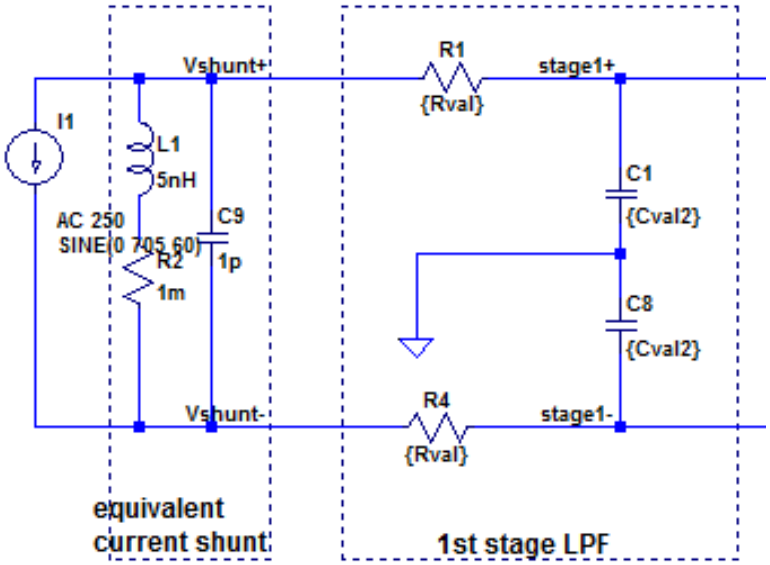


Figure 19-Schematic of first stage LPF

This 1st order LPF provides a cut off frequency (-3dB frequency) at 1.69 MHz and an attenuation of 20dB/decade. A pair of capacitors (C1, C8) are used for filtering the common mode noise that appears on both the top and bottom sides of the circuit.

The transfer function of the first stage LPF is calculated using Mathcad to determine the desired pole location, as shown in (14). The location of the first pole is calculated in (15). See Appendix A for the derivation of the first pole.

$$T1(s) = \frac{1}{s*C1*R1+1} \tag{14}$$

$$f_{pole1} = \frac{1}{2\pi} * \frac{1}{C1*R1} = 1.693 \text{ MHz} \tag{15}$$

The Pspice simulation of the first stage LPF, depicted in Figure 20, verifies the calculation of the first pole shown in (15).

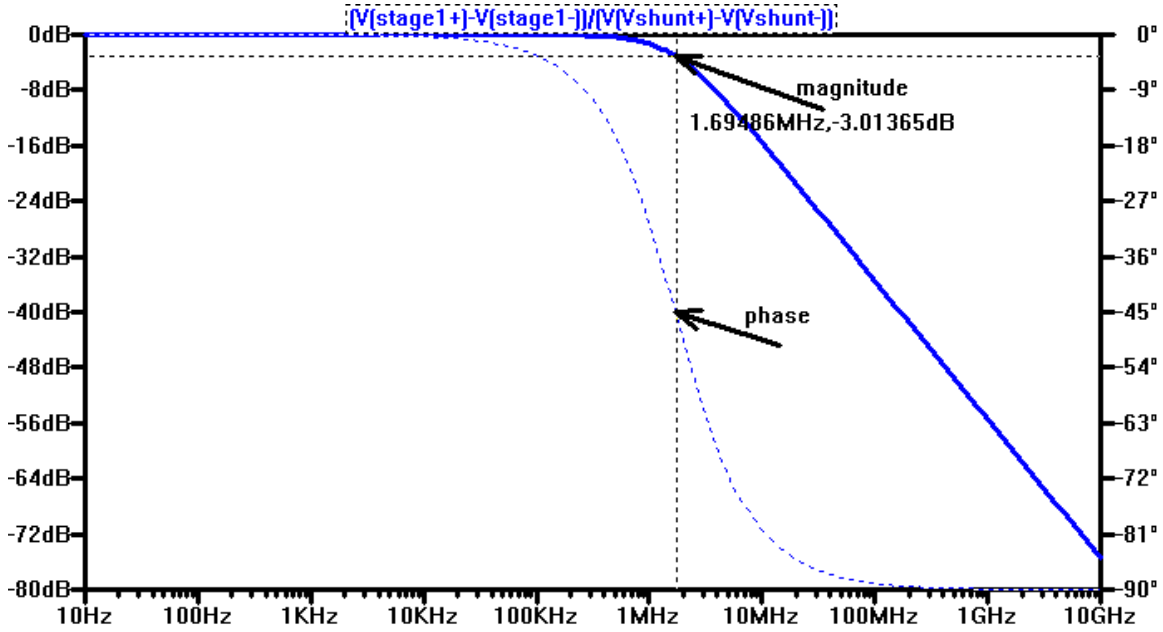


Figure 20-Frequency response of 1st stage filter

3.2.2.2. Design of Second stage LPF

The second stage of the LPF, as depicted in Figure 21, provides another roll off at 3.2 kHz and an attenuation of 20dB/decade. The capacitors and resistors are picked in regard to the safety requirements of the circuit, their availability, and ratings of the components, in order to provide the optimal performance. Here, capacitor pairs (C3, C6), (C4, C7) are used to attenuate common mode noise. Even though these two pairs have different grounds as mentioned at the beginning of Section 3.2.2, they will be considered one ground for simplifying the calculation in Appendix B.

The modulator ground is isolated from chassis ground by using ISO_GND plane. The purpose of having the modulator ground isolated is to prevent noise from the chassis from coupling in to affect the modulator performance.

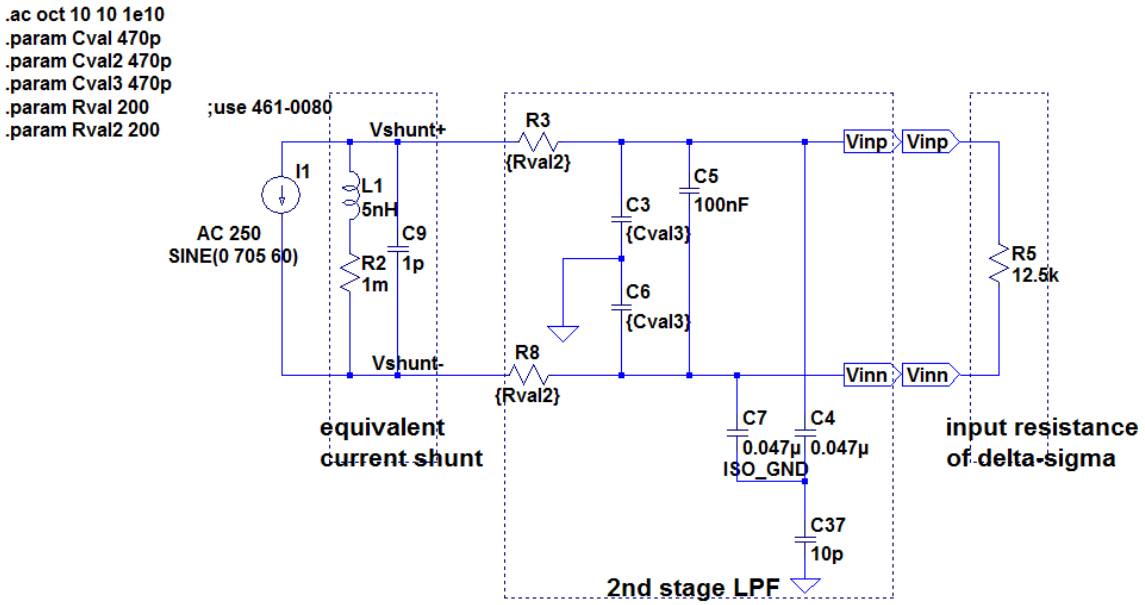


Figure 21-Second stage LPF

The second order LPF transfer function is given by (21). The formula for the second pole is given by (22). The detailed calculation is shown in Appendix B.

$$T1(s) = \frac{1}{s(C3*R3 + C5*R3) + 1} \tag{16}$$

$$f_{pole2} = \frac{1}{2\pi}\frac{1}{C3*R3+C4*R3+2C5*R3} = 3.216\ \text{MHz} \tag{17}$$

The 2nd stage LPF simulation, as depicted in Figure 22, verifies the calculation of the second pole. The simulation results confirm adequate performance.

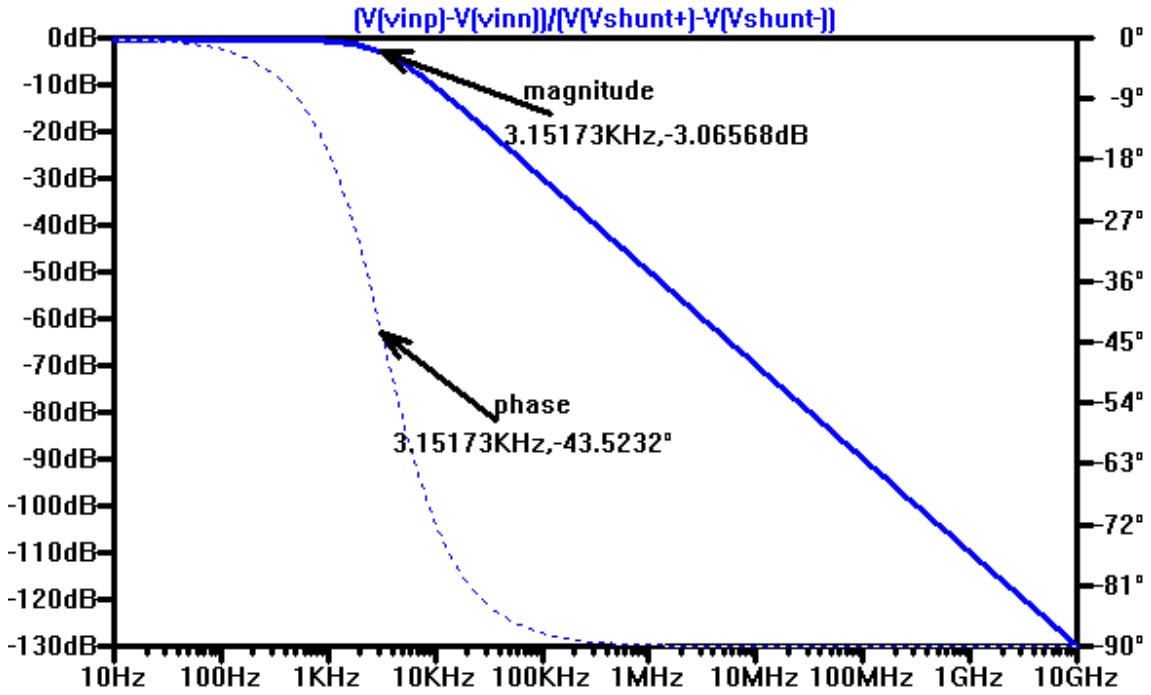


Figure 22-Frequency response of second stage LPF

3.2.2.3. Cascading two filters to make 2nd order LPF, Mathcad versus Pspice simulation

Theoretically, when cascading two 1st order filters together one would obtain a 2nd order filter with poles determined by each individual 1st order filter. Figure 23 shows the response of the 2nd order cascaded LPF by cascading two filter stages described in (14) and (16). As expected, the first roll off occurs at about 3.2 kHz with 20dB/decade of attenuation. The second roll off occurs at 1.69 MHz with another 20dB/decade of attenuation. The total attenuation after the second roll off is 40dB/decade.

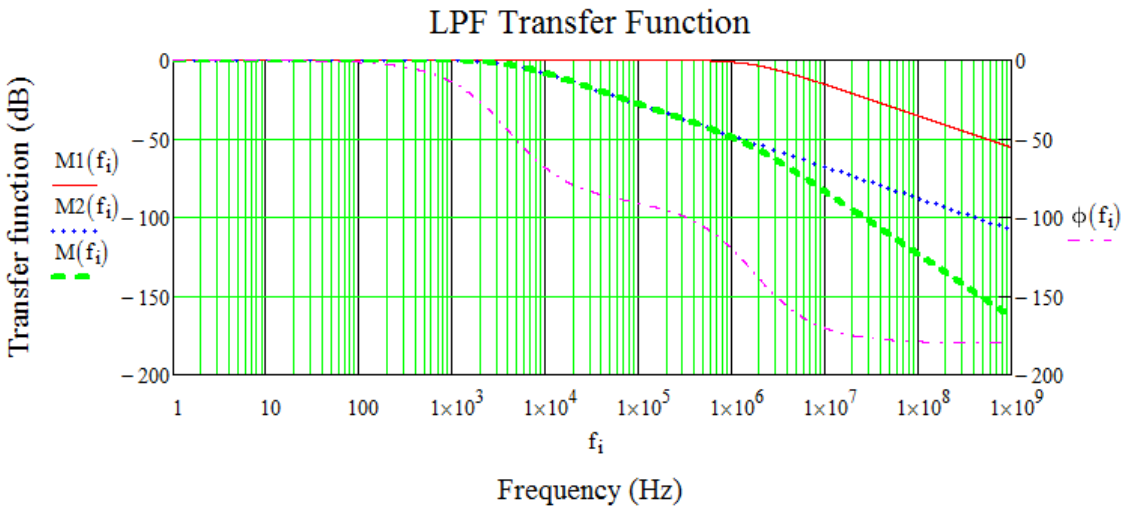


Figure 23-Cascaded 2nd order LPF transfer function response using Mathcad

In practice, each stage of the filter has its own dynamic impedance and it affects the neighboring network. As a result when cascading the stages together the poles in the cascaded circuit are no longer the same, as shown in Figure 24.

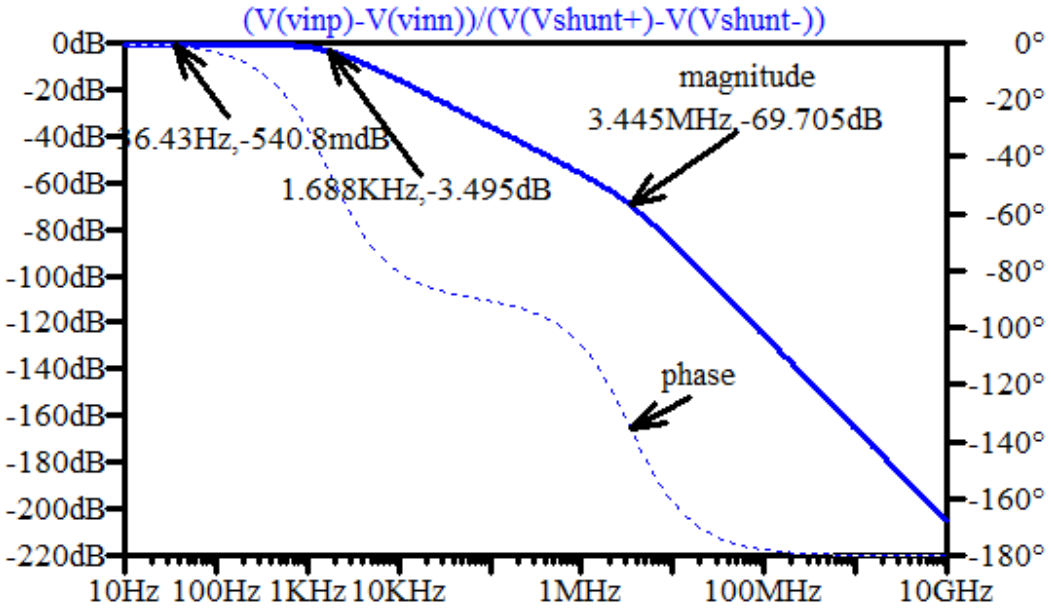


Figure 24- Pspice simulation of cascaded 2nd order LPF transfer function response simulation

Calculating the effect of the dynamic impedance is difficult and not practical. Therefore, the alternative of a Pspice simulation is a preferred choice.

3.2.3. Sigma-Delta Modulator (SDM)

The SDM takes a filtered analog signal from the LPF, samples it and converts to a single-bit digital stream of **1**s and **0**s accordingly to the level of the analog signal, as shown in Figure 25.

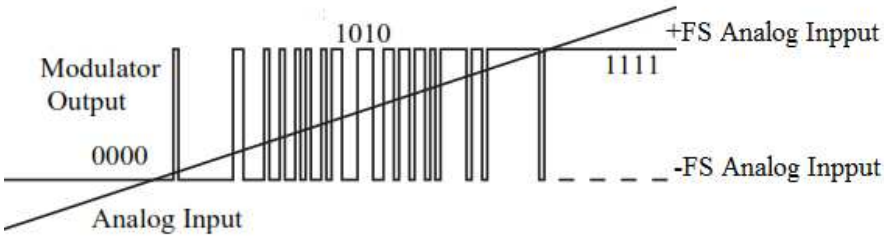


Figure 25-Modulator digital output stream versus analog input voltage

For example, consider a sinusoidal analog signal input. When the analog signal voltage is at a positive peak the modulator outputs all **1**s. When the analog input decreases toward 0V, the number of **1s** decreases and number of **0s** increases at the modulator output. When the analog input reaches 0V, the modulator outputs equal numbers of **1**s and **0**s. When the analog input becomes more negative, the modulator outputs more **0**s than **1**s; and eventually all **0**s as the voltage reaches negative peak.

The SDM uses an oversampling technique to sample an analog signal at a much higher rate than the Nyquist frequency. The Nyquist frequency is defined as twice the signal frequency, violating it by sampling below it causes an aliasing effect and the original signal cannot be fully reconstructed. In any analog-to-digital conversion the quantization noise is inevitable. It is the difference (error) between the analog value and the closest digital representation. The maximum quantization error of an ideal converter is ±1/2 LSB (Least Significant Bit), as shown in Figure 26.

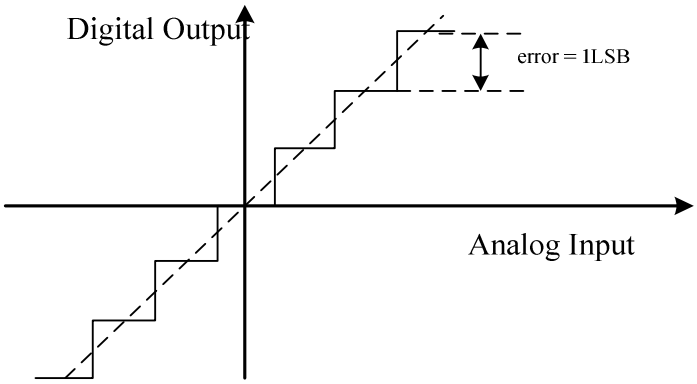


Figure 26-Quantization error in ideal AD conversion

Increasing the sampling frequency will not affect the signal power and the total quantization noise [11]. Therefore, the total ratio of signal-to-quantization noise (SNR) doesn't change. The SNR is defined as the ratio of the average signal power to the average noise power. However, oversampling spreads the same quantization noise over a larger frequency range. If the appropriate filter is used to filter out the noise outside of the signal band, the SNR is improved.

Knowing that increasing the oversampling ratio together with applying the digital filter improves the SNR, leads one to ask how much of an improvement an oversampling can offer.

For a frequency span from dc to the Nyquist frequency (Fs/2), the SNR of an ideal 1-bit ADC is approximated by (18) [12].

$$SNR = 6.02*N+1.76 \quad (18)$$

Where:

SNR: signal-to-noise ratio in decibel (dB).

N: number of bits in the converter. In this case of 1-bit ADC, N = 1.

The above equation depicts the maximum SNR with the assumption that the ADC is ideal. That is, only quantization noise exists. All other noise sources are ignored, such as thermal noise, reference noise, clock jitter, etc.

Another measure called signal-to-noise and distortion ratio (SINAD) to show the overall dynamic performance of an ADC. SINAD is defined as the ratio of the signal to noise plus the harmonic distortion. It is good to measure the overall performance of the ADC because

it includes all the components that make up noise and distortion. SINAD is converted into the effective-number-of-bits, ENOB, similar to (18), as follows:

$$SINAD = 6.02*ENOB+1.76 \quad (19)$$

As mentioned, SNR in (18) is calculated over Nyquist bandwidth range f_{Nyq}. The actual signal bandwidth is smaller. If a digital filter is used to filter out the noise outside the signal bandwidth f_s, then the SNR will be improved by a factor of k_F as shown in (20) [12].

$$k_F = \frac{f_s}{f_{Nyq}} = \frac{f_s}{2f_{sig}} \quad (20)$$

Where:

f_s: sampling frequency

f_{Nyq}: Nyquist frequency, which is twice the signal frequency f_{sig}.

The oversampling ratio, OSR, is defined as the ratio between the oversampling rate and the Nyquist rate [14]. In other words, the OSR tells how much faster than the Nyquist rate a particular ADC is oversampling. (20) can be re-written as:

$$k_F = \frac{f_s}{f_{Nyq}} = \frac{f_s}{2f_{sig}} = OSR \text{ , or in dB: } k_F = 10\log(OSR) \quad (21)$$

OSR is often expressed in a power of 2, or $OSR = 2^m$, where m is an integer.

Combining (18) and (21) the SNR becomes: [12]

$$SNR = 6.02*N+1.76+10\log(2^m) \quad (22)$$

Or equivalently,

$$SNR = 6.02*N+1.76+m*3dB \quad (23)$$

From (23), it can be seen that the SNR improves by 3dB, or 0.5 bit, for every doubling of the sampling frequency. Therefore, a 1 bit increase in resolution is equivalent to a 4x increase in oversampling (or 2^{2*1}).

Generally, to improve the equivalent resolution by just using oversampling it is required to oversample by a factor of 2^{2N} to get an N-bit in resolution. To achieve a 16-bit resolution the modulator has to oversample by a factor of 2^{32}, which is not realizable.

The SDM overcomes this limitation by employing oversampling and noise shaping techniques in conjunction with digital filtering. A first order SDM improves the SNR by approximately 9dB (or 1.5 bits) per every doubling of oversampling frequency. A second order SDM improves the SNR by 15dB (or 2.5 bits) for each doubling of oversampling [14],

[18]. Therefore, with the appropriate digital filter used, the SNR improves significantly more than the conventional ADC. Figure 27 shows the effect of oversampling with a conventional ADC versus oversampling and noise shaping with Sigma-Delta converter.

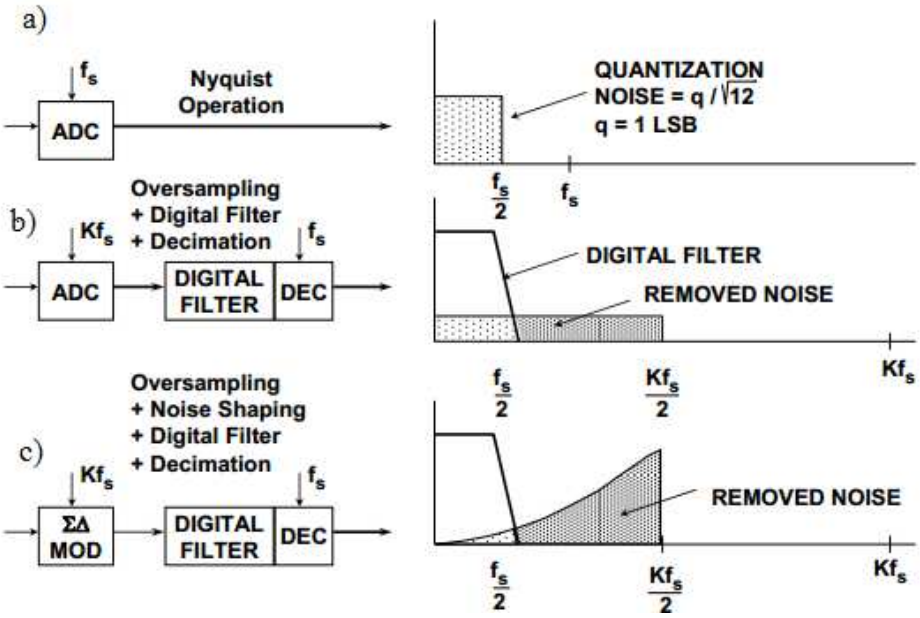


Figure 27-Effect of oversampling and noise shaping on SNR [6].

a) Without oversampling on conventional ADC

b) With oversampling factor K on conventional ADC and digital filter

c) With oversampling, noise shaping and digital filter on Sigma-Delta converter

The disadvantage of the SDM is its slow data output rate compared to conventional ADC due to the averaging method of the digital/decimation filter used (will be shown later in Section 3.2.4). The AMC1204 modulator used in this research has a data rate of 78 kSps (kilo-samples per second) [16]. In protection relay application, a 60 Hz AC signal is typically sampled at 8 kSps so the slower data output rate is not a concern. Depending on the applications in protection relays, it can take from 0.5 cycle to 3 cycles of a 60 Hz signal for a relay to examine a fault. That is, the protection relay makes a decision to trip, or not to trip the circuit breaker about 8 ms to 50 ms after the fault has occurred.

3.2.3.4. SDM's theory of operation

The first order SDM is comprised of four functional blocks: summing stage, integrator, comparator (1-bit ADC), and 1-bit DAC. Figure 28 shows a block diagram of a first order

SDM. For simplicity assume a DC analog voltage input at V_{IN}. The summing stage calculates the difference of V_{IN} and the analog voltage at node B. The integrator constantly ramps up or down at node A. As the voltage at node A reaches the threshold the comparator outputs 1 or 0 depending on its previous state. The 1-bit DAC converts the comparator logic output to analog voltage ($+V_{REF}$ or $-V_{REF}$), ready to feed back to the inverting input of the summing stage; and the sampling process repeats. The negative feedback through the DAC forces the average voltage at node B to be equal to V_{IN}. The average voltage at node B is controlled by the number of **1s** at the comparator output. As V_{IN} increases, the number of **1s** increases, as does the average voltage at node B; and vice versa. A single bit from the comparator doesn't provide any meaningful information. Only when a large number of samples are averaged, will the average voltage at node B becomes meaningful, implying the input voltage V_{IN}.

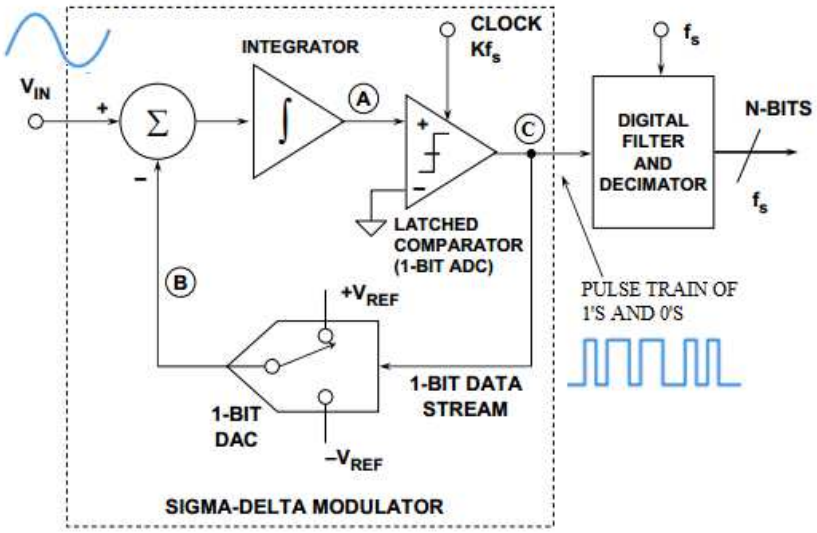


Figure 28-First order SDM functional block diagram[11]

The second order SDM in Figure 29 uses more than one summing stage and integrator to achieve a better (sharper) noise shaping function. The output of the first integrator is further differentiated with a 1-bit DAC output and fed into the second integrator. The second order SDM can further reduce the quantization noise in the frequency band of interest to achieve better SNR. However, third or higher order SDMs experience instability and are not

recommended even though there have been methods trying to improve the stability of the higher order SDMs [19].

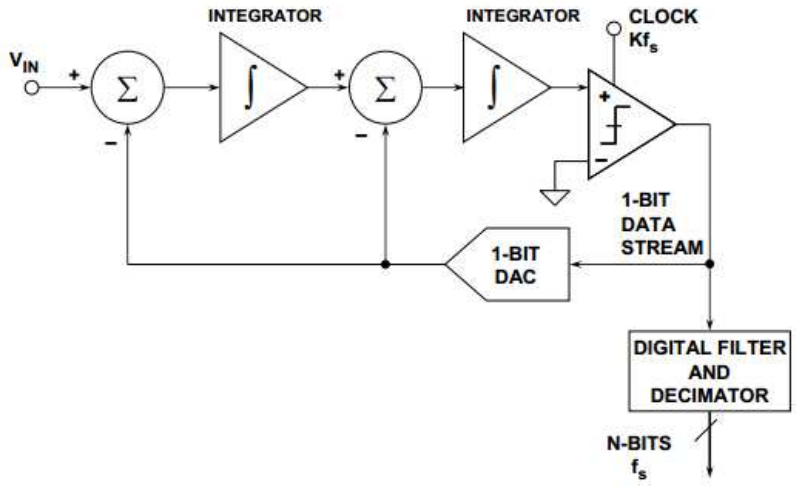


Figure 29-Second order SDM functional block diagram [11]

3.2.3.5. AMC1204 Sigma-Delta modulator

The SDM used in this circuit is a second order, isolated modulator with 1-bit digital output with a maximum sampling speed of 20MHz. This modulator is used to provide the galvanic isolation barrier between the analog and the digital network. The isolation is provided by the silicon dioxide (SiO_2) material that has been certified to provide isolation up to 4000V peak according to UL1577, IEC60747-5-5, and CSA standards [16]. The key specifications of the modulator include:

- SNR: 84 dB minimum.
- Common Mode Transient Immunity (CMTI): 15kV/µs.
- Full scale differential input voltage: ±320mV.
- Isolation voltage: 4000 V peak.
- Common mode rejection ratio (0-10kHz): 108dB.
- Effective Number of Bits (ENOB): 14

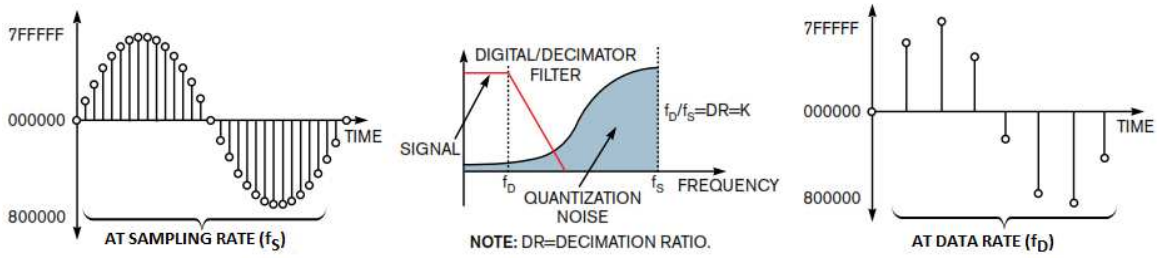
The AMC1204 modulator isolation characteristics are as follow:

Parameter	Test Conditions	Value	Unit
Maximum working insulation voltage per IEC		1200	V_{peak}
Partial discharge test voltage per IEC	t = 1s (100% production test), partial discharge < 5pC	2250	V_{peak}
Transient overvoltage	t = 60s t = 1s	4000 4800	V_{peak} V_{peak}

Table 3-AMC1204 modulator isolation characteristics [16]

3.2.4. Field Programmable Gate Array (FPGA) Implementation of digital LPF

A FPGA is used to implement a digital Low Pass Filter (LPF) to average and down sample the 1-bit stream code from the modulator and convert it to a digital representation of the analog voltage. The digital LPF rejects the high frequency-quantization noise and removes aliases beyond the band of interest. Shown in Figure 30, the analog signal is sampled by the SDM at sampling frequency, f_S, to get high resolution digital output (see Figure 30 a). The consequence of this high sampling rate is that the noise is shaped and pushed toward sampling frequency f_S; and the digital filter rejects noise beyond the frequency f_D (see Figure 30 b). This results in improvement in SNR since most of the noise is filtered out. Then, the filtered digital data output is decimated at frequency of f_D (see Figure 30 c).



a) b) c)

Figure 30-Digital/decimation filter[17].

a) High resolution discrete data output at sampling rate fs

b) Digital filter rejects high frequency noise and allows data at low frequency (f_D)

c) Output data rate at f_D

In the decimation process, M samples of the digital stream from the SDM are averaged to convert to a digital representation. Then one in every M samples is saved and the rest are

discarded. By doing this the original sampling frequency, f_s, is reduced to fs/M. A higher decimation ratio (larger M samples) results in better accuracy. However the system throughput will be slower. Note that the term 'decimation ratio' also implies 'oversampling ratio' as mentioned in earlier sections. In other words, M simply implies OSR.

The most popular digital filter being used in the SDM is the $Sinc^K$ function filter [14], where K is the order of the filter. The value of K should be 1 plus the order of the modulator [14]. For a second order SDM, a $Sinc^3$ filter is recommended. The filter with higher order has better SNR. Also, a higher the decimation ratio results in better SNR. Figure 31 compares the SNR graphs of 1st, 2nd, and 3rd order Sinc filters.

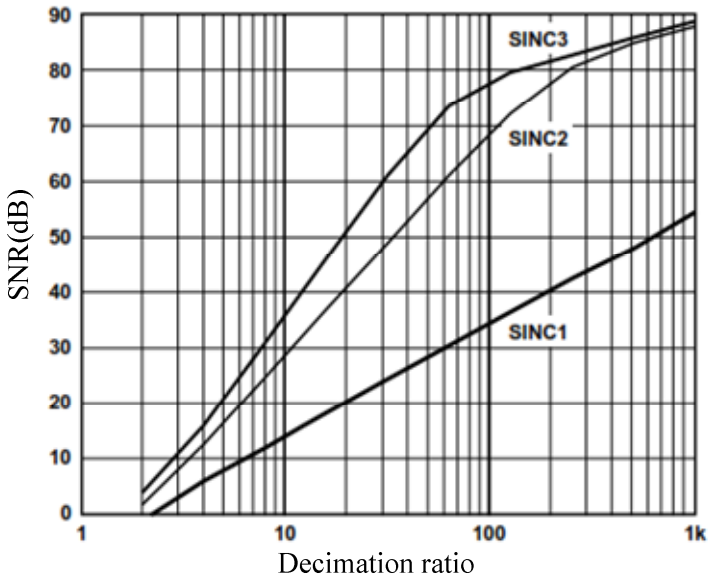


Figure 31-SNR vs. decimation ratio for different Sinc filter types [15].

The $Sinc^3$ function has the following transfer function:

$$H(z) = \frac{1}{M}\left(\frac{1-z^{-M}}{1-z^{-1}}\right)^3 \quad (24)$$

Where:

M: decimation ratio, also known as oversampling ratio (OSR).

The frequency response of the Sinc filter is obtained by evaluating (24) at $z=e^{j2\pi f}$

$$\left|H(e^{j2\pi f})\right| = \left|\left(\frac{\operatorname{sinc}(M\pi f)}{\operatorname{sinc}(\pi f)}\right)^3\right| = \left|\left(\frac{\sin(M\pi f)}{M\sin(\pi f)}\right)^3\right| \quad (25)$$

with: $\operatorname{sinc}(f) = \frac{\sin(f)}{(f)}$

The frequency response of the Sinc function with different orders is shown in Figure 32:

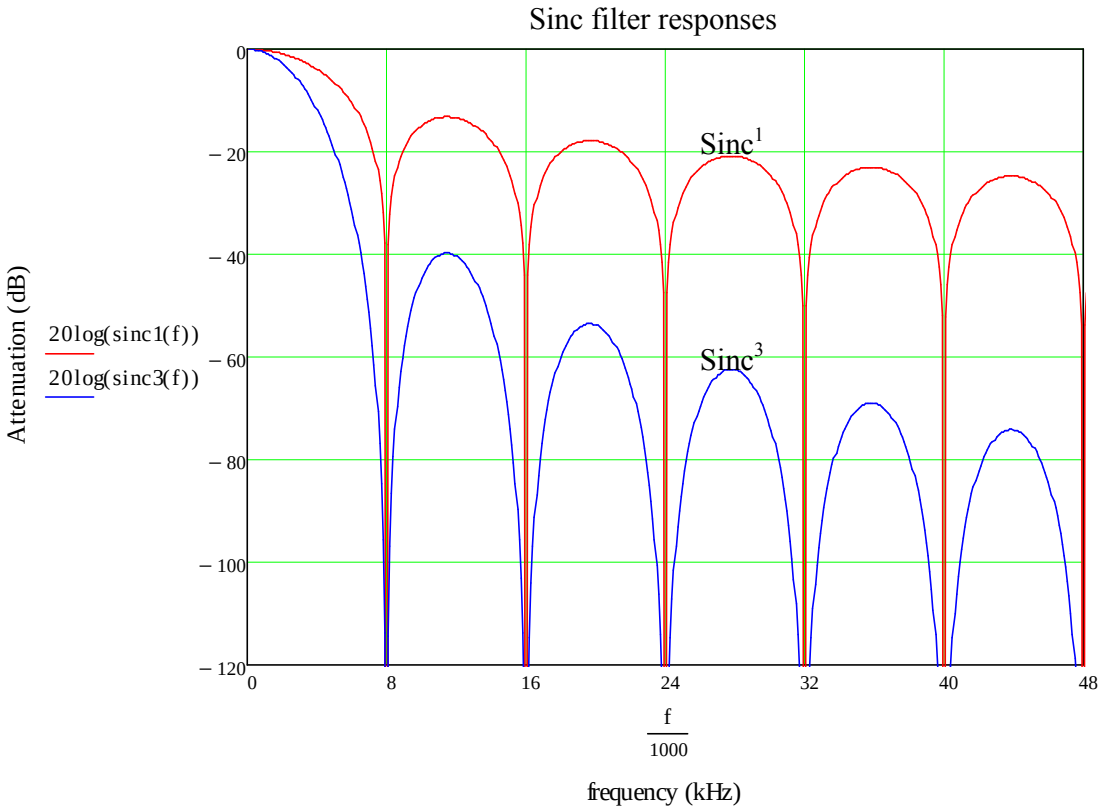


Figure 32-Frequency response of different Sinc filters.

The nulls exist at multiple frequencies of f = 1/M. If this frequency is the sampling frequency, f_S, then the nulls exist at multiples of $f = f_S/M = f_D$, (e.g. $f = n*f_D$, n = 1, 2, 3, …)

(24) can be re-written by factoring out

$$H(z) = \left(\frac{1}{1-z^{-1}}\right)\cdot\left(\frac{1}{1-z^{-1}}\right)\cdot\left(\frac{1}{1-z^{-1}}\right)\cdot\left(\frac{1-z^{-M}}{M}\right)\cdot\left(\frac{1-z^{-M}}{M}\right)\cdot\left(\frac{1-z^{-M}}{M}\right) \quad (26)$$

The first three terms in (26) are called integrators, and the last three terms are called differentiators. The implementation of $Sinc^3$ filter is done by cascading three integrator stages operating at high frequency f_S, followed by an equal number of differentiator stages operating at low frequency f_S /M [14],[20]. The block diagram in Figure 33 depicts an implementation of the (26). There is a switch between two filter sections that reduces the sampling rate from f_S to f_S /M. The M-period delays needed to realize the z^{-M} factors can be implemented by single delay blocks z^{-1} [14]. This structure is the most attractive for hardware implementation due to its efficiency and economical advantage [21]. This structure is also known as cascaded integrator-comb decimation filter (CIC).

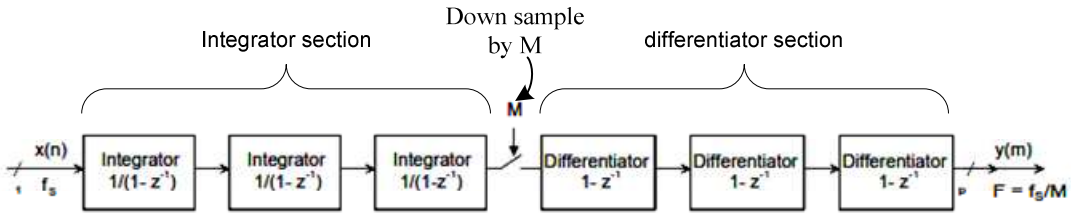


Figure 33-Basic implementation of $Sinc^3$ decimation filter.

The gain of the $Sinc^K$ filter with decimation ratio M is calculated using the following equation [20], [21]:

$$Gain_{dc} = M^K \tag{27}$$

Or, in terms of bits of resolution the gain is written as:

$$Gain_{nbit} = K \cdot \log_2(M) \tag{28}$$

The bus width of the FPGA is chosen to be 1 bit wider than $Gain_{nbit}$ to prevent overflow errors during the M clock cycles when the data is accumulated [22].

A $Sinc^3$ filter with a decimation ratio of 64 will have a gain of $64^3 = 262144$, or equivalent to 18 bits of resolution. This means it will need 18 registers, each of which holds one bit, and the bus width of the FPGA has to be at least 19 bits to prevent data overflow.

Table 4 lists the output word sizes for different decimation ratios of a $Sinc^3$ filter.

Sinc^3 filter (K = 3)			
Decimation ratio (M)	**$Gain_{dc}$**	**$Gain_{nbit}$ (bits)**	**Bus width (bits)**
4	64	6	7
8	512	9	10
16	4096	12	13
32	32768	15	16
64	262144	18	19
128	2097152	21	22
256	16777216	24	25

Table 4-Output word size vs. decimation ratio of 1-bit Sinc^3 filter.

From the SDM datasheet, the typical SNR is 88dB (under test conditions in which Sinc^3 filter is used with OSR = 256, and maximum working input voltage of ± 250mV peak to peak), as shown in Figure 34.

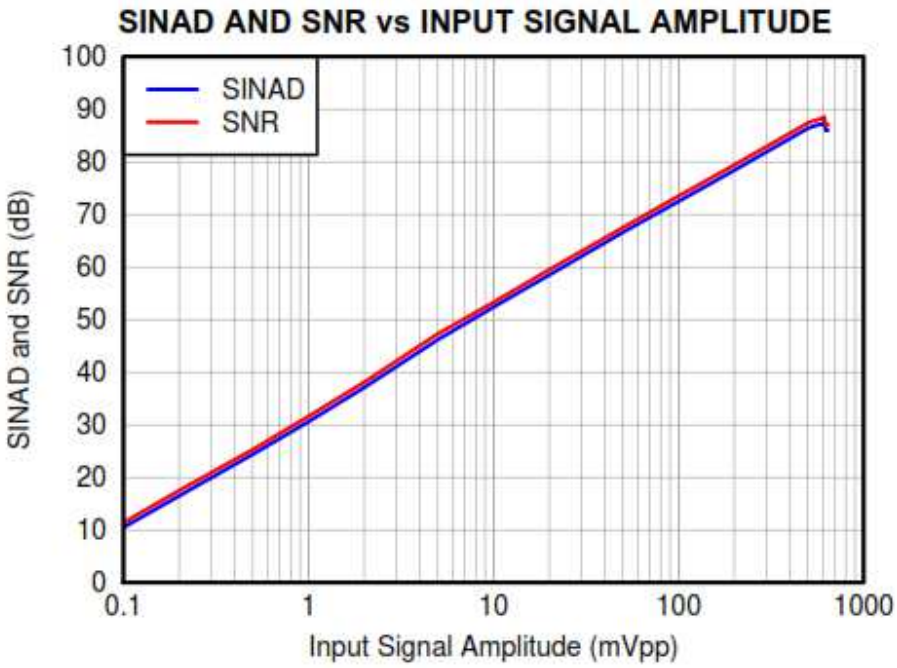


Figure 34-SNR with respect to input signal amplitude [16].

As a result, in order to maintain the specified level of SNR of 88dB, the OSR must be set at 256, and the input voltage must be at ± 250mV peak to peak. Note that the SNR is

proportional to the oversampling ratio OSR, and to the magnitude of the input voltage, as illustrated in Figure 31 and Figure 34, respectively.

With the current shunt of 1 mΩ and the current ranging from 5A to 20A RMS flows through it, the differential voltage across the current shunt is therefore at 5mV to 20mV RMS. That is, the voltage magnitude across the shunt referring to Figure 18 will be:

$$V(\text{shunt+}) - V(\text{shunt-}) = 5 \text{ mV RMS} = 5\sqrt{2} = 7.07 \text{ mV} \quad (29)$$

From the graph in Figure 34, at 5mV RMS input voltage the SNR is about 50dB; and by using (18), the effective number of bit (ENOB) is found to be about 8 bits. Similarly, with 500A RMS current the SNR is approximate about 88dB, and the equivalent ENOB is 14 bits. Although at an OSR of 256 the word size is 25 bits as shown in Table 4, the actual maximum resolution cannot be any higher than that of the modulator, which is 14 bits maximum as in the AMC1204.

For the test circuit, the modulator clock is set at similar rate as in present application at hand, at 12.5 MHz. The OSR is chosen to be 520 and therefore the data output rate at the FPGA is 12.5 MHz/520 = 24 kHz.

Chapter 4. Simulation

The purpose of the transient simulation is to ensure the circuit is immune to external electrical transients such as lightning, electrostatic discharge (ESD), and noise coming from switching networks.

According to the SDM datasheet [16], the minimum common-mode transient immunity (CMTI) is 15 kV/µs. The CMTI is the ability of the device to reject the fast rate of rise (or dV/dt) of common-mode transients. The CMTI is important because the high-frequency transients, when coupling through the parasitic capacitance across the isolation barrier of the Sigma-Delta modulator, can corrupt data. Therefore, it is important to slow down the rate of rise of the transients to below the CMTI specification to ensure data integrity. Shown in Table 5 are the simulated transients applied to the current shunt.

Transient	**Maximum rising edge dV / dt (kV/µs)**
2.5 kV RMS Dielectric (Hipot)	0.0013
4 kV Surge Immunity	9.6
2.5 kV SWC Damped Oscillatory	15.9
4 kV EFT/B	1340
8 kV ESD Contact Discharge	8000

Table 5-Transients to be tested on the current shunt

The right column in Table 5 depicts how rapidly the transient voltage can rise from 0V to its maximum. The units are in kV/µs. For example, the dielectric (hipot) transient can rise at 1.3 V/µs while the ESD surge can be up to 8 million V/µs. The goal here is to limit the voltage rate of rise of the transient at the input of the SDM to below the specified 15kV/µs. All the simulated transient waveforms show in the following sections of Chapter 4 are generated using Pspice generators, and their waveform characteristics are modeled accordingly to the IEEE and IEC standards, as cited in the following sections.

4.1.1.1. Dielectric (Hipot) Test (IEEE C37.90 – 2005, IEC 60255-5) [23]

The purpose of his test is to ensure that proper electrical insulation exists over the surface between circuits. This is performed as a safety test to ensure the risk of electric shock to persons is minimized by hardware design.

To simulate the common mode test, the output of the dielectric generator model is connected across the current shunt (refer to circuit schematic shown in Figure 18). For the application at hand, the passing criteria is that no more than 1mA RMS of leakage current is measured at the output of the generator, and that no breakdown or flashover should occur on the circuit. To meet IEEE standard, meeting only the latter requirement is adequate.

Shown in Figure 35 a) is the common mode voltage at the first stage LPF, V(stage1+), and the rate of rise of the voltage at the input node vinp of the modulator. The rate of rise in voltage at the modulator input due to the dielectric waveform is not a concern. Since the peak common mode voltage measured at the modulator input is about 3.5kV, surge capacitors at C1, C3, C6, and C8 must have a rating of 3.5kV or above in order to handle high transient voltage. For safety reasons, Y2 type safety surge capacitors are used to prevent electrical conduction through the capacitors to the chassis ground in case of capacitor failures. The Y2-capacitor will pop open in failure mode, prohibiting the transient current from flowing through it to ground.

Figure 35 c) shows the node voltage at the modulator input with respect to chassis ground. Note that the magnitude of this voltage is 3.5kV but when referenced to the isolator ground (e.g. V(vinp) – V(ISO_GND) the voltage is less than 300 mV. This value is within the limitation of ±320 mV at the modulator input [16]

The leakage current, I(R24), at the output of the generator shown in Figure 35 c) appears to be larger than the acceptance criteria of 1mA RMS. Reducing the value of either surge capacitance pairs to 100pF will bring the leakage current down to the acceptable level. However, this change has the adverse effects on the ability to slow down the rate of rise of the other transients. Simulation shows if surge capacitors at C1 and C8 are set to 100pF each, the leakage current reduces to 1mA RMS when subjecting to Dielectric test; but the rate of rise at the modulator input increase to 12 kV/µs when subjecting to EFT/B transient

test. This rise is still below 15 kV/µs limitation of the SDM. Most important, actual Type tests are necessary to verify the simulation result and finalize the component values.

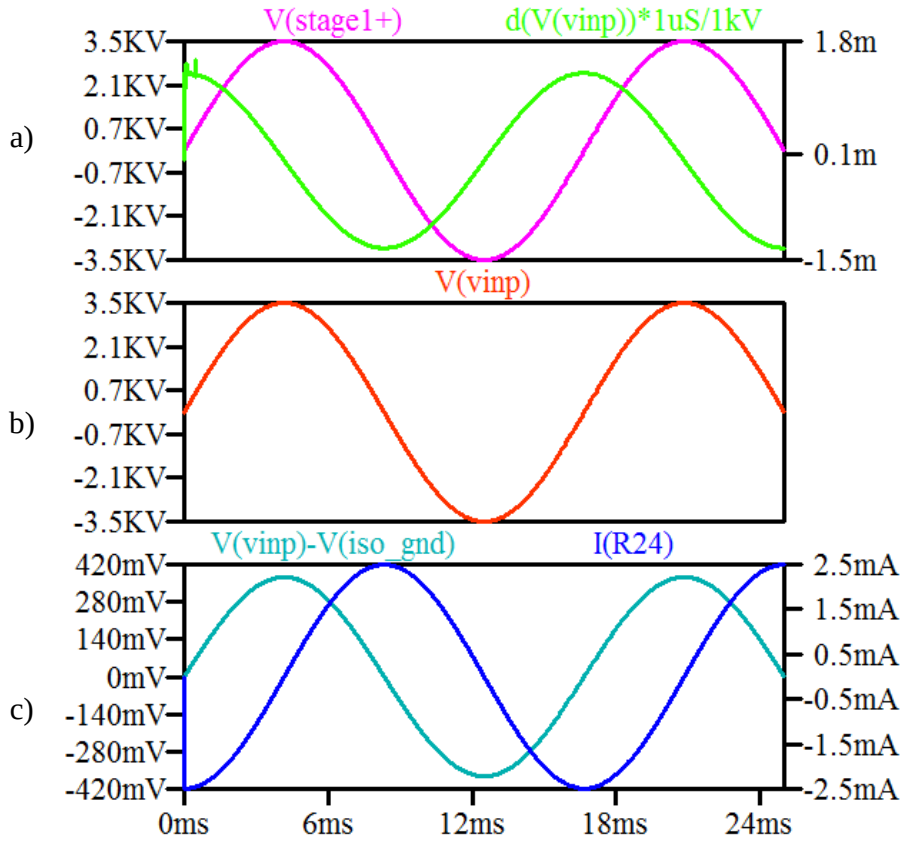


Figure 35-Dielectric transient simulation

a) Voltage across capacitor C1. Rate of change (dv/dt) of the transient at the input of the modulator.

b) Voltage at the input of the modulator.

c) Leakage current, differential voltage at the positive input to isolated ground of the modulator

4.1.1.2. Surge Immunity (IEC 60255-26 Section 7.2.7:2013, IEC 61000-4-5:2005) [24]

The objective of this test is to confirm that the circuit will operate correctly when energized and subjected to high-energy disturbances occurring on the power and interconnection lines caused by surge voltages from switching and lightning effects.

The transient signal is applied to one terminal of the current shunt with the generator return grounded (line-to-earth mode),

Shown in Figure 37 a) are the transient current pulse in the surge resistor R1 of the first stage LPF and the instantaneous power dissipation in the resistor. Figure 37 b) shows the transient current pulse and power dissipation in the resistor R3 of the second stage LPF. These waveforms help in choosing the right resistor of the first stage LPF that interfaces with high voltage transients.

The resistor selected for R1 and R3 has the following pulse voltage rating, as shown in Figure 36.

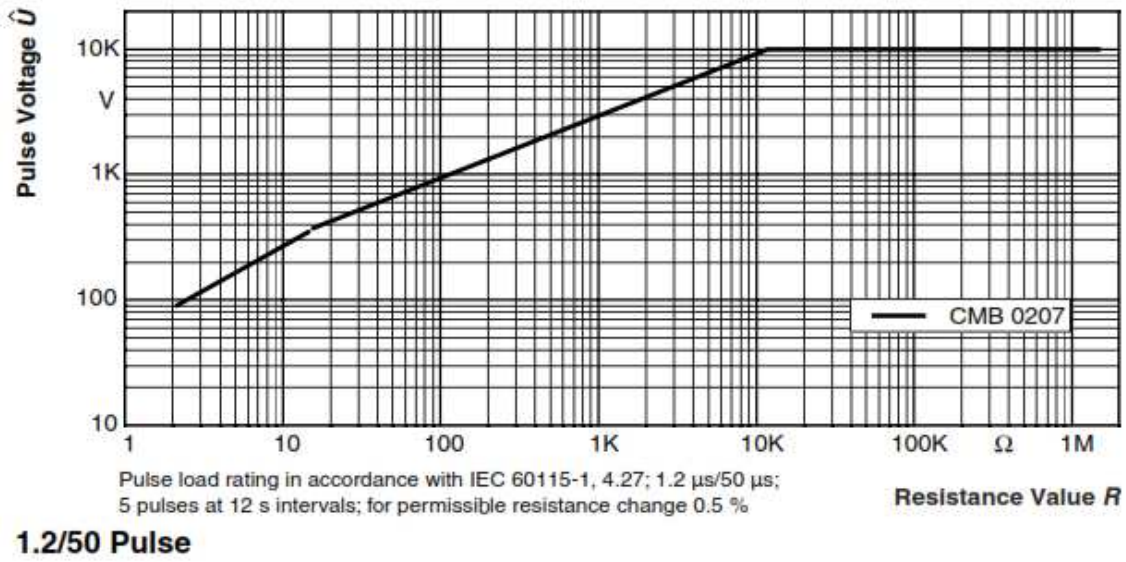


Figure 36-Pulse voltage of MELF resistor [27].

According to Figure 36, a 100 Ω resistor can handle up to 1kV of 50µs pulse voltage. The power dissipation of the resistor is calculated as follows:

$$P = \frac{(1kV)^2}{100\Omega} = 10kW \tag{30}$$

The rated energy dissipation during $\Delta t = 50\mu s$ is:

$$E = P*\Delta t = 10kW*50\mu s = 0.5J \tag{31}$$

The peak power dissipation of the resistor R1 shown in Figure 37 a) is 3.3 kW in 2µs. Applying (31) the resistor energy dissipation can be seen to be lower than the rated dissipation.

Figure 37 c) verifies that the rate of rise at the modulator input is less than the specified 15kV/µs. Figure 37 d) shows the input voltage with respect to the isolation ground is less than ±320 mV limit.

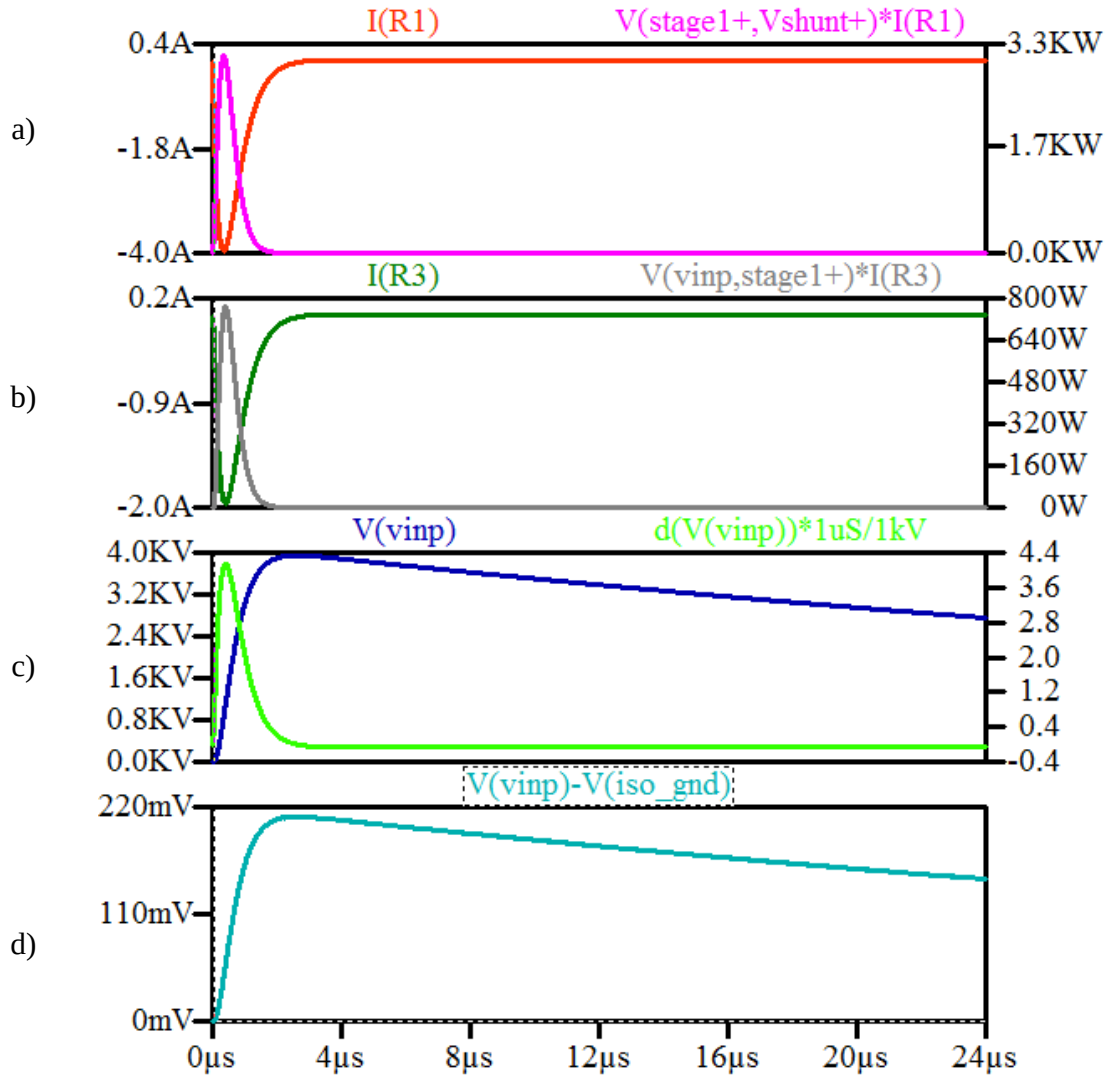


Figure 37-Surge Immunity simulation

a), b) Currents and instantaneous power in resistors R1 and R3 of the LPF caused by the transient

c) Node input voltage and rate of change of the transient at the SDM input

d) Voltage surge at SDM input due to the transient

4.1.1.3. IEC SWC Oscillatory (IEC 60255-26 Section 7.2.6) [24]

The objective of this test is to confirm that the circuit will operate correctly when energized and subjected to repetitive damped oscillatory waves such as those originating from the closing or opening of circuit breakers in high voltage substations or power plants.
The transient signal is applied to one terminal of the current shunt with the generator return grounded (line-to-earth mode).
Similar to what was displayed in the previous section, the simulation in this section is used to determine the maximum power dissipation of the LPF components and to verify that the modulator input voltages are within the datasheet's limitation. As shown in Figure 38, all the parameters of interest increase but are still within the limitation. From observation, the current flowing through the front end resistor appears to be larger compared to the previous transients. That is because when transient frequency of the signal increases, the impedance of the surge capacitors of the passive LPF decreases, resulting more current flow in the surge resistors. The peak power dissipation measurement helps in selecting the correct surge resistors.

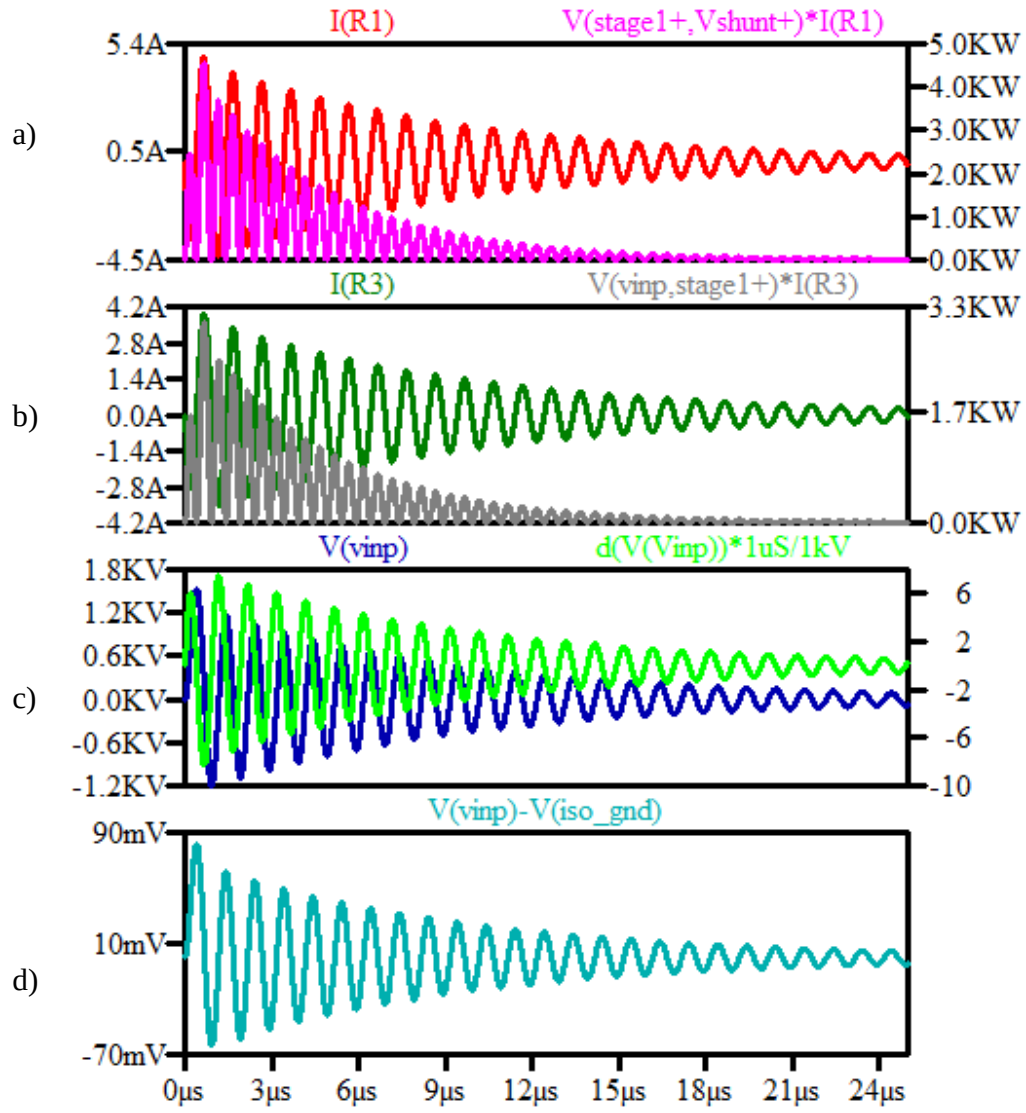


Figure 38-SWC transient simulation.

a), b) Currents and instantaneous power in resistors R1 and R3 of the LPF caused by SWC

c) Node input voltage and slope of the SWC transient at the SDM input

d) Voltage surge at SDM input due to SWC transient.

Figure 39 shows that the voltages at the input of the SDM and its isolated ground all move together, allowing the differential input voltage range to stay within the specified ±320mV, as shown in Figure 38 d).

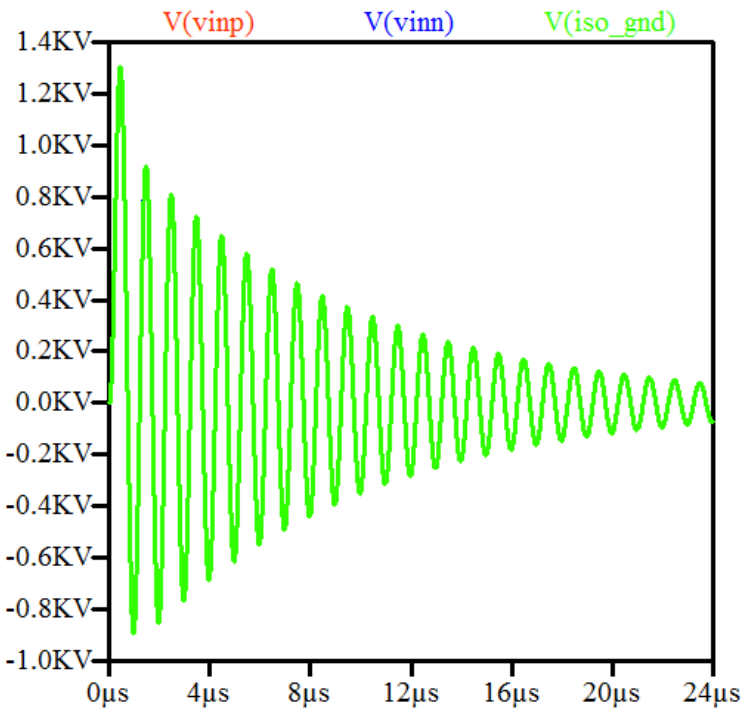


Figure 39-SWC transient simulation. Isolated ground moves together with inputs.

4.1.1.4. IEEE SWC Fast Transient (IEEE C37.90.1 – 2002) [25]

The purpose of this test is to ensure the circuit behaves normally when subjected to repetitive electrical transients.

Similar signals are measured in Figure 40 as in the previous sections. Notice in Figure 40 a) that the peak power dissipation of the resistor R1 is 33kW with a pulse width of 50ns. By applying (31) the energy dissipation is calculated as:

$$E = P*\Delta t = 33kW*50ns = 1.5mJ \quad (32)$$

The selected resistor with rated energy dissipation of 0.5J is sufficient for handling this type of surge energy.

The other signals shown in Figure 40 b), c), d) are within the limitations.

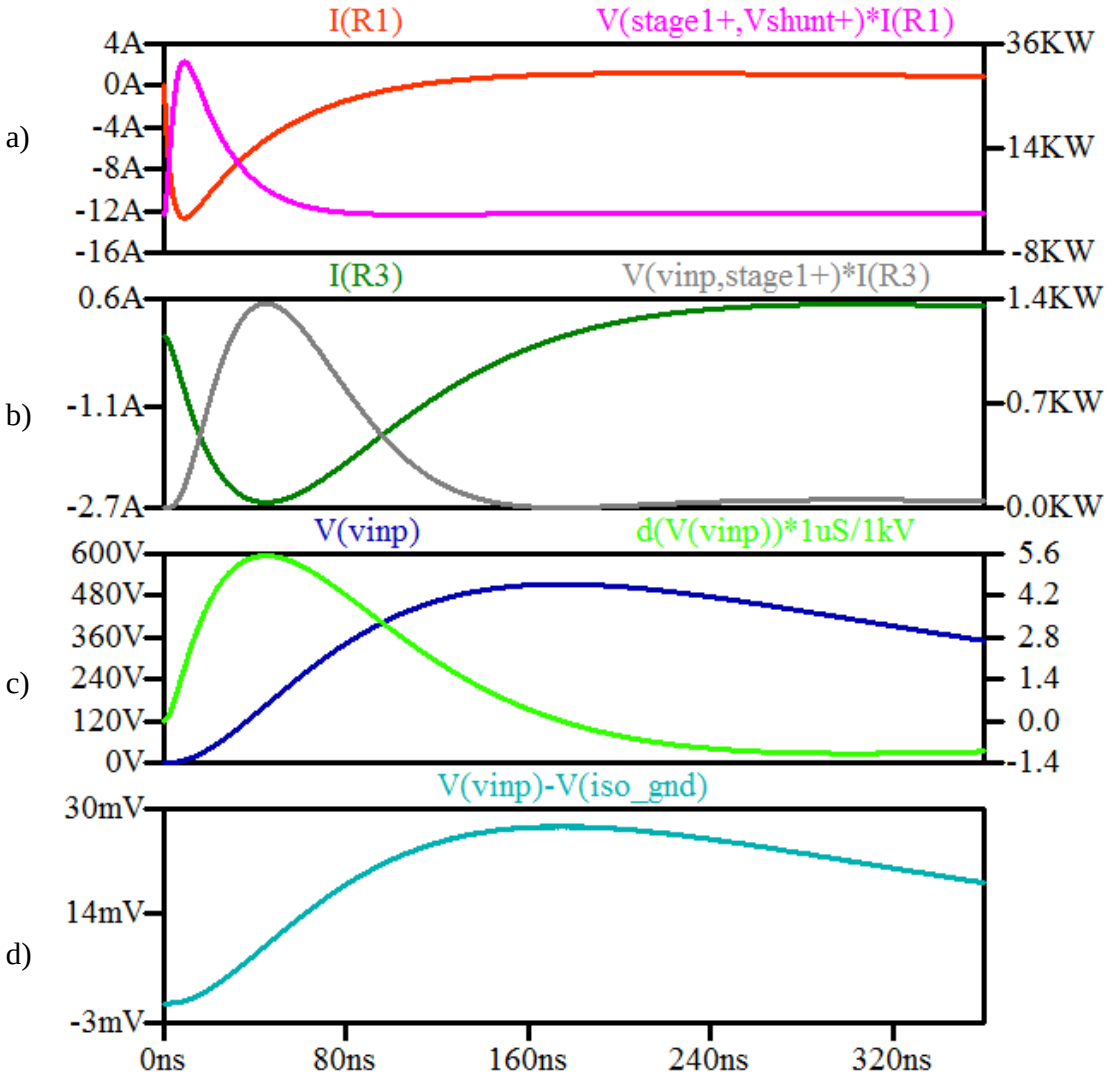


Figure 40-EFTB and SWC Fast Transient simulation

a), b) Currents and instantaneous power dissipation in resistors R1 and R3 of the LPF caused by SWC

c) Node input voltage and slope of the SWC transient at the SDM input

d) Voltage surge at SDM input due to SWC transient.

4.1.1.5. Electrostatic Discharge (IEC 60255-26 Section 7.2.3, IEC 61000-4-2, IEEE C37.90.3) [24], [26]

The purpose of this test is to ensure that the circuit will not mis-operate under an Electrostatic Discharge event (ESD), which occurs when a user without proper grounding operates the devices and the human body static charge is transferred to the devices. There are two discharge methods in a normal ESD event, direct and indirect discharge. This Pspice model simulates only the direct discharge method. The ESD generator output is connected to one terminal of the current shunt. Simulation results are shown in Figure 41.

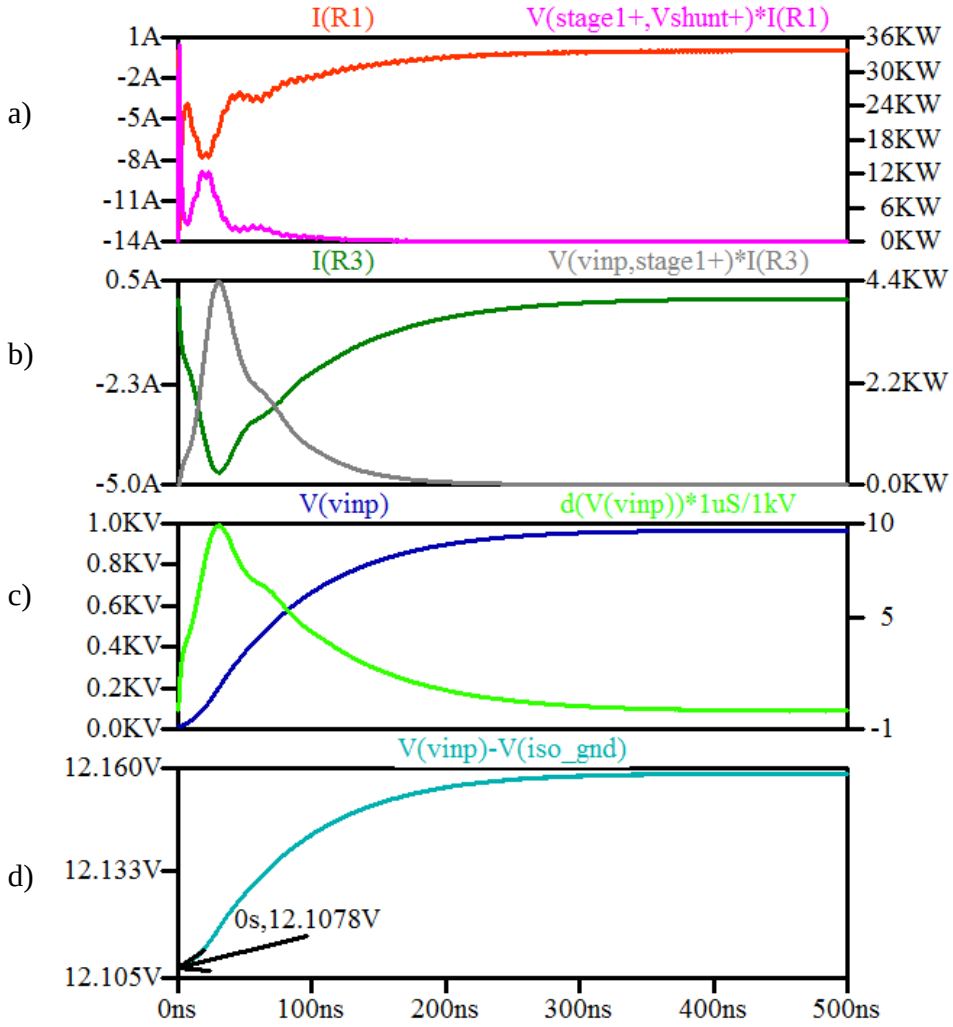


Figure 41-ESD simulation.

a) Current in resistor R1 and instantaneous power dissipation.

b) Current in resistor R3 and instantaneous power dissipation.

c) Voltage across capacitor C1. Rate of change (dv/dt) at the input of the modulator.

d) The modulator's input voltage to isolated ground is 12V.

From the ESD simulation, Figure 41 d) shows the voltage at the modulator input to isolated ground is 12V. This may be due to the inaccurate Pspice models of the capacitors C4 and C7, e.g. lack of the parallel leakage resistance, equivalent series resistance (ESR), and equivalent series inductance (ESL). Adding a 10 kΩ parallel resistor to C4 and C7 brings

the voltage down to 55mV (see Figure 42). An ESD test on the actual circuit will be needed to verify the ESD simulation test results.

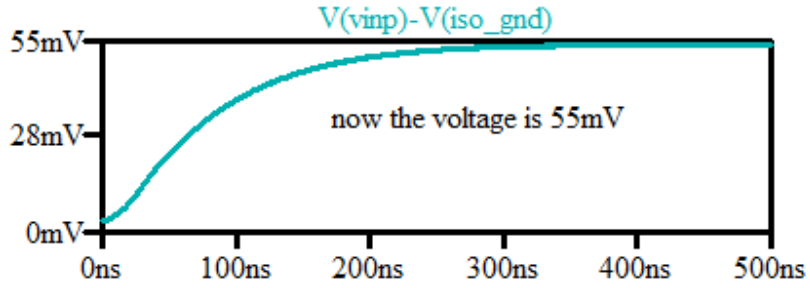


Figure 42-ESD simulation with the addition of parallel resistor. The Sigma-Delta input voltage is now less than 55mV.

4.1.1.6. Common Mode Rejection Ratio (CMRR) Simulation

This simulation measures the ability of the LPF circuit to reject the common mode noise from the external environment to the circuit. In theory, the common mode voltage appears equally to both inputs of the modulator so that the differential input voltage is unaffected. In practice, the component mismatch between the resistors and capacitor in the LPF circuit creates voltage difference at the modulator input that affects the differential input voltage and must be considered. The CMRR is defined as the ratio of the differential mode gain to the common mode gain of a circuit, as shown in (33). Refer to schematic in Figure 18 for relevant voltage labeling.

$$\mathrm{CMRR} = \frac{\mathrm{Adm}}{\mathrm{Acm}} = \frac{\dfrac{\mathrm{V(vinp)} - \mathrm{V(vinn)}}{\mathrm{V(Vshunt+)} - \mathrm{V(Vshunt-)}}}{\dfrac{\mathrm{V(vcmo+)} - \mathrm{V(vcmo-)}}{\mathrm{V(Vcmi)}}} \tag{33}$$

The plot of CMRR is shown in Figure 43. This is done by first plotting the differential gain of the LPF, Adm, which is the ratio of the LPF's output voltage to its differential input voltage at the shunt as shown in Figure 24. Then the LPF common mode gain is simulated by applying the common mode current to both ends of the resistor shunt while adding the typical tolerance to the resistors and capacitors by 1% and 20%, respectively. This method creates an offset voltage, V(vcmo+) - V(vcmo-), across the LPF output. The ratio of the output voltage to common mode input voltage is the common mode gain, Acm. Figure 43 shows the plot of CMRR. At the frequency of interest of 60 Hz, the CMMRR is measured

at 88dB. In practice, a device with CMRR at 80dB or better at the frequency of interest is adequate.

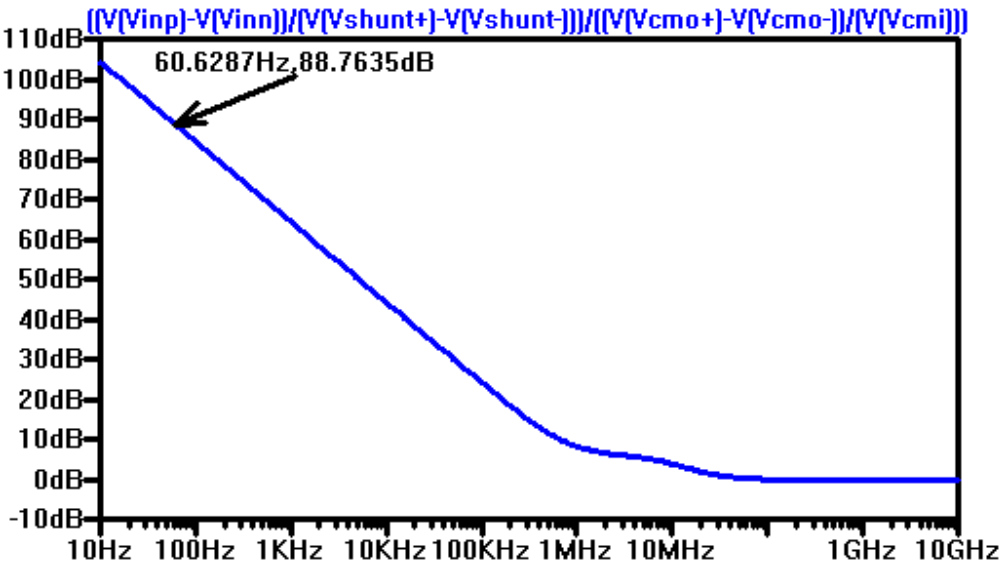


Figure 43-Common Mode Rejection Ratio.

Chapter 5. Functional Test of the SDM Circuit

The complete fabricated PCB of the SDM circuit was created with the help of several groups. The PCB design group creates the PCB layout. A mechanical engineer who designs the chassis. The configuration group generates the Bill of Materials to be ready for building the prototype. The manufacturing group builds the complete prototype, as shown in Figure 44. The SDM circuit is shown within the rectangle. The circuit is functionally tested to verify its performance according to the modulator datasheet.

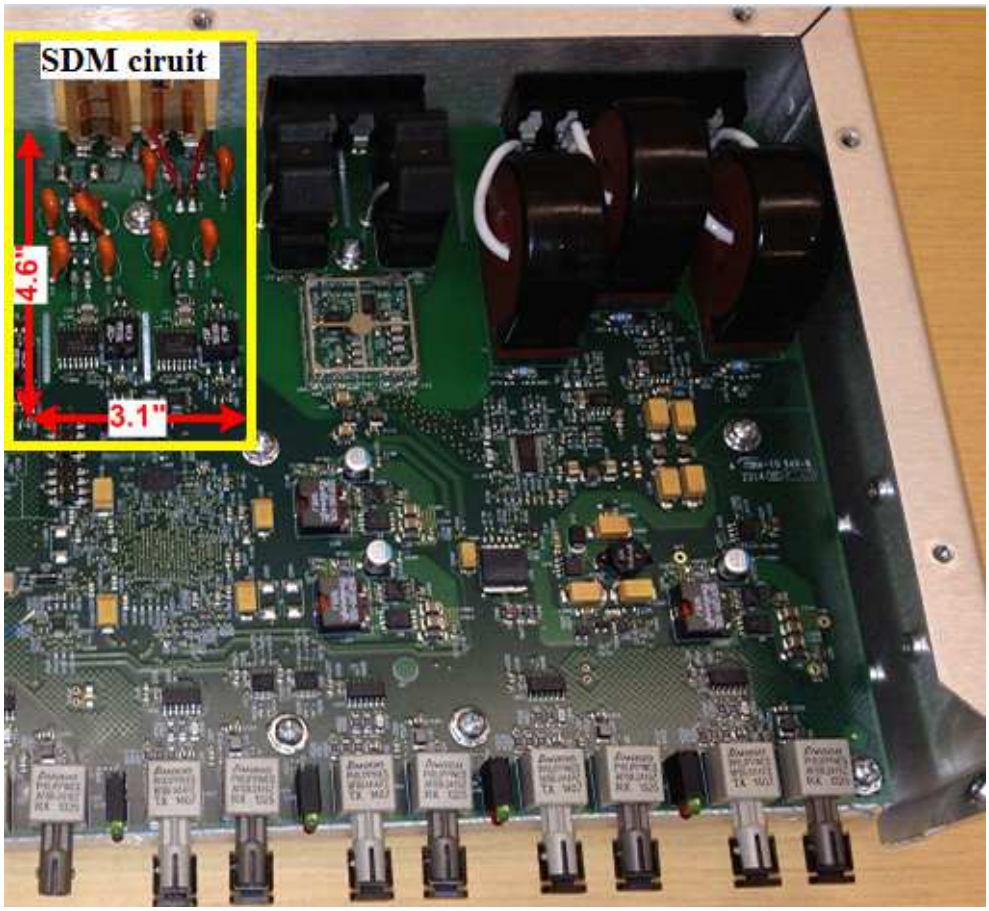


Figure 44-Complete fabricated SDM PCB

To verify the signal-to- noise and distortion ratio (SINAD) and the SNR against the datasheet spec, the shunt is removed, and a 60 Hz voltage from a function generator is applied across the shunt's mounting holes on the PCB. The SNR and SINAD are calculated using Fast Fourier Transform analysis (FFT) on the data output (see Appendix D). Table 6

shows the SNR; and Table 7 shows the calculated SINAD, and ENOB over the modulator input voltage sweep. The maximum voltage is ±250 mV peak-to-peak at the modulator inputs, a level that the SDM still guarantees a linear operation. The calculated SNR and SINAD are approximate 5dB to 7dB below the datasheet specification. This is possibly caused by different test setup, in which one setup may experience worse noise than the other.

SNR	**Voltage at the modulator inputs (mVpp)**		
	10mV	100mV	500mV
Calculated SNR of the SDM circuit (dB)	46.4	65.3	77.6
SNR from datasheet	53	74	81

Table 6-SNR verification of the SDM

SINAD	**Voltage at the modulator inputs (mVpp)**		
	10mV	100mV	500mV
Calculated SINAD of the SDM circuit (dB)	45.7	64.5	75.9
Calculated ENOB of the SDM (bits)	7.3	10.4	12.3
SINAD from datasheet	52	73	80

Table 7-Calculated SINAD and ENOB of the SDM

To test the SNR of the circuit under application of current ranging from 5A to 20 RMS, a 1mΩ current shunt is installed on the PCB. Different current values are applied through the shunt and the calculated SNR, SINAD, ENOB, and noise floor are recorded in Table 8. Due to the limitation of the AC current source, 16 A RMS is the maximum applied current in the shunt.

Parameters	Voltage at the modulator inputs (mVpp)		
	9.09mV (5A)	18.17mV (10A)	29.03mV (16A)
SNR (dB)	47.1	53.1	57.3
SINAD (dB)	47.1	52.8	54.5
ENOB (bits)	7.5	8.5	8.8
Noise Floor (dB)	80.3	86.6	90.1
SINAD from datasheet	52	58	63

Table 8-Calculated SNR, SINAD, ENOB, and noise floor under test current sweep.

In order to compare the noise floor and CMRR between the SDM circuit to that of the CT, a separate experiment was conducted on the commercial CT circuit shown in Figure 4. The test was conducted on three CT channels, IA, IB, and IC (see Appendix E). The noise floor is calculated by taking the ratio of 5A reading and 0A reading at the CT's secondary winding. The CMRR is calculated by taking the ratio of the differential mode gain, Adm, when subjecting to 5A current, to the common mode gain, Acm, when subjecting to 3kV common mode signal. Table 9 shows the results of the test.

	IA	IB	IC
Noise Floor (dB)	94.1	91.7	92.0
CMRR (dB)	107.1	107.6	107.6

Table 9-Calculated Noise Floor and CMRR of CT channels

The comparison of noise floor in between the SDM and CT circuits in Table 8 and Table 9 shows that the CT circuit has superior noise floor. Similarly, the CMRR of the CT circuit is 107 dB, while the simulated CMRR of the SDM circuit in Figure 43 is 88 dB. Again the CT circuit's CMRR is unmatched for the SDM circuitry. This means the CT circuit has better SNR and ENOB compared to SDM circuit. To further compare apples-to-apples on these parameters additional tests on the CT circuits will be needed.

Chapter 6. Conclusion

Throughout the research on various current sensing devices, the current shunt appears to be the best fit for the application at hand. The design and simulation of the LPF show that it can protect the modulator from the destructive electrical transients, ensuring the signal data integrity. However, functional tests performed on the SDM and CT circuits reveal that the CT circuits have better dynamic performance due to its higher noise floor and CMRR.

In order to consider using the SDM circuit as an alternate current sensing device to the CT circuit, the SDM needs to perform the same or better than its rival. Comparison on the noise floor and CMRR suggests the SDM circuit need to improve on these aspects. A possible solution to improve the noise floor is to increase the current shunt resistance so that the signal current creates a higher differential voltage across the shunt. At the same time a better grounding scheme is required to reduce the noise coupling into the shunt. The drawback of this solution is that it will increase the power dissipation of the shunt, especially under fault conditions where the current surge in the shunt reaches hundreds amperes. Therefore, care must be taken to avoid current shunt failure under such situations.

For low frequency application (less than 100 Hz) the SDM circuit offers a fair solution for current sensing application. In spite of the economic advantage of the SDM circuit, with its relative low noise floor and CMRR compared to the CT circuit in an application at hand, the SDM circuit may not be a solution to replace the CT.

Chapter 7. Future work

- The complete board needs to go through a full round of tests with the actual transients listed in Chapter 4 in addition to other type tests to know whether it passes all the required industrial standards.
- The current shunts need to be tested with 500A RMS for one second. Then the shunt needs to be measured to determine how much its resistance varies during the high current test. Also, the metal strips, on which the current shunts elements are welded across, are soldered onto the PCB. Under 500A RMS current they may get hot enough to melt the solder flux. Therefore, the temperature at the solder joint needs to be monitored.
- Research of other resistor structures and configurations of sensing leads is needed to further improve the accuracy.
- The LPF circuit design needs to improve on the dielectric insulation capability as discussed in Section 4.1.1.1
- The circuit needs to be tested with the actual Impulse Voltage Withstand transient to verify that there will be no disruptive discharge (spark-over, flashover, or puncture) during test.

Appendix A

Calculation of First Stage Filter

Impedance of the capacitor C1:

$$Z1 = \frac{1}{s \cdot C1}$$

$$T1(s) = \frac{Z1}{R1 + Z1} = \frac{\frac{1}{s \cdot C1}}{R1 + \frac{1}{s \cdot C1}} = \frac{1}{s \cdot C1 \cdot R1 + 1}$$

$$T1(s) := \frac{1}{s \cdot C1 \cdot R1 + 1}$$

$$T1(f) := \frac{1}{[(2\pi \cdot f)j]C1 \cdot R1 + 1}$$

Poles:

$$f_{pole1} := -\frac{1}{2\pi} \cdot \left(-\frac{1}{C1 \cdot R1} \right)$$

$$f_{pole1} = 1.693 \cdot MHz$$

Table 10-Calculation of the first stage of the LPF

Appendix B

Calculation of Second Stage Filter

From differential mode view, node Capacitor C3 and C6 appear to be in series. The capacitor C37 is small and neglected to simplify calculation. Therefore, the capacitors C4 and C7 are considered to be in series. The equivalent capacitances are:

$$C_{eq1} = \frac{C3 \cdot C6}{C3 + C6} = \frac{C3}{2}$$

$$C_{eq2} = \frac{C4 \cdot C7}{C4 + C7} = \frac{C4}{2}$$

The total equivalent capacitance:

$$C_{eq} = C_{eq1} + C5 + C_{eq2} = \frac{C3}{2} + C5 + \frac{C4}{2} = \frac{C3 + C4 + 2C5}{2}$$

$$Z_{eq} = \frac{1}{s \cdot C_{eq}} = \frac{2}{s \cdot (C3 + C4 + 2C5)}$$

$$R_{eq} = R3 + R4 = 2R3$$

The second stage LPF transfer function is derived as:

$$\frac{\frac{2}{s \cdot (C3 + C4 + 2C5)}}{2R3 + \frac{2}{s \cdot (C3 + C4 + 2C5)}} \left| \begin{array}{l} \text{simplify} \\ \text{explicit} \\ \text{collect}, s \end{array} \right. \rightarrow \frac{1}{s \cdot (C3 \cdot R3 + C4 \cdot R3 + 2 \cdot C5 \cdot R3) + 1}$$

$$T2(s) = \frac{Z_{eq}}{R_{eq} + Z_{eq}} = \frac{\frac{2}{s \cdot (C3 + C4 + 2C5)}}{2R3 + \frac{2}{s \cdot (C3 + C4 + 2C5)}} = \frac{1}{s \cdot (C3 \cdot R3 + 2 \cdot C5 \cdot R3) + 1}$$

check algebra

$$\frac{\frac{2}{s \cdot (C3 + C4 + 2C5)}}{2R3 + \frac{2}{s \cdot (C3 + C4 + 2C5)}} - \frac{1}{s \cdot (C3 \cdot R3 + C4 \cdot R3 + 2 \cdot C5 \cdot R3) + 1} = 0$$

Second pole location:

$$s \cdot (C3 \cdot R3 + C4 \cdot R3 + 2 \cdot C5 \cdot R3) + 1 = 0 \left| \begin{array}{l} \text{solve}, s \\ \text{explicit} \end{array} \right. \rightarrow -\frac{1}{C3 \cdot R3 + C4 \cdot R3 + 2 \cdot C5 \cdot R3}$$

$$f_{pole2} := -\frac{1}{2\pi} \cdot \left(-\frac{1}{C3 \cdot R3 + C4 \cdot R3 + 2 \cdot C5 \cdot R3} \right) = 3.216\,\text{kHz}$$

Table 11- Calculation of the second stage of the LPF

Appendix C

Dielectric Waveform Spice Model

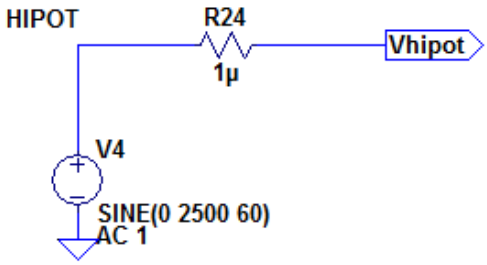


Figure 45-Hipot waveform generator

Dielectric Waveform Characteristics

The dielectric test waveform shown in Table 12 is required by the IEEE and IEC standards.

Standard severity levels	Frequency
2.5 kV RMS	60 Hz

Table 12-Dielectric voltage waveform characteristics

Simulated Hipot Test Waveform

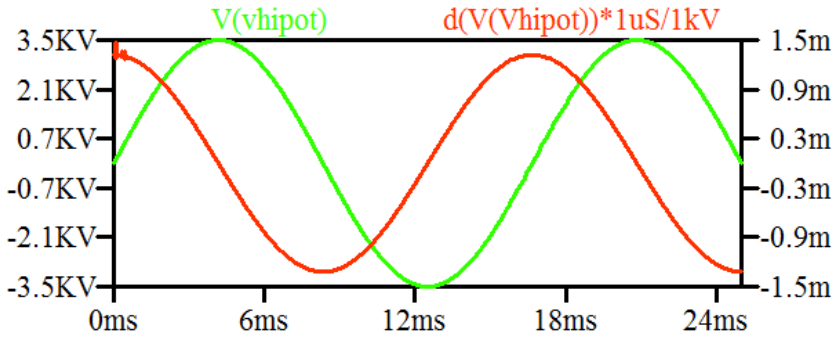


Figure 46-Hipot waveform and rate of rise

Surge Immunity Spice Model

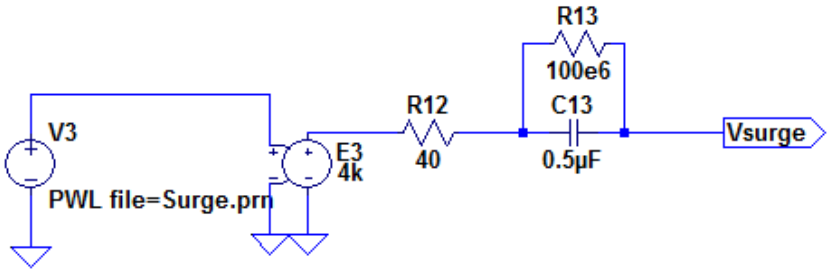


Figure 47-Surge Immunity generator

Surge Immunity Waveform Characteristics

Standard severity level	**Parameter**	**Expected Value**
4 kV	Rise time	1µs
	Duration (time to half value)	50µs

Table 13-Surge Immunity transient characteristics

Simulated Surge Immunity Test Waveform

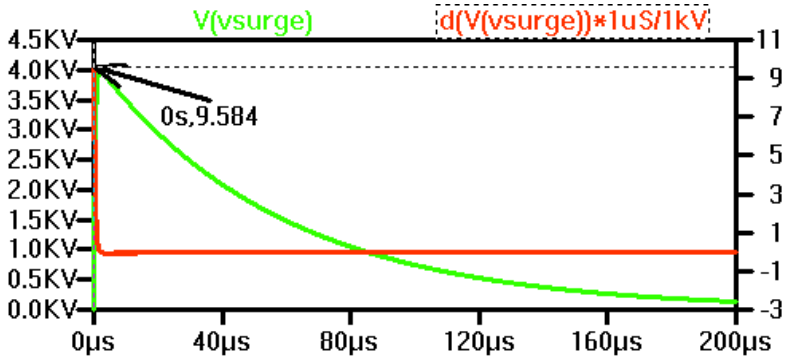


Figure 48-Surge Immunity waveform and rate of rise

IEC SWC Oscillatory Spice Model

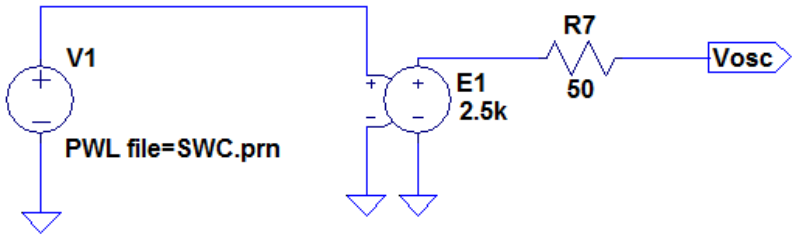


Figure 49-SWC oscillatory generator

IEC SWC Oscillatory Waveform Characteristics

Standard severity level	Parameters	Expected Value	Acceptable Range
2.5kV	Rise Time	75ns ± 20%	60 – 90ns
	Oscillation Frequency	1MHz ± 10%	0.9 – 1.1MHz
	Waveform Decay	See Note 1	
	Open Circuit Voltage	2.5kV ± 10%	2.25 – 2.75kV
	Short Circuit Current	12.5A ± 20%	10 – 15A
	Output Impedance	200Ω	N/A

Table 14-SWC Oscillatory waveform characteristics

Note 1: peak 5 of the waveform is to be greater than 50%, and peak 10 is to be less than 50% of the peak voltage.

IEC SWC Oscillatory Test Waveform

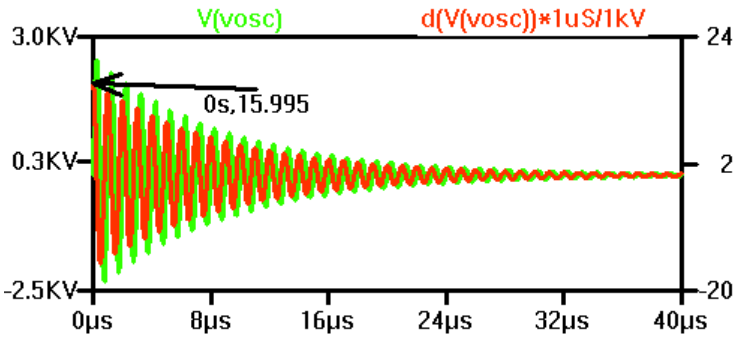


Figure 50-SWC Oscillatory waveform and rate of rise

IEEE SWC Fast Transient Spice Model

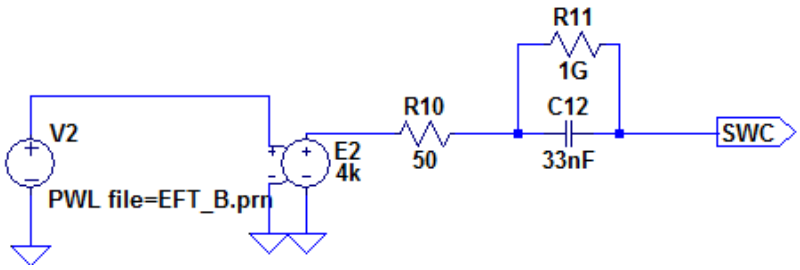


Figure 51-IEEE SWC Fast Transient generator

IEEE SWC Fast Transient Waveform Characteristics

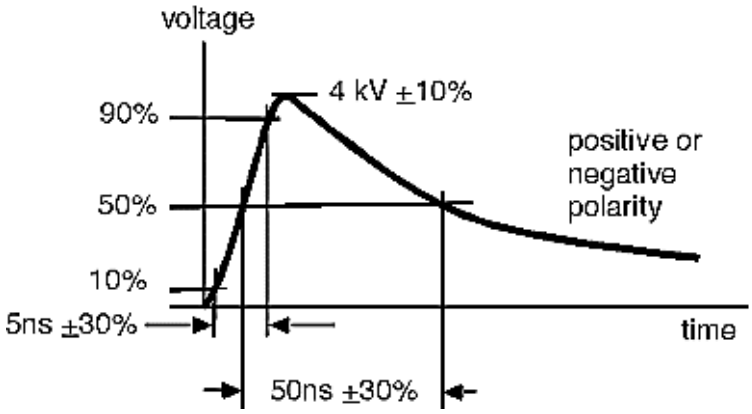


Figure 52-IEEE SWC Fast Transient waveform characteristics [25].

IEEE SWC Fast Transient Test Waveform

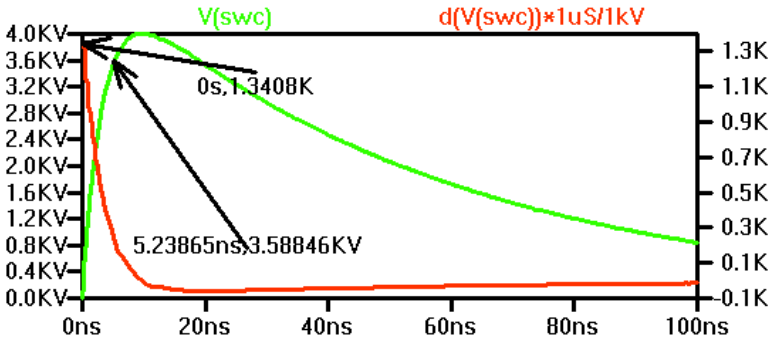


Figure 53-Simulated IEEE SWC Fast Transient waveform and rate of rise

Electrostatic Discharge Spice Model

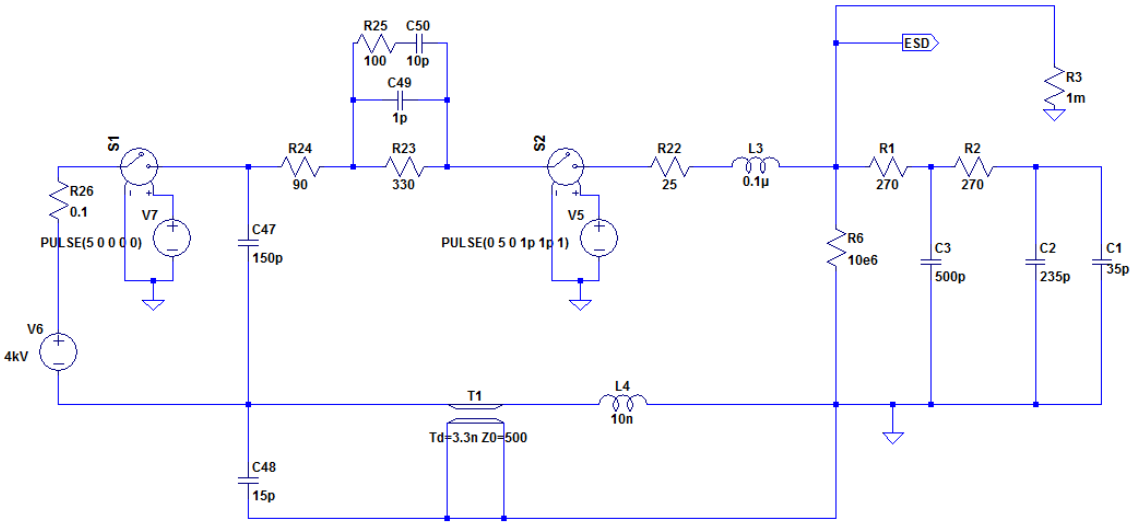


Figure 54-ESD generator

ESD Waveform Characteristics

Voltage	Parameters	Acceptable Range
8kV	Rise Time	700ps – 1ns

Table 15-ESD voltage waveform characteristics

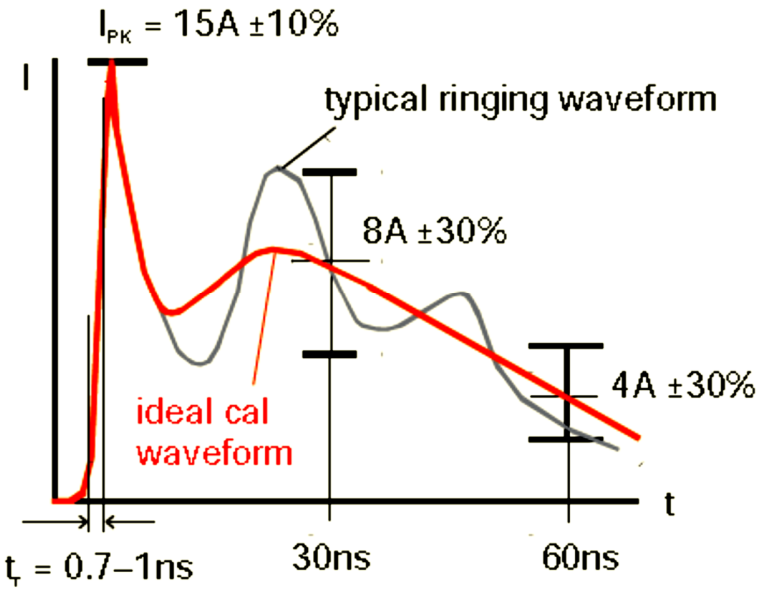


Figure 55-Typical ESD current waveform at 4kV.

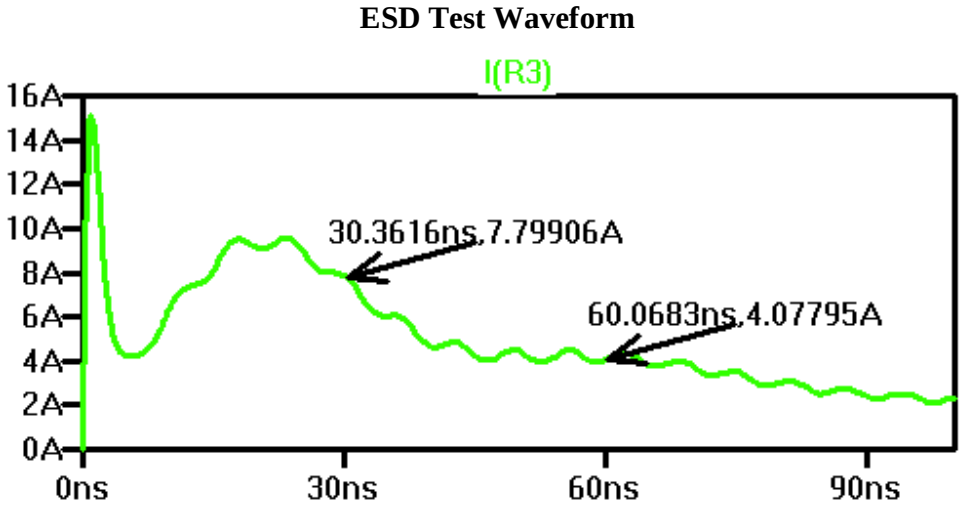


Figure 56-Simulated ESD current waveform at 4kV.

Appendix D

Sinc^3 Filter VHDL implementation

VHDL code implementation is based on the block diagram in Texas Instrument Application report [20], as shown in Figure 57 and Figure 58.

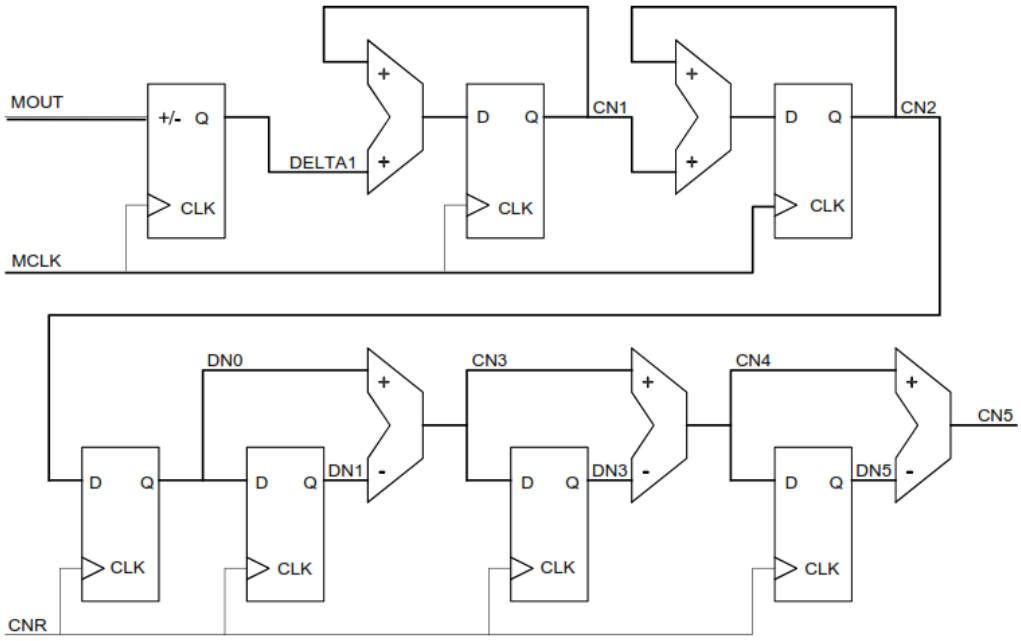


Figure 57-Sinc^3 filter implementation block diagram [20].

```
library IEEE;
use IEEE.std_logic_1164.all;
use IEEE.std_logic_unsigned.all;


entity FLT is
  port(RESN, MOUT, MCLK, CNR : in std_logic;
       CN5                   : out std_logic_vector(24 downto 0));
end FLT;

architecture RTL of FLT is

 signal DN0, DN1, DN3, DN5 : std_logic_vector(24 downto 0);
 signal CN1, CN2, CN3, CN4 : std_logic_vector(24 downto 0);
 signal DELTA1             : std_logic_vector(24 downto 0);
begin

  process(MCLK, RESn)
  begin
    if RESn = '0' then
      DELTA1 <= (others => '0');
    elsif MCLK'event and MCLK = '1' then
      if MOUT = '1' then
        DELTA1 <= DELTA1 + 1;
      end if;
    end if;
  end process;

  process(RESN, MCLK)
  begin
    if RESN = '0' then
      CN1 <= (others => '0');
      CN2 <= (others => '0');
    elsif MCLK'event and MCLK = '1' then
      CN1 <= CN1 + DELTA1;
      CN2 <= CN2 + CN1;
    end if;
  end process;

  process(RESN, CNR)
  begin
    if RESN = '0' then
      DN0 <= (others => '0');
      DN1 <= (others => '0');
      DN3 <= (others => '0');
      DN5 <= (others => '0');
    elsif CNR'event and CNR = '1' then
      DN0 <= CN2;
      DN1 <= DN0;
      DN3 <= CN3;
      DN5 <= CN4;
    end if;
  end process;

  CN3 <= DN0 - DN1;
  CN4 <= CN3 - DN3;
  CN5 <= CN4 - DN5;

end RTL;
```

Figure 58-Referenced Sinc^3 filter VHDL code used to implement the FPGA [20]

SNR, SINAD calculation pseudo code/algorithm

Generate windowing function that works for 60Hz SNR calculation
Generate FFT magnitude of a signal and its frequency vector.
Find signal fundamental frequency
Removing dc bins
Remove 60 Hz power supply noise
Find noise floor starting at dc by removing the fundamental
Get the root-mean-square of the noise (including harmonics)
Calculate noise from the equation below:
Noise = 20*log10((magnitude of fundamental signal) / (root-mean-square of the noise))
Calculate FFT gain from the equation below:
fft_gain = 10*log10(M/2), where M is the number of signal samples in FFT for this research, M = 4096
Calculate SINAD and ENOB by using equation below:
sinad = noise_db-fft_gain
enob = (sinad-1.76)/6.02
Remove the harmonics from the noise
Get the root-mean-square of the noise (without harmonics)
Calculate noise floor from the equation below:
noise_floor = 20*log10((magnitude of fundamental signal) / (root-mean-square of the noise without harmonics))
Calculate SNR from the equation below:
snr = noise_db-fft_gain

Refer to Figure 59 for illustration of the SNR and noise floor.

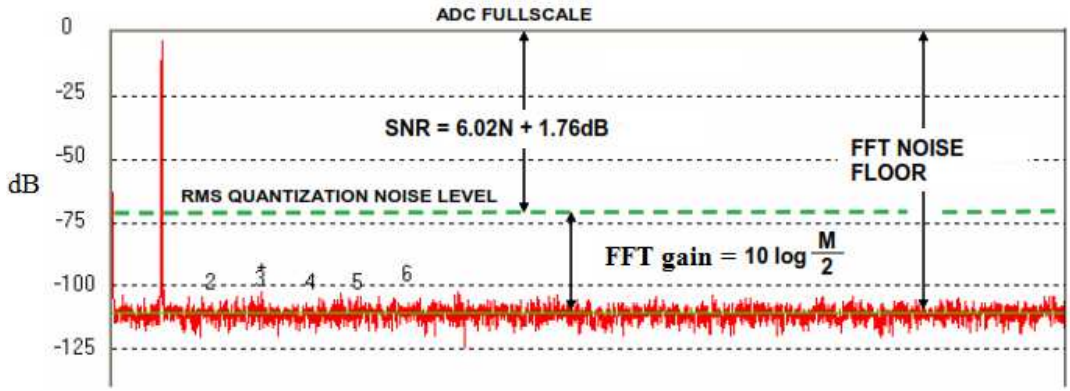


Figure 59- Illustration of SNR and noise floor in frequency domain using FFT [12]

Appendix E

CMRR and Noise Floor test on CT circuit

	VA(kV)	VB(kV)	VC(kV)	VS(kV)	IA(A)	IB(A)	IC(A)
Shorted	0.006	0.007	0.006	0.006	0.098	0.129	0.125
Applied	299.528	299.188	299.124	299.591	4986.358	4984.847	4984.772
3kVac	0.137	0.020	0.107	0.091	6.601	6.269	6.235
Ratio	47468.780	45400.303	51132.308	49601.159	50881.204	38642.225	39878.176
Floor (dB)	93.528	93.141	94.174	93.910	94.131	91.741	92.015
Adm	998.427	997.293	997.080	998.637	997.272	996.969	996.954
Acm	0.046	0.007	0.036	0.030	0.004	0.004	0.004
Ratio	21863.358	149594.000	27955.514	32922.088	226618.300	238547.472	239844.683
CMRR (dB)	86.794	103.498	88.929	90.350	107.106	107.551	107.599

Windows User:
Apply current : 5A
meter reading: 4986.36A
Adm = Io/Iin =
4986.36/5

Windows User:
Burden resistor: 2 ohm

Vin: 3kV
Io: 6.601
=>Vo = 6.601*2ohm = 13.2V

Acm = Vo/Vin = 13.2V/3000V

Windows User:
Common mode Gain:
Acm = Vout/VCMin
Acm = Vout *1kV/Vin

Windows User:
Differential Gain:
Adm = V(differential out)/V(differential in)
Adm = Vout/Vin = Vout*1kV/Vin

Vin: applied input voltage
Vout: meter reading in kV

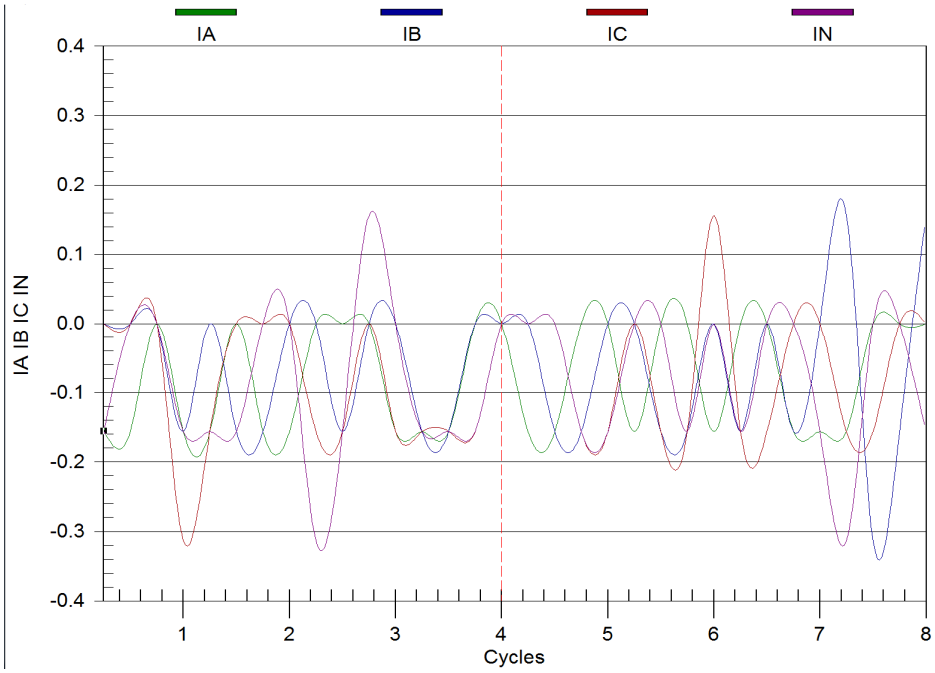


Figure 3 – Noise Floor Filtered Data for IA, IB, IC, and IN

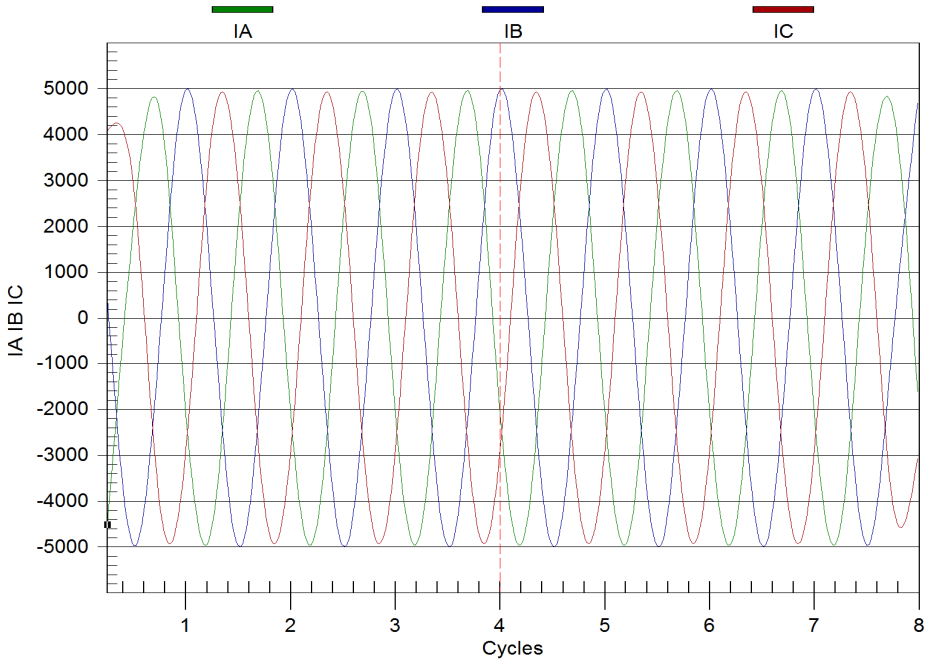


Figure 10 – Applied Signal Filtered Data for IA, IB, and IC

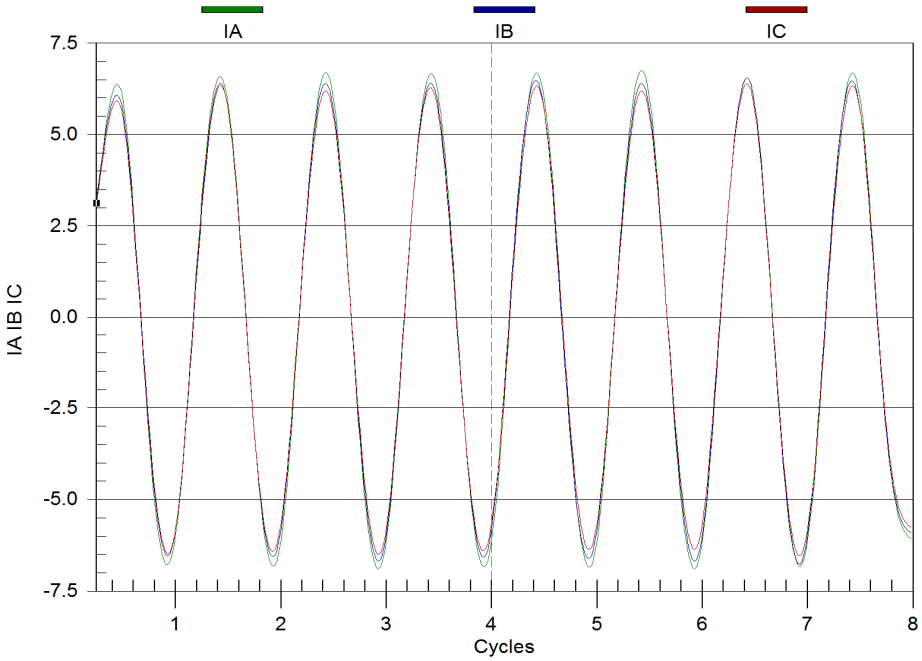


Figure 16 – 3kVac Common Mode Filtered Data for IA, IB, and IC

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