INVESTIGATION OF FAULT LOCATION PERFORMANCE UTILIZING SYNCHRONIZED PHASOR MEASUREMENTS WITH A TWO-ENDED FAULT LOCATION IMPEDANCE METHOD

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Authorization to Submit Thesis

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Abstract

Transmission lines are essential parts of electrical grids. Thus, utilities cannot afford to have any transmission line out service because it can result in power outages and overloading of other lines in the same grid. However, transmission lines are exposed to faults caused by short circuits, birds, adverse weather conditions, and human made accidents. Transmission line faults can be temporary or permanent. Temporary faults are mostly self-cleared when the line is temporarily de-energized. But, permanent faults do not self-clear due to damage to transmission line infrastructure. Most of these faults result in mechanical damage to power lines, poles, or insulators which need to be repaired before returning the line to service. For this reason, transmission line faults must be located accurately to allow field crews to more quickly arrive at the scene and repair the faulted equipment as soon as possible.

The most obvious method to locate the faulted equipment is just to patrol the whole line, but the main obstacles following that method are the geographical layout in some sections of the line making difficult for the field crews accessing to the scene, the long time it takes to patrol the line and the associated high cost which makes it uneconomical. Meanwhile, if the utility has a software tool to rapidly and accurately calculate fault location under any power system conditions, the utility will reduce the restoration time of the line with less cost and reduce customer outage time by pointing field crews to narrow range of the line to check.

Fault location algorithms are one method that utilities use for fast and accurate fault location. However these fault location algorithms are typically embedded in fault locator devices or protective relays. This is an obstacle because in order to get the fault location out those devices, they need to be interrogated and normally these devices are located in remote areas. Now with the advances in synchrophasor technology, it is possible to automatically collect synchronized phasor

measurements in a convenient central location such as operating center or dispatch center and perform fast and accurate fault location based on synchronized phasor measurements.

For this thesis, an impedance based fault location technique will be implemented in a hardware in the loop simulation environment because it is simple and practical method. However, the performance of this fault location technique is enhanced by utilizing very accurate real-time synchronized phasor measurement data. The accuracy of this modified impedance based fault location technique will be evaluated.

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Dedication

“Dedicated especially to my wife Maria, my daughter Carmen, and my son Enrique. Thank you for being the reason to look forward to the next day.”

“Also dedicated to my parents Josaphat and Antonia for their entire support in my life”

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Chapter 1 - Introduction

Power systems are complex electrical grids made of transmission lines, buses, generators, and transformers. One of the main components in the electrical grids are transmission lines because their function is to transfer power from generation areas to the load centers. For that reason, without transmission lines it becomes very difficult for utilities to deliver energy to customers. However, transmission lines are fragile components of the power systems subject to faults due to several factors such as tree contacts, animal contacts, insulation deterioration and extreme weather that can cause short circuits and leave the lines out service for seconds, minutes, hours and days. Due to the importance of delivering power to customers, utilities today cannot afford to have any high voltage transmission line out service for very long. For that reason, short circuits in transmission lines not only have to be electrically isolated from the power system; the short circuit location also needs to be found very quickly in order to determine the root cause of the short circuit. As a result, fault location became a very important process for utilities because it allows faster repair of any mechanical damage in transmission line equipment, resulting in restoration power to customers as soon as possible.

1.1 What is Fault Location?

Each time that there is a short circuit in any transmission line, line protective relays sense the short circuit currents and send a control signal to open the transmission line circuit breakers of the faulted line in order to isolate the fault from the power system. There are two types of faults momentary or sustained faults. If it is a momentary fault, line protective relays will restore the line quickly by reclosing circuit breaker after a preset time. If it is a sustained fault, line protective relays, after sensing that the fault is sustained, will open the line circuit breakers and leave the line out service for an indefinite time. Either a momentary or sustained fault causes damage in

equipment which needs to be repaired. So, before trying to restore the line during sustained faults, utility needs to find the specific location of the fault and have a line crew perform repair. Fault location refers to the process that tries to determine the exact location where the fault occurred on the faulted transmission line. It becomes very important for the utility to have the exact location of the fault in order to properly coordinate and dispatch transmission line crews to find the trouble and restore power service. As an example, once utility has determined where the fault location is on the transmission line, transmission line crews can be sent to a specific location to repair the damaged transmission line equipment rather than needing to patrol distances of tens of miles or more.

1.2 Thesis Purpose

The purpose of this thesis is to investigate the improving of fault location accuracy utilizing impedance based fault location algorithms in conjunction with real-time synchronized phasor measurement data. Since it is important to have a fast, automated fault location tool, a simple and practical fault location algorithm will be developed to determine fault location. To validate the results a relative error on a line length based percent error technique will be used.

1.3 Thesis Objectives

- Use a real 500 kV transmission network modeled in RTDS to simulate fault disturbances
- Manually retrieve all synchronized phasor data from phasor data concentrators (PDC)
- Manually run all synchronized phasor data through the fault location algorithm
- Verify that the fault location algorithm identified the correct faulted transmission line
- Verify that the fault location algorithm determined the correct fault type

- Verify that the fault location algorithm determined correct fault location in miles using traditional one-ended and two ended fault location methods supplemented with synchronized phasor measurements data
- Analyze fault location performance utilizing synchronized phasor measurements under various power system conditions such as high impedance faults, faults during line overload conditions, combined effects of line overload and high impedance fault, faults with a weak source on one end, faults with series capacitor inserted in a compensated line, and faults with maximum DC offset.

Chapter 2 - Fault Location Fundamentals

As mentioned in the introduction, double-ended fault location is basically determining the distance between devices sensing the faulted voltages and currents to the fault in the transmission line. During the fault location process, the main objective is to determine the exact location of line pole, tower structure or conductor where the fault occurred in order to fix faulted equipment and restore service to customers quickly. Some of the tools used to perform fault location are microprocessor devices like protective relays and/or Digital Fault Recorders or short circuit analysis software like ETAP, ASPEN, KSM, etc. In the next section some typical fault location methods will be discussed in detail. [1]

2.1 Fault Location Methods

Today there are several methods for determining fault location, but the four most common methods used by utilities are line patrolling, customer call centers, short circuit analysis and fault location algorithms.

2.1.1 Line Inspection

The first method is line patrolling. Line patrolling is basically a brute force method. Typically when a sustained or momentary fault happens on a transmission line, the transmission line department from the utility is dispatched to determine the fault location along transmission lines by patrolling the whole line pole by pole or tower by tower using helicopters or utility trucks. Typically, the transmission line crews are divided in groups where each group focuses on a specific part of the transmission line. However, patrolling the line can take several crew shifts, lasting days and many field personnel. Therefore, this method is very time consuming and in many cases becomes

unpractical and uneconomical, especially for long lines located in terrain where the transmission lines are inaccessible by land, requiring helicopters to complete the line patrolling, and resulting in a very challenging effort to find the exact fault location, especially at night.

2.1.2 Customer Call Center

The second method is using a customer call center. This fault locating method is mostly used in distribution systems and was one of the first fault location methods implemented. In this case, each utility has a customer call center where they receive calls from customers and attend to customer needs. When a fault happens in the power system, the fault is isolated by the protective equipment leaving customers without power. When this series of events happens, the customers living in the area where the power outage occurred call the utility call center to request power restoration. After the utilities start receiving many phone calls from the same area where customers are without power, utilities ask customers for information such as home address or street intersections where customers without power live. Once the utility has the geographic location of customers without power, they pass that information to the utility mappers and utility transmission line crews to figure out what line or part of the distribution feeder is faulted. Thus this method is not very practical because it is time consuming, and uneconomical because requires many line crews patrolling a big geographical area.

2.1.3 Short Circuit Analysis

The third method is analyzing fault signatures. This method requires knowledge of power system theory for fault analysis. When faults occur on transmission lines, line protective microprocessor or fault detectors devices generate fault event data in their embedded memory. In order to start performing the fault location, all these relay or fault detector fault events need to be retrieved

from the devices for analysis. Analyzing fault signatures allows engineers to determine fault location because each fault signature is a function of the distance between the relay or fault detector sensing the faulted voltages and currents and the fault location. So during the fault location process utilizing short circuit analysis, the main objective is to retrieve the fault events from protective or fault detector devices and mimic what the protective or fault detector sensed during the fault in the short circuit analysis software by matching the ABC domain phasors and 012 symmetrical components. Once the real fault signature is matched in the short circuit analysis software a percentage of the transmission line where the fault signature was matched is determined. After the percentage of the line where the fault occurred is determined, it is multiplied by the total length of the line in miles and the result will be the fault location in miles from the line relay to the fault. The challenge of this fault location method is that it requires reliable communication to download fault events from relays or fault detectors located at remote stations. If communication fails, utilities need dispatch field personal to download relay events at the remote stations which can take a long time for arriving at the remote stations. Fault resistance can also complicate this approach.

2.1.4 Fault Location Algorithm

The fourth method is the use of fault location algorithms. Thanks to the advance in technology for relaying, relay engineers are able to program fault location algorithms in microprocessor relays or fault detector devices. It totally revolutionized the way to determine fault locations in transmission line when it became available. There are various types of fault location algorithms such as impedance based fault location algorithms, traveling wave based fault location algorithms, knowledge based fault location algorithms, and high frequency component based fault location algorithms.

Traveling wave based fault location algorithms calculate the fault distance by accurately measuring the time the traveling-waves arrive at the line terminals and use knowledge of the propagation velocity of the line. Normally traveling waves occur after faults, switching or lightning strikes. When a fault occurs in a transmission line, voltage and current transients will travel toward the line terminals. These transients will continue bounce back and forth between the fault point and the line terminals with attenuation due to losses and refractions until they reach a faulted steady state. The time of arrive of the incident waves can be used to calculate fault locations.

Knowledge based fault location algorithms calculate the fault distance using methods like expert system techniques. These techniques measure voltage and current, analyze setting coordination, post fault event record files, and determine fault sectioned. Artificial neural network techniques solve classification and optimization engineering problems that can be applied for fault location using voltage and current data, breaker status and relay targets. Another option is the use of fuzzy logic techniques. These knowledge based fault location algorithms require switch status, line measurements, atmospheric conditions, and fault detection device information, and basically use pattern modeling.

High frequency based fault location algorithms calculate the fault distance by using high frequency components to identify the path of the fault (line or ground) and then compute the fault location along the identified path based on power-frequency signals. High frequency signals are generated in the range of Hz to KHz due to fault conditions. A lot of these inject high frequency signals.

Impedance based fault location algorithms calculate the fault distance using the known per unit length impedance of the line, voltage and current data and traditional circuit analysis like Kirchhoff's voltage and current laws. Since this thesis will be focusing on impedance based fault location, impedance based fault location will be discussed in further detail in the next section.

2.2 Impedance Based Fault Location Algorithm Fundamentals

Impedance based fault location algorithms are used by line protective relays or fault detector devices to determine the exact location in miles within the faulted transmission line in a matter of milliseconds. Impedance based fault location techniques are the most practical for implementation out the four discussed above. However, these algorithms are susceptible to sources of errors such as system load conditions, effects of non-homogeneous systems, fault resistance, inaccurate fault type identification, influence of zero sequence mutual impedance, incorrect line parameters, un-transposed lines, shunt reactors and CT/PT measurements errors. Impedance based fault location algorithms can be divided in two types: one-ended and two-ended fault location algorithms. All of these algorithms are based on the apparent impedance looking into the transmission line from the relay terminal. Therefore, all impedance based fault location algorithms measure impedance to the fault and then compare it to the actual positive sequence line impedance.

2.2.1 One-Ended Fault Location Algorithms

One-ended impedance-based fault location algorithms calculate fault location from the apparent impedance seen looking into the line from one end. The best application for decent performance of one-ended fault location is for homogeneous systems where the source impedance and line impedance angle are the same and the ratios of Z0/Z1 are real and equal.

a. One-Ended Simple Impedance Method [1]

In terms of equipment, one-ended simple Impedance method algorithms require microprocessor based devices that can measure three-phase voltages and currents and are also capable of running fault location algorithms. In terms of fault calculation, one-ended simple impedance method

algorithms require phase to ground voltages and phase currents, and a correct fault type identification algorithm which provides faulted phase or phases. The factors that affect correct fault calculation using one-ended simple impedance method algorithms are:

- The combined effect of heavy load current and fault resistance
- Inaccurate fault type identification
- Influence of zero sequence mutual coupling effects
- Uncertainty of zero sequence impedance information
- Insufficient accuracy of line parameters
- Presence of shunt reactors and capacitors
- Low flow unbalance
- Series capacitor compensated lines
- Measurement errors such as CT or PT error
- Analog to digital conversion process error
- Filtering system error
- Clock sampling rate error

Table 2.1 lists the equations used in one-ended simple reactance method.

Table 2.1: One-Ended Simple Impedance Method Equations Based on Fault Type

Fault Type	**Positive-Sequence Impedance (mZ1L=)**
a-ground	$\frac{Va}{Ia + K0 \cdot 3 \cdot IG}$
b-ground	$\frac{Vb}{Ib + K0 \cdot 3 \cdot IG}$
c-ground	$\frac{Vc}{Ic + K0 \cdot 3 \cdot IG}$
a-b or a-b-g	$\frac{Vab}{Iab}$
b-c or b-c-g	$\frac{Vbc}{Ibc}$
c-a or c-a-g	$\frac{Vca}{Ica}$
a-b-c	Any of the following $\frac{Vab}{Iab}, \frac{Vbc}{Ibc}, \frac{Vca}{Ica}$

Where

K0 is (Z0L-Z1L)/3Z1L, zero sequence correction factor

Z1L is the positive sequence line impedance

Z0L is the zero sequence line impedance

IG is the residual current (3I0, zero sequence current)

m is the per unit distance to the fault (e.g. distance to fault in miles or kilometers divide by total line length in miles or kilometers)

b. One-Ended Modified Takagi Reactance Method [1]

There are two commonly applied Takagi One-Ended Impedance methods. The first one is a method which improves the simple reactance impedance method by reducing the effect of load flow and fault resistance. The second one is the modified Takagi method that uses zero sequence angle correction to reduce low flow effects. Therefore, the second method does not required pre-fault

data. The one-ended modified Takagi reactance method algorithms have some similarities to the one-ended simple impedance method algorithms. In terms of equipment, one-ended modified Takagi reactance method algorithms require a microprocessor-based device that uses measured three phase voltage and current and is also capable of running fault location algorithms. In terms of fault location calculation, one-ended modified Takagi reactance algorithms require local phase to ground voltages and phase currents, local negative sequence current components, and a fault type identification algorithm. The factors that affect the accuracy of the fault calculation one-ended modified Takagi reactance method algorithms are:

- The combined effect of heavy load current and fault resistance
- Inaccurate fault type identification
- Influence of zero sequence mutual coupling
- Uncertainty of zero sequence impedance
- Insufficient accuracy of line parameters
- Presence of shunt reactors and capacitors
- Low flow unbalance
- Series capacitors for compensated lines
- Measurement errors such as CT or PT error, analog to digital conversion process error
- Filtering system error
- Clock sampling rate error

Table 2.2 lists the equations used in the one-ended modified Takagi reactance method. Each equation is applied depending on the type of fault.

Table 2.2: One-Ended Modified Takagi Reactance Method Equations by Fault Type

Fault Type	Impedance (m=)
a-ground	$\frac{\mathrm{Im}\left(\mathrm{Vag}\cdot\overline{\mathrm{I2a}}\right)}{\mathrm{Im}(\mathrm{Z1L}\cdot\mathrm{Iag}+\mathrm{K0}\cdot\mathrm{IG})\cdot\overline{\mathrm{I2a}}}$
b-ground	$\frac{\mathrm{Im}\left(\mathrm{Vbg}\cdot\overline{\mathrm{I2b}}\right)}{\mathrm{Im}(\mathrm{Z1L}\cdot\mathrm{Ibg}+\mathrm{K0}\cdot\mathrm{IG})\cdot\overline{\mathrm{I2b}}}$
c-ground	$\frac{\mathrm{Im}\left(\mathrm{Vcg}\cdot\overline{\mathrm{I2c}}\right)}{\mathrm{Im}(\mathrm{Z1L}\cdot\mathrm{Icg}+\mathrm{K0}\cdot\mathrm{IG})\cdot\overline{\mathrm{I2c}}}$
a-b or a-b-g	$\frac{\mathrm{Im}\left(\mathrm{Vab}\cdot\mathrm{j}\,\overline{\mathrm{I2c}}\right)}{\mathrm{Im}\left(\mathrm{Z1L}\cdot\mathrm{Iab}\cdot\mathrm{j}\cdot\overline{\mathrm{I2c}}\right)}$
b-c or b-c-g	$\frac{\mathrm{Im}\left(\mathrm{Vbc}\cdot\mathrm{j}\,\overline{\mathrm{I2a}}\right)}{\mathrm{Im}\left(\mathrm{Z1L}\cdot\mathrm{Ibc}\cdot\mathrm{j}\cdot\overline{\mathrm{I2a}}\right)}$
c-a or c-a-g	$\frac{\mathrm{Im}\left(\mathrm{Vca}\cdot\mathrm{j}\,\overline{\mathrm{I2b}}\right)}{\mathrm{Im}\left(\mathrm{Z1L}\cdot\mathrm{Ica}\cdot\mathrm{j}\cdot\overline{\mathrm{I2b}}\right)}$
a-b-c	$\frac{\mathrm{Im}\left(\mathrm{V_{LL}}\cdot\overline{\mathrm{I_{LL}}}\right)}{\mathrm{Im}\left(\mathrm{I_{LL}}\cdot\overline{\mathrm{I_{LL}}}\right)}$

Where

K0 is (Z0L-Z1L)/3Z1L

Z1L is the positive sequence line impedance

Z0L is the zero sequence line impedance

I2a* is the complex conjugate of phase a reference negative sequence current

I2b*= a*I2a is the complex conjugate of phase b reference negative sequence current

I2c*=a^2*I2a is the complex conjugate of phase c reference negative sequence current

IG is the residual current (3I0)

VLL is the line-line voltage

ILL is the line-line current

ILL* is the complex conjugate of the line-line current

m is the per unit distance to the fault

2.2.2 Two-Ended Fault Location Algorithms

Two-ended impedance-based fault location algorithms calculate fault location from the apparent impedance seen looking into the line from both the local and remote ends. Thus, two-ended fault location algorithms need a communication channel to share phasor data between the local and remote line terminals. The best application of two-ended fault location for accurate response is for both homogeneous and non-homogeneous systems. These methods overcome many of the accuracy challenges from one-ended impedance methods.

a. Two-Ended Modified Takagi Negative Sequence Reactance Method [1]

In the two-ended modified Takagi negative sequence method, the main characteristic is that it uses a total negative sequence current which is the local current plus remote current to reduce the effect of load current. In terms of equipment, the two-ended modified Takagi negative sequence reactance method algorithms require microprocessor-based devices that can measure local three phase voltage and current and can receive remote three-phase voltage and current data with a time code stamp, have remote channel communication to transfer phasor data between local and remote terminals and are capable of running fault location algorithms. In terms of fault calculation, two-ended modified Takagi negative sequence reactance method algorithms required local phase to ground voltages and phase currents, local and remote negative current sequence components, a fault type identification algorithm, and correlation of time stamp or targeting information.

Two-ended negative sequence method is immune to:

- Fault resistance
- System non-homogeneity

Factors that affect correct fault calculation two-ended modified Takagi negative sequence reactance method algorithms are:

- Inaccurate fault type identification
- Insufficient accuracy of line parameters
- Presence of shunt reactors and capacitors
- Series capacitors for compensated lines
- Measurement errors such as CT or PT error, analog to digital conversion process error
- Filtering system error
- Clock sampling rate error
- Data alignment error
- Channel communication failure

Table 2.3 lists the equations used in the two-ended modified Takagi negative reactance method. Each equation is applied depending on the type of fault.

Table 2.3: Two-Ended Modified Takagi Negative Sequence Reactance Method Equations by Fault Type

Fault Type	Impedance (m=)
a-ground	$\frac{\mathrm{Im}\left(\mathrm{Vag}\cdot\overline{\mathrm{I2Ta}}\right)}{\mathrm{Im}\left[\mathrm{Z1L}\cdot(\mathrm{Ia}+\mathrm{K0}\cdot\mathrm{IG})\cdot\overline{\mathrm{I2Ta}}\right]}$
b-ground	$\frac{\mathrm{Im}\left(\mathrm{Vbg}\cdot\overline{\mathrm{I2Tb}}\right)}{\mathrm{Im}\left[\mathrm{Z1L}\cdot(\mathrm{Ib}+\mathrm{K0}\cdot\mathrm{IG})\cdot\overline{\mathrm{I2Tb}}\right]}$
c-ground	$\frac{\mathrm{Im}\left(\mathrm{Vcg}\cdot\overline{\mathrm{I2Tc}}\right)}{\mathrm{Im}\left[\mathrm{Z1L}\cdot(\mathrm{Ic}+\mathrm{K0}\cdot\mathrm{IG})\cdot\overline{\mathrm{I2Tc}}\right]}$
a-b or a-b-g	$\frac{\mathrm{Im}\left(\mathrm{Vab}\cdot\mathrm{j}\,\overline{\mathrm{I2Tc}}\right)}{\mathrm{Im}\left[\mathrm{Z1L}\cdot(\mathrm{Iab})\cdot\mathrm{j}\,\overline{\mathrm{I2Tc}}\right]}$
b-c or b-c-g	$\frac{\mathrm{Im}\left(\mathrm{Vbc}\cdot\mathrm{j}\,\overline{\mathrm{I2Ta}}\right)}{\mathrm{Im}\left[\mathrm{Z1L}\cdot(\mathrm{Ibc})\cdot\mathrm{j}\,\overline{\mathrm{I2Ta}}\right]}$
c-a or c-a-g	$\frac{\mathrm{Im}\left(\mathrm{Vca}\cdot\mathrm{j}\,\overline{\mathrm{I2Tb}}\right)}{\mathrm{Im}\left[\mathrm{Z1L}\cdot(\mathrm{Ica})\cdot\mathrm{j}\,\overline{\mathrm{I2Tb}}\right]}$
a-b-c	$\frac{\mathrm{Im}\left[\mathrm{VA_{LG}}\cdot\left(\overline{\mathrm{ITOTAL}}\right)\right]}{\mathrm{Im}\left[\mathrm{Z1_{line}}\left(\mathrm{IA_L}\right)\cdot\left(\overline{\mathrm{ITOTAL}}\right)\right]}$

Where

K0 is (Z0L-Z1L)/3Z1L

Z1L is the positive sequence line impedance

Z0L is the zero sequence line impedance

I2Ta* is the complex conjugate of total (local + remote) phase a referenced negative sequence current

I2Tb*= a*I2Ta is the complex conjugate of total (local + remote) phase b referenced negative sequence current

I2Tc*=a^2*I2Ta is the complex conjugate of total (local + remote) phase c referenced negative sequence current

b. Two-Ended Negative Sequence Method [1]

The two-ended negative sequence method differs from the two-ended modified Takagi method by using only local and remote three phase negative sequence voltage and current in comparison with two-ended modified Takagi method that uses local three phase positive sequence voltage and current with local and remote negative sequence currents. In terms of equipment, two-ended negative sequence method algorithms require microprocessor based devices that can measure local three phase voltages and currents and can receive remote three phase voltages and currents data with time code stamps, have a remote channel communication to exchange phasor data between local and remote line terminals and are capable of running fault location algorithms. In terms of fault calculation, two-ended negative sequence method algorithms require local and remote negative current sequence components, a fault type identification algorithm, correlation of time stamp or targeting information and pre-fault load data.

Two-ended negative sequence method is immune to:

- Fault resistance
- System non-homogeneity
- Effects of zero sequence line impedance
- Effects of zero sequence mutual coupling

Factors that affect correct fault calculation two-ended negative sequence method algorithms are:

- Inaccurate fault type identification
- Insufficient accuracy of line parameters
- Presence of shunt reactors and capacitors
- Series capacitors for compensated lines

- Measurement errors such as CT or PT error, analog to digital conversion process error
- Filtering system error
- Clock sampling rate error
- Data alignment error
- Channel communication fail

Table 2.1 lists the equation used in the two-ended negative sequence method. This equation is applied for all type of faults except 3 phase fault.

Table 2.4: Two-Ended Negative Sequence Method equation

Fault Type	**Impedance (m=)**
Any of the following a-ground, b-ground, c-ground, a-b, a-b-ground, b-c, b-c-ground, c-a, c-a-ground All except 3 phase faults	$\frac{V2S - V2R + I2R \cdot Z1L}{(I2S + I2R) \cdot Z1L}$

Where

V2S is the local negative sequence voltage

V2R is the remote negative sequence voltage

I2S is the local negative sequence current

I2R is the remote negative sequence current

Z1L is the positive sequence impedance

2.3 Fault Location Algorithm Error Sources

To improve accuracy of fault location it is necessary to reduce errors in the fault location calculation. The source of error typically depends on how the power system behaves during the fault. The following are impedance based fault location sources of error.

Line overload condition – the overload condition occurs when the utility tries to push more current in the transmission line than the transmission line is rated for. The combined effect of overload, direction of power flow and fault condition causes the fault location apparent impedance to decrease and the fault location looks closer than the actual fault location. This source of error applies mostly to one-ended methods.

Fault resistance – fault resistance is the resistance of an arc for phase to phase faults or the resistance from the faulted phase to foot of the transmission tower or trees for line to ground faults. In general as the fault resistance increases the apparent impedance between the fault detector device and the fault point location looks farther away than the actual fault location.

Infeed effect (tap lines) - when there is a tapped load between the fault detector device and fault point location, in general it will decrease apparent impedance and make the fault look closer than fault location than the actual fault location. When there is tapped generation between the fault detector and fault point location, it will increase in general the apparent impedance and makes the fault location look farther away than the actual fault location.

Zero sequence mutual coupling effects – mutual coupling effects occur when two transmission lines are in parallel. Zero sequence mutual coupling impacts on how zero sequence currents flow in the non-faulted and faulted transmission line during faults with ground current. If zero sequence current on the coupled line and the fault current on the faulted line flow in the same direction, apparent impedance decreases. Thus fault location look closer than the actual fault location. If the zero sequence current on the coupled line and the fault current on the faulted line flow in opposite directions, the apparent impedance increases. Thus fault location looks farther away than the actual fault location.

Uncertainty of zero sequence impedance – line to ground fault location algorithms require knowing an accurate zero sequence impedance of the line. However, it is very difficult to obtain an accurate zero sequence impedance for the line because it depends on the soil resistivity which is difficult to measure and may be changeable. A 100 to 1 variation in earth resistivity can produce a 2 to 1 change in zero sequence impedance. Therefore, zero sequence impedance could be inaccurate, resulting in an inaccurate fault location calculation.

Inaccurate fault type identification – algorithms make faulted phase selection based on calculations that determine the angle difference between zero and negative sequence current components to reduce the effect of load current on the phase selection. Another problem for fault type identification is the evolving faults. During evolving faults, fault location algorithms may require going from a line to ground loop to a phase to phase loop. If algorithm fails to select the correct fault type, the results from the fault location algorithm will be inaccurate.

Inaccuracy of line parameters – algorithms require correct positive, negative and zero sequence impedances in order to do an accurate fault location. One of the most used methods of calculating the positive, negative and zero sequence impedance is the Carson's line method.

Effect on non-transposed lines – the practice of transposing lines helps to equalize the mutual impedances between the phases. When the line is non-transposed depending on the conductor arrangement, it results in an unbalanced line with individual phase impedances that are different from the calculated values based on fully transposed line. As the length of the line increases, the error increases as well because it makes bigger impedance unbalance resulting in inaccurate line parameters calculations and therefore in an increased error of fault location, especially for one-ended algorithms.

Series Capacitors – series capacitors normally have MOV for overvoltage protection. The capacitor by itself can introduce steady-state and transients problems that can affect the fault location impedance algorithm calculation. When the MOVs conduct to protect series capacitors during faults, they introduce non-linearities that affect the fault location algorithm. In a case, where there are thyristor controlled capacitors they also introduce harmonic currents in line which also affect the fault location algorithm calculation.

CT or PT measurements error – CTs and PTs are not ideal instruments and they introduced small tolerable measurement errors when they operate under the normal conditions. However, when they operate under electrical disturbances like faults, CTs may saturate or CVTs may produce transients. When a CT saturates, it introduces non-linearities, or in the worst case will not produce secondary current that can be measured by fault detector devices. In the case of CVTs, during electrical disturbances CVT transient response creates fundamental frequency under voltages that also affect the fault location calculation.

Hardware or software error – the typical errors from hardware or software are analog to digital process errors, filtering system errors, and clock sample rate errors. Microprocessor devices use A/D converters to convert the analog quantities into digital data. However when the conversion process from analog to digital fails because hardware or software errors the microprocessor-based device will not be capable of producing correct phasor data resulting in a wrong fault location calculation.

2.4 Characterization of Fault Location Error Calculation

2.4.1 Determination of Measurement Error

There are several methods for determining the measured fault location error. The three methods for determining the measured error are absolute error, relative error based on line length, and traditional relative error. Comparing the error methods, absolute error provides a value regardless of the line length and relative errors are more useful to compare fault location methodologies independently of the power system.

2.4.2 Methods to Calculate Fault Location Error

Since there are several sources that introduce errors in fault location, the fault location error needs to be quantified. The following are three methods to determine measurement errors in fault location calculation.

a. Absolute Error

$$e_a := \left| m_m - m_t \right| \tag{2.1}$$

Where

e_a Absolute error

m_m measured fault location in p.u., percentage, or length

m_t true fault location in p.u, percentage, or length

b. Relative Error Based on Line Length

$$e_l := \frac{\left| m_m - m_t \right|}{L} \tag{2.2}$$

Where

e_l Relative error based on line length

m_m Measured fault location in p.u., percentage, or length

m_t True fault location in p.u, percentage, or length

L Line length

c. Traditional Relative Error

$$e_t := \frac{\left|m_m - m_t\right|}{m_t} \tag{2.3}$$

Where

e_t Relative error

m_m Measured fault location in p.u., percentage, or length

m_t True fault location in p.u, percentage, or length

Depending on the purpose of the error calculation and the type of fault location algorithm, it is necessary to determine which error method is the best when comparing errors from various algorithms. For this thesis work, the relative error based on the line length will be used because the combination of source impedance ratios and fault location may have an effect when comparing errors of various algorithms if not referenced to line length.

Chapter 3 - Synchrophasor Technology Fundamentals

3.1 What are Synchrophasors and How They are Used?

In the past, EMS and SCADA systems had an acceptable performance for monitoring, control, and optimization functions in power systems. However, as power systems started becoming more complex with the integration of third party generation including renewable energy sources, the need has arisen an opportunity for new technology to meet the new challenges in monitoring, controlling and optimizing complex power systems. One of the new emerging technologies for power systems is time synchronized phasors known as synchrophasors. Synchrophasor measurement systems are now being adopted by many utilities as the new way to monitor and optimize power systems. Some utilities are beginning to use them in system control as well.

Synchrophasor technology is based on measurement of analog voltages and currents from the power system which are processed to produce digital phasors synchronized to an absolute time reference provided by the global positioning system (GPS).

One key component in synchrophasor technology is the phasor measurement unit (PMU). The Phasor Measurement Unit concept was developed in the 1980's with the purpose implementing synchronized phasor measurement theory to use the phasor measurements unit in a lab environment only. Now advances in technology have allowed the phasor measurement unit to go from a lab environment to a production environment. As a result, many utilities or power authorities around the world have adopted the synchrophasor technology in protection and monitoring areas.

Some of the key benefits of the use of synchrophasors in power systems are the following:

- Wide-area visualization
- Oscillation detection
- Generation model and parameter validation
- Island detection
- Voltage instability monitoring
- Event analysis
- Identification of potential mal-function of devices in the grid

Here are some collected experiences across the world where phasor data units (PMUs) have been installed to monitor or manage electrical grids.

3.2 Synchrophasor Technology Deployment around the World

3.2.1 U.S Deployment of Synchrophasor Technology

In the U.S., the Department of Energy has been the leader in the research and deployment of synchrophasor technology and is pushing the adoption and maturity of this technology all across the nation. The big efforts from the U.S. Department of Energy to accelerate the deployment of synchrophasor technology and the combined partnership from industry have produced technical standards and also created a community of users called the North American Synchrophasor Initiative (NASPI). [2]

The deployment of synchrophasors in the western region of the United States has been made to improve system reliability and increase the understanding of system behavior. The synchrophasor applications include system performance baselining, event analysis, model validation, instability and oscillation detection, reactive power management, restoration, harmonic determination, transient analysis, and fault location. The benefits of deployed syncrophasors in the U.S. western

region are data analysis of system events, system modeling improvements to have more accurate dynamic models to provide benefits to operation and system planning under complex grid conditions, situational awareness that tracks the phenomena such as voltage, angle, frequency instability, angle pairs between two geographically diverse interconnected systems, and thermal overloads.

The deployment of synchrophasor technology in the eastern region of the United States has been done to enhance monitoring and improve the data model by placing priority on internal and external area ties, major generation clusters, wind, load centers, key corridors, and FACTS devices. The New York System Independent Operator (NYSIO) and Pennsylvania-New Jersey-Maryland interconnection LLC (PJM) also have a common goal of expanding their PMU networks with PMU networks in New England, Mid-Atlantic, Midwest, and Ontario, Canada to create a better situational awareness throughout the eastern United States. The value of the deployment of synchrophasor in the eastern region has generated better dynamic models of grid elements like generators and FACTS devices such as static var compensators and static synchronous compensators. It also has help to better understanding of dynamic behavior of loads. Synchropahsors in the eastern region are a proven tool for event detection like oscillation detection and post event analysis.

The deployment of synchrophasor technology in the Electric Reliability Council Of Texas (ERCOT) region focuses on three main tasks: oscillation detection and alarming, generator model validation, and post-disturbance analysis and reporting. The benefits of the deployment of synchrophasor measurements in the ERCOT region are the real-time visualization and alarming during voltage transients, angle difference transients, frequency transients, and oscillatory events to have a better understanding of the system dynamics.

3.2.2 Wide-area Monitoring in the Continental European Power System

In 2013, Italy and Switzerland started using synchrophasors for wide area monitoring systems as an additional tool for power system operational analysis. The PMU applications currently used in Italy and Switzerland are: fault analysis support, comprehensive system load monitoring, dynamic line thermal monitoring, and power system restoration support tools. The PMU systems implemented in Italy and Switzerland so far have delivered key measurements used to prepare, observe and improve dynamic system behavior at a wide area level, in order to have a very useful picture of the system state. [2]

3.2.3 WAMS Initiatives in India

In the past decades, the Indian grid has suffered with respect to power system stability. All these problems were caused by the limitations like lack of time stamped data, lack of synchronization, modeling errors and skewed data from SCADA/EMS used to monitor the system. As a result, India has implemented wide area monitor system pilot projects using PMUs. Some of the benefits seen using PMUs in India are high data precision, synchronized measurements, fast rate of data communications, and metering for voltage angle measurements. A key benefit for synchrophasors is the ability to measure volt angles. [2]

3.2.4 Recent Developments and Applications of PMU/WAMS in China

In the efforts to convert China's electrical grid from conventional to smart grid, China has focused on the implementation of PMUs to have a wide area monitoring system. China has four areas of synchrophasor application. In the system modeling area, China has time synchronization and data measurements applications, load modeling, and generator parameter identification applications. In

the monitoring and analyzing real-time power system dynamics area, China has substation state estimation, low frequency oscillation detection, and identifying power grid disturbances applications. In the wide area control and protection area, China has an intelligent alarm system for cascading tripping, wide area damping control, and wide area protection applications. So far the benefits are still under evaluation, but most of the synchrophasor projects already commissioned have shown excellent performance and strong potential. However, the huge amount of data measured by Chinese PMUs remains far from being fully exploited to meet all smart grid requirements and goals. [2]

3.3 Synchrophasor Measurement Fundamentals

The IEEE C37.118.1 standard was developed to define synchronized phasor (synchrophasor), frequency and the rate of change of frequency (ROCOF) measurements. [3]

3.3.1 Synchrophasor measurement

In general terms, a synchrophasor is a digital phasor that is created by processing instantaneous digital samples of voltage or current waveforms through digital filters producing magnitude and phase angle in rectangular form or polar form.

a. Phasor definition

Power systems are physically characterized by an alternating voltage or current signal. This alternating signal, voltage or current, is a time-varying sinusoidal signal that have the form of a sine or cosine. In order to analyze any alternating voltage or current signal, it is necessary to know the voltage or current value at any instant in time. To achieve it, a time domain equations must be

used. So the mathematical expression in time domain of a sinusoidal waveform is defined by the following equation:

$$x(t) := Xm \cdot \cos(\omega \cdot t + \phi) \tag{3.1}$$

The phase angle in equation (3.1) is the angle relative to a reference angle.

Power systems also can be analyzed in frequency domain using phasors. A phasor is a complex number with an amplitude and angle and it is defined for an angular frequency which means that analysis with other phasors must be done with the same time scale and frequency. The mathematical expression of a phasor for a cosine is defined by the following equation:

$$X := \frac{Xm}{\sqrt{2}} \cdot e^{j \cdot \phi} \tag{3.2}$$

Where

$\frac{Xm}{\sqrt{2}}$ is the root-mean square (rms) magnitude of the waveform

$e^{j\Phi}$ is the phase angle of the waveform

b. Synchrophasor definition

A synchrophasor is made of two main parts. The first part is the measured phasor and the second part is the time synchronization. The synchrophasor measurement representation is the instantaneous magnitude (Xm) of equations (3.1) and (3.2) and the instantaneous phase angle (ϕ of equations (3.1) and (3.2)). The definition of synchrophasor states that the angle ϕ is the offset of the cosine function at the nominal system frequency synchronized to the Universal Time Coordinated (UTC).

For time synchronization, the phasor measurement unit (PMU) must have a reliable and accurate time source such as the Global Positional System (GPS) in order to provide accurate time traceable to Universal Time Coordinated (UTC) to keep synchronized.

c. Measurement Time Synchronization

As mentioned in the synchrophasor definition part, all phasor measurements units must have the capability of receiving time from reliable and accurate source that can provide time traceable to UTC with sufficient accuracy. One example of an accurate time source is the Global Positioning System (GPS). The time source must have sufficient accuracy in order to keep the following errors within required limits:

- Total vector error (TVE)
- Frequency error (FE)
- The rate of change of frequency (ROCOF) error

d. Time Tags

In phasor measurement units (PMU), the phasor measurements are the estimated phasor representation of sinusoidal waveform. The estimate is made for the signal at a particular instant of time, and that time is represented by the phasor time tag. The synchrophasor measurement tagged with the Coordinated Universal Time (UTC) consists of three numbers: a second-of-century (SOC) count, a fraction of second (FRACSEC) count, and a message quality flag.

3.3.2 Synchrophasor Measurement Estimation

A phasor measurement unit (PMU) must be able to calculate and report the phasor estimates for single phase or positive sequence per the IEEE C37.118.1 standard.

a. Frequency Estimation

Synchrophasors are calculated in relation to the system nominal frequency. If the sinusoidal signal is represented by the following:

$$x(t) := Xm \cdot \cos(w \cdot t + \theta) \tag{3.3}$$

Where

$$w := 2\pi \cdot f \cdot t$$

Then the formula for frequency becomes:

$$f(t) := \frac{1}{2\pi} \cdot \left(\frac{d}{dt} w \right) \tag{3.4}$$

b. Rate of Change of Frequency (ROCOF) Estimation

The rate of change of frequency is defined as the rate of change in deviation of frequency from the nominal frequency. The rate of change of frequency is defined as in (3.5):

$$ROCOF(t) := \frac{d}{dt}(f(t)) \tag{3.5}$$

3.3.3 Synchrophasor Measurement Evaluation

A phasor measurement unit (PMU) should be capable of determining if phasor estimates are within the measurement requirements. Since synchrophasor theoretical values and the measured values may have differences in amplitude, phase and frequency, it is necessary to consider total vector

error, frequency error, and rate of change of frequency error quantities in qualifying measurements.

a. Total Vector Error (TVE)

The total vector error is referred as the difference between the measured phasor and the actual phasor. The allowable maximum total vector error for measured phasors, voltage or current, should be equal or less than one percent (≤ 1%) which corresponds to either maximum phase error of 0.57° or magnitude error of 1%. Synchrophasor measurements shall be evaluated using TVE criteria. The total vector error is defined as follows:

$$\mathrm{TVE} := \frac{\left|\mathrm{V_{measured}} - \mathrm{V_{actual}}\right|}{\mathrm{V_{actual}}} \tag{3.6}$$

The error of the estimated phasor for low quality field data can be written as follows:

$$\mathrm{Verror} := \mathrm{Vmeasured} - \mathrm{Vactual} \tag{3.7}$$

Where

Vmeasured is the measured phasor

Vactual is the ideal phasor

b. Frequency Error (FE)

When the time source varies its timing, it will cause an error in the frequency measured by the phasor measurement unit (PMU). Frequency error is the difference between the measured frequency and the actual frequency.

The maximum steady-state frequency error allowed for phasor measurement is 0.005Hz which corresponds to time source FE of 0.083MHz in a 50Hz system or time source FE of 0.1MHz in a 60Hz system.

The frequency error must be evaluated using following definition:

$$FE := \left| f_{nominal} - f_{measured} \right| \tag{3.8}$$

Where

fmeasured is the measured frequency

fnominal is the nominal frequency

The measured and nominal frequency values are for the same instant of time given by the time tag of phasor estimated values.

c. Rate of Change of Frequency (ROCOF) Error

The maximum steady-state rate of change of frequency error allowed for phasor measurement is 0.01Hz/s. The rate of change of frequency error must be evaluated using the following definition:

$$RFE := \left| \left(\frac{d}{dt} f_{nominal} \right) - \left(\frac{d}{dt} f_{measured} \right) \right| \tag{3.9}$$

d. Measurement Response Time

The measurement response time is the time that a measurement takes to go from one steady-state value to a new steady-state after a step change is applied to the input.

e. Measurement Delay Time

The measurement delay time is the time that a measurement takes to go from the instant a step change is applied to the PMU input to 50% of the transition between the initial steady-state value and the final steady-state value.

f. Measurement Reporting Latency

Latency is the time delay from when an event occurs on the power system to the time that the event is reported in data in the PMU. Latency depends in many factors like reporting rate, performance class, estimation method, measurement filtering, and PMU processing time.

g. Operational Measurement Errors

The phasor measurement unit must be capable of assigning flags to each phasor estimate to indicate internal problems encountered during the measurement process. The errors that need to be flagged are A/D errors, memory overflow and any other condition that can cause an error in the measurement.

3.3.4 Measurement Reporting

In general, each phasor estimate must report three measurements: synchrophasor, frequency and the ROCOF data. All three measurements shall be reported at a constant rate, for the same time stamp and the reporting time shall be evenly spaced.

a. Reporting Rates

The phasor measurement unit (PMU) reports phasor measurements in frames. So PMUs must support data rates at sub-multiples of the nominal power system frequency. Required rates are based on 50Hz and 60Hz system references. At 50Hz, the required reporting rates are 10, 25 and 50 frames per second. At 60Hz, the required reporting rates are 10, 12, 15, 20, 30 and 60 frames per second.

b. Reporting Times

For a reporting rate X frame per second (fps), the reporting times must be space evenly through each second with a frame number 0 coincident with a 1 pulse per second (PPS) signal provided by Global Positional System (GPS). These reporting times are used to determine the instantaneous values of the synchrophasor.

3.3.5 Synchrophasor Measurement Compliance

a. Performance Classes

The synchrophasor standard defines two classes of performance: P class and M class. The P class is intended for applications that require fast response and does not need explicit filtering. Protection applications normally require fast response. The M class is intended for applications that do not require fast response and can be affected by aliased signals. Monitoring applications normally required high precision, but do not require fast response.

3.4 Synchrophasor Network Communication Fundamentals

The simple structure of a synchrophasor network consists of phasor measurement units (PMUs) and phasor data concentrators (PDCs). The synchrophasor data collection can be designed in different ways. Typically, if multiple intelligent electronic devices (IEDs) in a substation provide synchronized phasor measurements to a local phasor data concentrator (PDC), the PDC may be installed in the substation. Or if many phasor measurement units (PMUs) are installed in various key substations, they can instead send real-time synchronized phasor measurement data to a phasor data concentrator (PDC) installed at strategic location where the data can be collected. In general, synchrophasor network communication system has four main elements: PMUs, network communication system, PDCs and data storage.

Phasor Measurement Unit (PMU) – estimates synchronized phasor measurement, frequency, and rate of change of frequency from voltage or current signals and a time synchronizing signal. Voltage and current synchrophasors are based on digital sampling of sinusoidal waveforms and time stamped with a precise time signal. The phasor measurement unit (PMU) is a logical device that also provides optional information such as calculated megawatts (MW) and megavars (MVARS) and Boolean status words such as breaker status. The phasor measurement unit (PMU) can be a stand-alone physical device or integrated in a multifunctional device such as a protective relay, Digital Fault Recorder (DFR), or meter. The phasor measurement unit has the capability of recording the data locally or transmitting it in real-time to a central location.

Network Communication System – This network provides the transport medium for synchronized phasor data from Phasor Measurements Units (PMUs) to Phasor Data Concentrators (PDCs) and Super Phasor Data Concentrators (SuperPDCs). Synchrophasor data communication can be provided by a private production-grade Local-Area Network (LAN) or Wide-Area Network (WAN)

that should offer acceptable security availability, and meet functional requirements for synchrophasor system architecture known as “NASPInet”, which provides flexible, fast, vendor-agnostic, and secure transportation of phasor measurements from data collection points to various levels of Phasor Data Concentrators (PDC’s) to the phasor data application point.

Phasor Data Concentrator (PDC) – This is a node in the network where synchrophasor data from a number of phasor measurement units (PMUs) or phasor data concentrators (PDCs) is correlated and fed out as a single stream to higher level phasor data concentrators (PDCs) or synchrophasor applications. When the phasor data concentrator receives the synchrophasor data, it correlates or time-aligns the data by time tags to create a subsystem wide measurement. The phasor data concentrator has additional functions such as various quality checks and appropriate flags inserted into the correlated data, checks for disturbance flags and records data files for analysis, records the performance, monitors overall system, displays the results, and has specialized output to communicate with SCADA or EMS systems. A Phasor Data Concentrator can have the capability to store data as long it has an integrated historian.

Data Storage – Data storage stores all synchronized phasor data produced by the phasor measurement units. The data storage system can be integrated with the Phasor Data Concentrator (PDC), or be stand-alone data historians or traditional database systems.

3.5 Synchrophasor Message Communication Services

Synchrophasor data can be transmitted using two types of communication: serial communication or network communication.

3.5.1 Serial Communication

Synchrophasor data must first be mapped into the serial communication interface. RS-232 is commonly used for serial communication and data is sent byte by byte using functions that access the serial interface. The serial communication system may apply ordering and encoding within the communication system. As long as compatible devices are used at both ends, the data can be written into and read from the serial interface.

3.5.2 Network Communication

Synchrophasor data must be mapped into the transmission control protocol (TCP) or the user datagram protocol (UDP). Synchrophasor data shall be written and read using internet protocol (IP) standard input-output functions. The IP may be carried over Ethernet with stacked protocols where each message layer is encapsulated to the next one down to the transport layer, where the message is sent.

a. Synchrophasor Communication Methods for Internet Protocol

Data transmission using internet protocol is a real-time method where data is sent immediately after measurement is made using a predefined constant interval. Using this standard, synchronized phasor data can be carried over any communication system that has sufficient bandwidth that allows using this message structure. The required bandwidth will be dictated by the reporting rate and the message size. Using internet protocol, cyber security can be addressed in the communications used to transport synchronized phasor data.

b. Transmission Using Internet Protocol over Ethernet

Phasor measurements systems commonly use the internet protocol over network communications. The common methods for communication using internet protocol are:

Client-Server – The device providing the data is the server and the device receiving the data is the client. For synchrophasor systems, the phasor measurement unit, phasor data concentrator or any other device that will output synchrophasor data perform the server function. A phasor data concentrator (PDC) or any other device that receives synchrophasor data does the client function. In cases where data transmission is initiated by command, the client initiates contact and controls data flow with commands.

Basic Modes of Operation: spontaneous and commanded – With spontaneous operation, the server sends data by user datagram protocol to a designated destination without stopping, whether a receiving device is present or not. The stream is initiated by a function in the device accessed separately from data operations. With commanded operation, the sender only sends data when the client requests it using the standard start and stop commands.

Transmission Control Protocol Only Method - This method has a single transmission control protocol (TCP) connection over which commands, data, header and configuration frames are passed. The client only needs to know the server address. Transmission control protocol is a connection based protocol, thus it is strictly a 1-to-1 connection, so if data is required by more than one client, it has to be sent separately to each destination. This increases traffic and requires that phasor measurement units (PMU) support multiple transmission control protocol connections. The transmission control protocol requires two-way communication to make a connection. During the transmission of synchrophasor data, transmission control protocol data management services apply

to all data; as a result the link is easy to administer, troubleshoot, and manage. One transmission control protocol disadvantage is that with high rates and continuous data transmission, a single dropped data packet can cause data backup in the transmission control protocol mechanism that can cause an interval of data loss. If the data is recovered, all data is delayed which it worse than the loss of one packet for real-time applications.

User Datagram Protocol Only Method - This method uses straight user datagram protocol for communication in both directions for phasor measurement unit messages, including commands, data, header and configuration. The client must know the server address and the port number. The advantages of using UDP are reduced bandwidth requirements and elimination of the backup delay due to data dropouts. The disadvantage is that server-client communication is not confirmed so it is difficult to locate problems if the communication has issues. With UDP, data is not re-transmitted in case of error, so error packets are permanently lost. If the data is sent to a unicast IP address, it then must be sent to each client separately. If the data is sent to a multicast IP address, it then allows various clients to receive it, minimizing traffic network.

Combined Transmission Control Protocol / User Datagram Protocol Method – This method uses transmission control protocol for commands, header, and configuration communications, and user datagram protocol for sending data. The server address and port must be known to the client. And the client port UDP must be known to the servers, in the case of PMUs, if the UDP message is sent by multicast, that address the address must be known to the server as well. The commands, header and configuration communication are secured by the transmission control protocol link and the data is sent by user datagram protocol. This method has the advantage of more secure transmission on critical data portions and minimal delay or backup risk on streaming. Data will not be replaced if corrupted.

Spontaneous Data Transmission Method – This method continuously sends data out in the IEEE 37.118 format to a preset destination. The data is sent by UDP and can be unicast, multicast, or broadcast. The output is initiated by a device or device interface. Since the data is sent by user UDP, a destination device does not need to be present. This mode is useful for sending data using multicast to many clients that may be coming online or offline randomly. It allows steady supply of data without interruption and can be used when two-way communication is prohibited such as through a firewall.

3.6 Synchrophasor Data Transfer Fundamentals

The purpose of the IEEE C37.118.2 standard is to define a method for exchange of phasor measurement data between equipment. Data transfer specifies messaging including types, uses, contents, and data format for real-time communications between PMUs, PDCs and synchrophasor computer applications. In general, IEEE C37.118.2 synchrophasor data transfer is handled by exchanging four messages types: data message, configuration message, header message, and command message. The first three messages are transmitted from a data source (PMU/PDC) and the last one (Command) is received by the PMU or PDC.

3.6.1 Synchrophasor Package Data

Once a PMU is ready to transmit digital synchronized phasor data into the network, the PMU must ensure that the digital synchronized phasor data contains the following information within the guidelines:

- Current or voltage phasor value
- Frequency value
- Rate of change of frequency value

- Measurement time tag word containing: SOC, FRACSEC, and message time quality flag
- Total Vector Error (TVE) less than 1%
- Frequency Error (FE) less than 0.083MHz in a 50Hz system or 0.1MHz in a 60Hz system
- Rate of change of frequency (ROCOF) error less than 0.01Hz/s
- Time-aligned measurements

3.6.2 Multiple Data Streams Communication from PMUs to PDCs

Once the PMU or PDC is ready to transmit synchrophasor data into the network, it can transmit its data in one or more separate streams. Each stream may have different content and may be sent at a different rate. Each stream is individually controllable, has its own IDCODE and a separation control for sending data to different devices with different purposes, allowing latency control and P-class or M-class supply. The destination of each stream may be to a different device or location. For example, local PDCs collect and time-align synchrophasor stream data from multiple phasor measurement units and feed the data to applications. Mid-level regional PDCs collect the synchrophasor stream data from multiple phasor data concentrators, conduct data quality check and feed the data to applications. Higher level phasor data concentrators or super phasor data concentrators (SuperPDCs) both collect and archive synchrophasor stream data. Each layer in the hierarchy may have different data services such as latency, quality and resolution and also have requirements such as archival and event triggering.

3.6.3 Synchrophasor Message Format

Message application refers to the format of messages to and from a PMU or PDC for use in real-time network communication of synchronized phasor data. The frame messages must be transmitted in their entirety as they are specified. Frames can be transmitted in two ways: one way

is using stacked protocols such as manufacturing messaging protocol (MMS) or IP, and a second way using direct systems like raw Ethernet or RS-232 serial. When frame messages use stacked protocols, the frame should include sync and CRC-CCITT (data integrity message) and it has to be written and read from the application layer interface. When frame messages use direct systems, the frame only sends a CRC-CCITT message to assure data integrity.

If the PMU or PDC needs to transmit real-time synchronized phasor data with other systems, the IEEE C37.118.2 protocol is required. This message protocol can be used with a single phasor measurement unit or a secondary system that receives data from several phasor measurement units.

If the phasor measurement unit or phasor data concentrator is used only for synchronized phasor data archiving or recording, the IEEE C37.118.2 protocol is not required.

3.6.4 Message Framework

There are four messages types: data, configuration, header, and command.

- Data messages are the measurements made by the phasor measurement unit.
- Configuration is a machine-readable message describing the data types, calibrator factors, and other meta-data that the phasor measurement unit or phasor data concentrator sends.
- Header information is human readable descriptive information sent from a phasor measurement unit or phasor data concentrator provided to the user.
- Commands are machine-readable codes sent to the phasor measurement units or phasor data concentrators for control or configuration.

In normal operations the phasor measurement unit sends data frames. So when a phasor measurement unit (PMU) transmits, it formats the data as frames. Commands and other messages

that are not understood such as an unimplemented feature, incorrect IDCODE, or bad CRC, are discarded. In all frames, the SYNC word is transmitted first and the CHECK word is transmitted last. Two and four byte words including integer and floating point numbers are transmitted most significant byte first. All frame types use the same order and format.

a. Data Frame Structure

The data frame message contains the synchronized phasor measurements made by the phasor measurement unit (PMU). In normal operation, the phasor measurement unit (PMU) continuously streams the data messages. Table 3.1 shows each function and its size of the data frame structure.

Table 3.1: Data Frame Organization

No.	Field	Size (bytes)
1	SYNC	2
2	FRAMESIZE	2
3	IDCODE	2
4	SOC	4
5	FRASEC	4
6	STAT	2
7	PHASORS	4xPHNMR or 8xPHNMR
8	FREQ	2/4
9	DFREQ	2/4
10	ANALOG	2xANNMR or 4xNNMR
11	DIGITAL	2xDGNMR
	Repeat 6 to 11	
12+	CHK	2

b. Configuration Frame Structure

A configuration frame is a machine-readable BINARY data set containing information and processing parameters for the synchronized phasor data stream. There are three types of configuration frame messages CFG-1, CFG-2 and CFG-3. CFG-1 indicates all of the data the

PMU/PDC is capable of reporting. CFG-2 indicates measurements currently being reported (transmitted) in the data frame.

Configuration frame CFG-1 and CFG-2 organization

Table 3.2 shows each function and its size of the configuration frame CFG-1 andCFG-2 structure.

Table 3.2: CFG-1 and CFG-2 Frame Organization

No	Field	Size (bytes)
1	SYNC	2
2	FRAMESIZE	2
3	IDCODE	2
4	SOC	4
5	FRACSEC	4
6	TIME_BASE	4
7	NUM_PMU	2
8	STN	16
9	IDCODE	2
10	FORMAT	2
11	PHNMR	2
12	ANNMR	2
13	DGNMR	2
14	CHNAM	16x(PHNAM+ ANNMR+ 16xDGNMR)
15	PHUNIT	4xPHNMR
16	ANUNIT	4xANNMR
17	DIGUNIT	4xDGNMR
18	FNOM	2
19	CFGCNT	2
		Repeat 8-19
20	DATA_RATE	2
21	CHK	2

Configuration frame CFG-3 organization

Configuration frame 3 includes the basic information that is in configuration CFG-1 and CFG-2, but adds a number of fields defining PMU characteristics and quantities being sent such as PMU and

signal information and has an extendable frame. Table 3.1 shows each function and its size of the configuration frame CFG-3.

Table 3.3: CFG-3 Frame Organization

No	Field	Size (bytes)
1	SYNC	2
2	FRAMESIZE	2
3	IDCODE	2
4	SOC	4
5	FRACSEC	4
6	CONT_IDX	2
7	TIME_BASE	4
8	NUM_PMU	2
9	STN	1-256
10	IDCODE	2
11	G_PMU_ID	16
12	FORMAT	2
13	PHNMR	2
14	ANNMR	2
15	DGNMR	2
16	CHNAM	1-256 per Name
17	PHSCALE	12xPHNMR
18	ANSCALE	8xANNMR
19	DIGUNIT	4xDGNMR
20	PMU_LAT	4
21	PMU_LON	4
22	PMU_ELEV	4
23	SVC_CLASS	1
24	WINDOW	4
25	GRP_DLY	4
26	FNOM	2
27	CFGCNT	2
	Repeat 9-27	
28	DATA_RATE	2
29	CHK	2

c. Header Frame Structure

The header frame is human-readable information about the phasor measurement unit, the data sources, scaling, algorithms, filtering and other information. The header message provides user defined descriptive information sent from the phasor measurement unit or phasor data

concentrator. The command functions include: turn-off transmission, turn-on transmission, send header, send CFG-1 frame, send CFG-2 frame, and send CFG-3 frame. Table 3.4 shows each function and its size of the header frame message.

Table 3.4: Header Frame Message Organization

No	Field	Size (bytes)
1	SYNC	2
2	FRAMESIZE	2
3	IDCODE	2
4	SOC	4
5	FRACSEC	4
6	DATA 1	1
K+6	DATA K	1
K+7	CHK	2

d. Command Frame Structure

The command frame contains commands that a data sending device must be able to receive and is used for the device to take appropriate actions. Table 3.5 shows each function and its size of the command frame message.

Table 3.5: Command Frame Message Organization

No	Field	Size (bytes)
1	SYNC	2
2	FRAMESIZE	2
3	IDCODE	2
4	SOC	4
5	FRACSEC	4
6	CMD	2
7	EXTFRAME	0-65518
8	CHK	2

3.7 Precision Time Protocol (PTP) Standard for Synchrophasor Measurements

The main objective of synchrophasor technology is to measure currents and voltages synchronously at different line terminals within a power system. Thus, it is important for this technology to have a high precision time to synchronize all of phasor measurements. In order to achieve this synchronization of phasors, it is necessary to have a time source and a communication network protocol to distribute the time reference within the PMU network. [4]

The Global Position System (GPS) is normally is used as the source for time reference in synchrophasor technology in North America. Since synchrophasor time synchronization has to have a resolution in the order of microseconds or less, it is necessary to have a reliable timing source as a time reference. GPS can provide accurate clock settings needed for synchronizing phasor measurements. GPS is a group of satellites that provide clock signal to ground based receivers. In the application at hand, these GPS receivers re-distribute the GPS time reference to phasor measurements units. [5]

To distribute the time reference over the PMU network, IEEE 1588 Precision Time protocol (PTP) [6] typically is used. IEEE 1588 provides high precision synchronization, interoperability, robust response to network failures and deterministic control of the delivered time quality. It also specifies the preferred physical layer higher level protocol used for PTP messages. IEEE 1588 PTP clock synchronization model in general defines the following:

- The protocol enables precise synchronization of clocks in technologies such as network communication, local computing and distributed objects

- The protocol is applicable to systems communicating by local area networks supporting multicast messaging including Ethernet
- The protocol enables heterogeneous systems that include clocks of various precision, resolution, and stability to synchronize to a grandmaster clock
- The protocol supports system-wide synchronization accuracy in the sub-microsecond range with minimal network and clock computing resources
- The protocol includes mappings to User Datagram Protocol (UDP) / Internet Protocol (IP), DeviceNet, and a layer-2 Ethernet implementation. It includes formal mechanisms for message extensions, higher sampler rates, correction for asymmetry, and a clock type to reduce error accumulation in large topologies
- The protocol supports unicast and multicast messaging

3.7.1 Precision Time Protocol Systems

A precision time protocol (PTP) system is a network system containing a combination of PTP devices and non-PTP devices. PTP devices include ordinary clocks, boundary clocks, end-to-end transparent clocks, peer-to-peer transparent clocks, and management nodes. Non-PTP devices include bridges, switches, routers, computers, printers and other devices within the network. PTP is a distributed protocol that specifies how real-time clocks in the system synchronize with each other. The clocks are organized into a master-slave synchronization hierarchy with the grandmaster clock at the top determining the reference time for the entire system. The synchronization is achieved by exchanging PTP timing messages with slaves using time information to adjust their clocks to the time of their master. Devices in a PTP system communicate with each other via a communication network. The network includes translation devices between segments implementing different

network communication protocols. The protocol executes within domains. All PTP messages, data sets, state machines and other PTP entities are associated with a particular domain.

3.7.2 Precision Time Protocol Message Classes

The protocol defines both event and general PTP messages. Event messages are Sync, Delay_Req, Pdelay_Req and Pdelat_Resp. General messages are Announce, Follow_up, Delay-Resp, Pdelay_Resp_Follow_up, management, and signaling. The Sync, Delay_Req, Follow_up, and Delay_resp are messages that generate and communicate timing information needed to synchronize ordinary and boundary clocks using the delay-respond mechanism. The Pdelay_req, Pdelay_Resp, and Pdelay_Resp_Follow_up messages are used to measure the link delay to correct timing information in Sync and Follow_up messages. The announce message is used to establish the synchronization hierarchy. The management messages are used to update the PTP data sets maintained by clocks. The signaling messages are used for communication between clocks for other purposes.

3.7.3 Precise Time Protocol (PTP) Devices

Ordinary Clock – A clock that has a single Precision Time Protocol (PTP) port in a domain and maintains the time scale used in domain. It can be a source of time.

Boundary Clock – A clock that has multiple Precision Time Protocol (PTP) ports in a domain and maintains the time scale used in that domain. It can be a source of time.

End-to-End Transparent Clock – A clock that supports the use of an end-to-end delay mechanism between the slave and master clocks

Peer-to-Peer Transparent Clock – A clock that provides Precision Time Protocol (PTP) event transit information, propagation delay of the link connected to the port receiving the PTP event message

Management Node – A device that configures and monitors clocks

3.7.4 Precision Time Protocol Synchronization

The protocol requires functions that establish the master-slave hierarchy and that synchronize the clocks.

Establishing Master-Slave Hierarchy - Within a domain each ordinary and boundary port executes an independent copy of the protocol state machine. For state decision events each port analyzes the contents of all Announce messages received on the port. Using the best master clock algorithm, the Announce message contents and the contents of the data sets associated with ordinary and boundary clocks are analyzed to determine the state of each port of the clock.

3.7.5 Synchronizing Clocks

In a PTP system, the boundary and ordinary clocks synchronize by exchanging PTP timing messages on the communication path linking the two clocks. At the conclusion of this exchange message the slave possesses all four timestamps which are used to compute the offset of the slave clocks with respect to the master and compute the propagation time between the two clocks.

Chapter 4 - Fault Location Estimation Based on Synchronized Phasor Measurements

This chapter will review the benefits of utilizing synchronized phasor measurements for fault location application as well as a summary of research work and studies conducted on fault location application using synchronized phasor measurements.

4.1 Benefits of Utilizing Synchronized Measurements for Fault Location Estimation

As described earlier, a synchrophasor is a real-time measurement that estimates current and voltage phasor values from the power system. The benefit of using synchronized phasors measurements for protection and control applications is tremendous because it allows system operators understand the behavior of power system in real time, resulting in better corrective actions during power system disturbances. [5] Utilizing synchronized phasors for fault location application also has a similar outcome.

The benefits of utilizing synchronized phasor measurements for fault location are the following:

- Fault location can be performed using data from more than one line terminal
- Fault location calculation can be determined in a matter of milliseconds
- Improves fault location accuracy
- Helps to quickly identify a faulted line in the power system
- Provides a fault location backup tool for protective relays
- Provides pre-fault power flow and its direction from all line terminals
- Reduces restoration time of transmission lines out service due to faults

- Helps crews to repair quickly damaged equipment
- Reduces outage time

4.2 Research work for fault Location Utilizing Synchrophasor Measurements

Most of the research work on fault location utilizing synchronized voltages and currents phasor measurements can be divided into four categories:

- Two-ended fault location
- Fault location on three terminal or multi-terminal lines
- Adaptive Fault location
- Fault location on series-compensated lines

4.2.1 Literature Review on Fault Location Estimation on Two-Terminal Line Utilizing Synchronized Phasor Measurements

The main goal of two-end fault location algorithms is to overcome the limitations of single-end fault location techniques in order to improve fault location accuracy. These two-end fault location algorithms can be considered complete or incomplete. A complete algorithm is characterized as using three phase voltages and currents from both line terminals. An incomplete algorithm is characterized for using three phase voltages from both line terminals with three phase currents from only one line terminal or three phase currents from both line terminals with three phase voltages from only one line terminal or only three phase voltages from both line terminals. The following studies focus on two-end line terminal fault location based on synchronized phasor measurements.

“A Study of Synchronized Sampling Based Fault Location Algorithm Performance under Power Swing and Out-of-Step Conditions” Authors: Nan Zhang and Mladen Kezunovic [7]

One study focuses on the performance of a Synchronized Sampling Fault Location (SSFL) algorithm under power swing and out-of-step condition disturbances. The SSFL algorithm uses raw voltages and currents synchronously taken from two ends of the transmission line. The SSFL was derived by solving the classical differential line equations. The study derives two types of algorithms one for short lines and one for long lines, both using lumped RL and distributed RCL. For short lines less than 50 miles, the algorithm calculates the fault point using the minimum least squares estimate method. For long lines more than 50 miles, the algorithm calculates the fault point using voltage and current profiles along the line based on Bergeron’s equation. The final location is calculated by an indirect method that initiates the calculation by transferring line parameters, and the voltages and currents into a modal domain decoupled system. Then the algorithm partitions the line into equal segments and builds voltage profiles for each point starting from the sending end and the receiving end. Once the voltage profiles have been built, the algorithm approximates the fault point by looking for the point that has the minimum voltage difference calculated using the data from the two ends. Finally, the algorithm builds a short line model surrounding the approximate fault point to refine the location. According to the study, the accuracy of the fault location depends on the synchronization, sampling rate and the line models. It is less affected by the load conditions of the system or fault parameters because there are no assumptions regarding them. To test the method, this study used a WECC 9-bus system simulated in the Alternate Transient Program (ATP). After the power swing condition and Out-of-Step condition are simulated for the test, the measurements obtained from those simulations were fed into the Synchronized Sampling Fault Location (SSFL) algorithm to calculate the fault location. Based in theoretical analysis and ATP simulations, the conclusion of the study was that the accuracy of the SSFL algorithm was affected by the power

swing and out-of-step system conditions with a maximum error of 8 percent. Short lines were less affected during the system disturbances than the long lines. Both short line and long line algorithms perform well for line to ground faults, but they did not perform well for phase to phase faults.

"New Fault Location Scheme for a Two-Terminal Transmission Line Using Synchronized Phasor Measurements" Author: Sukumar M. Brahma [8]

Another approach to determine fault location using synchronized voltage and current phasors from both line terminals first tries to estimate the source impedances from the bus impedance matrix at the time of the fault. In this study, the data was simulated using an EMTP program and then ran through the algorithm. If the bus impedance matrix is not updated to reflect the system condition changes in the source impedances, the results will be incorrect. The method assumes that the lines are transposed. The estimate of the source impedances uses the typical voltage drop equations from the system to the fault location to calculate the source impedance. The fault location is based on the fundamental definition of an element in the bus impedance matrix where the voltage produced at the node and the current injected at the same node produces the Thevinen source impedance. The fault location algorithm modifies the impedance matrix to create a new bus. Then the measured positive sequence fault current is assumed to be injected into the new bus. Finally the algorithm computes the voltages and current at the new bus creating the actual fault point. This algorithm was tested on a 138kV transmission line simulated in EMTP applying all types of faults at different locations in the line.

"A Fault Location Technique for Transmission Lines Using Phasor Measurements" Authors: Abdolhamid Rahideh, Mohsen Gitizadeh, Sirus Mohammadi [9]

This study on two-terminal line fault location presents a fault location technique for two-terminal multi-section compound transmission lines using synchronized phasor measurements embedded in

digital protective relays. Multi-section compound transmission lines are very unique because the line combines sections of overhead lines with underground cables which make the line characteristics unique. To provide fault location this study proposes an innovative fault location approach to distinguish an internal fault on a compounded line from an external fault as well as estimating the fault location for a internal fault. The algorithm uses synchronized voltage and current phasors that are decoupled using the symmetrical component transformation. Then the algorithm uses the calculated values to form impedance and admittance matrices to find the voltages and currents at each terminal of the faulted line. The fault is assumed to occur at point X which in this study is called index D. For a two-section compound line where the left side section is overhead and the right side section is underground cable. At the termination where the overhead line ends and underground cable begins is assumed to be a virtual tap point P. If the fault is assumed to be in the underground power cable section, the algorithm calculates the voltages and currents at the point P and at the end of the underground cable to determine the fault location index D. If the fault is assumed to be in the overhead line section, the algorithm calculates the voltages and current at the beginning of the overhead line section and at the point P to calculate the fault location index D. To determine the faulted section for a two-terminal compounded line, the following guideline is used. If index D2 is less than zero and index D1 is between zero and one, the fault occurred on the underground cable and D1 is the actual location of the fault. If the index D2 is between zero and one and D1 is bigger than one, the fault occurred in the overhead line and (1-D1) is the actual location of the fault. If index D2 is equal to zero and index D1 is equal to one, the fault occurred at the virtual point P. Extensive simulation studies were done using transposed and untransposed double circuit lines to prove that this algorithm is accurate. This proposed algorithm has already been implemented in the Taiwan power system.

4.2.2 Literature Review on Fault Location Estimation on Three Terminal or Multi-Terminal Line Utilizing Synchrophasor Measurements

Multi-terminal lines are the lines with three or more terminals. These types of multi-terminal and tapped lines are used for economical or environmental reasons. Typically, the tapped lines feed only loads supplying passive networks and the remaining terminals are terminated by active networks. Some fault location algorithms for three terminal lines based on synchronized measurements utilize three phase currents from all three terminals and three phase voltages from the terminal where the fault locator is installed. Some fault location algorithms for multi-terminal lines based on synchronized measurements utilize three phase voltages and currents from all the line terminals. The following are papers that are focus on multi-terminal line fault location based on synchrophasor measurements.

"Fault Location Scheme for a Multi-Terminal Transmission Line Using Synchronized Voltage Measurements" Author: Sukumar M. Brahma [10]

One study on multi-terminal fault location proposes a new scheme to locate faults on a multi-terminal transmission line. This algorithm first determines the faulted section and then locates the fault on this section using synchronized voltage measurements. According to this study the main advantage is that the current transformer errors in the current measurements can be avoided. Even though both synchronized voltage and current measurements were available this scheme only used synchronized voltage measurements. The scheme first derives the Thevenin equivalent of the system to find the equivalent impedances at the buses, creating an impedance matrix. Then the algorithm calculates the voltages at tap points from the two terminals. Finally a simple comparison of these voltages at different tap points is used to identify the faulted section. Once the faulted

section is identified, the algorithm starts looking for the precise location of the fault within the faulted section. To locate the fault the algorithm perform a three phase analysis by producing an impedance/admittance matrix where IF is the three phase current and ZF is the three phase fault impedance. This algorithm was tested with a five terminal line simulated in EMTP applying different types of faults with various fault resistances. All of these faults were created at different sections of the five-terminal transmission line. In all cases the algorithm identified the terminal section correctly with a reasonable fault location percentage error.

"A Fault Location Algorithm for Transmission Lines Tapped Leg - PMU Based Approach" Authors: C-S Yu, C-W Liu, Y-H Lin [11]

The second study on multi-terminal fault location algorithms makes the following assumptions: that the fault impedance is pure resistive and the fault type is a prior input. The algorithm considers a three phase transposed line with tapped leg and the system beyond the tapped leg can be a generator, load or combined system. The algorithm starts with calculating admittance and impedance matrices with voltage and current measured from the receiving end of the line. For this algorithm the transmission line is basically divided into two parts, the left and the right part with respect to the tapped leg. So the algorithm first simultaneously calculates two fault locations one on the right side of the tapped line and the other on the left side of the tapped line. This algorithm uses Gauss-Seidel numerical method and a two-port network approach to determine the fault location on each side of the tap. However, the algorithm still has to determine in which side of the tapped leg the fault is on. This algorithm has a fault side selector subroutine. This subroutine looks at a fault location value on each side of the tapped leg and can be divided into five conditions. The first and second condition establishes that the fault location has a fixed fault location value on both sides. The third conditions establish that the fault location has a fixed fault location only on the left

side of the tapped line. The fourth condition establishes that the fault location has a fixed fault location value only on the right side of the tapped line. The fifth condition establishes that the fault location does not have a fixed fault location on either side of the tapped leg. If the algorithm selects conditions three or four that is the correct side of the fault location.

"A Novel Fault Location Algorithm for Multi-Terminal Lines Using Phasor Measurement Units"

Authors: K-P Lien, C-W Liu, C-S Chen, C-S Yu [12]

This study proposes an algorithm that is based on a transmission line model and synchronized positive sequence voltages and currents. This algorithm uses the principles of two-terminal and three-terminal fault location algorithms. It calculates the fault location by identifying which section of the multi-terminal line was faulted. In order to discriminate a non-faulted line section or to locate the faulted section, the algorithm has four special relationships as follows: If all fault location indices are equal to each other and fall into the bus and the first tap of the line the fault has occurred between the bus and the first tap. If one of the indices is a maximum the index is the actual fault location was away from the bus. If some indices are equal or bigger than the remaining indices the fault occurred between the line taps. If all the indices do not converge the fault is declared as an external fault. Once the section of the line has been determined, the algorithm uses positive sequence measurements of each terminal of the line and then applies the two-terminal fault location principle to calculate the fault point voltage and the fault location within the faulted section of the line. This algorithm is independent from fault and system conditions such as fault resistance, pre-fault load flows, shunt capacitances, fault positions and fault types. The fault location method is very simple and its computational cost is low.

4.2.3 Literature Review on Adaptive Fault Location Estimation Utilizing Synchrophasor Measurements

The uncertainty of the line parameters could substantially affect the accuracy of the fault location. The main goal of adaptive fault location is to achieve a better fault location accuracy by calculating a proper estimate of line parameters and system impedance. Typically environmental conditions and operating conditions of the transmission lines affect its sag. As the conductor current increases, its temperature increases, and consequently, its sag increases. The line resistance changes with the line temperature and also the line reactance changes since it depends on distance between the phase conductors which is affected by the line sag. The line parameters can be calculated using pre-fault angle and magnitude measurements for voltage and current. Adaptive fault location algorithms utilize three phase voltages and currents from both ends of the line. The following papers are focus on adaptive fault location based on synchrophasor measurements.

"An Adaptive PMU Based Fault Detection/Location Technique for Transmission Lines" Authors: J-A Jiang, J-Z Yang, Y-H Lin, C-W Liu, J-C Ma [13]

This study focuses on an algorithm that calculates a fault detection/location index in terms of Clarke components using synchronized voltages and currents. It also estimates the line parameters which help to solve some uncertainty of parameters caused by the aging of the transmission line. In order to eliminate system noise and measurement errors the method uses a Discrete Fourier Transform (DFT) to extract the fundamental frequency with high accuracy. This algorithm uses the Clarke transformation to calculate the faulted voltages and currents and then calculates the fault location index D. Index D is hardly effected by the variations of source impedance, loading change, fault impedance, and fault angle inception, and fault type. Each fault produces a zero, alpha, and

beta modal waves. For line to ground faults there is no Beta modal wave and only zero and alpha modal waves. For three phase faults, zero, alpha and beta modal waves are present. So this algorithm will provide more accurate fault location when all three Clarke transformation modal waves are present. After the location is calculated, the values are run through the Discrete Fourier filter to achieve a high degree of accuracy.

"An Adaptive Fault Locator for Transmission Lines Tapped with a Source of Generation" Authors: Y-H Lin, C-W Liu, J-A Jiang, J-Z Yang [14]

This study proposes a fault location algorithm utilizing synchronized phasor measurements which calculates a faulted section discrimination index taking into account the effects caused by the tapped line. This algorithm has an adaptive scheme that estimates the source impedance. This algorithm is divided into two parts. The first part will focus on identifying the faulted section. The second part will focus on calculating the fault location. The algorithm starts the fault location calculation by extracting the positive sequence from the three phase voltages and currents. Then the algorithm calculates the source impedance using the positive sequence components. After calculating the source impedance, the algorithm determines the faulted section by calculating a discrimination index using the real part of a complex number. The indices are Dcal and Dpre. If Dcal bigger than Dpre, the faulted section is on the left of the tap location. If Dcal smaller than Dpre, the faulted section is on the right of the tapped line. If Dcal is equal than Dpre, the faulted section is at tap point. Once the algorithm knows which section of the line is faulted, it uses the second algorithm on the right or left fault location section.

4.2.4 Literature Review on Fault Location Estimation on Series-Compensated Lines Utilizing Synchrophasor Measurements

Fault location algorithms for series-compensated line based on synchrophasor measurements do not need the series compensation device model or the protection function of series device to predict the voltage drop. Instead, two iterative steps are performing: a prelocation step and a correction step are used to calculate the voltage drop and fault location. The following papers focus on fault location on series-compensated lines based on synchrophasor measurements.

"A New Fault Location Algorithm for Series Compensated Lines Using Synchronized Phasor Measurements" Authors: C-S Yu, C-W Liu, J-A Jiang [15]

In order to do fault location in transmission lines with series capacitors, a series compensation model is traditionally needed to be able to calculate its voltage drop across the device. However doing so, it may introduce some errors due to inaccuracy of the model or from the uncertainty from the protection function for the series device. This study introduces a new way to do fault location. The method uses an algorithm that does not need the series model device in order to calculate the voltage drop. Instead, in order to calculate the voltage drop and calculate the fault location, the algorithm uses two iterative steps, a pre-location step and a correction step. When the fault occurs, the algorithm will use time synchronized three phase voltages and three phase currents from both ends of the line as inputs in the pre-location step to calculate the faulted voltage and the fault current and then calculate the per unit fault location called D. If the D value converges, the fault location will be displayed. If the D value does not converge, the algorithm uses the correction step to calculate the unknown voltage drop, called Vser, of the series device. Using two-port network theory the algorithm will calculate the unknown voltage drop of the series device and re-use this to

re-calculate the D value. This process will be repeated until the algorithm calculates the fault location accurately.

“Accurate Fault Location Algorithm for Transmission Lines in the Presence of Series-Connected Flexible AC Transmission System Devices” Authors: J. Sadeh, A. Adinehzadeh [15]

Synchronized data is used from both ends of the transmission line and applied to a distributed parameter line model in time domain to find the location of the fault. The algorithm has three parts. The first part assumes that the fault is on the left side of the compensator. The second part assumes that the fault is on the right side of the compensator. The third part provides the fault location. This method uses two-end three phase voltages and one-end three phase current. When the fault occurs the algorithm will calculate the fault point in terms of the source voltages and currents with respect to time. It will first assume the fault occurred on either the left or right side of the compensation. Finally the algorithm will determine the fault location using an enumeration method as an optimization tool.

Chapter 5 – Fault Location Testing Utilizing Synchronized Phasor Measurements

In order to analyze the performance of an impedance based fault location algorithm utilizing synchronized phasor measurements, it is necessary to have phasor measurements units (PMU) and phasor data concentrators (PDC) as test equipment. Thus, the testing of this thesis investigation will be conducted at a synchrophasor Proof of Concept (POC) Lab.

5.1 Proof of Concept (POC) Lab

In general, the laboratory has production grade equipment with a network architecture that mimics what the utility has installed in real substations across its service territory.

5.1.1 500 kV System modeled in RTDS at the Proof of Concept (POC) Lab

In order to simulate faults or other power system disturbances, the POC lab has a 500 kV system modeled in RTDS with actual generation and real impedances of the system. In RTDS, some of the modeled 500 kV lines have fault initiation tools for different fault types, fault percentage location options, fault impedance options, and fault incident angle options.

For the purpose of this thesis investigation, a RTDS simulation model with four 500 kV lines will be used to simulate fault events and then retrieve the PMU data collected from those fault events. In the north part of the system, two 500 kV lines were selected MA-RM #1 and RM-TM #2. In the central part of the system, one 500 kV line was selected, the LB-GA #1 line. In the south part of the system, one line was selected, the MID-VIN #1 line. The lines were selected with the intention to see how the whole 500 kV system behaves when there is an electrical disturbance in the north part of the system or in the south part of the system.

5.1.2 500 kV System Characteristics

In the U.S Western Electric Coordinating Council (WECC) region, the 500 kV system is the backbone of the electrical grid. The 500 kV system covers California, Oregon, Washington, Nevada, Idaho and Montana and its main function is to bring energy from generation centers in Washington and Oregon area to the load centers in California. In California, the 500 kV system begins in the north at the California-Oregon border which is best known as COB and in the south near the Los Angeles area at a location best known as path 26.

The characteristics of the 500 kV system are: the system is a non-homogeneous system meaning source angle impedance is not always the same as the line impedance angle. Ninety percent of the lines are homogeneous lines, meaning the same impedance per length is distributed through the whole line length. Examples of these lines are lines that have the same conductor and tower construction throughout. All the lines are series capacitor compensated and breakers can be operated in three pole mode or single pole mode. The 500 kV substations have breaker and a half (BAAH) schemes for switching flexibility and the 500 kV system also include one nuclear power plant with two generation units of 1 gigawatt each.

5.1.3 PMU Network System Topology at the Proof of Concept (POC) Lab

The POC Lab equipment can be divided into five types of components: GPS clocks, Phasor Measurement Units (PMUs), local area network (LAN), Phasor Data Concentrators (PDCs), and Super Phasor Data Concentrators (SuperDPCs).

POC Clocks – The lab has two GPS clocks. A Symmentricom clock is the primary GPS clock source. Symmentricom uses IEEE 1588 Precise Time Protocol (PTP) standard to provide a clock time signal to the equipment which gets distributed through the network. An Arbirter Systems clock is the

secondary GPS clock source. Arbiter Systems uses IRIB-B standard to provide the clock time signal to the equipment and the signal gets distributed via coaxial cable.

POC Phasor Measurement Unit (PMU) – The lab has SEL, ABB, and GE Phasor Measurement Units (PMUs) providing synchronized phasor data in the IEEE C37.118.1 standard at a rate of 120 frames per second. The lab phasor measurement units have the capability to produce either M-Class synchronized phasor data for metering applications or P-Class synchronized phasor data for protection applications.

POC Network Architecture – The network transports the lab synchronized phasor data from the PMUs to GE P30 PDCs and Dell servers used as super SuperPDCs. The synchronized phasor data produced in the lab is exchanged by a private Local-Area Network (LAN) using the IEC 61850-90-5 standard protocol for Power Utility Automation. In the lab, the IEEE C37.118.2 compliant devices like the phasor measurement units (PMUs) or phasor data concentrators (PDCs) are mapped to the IEC 61850-90-5. IEC 61850-90-5 exchanges data starting with a physical device such as a PMU. Each physical device has one or more logical devices like a PMU function. Within a logical device there are one or more logical nodes acting using analog values. Each logical node contains one or more Common Data Class elements like A phase voltage. Common Data Class elements contain one or more data attributes like A phase voltage magnitude and A phase voltage angle. The IEC 61850-90-5 communication uses TCP/IP.

Phasor Data Concentrator (PDC) – The PDCs installed in the lab are GE P30 units. They are IEEE C37.118 compliant devices and have the capability to exchange synchronized phasor data with other GE P30 Phasor Data Concentrators, and with SEL, ABB, and GE phasor measurement units or with the Dell servers used as SuperPDCs.

Data Storage – The data storage system in the lab is in the form of historians. These historians are integrated in the GE P30 Phasor Data Concentrators and Dell servers used as SuperPDCs.

5.1.4 Panel Arrangement at the Proof of Concept (POC) Lab

The synchrophasor lab has approximately 10 panels divided into three types: collection point panels, data storage panels and data exchange panels.

Collection Point Panel – This panel has installed GE, ABB, and SEL Phasor Measurement Units and the Omicron amplifier sets. The function of this panel is to produce all the synchronized phasor data.

Data Storage Panel - This panel has the GE Phasor Data Concentrator units. The function of this panel is to collect and store all synchronized phasor data produced by the Phasor Measurement Units installed in the collection point panels.

Exchange Data Panel – This panel has the Dell Super Phasor Data Concentrators. The function of this panel is to exchange synchronized phasor data to external use points or with the lab Phasor Data Concentrators.

5.1.5 Synchrophasor Visualization at the Proof of Concept (POC) Lab

The POC lab has various TV monitors for monitoring the following:

- Real-time synchronized phasor data such as frequency, watts, vars, voltage, and current from the 500 kV system modeled in RTDS
- Visualizing the 500 kV system topology modeled in RTDS
- 500 kV system power flow

5.1.6 Synchrophasor Application Point at the Proof of Concept (POC) Lab

The POC lab has various computers to run applications to analyze synchronized phasor data. The following computer software applications are installed in the lab computers to analyze phasor data:

- UR Enervista (GE)
- P30 (GE)
- ACselerator (SEL)
- PCM600 (ABB)

5.2 Synchronized Phasor Data Generation Process at the Proof of Concept (POC) Lab

A specific transmission line from the 500 kV system modeled in RTDS is selected to apply a fault. After the transmission line is faulted, the voltage and current fault simulation is processed by the RTDS software and hardware. As the RTDS processes the data, it generates analog low level control signals (millivolts and milliamps) containing information of voltages and currents measured on the faulted line. Then these analog low level control signals are sent from RTDS to Omicron amplifiers. The Omicron amplifier amplifies the low level signals from milliamps and millivolts to amps and volts, which are injected in the phasor measurement units as PT and CT secondary values. Finally, the phasor measurement unit (PMU) will convert the analog data received from Omicron amplifiers into digital data using sampling processes. Once the analog data is digitized and converted into synchronized phasor data, it is sent to the PDCs and SuperPDCs for processing, storage or data exchange.

5.3 Type of Synchronized Phasor Data Collected for the Thesis Investigation

All synchronized phasor data used for this thesis was retrieved from different GE P30 Phasor Data Concentrators. The synchronized phasor data collected is P-Class and was downloaded at 120 frames per second using a comma separated variable (*.csv) file format.

5.4 Fault Location Algorithm

The algorithm created for this thesis investigation is a two-terminal fault location algorithm that reads three phase voltages and three phase currents from each line terminal of four of the lines in the system. Once the algorithm performs the fault location, it will provide the following information:

- Name of the line faulted
- Type of fault
- Fault location in percentage of length
- Fault location in miles from one terminal

The user is required to enter the following settings in the algorithm:

- Nominal voltage of the system
- MVA base value
- Positive sequence impedance of each line in the system
- Zero sequence impedance of each line in the system
- Name of each line in the system

The algorithm is divided into two parts. Part 1 focuses on determining which line was faulted from all the lines in the 500 kV system and part 2 focuses in determining the fault location on the faulted line.

5.4.1 Algorithm part 1

Step 1 – The algorithm reads three phase voltage and current synchronized phasor data from both ends of each line in the system.

Step 2 – The algorithm calculates positive, negative, and zero sequence symmetrical components from the three phase voltage and current synchronized phasor data of each measurement location

Step 3 – The algorithm determines the faulted line using the negative sequence current, phase voltage and directionality of the current from the data from each line in the system

Step 4 – Once the faulted line has been determined, the algorithm selects the positive sequence, negative sequence, and zero sequence voltages and currents from the local and remote terminals of the faulted line

Step 5 – The algorithm selects the positive and zero sequence data for the faulted line, which will be used for the fault location calculation

5.4.2 Algorithm part 2

Step 1 - Using the local and remote synchronized phasor data of the faulted line, the algorithm determine the type of fault using a fault type identification algorithm

Step 2 – Calculates the fault location in percentage of length and in miles from the local line terminal

Step 3 – The algorithm provides the results

Note: See appendix A for more algorithm details

5.5 Test Program

5.5.1 Lines under Test

Line 1 – 500 kV MLN - RM #1 (L=94.46 miles)

Line 2 – 500 kV RM – TM #2 (L=89.46)

Line 3 – 500 kV GAT – LB # 2 (L=80.85 miles)

Line 4 – 500 kV MWY-VCN # 1 (L=112.6 miles)

5.5.2 PDC Synchrophasor Data (All P-Class PMU data)

PDC-01

- MLN-RM # 1 Line (PDC-01 provides data from both the MNL and RM ends of the line)
- RM-TM # 2 Line (PDC-01 provides only data from the RM line end)

PDC-11

- RM-TM # 2 Line (PDC-11 provides only data from the TM line end)

PDC-21

- GAT – LB # 2 Line (PDC-21 provides data from both the GAT and LB ends of the line)

PDC-51

- MWY-VCN # 1 Line (PDC-51 provides data from both the MWY and VCN ends of the line)

5.5.3 Test Cases

Case 1 - Power System Conditions: Normal system and bolted faults applied in the following lines

a. Line 2 – 50% CG

b. Line 3 – 20% ABC

c. Line 4 – 50% BC

Case 2 - Power System Conditions: Parallel line(s) in the same corridor out of service to create line overload condition and faults applied on the following overloaded lines

a. Line 1 – 40% BCG

b. Line 2 – 25% CG

c. Line 4 – 50% ABC

Case 3 - Power System Conditions: Normal system and high impedance faults applied in the following conditions:

a. Line 1 – 60% CG with 10 ohms fault impedance

b. Line 1 – 20% AB with 20 ohms fault impedance

c. Line 1 – 40% ABC with 30 ohms fault impedance

Case 4 - Power system conditions: Normal system and faults applied with maximum DC offset on the following lines

a. Line 1 – 30% AG with maximum DC offset

b. Line 2 – 20% BC with maximum DC offset

c. Line 3 – 40% ABC with maximum DC offset

Case 5 - Power system conditions: Normal system and high impedance faults applied with maximum DC offset in the following conditions:

a. Line 1 – 60% CG with 2 ohms resistance and maximum DC offset

b. Line 1 – 40% AB with 6 ohms resistance and maximum DC offset

c. Line 1 – 50% ABC with 10 ohms resistance and maximum DC offset

Case 6 – With normal power system conditions apply faults with series capacitor compensation of 75% inserted on the following lines

a. Line 1 – 30% CG with series capacitors inserted in the line

b. Line 2 – 40% AB with series capacitors inserted in the line

c. Line 3 – 60% ABC with series capacitors inserted in the line

Case 7 – Taking generation out of service to create weak source on one end of the following lines and then apply the faults

a. Line 1 – 40% CG with one end weak source

b. Line 2 – 50% AC with one end weak source

c. Line 3 – 70% ABC with one end weak source

Case 8 – Lines out of service to create overload conditions on the following lines and the following high impedance faults applied:

a. Line 1 – 40% CG with 5 ohm resistance and overload condition

b. Line 1 – 50% AC with 10 ohm resistance and overload condition

c. Line 1 – 70% ABC with 15 ohm resistance and overload condition

Case 9 – Generation or lines out of service create a weak source and apply faults with maximum DC offset on the following lines:

a. Line 1 – 40% CG with maximum DC offset and weak source on one end

b. Line 2 – 10% AC with maximum DC offset and weak source on one end

c. Line 3 – 50% ABC with maximum DC offset and weak source on one end

Case 10 – With normal power system insert series capacitors with 75% compensation on the following lines and apply high impedance faults:

a. Line 1 – 40% CG with 3 ohm resistance and series capacitor inserted on the line

b. Line 2 – 50% AC with 6 ohm resistance and series capacitor inserted on the line

c. Line 3 – 70% ABC with 9 ohm resistance and series capacitor inserted on the line

5.6 Test Results

Each case was tested under the various system operations and fault conditions described above. For this investigation, four homogeneous overhead 500 kV transmission lines were used to simulate faults. The propose fault location algorithm uses two-ended positive and negative sequence impedance based method equations.

The performance index given in terms of the error percentage is defined as follows:

$$\text{Error} := \frac{\left|\text{actual\_location} - \text{estimated\_location}\right|}{\text{total\_line\_length}} \cdot 100\% \quad (5.1)$$

For test results, synchrophasor data was gathered in frames. A frame represents one measurement with timestamps on three phase voltages and currents. The fault location was calculated using one frame at a time produced during the same fault. The following tables summarize the fault location performance results for each fault.

Table 5.1: CASE 1a results for CG fault at 50% (44.7 miles) of the line under normal system conditions

	PMU Frame 28	PMU Frame 29	PMU Frame 30	PMU Frame 31	PMU Frame 32
Negative Sequence Algorithm Calculated Fault Location (miles)	Unable to Calculate	47.2	47.2	47.2	47.2
Negative Sequence Algorithm Fault Location Error (percent)	N/A	0	0	0	0
Positive Sequence Algorithm Calculated Fault Location (miles)	Unable to Calculate	57.7	49.29	50.1	49.1
Positive Sequence Algorithm Fault Location Error (percent)	N/A	11.1	2.2	3.0	2.3
Proposed Fault Location Algorithm Selected Correct Faulted Line (Yes/No)	No	Yes	Yes	Yes	Yes
Proposed Fault Location Algorithm Selected Correct Fault Type (Yes/No)	No	Yes	Yes	Yes	Yes

Table 5.1 comments: Proposed algorithm could not determine fault location with the synchrophasor data measured in frame 28. Fault started evolving when frame 28 was measured.

Table 5.2: CASE 1b results for ABC fault at 20% (16.17 miles) of the line under normal system conditions

	PMU Frame 28	PMU Frame 29	PMU Frame 30	PMU Frame 31	PMU Frame 32
Negative Sequence Algorithm Calculated Fault Location (miles)	N/A	N/A	N/A	N/A	N/A
Negative Sequence Algorithm Fault Location Error (percent)	N/A	N/A	N/A	N/A	N/A
Positive Sequence Algorithm Calculated Fault Location (miles)	19.8	19.8	17.02	19.9	19.9
Positive Sequence Algorithm Fault Location Error (percent)	4.5	4.5	1.2	4.7	4.7
Proposed Fault Location Algorithm Selected Correct Faulted Line (Yes/No)	Yes	Yes	Yes	Yes	Yes
Proposed Fault Location Algorithm Selected Correct Fault Type (Yes/No)	Yes	Yes	Yes	Yes	Yes

Table 5.2 comments: For three phase fault, negative sequence algorithm was not used because the fault does not produce significant negative sequence component quantities.

Table 5.3: CASE 1c results for BC fault at 50% (56 miles) of the line under normal system conditions

	PMU Frame 28	PMU Frame 29	PMU Frame 30	PMU Frame 31	PMU Frame 32
Negative Sequence Algorithm Calculated Fault Location (miles)	47.1	47.1	56.3	47.2	47.2
Negative Sequence Algorithm Fault Location Error (percent)	5.5	5.5	2.6	5.4	5.4
Positive Sequence Algorithm Calculated Fault Location (miles)	65.1	88.1	68.1	57.1	57.1
Positive Sequence Algorithm Fault Location Error (percent)	12.7	31	13.1	3.3	3.3
Proposed Fault Location Algorithm Selected Correct Faulted Line (Yes/No)	Yes	Yes	Yes	Yes	Yes
Proposed Fault Location Algorithm Selected Correct Fault Type (Yes/No)	No	No	Yes	No	No

Table 5.3 comments: Proposed algorithm was able perform fault location and determine faulted line from all frames.

Table 5.4: CASE 2a results for BCG fault at 40% (37.7 miles) of the line under line overload condition

	PMU Frame 28	PMU Frame 29	PMU Frame 30	PMU Frame 31	PMU Frame 32
Negative Sequence Algorithm Calculated Fault Location (miles)	31.02	31.02	31.02	32	34.3
Negative Sequence Algorithm Fault Location Error (percent)	7.1	7.1	7.1	6.1	3.6
Positive Sequence Algorithm Calculated Fault Location (miles)	30.6	30.6	30.6	29.1	24
Positive Sequence Algorithm Fault Location Error (percent)	7.5	7.5	7.5	9.1	14.5
Proposed Fault Location Algorithm Selected Correct Faulted Line (Yes/No)	Yes	Yes	Yes	Yes	Yes
Proposed Fault Location Algorithm Selected Correct Fault Type (Yes/No)	Yes	Yes	Yes	Yes	Yes

Table 5.4 comments: Proposed algorithm was able to perform fault location, determine the faulted line and the fault type with synchrophasor data from each frame

Table 5.5: CASE 2b results for CG fault at 25% (22.3 miles) of the line under line overload condition

	PMU Frame 28	PMU Frame 29	PMU Frame 30	PMU Frame 31	PMU Frame 32
Negative Sequence Algorithm Calculated Fault Location (miles)	18.9	19.8	18.2	21.5	19.3
Negative Sequence Algorithm Fault Location Error (percent)	0	2.6	4.47	0.7	3.2
Positive Sequence Algorithm Calculated Fault Location (miles)	88.7	29.2	20.2	19.3	21.4
Positive Sequence Algorithm Fault Location Error (percent)	78	7.8	2.3	3.2	0.8
Proposed Fault Location Algorithm Selected Correct Faulted Line (Yes/No)	Yes	Yes	Yes	Yes	Yes
Proposed Fault Location Algorithm Selected Correct Fault Type (Yes/No)	Yes	Yes	Yes	Yes	Yes

Table 5.5 comments: Proposed algorithm was able to perform fault location, determine the faulted line and the fault type with synchrophasor data from each frame

Table 5.6: CASE 2c results for ABC fault at 50% (56.3 miles) of the line under line overload condition

	PMU Frame 28	PMU Frame 29	PMU Frame 30	PMU Frame 31	PMU Frame 32
Negative Sequence Algorithm Calculated Fault Location (miles)	N/A	N/A	N/A	N/A	N/A
Negative Sequence Algorithm Fault Location Error (percent)	N/A	N/A	N/A	N/A	N/A
Positive Sequence Algorithm Calculated Fault Location (miles)	Unable to Calculate	90.7	72.3	60.7	60.8
Positive Sequence Algorithm Fault Location Error (percent)	N/A	30.5	14.2	3.9	3.9
Proposed Fault Location Algorithm Selected Correct Faulted Line (Yes/No)	No	Yes	Yes	Yes	Yes
Proposed Fault Location Algorithm Selected Correct Fault Type (Yes/No)	No	No	Yes	Yes	Yes

Table 5.6 comments: Proposed algorithm could not determine fault location with the synchrophasor data measured in frame 28. Fault started evolving when frame 28 was measured. For three phase fault, negative sequence algorithm was not used because the fault does not produce significant negative sequence component quantities.

Table 5.7: CASE 3a results for CG fault at 60% (56.6 miles) of the line with 10 Ohm fault resistance

	PMU Frame 28	PMU Frame 29	PMU Frame 30	PMU Frame 31	PMU Frame 32
Negative Sequence Algorithm Calculated Fault Location (miles)	31.1	39.09	31.1	31	31.1
Negative Sequence Algorithm Fault Location Error (percent)	26.1	26	27	27	27
Positive Sequence Algorithm Calculated Fault Location (miles)	32.5	32.9	32.6	32.8	32.7
Positive Sequence Algorithm Fault Location Error (percent)	24.9	25	25.3	25.4	25.3
Proposed Fault Location Algorithm Selected Correct Faulted Line (Yes/No)	Yes	Yes	Yes	Yes	Yes
Proposed Fault Location Algorithm Selected Correct Fault Type (Yes/No)	Yes	Yes	Yes	Yes	Yes

Table 5.7 comments: Proposed algorithm was able to perform fault location, determine the faulted line and the fault type with synchrophasor data from each frame

Table 5.8: CASE 3b results for AB fault at 20% (18.8 miles) of the line with 20 Ohm fault resistance

	PMU Frame 28	PMU Frame 29	PMU Frame 30	PMU Frame 31	PMU Frame 32
Negative Sequence Algorithm Calculated Fault Location (miles)	31.2	31.3	31.1	31.1	31.1
Negative Sequence Algorithm Fault Location Error (percent)	13.15	13.19	13.7	13.7	13.7
Positive Sequence Algorithm Calculated Fault Location (miles)	51.8	33.2	32.3	32.3	32.3
Positive Sequence Algorithm Fault Location Error (percent)	34.8	15.2	15	15	15
Proposed Fault Location Algorithm Selected Correct Faulted Line (Yes/No)	Yes	Yes	Yes	Yes	Yes
Proposed Fault Location Algorithm Selected Correct Fault Type (Yes/No)	No	No	Yes	No	No

Table 5.8 comments: Proposed algorithm was able perform fault location and determine faulted line from all frames.

Table 5.9: CASE 3c results for ABC fault at 40% (37.7miles) of the line with 30 Ohm fault resistance

	PMU Frame 28	PMU Frame 29	PMU Frame 30	PMU Frame 31	PMU Frame 32
Negative Sequence Algorithm Calculated Fault Location (miles)	N/A	N/A	N/A	N/A	N/A
Negative Sequence Algorithm Fault Location Error (percent)	N/A	N/A	N/A	N/A	N/A
Positive Sequence Algorithm Calculated Fault Location (miles)	78.1	38.1	34.4	33.5	33.2
Positive Sequence Algorithm Fault Location Error (percent)	42.7	0.4	3.4	4.4	4.2
Proposed Fault Location Algorithm Selected Correct Faulted Line (Yes/No)	Yes	Yes	Yes	Yes	Yes
Proposed Fault Location Algorithm Selected Correct Fault Type (Yes/No)	No	Yes	Yes	Yes	Yes

Table 5.9 comments: For three phase fault, negative sequence algorithm was not used because the fault does not produce significant negative sequence component quantities. Proposed algorithm was not able to determine the fault type from frame 28.

Table 5.10: CASE 4a results for AG fault at 30% (28.3 miles) of the line with maximum DC offset

	PMU Frame 28	PMU Frame 29	PMU Frame 30	PMU Frame 31	PMU Frame 32
Negative Sequence Algorithm Calculated Fault Location (miles)	31.17	31.74	31.18	31.18	30.3
Negative Sequence Algorithm Fault Location Error (percent)	3.02	3.6	3.02	3.02	2
Positive Sequence Algorithm Calculated Fault Location (miles)	32.7	32.7	32.7	32.7	32.3
Positive Sequence Algorithm Fault Location Error (percent)	4.6	4.6	4.6	4.6	4.2
Proposed Fault Location Algorithm Selected Correct Faulted Line (Yes/No)	Yes	Yes	Yes	Yes	Yes
Proposed Fault Location Algorithm Selected Correct Fault Type (Yes/No)	Yes	Yes	Yes	Yes	Yes

Table 5.10 comments: Proposed algorithm was able to perform fault location, determine the faulted line and the fault type with synchrophasor data from each frame

Table 5.11: CASE 4b results for BC fault at 20% (17.8 miles) of the line with maximum DC offset

	PMU Frame 28	PMU Frame 29	PMU Frame 30	PMU Frame 31	PMU Frame 32
Negative Sequence Algorithm Calculated Fault Location (miles)	20.5	20.24	18.9	20.1	20.3
Negative Sequence Algorithm Fault Location Error (percent)	2.8	2.7	1.22	2.5	2.7
Positive Sequence Algorithm Calculated Fault Location (miles)	19.4	19.4	18.1	30.6	92.7
Positive Sequence Algorithm Fault Location Error (percent)	1.7	1.7	0.32	14.3	84
Proposed Fault Location Algorithm Selected Correct Faulted Line (Yes/No)	Yes	Yes	Yes	Yes	Yes
Proposed Fault Location Algorithm Selected Correct Fault Type (Yes/No)	Yes	Yes	Yes	Yes	Yes

Table 5.11 comments: Proposed algorithm was able to perform fault location, determine the faulted line and the fault type with synchrophasor data from each frame

Table 5.12: CASE 4c results for ABC fault at 40% (32.34 miles) of the line with maximum DC offset

	PMU Frame 28	PMU Frame 29	PMU Frame 30	PMU Frame 31	PMU Frame 32
Negative Sequence Algorithm Calculated Fault Location (miles)	N/A	N/A	N/A	N/A	N/A
Negative Sequence Algorithm Fault Location Error (percent)	N/A	N/A	N/A	N/A	N/A
Positive Sequence Algorithm Calculated Fault Location (miles)	22.6	21.3	17.1	20	20
Positive Sequence Algorithm Fault Location Error (percent)	12	13.6	18.8	15.2	15.2
Proposed Fault Location Algorithm Selected Correct Faulted Line (Yes/No)	Yes	Yes	Yes	Yes	Yes
Proposed Fault Location Algorithm Selected Correct Fault Type (Yes/No)	Yes	Yes	Yes	Yes	Yes

Table 5.12 comments: For three phase fault, negative sequence algorithm was not used because the fault does not produce significant negative sequence component quantities.

Table 5.13: CASE 5a results for CG fault at 60% (56.6 miles) of the line with 2 Ohms and maximum DC offset

	PMU Frame 28	PMU Frame 29	PMU Frame 30	PMU Frame 31	PMU Frame 32
Negative Sequence Algorithm Calculated Fault Location (miles)	Unable to Calculate	47.2	47.2	47.3	47.3
Negative Sequence Algorithm Fault Location Error (percent)	N/A	10	10	9.9	9.9
Positive Sequence Algorithm Calculated Fault Location (miles)	Unable to Calculate	59.9	49.9	50.3	49.6
Positive Sequence Algorithm Fault Location Error (percent)	N/A	3.4	7.5	3.5	7.4
Proposed Fault Location Algorithm Selected Correct Faulted Line (Yes/No)	No	Yes	Yes	Yes	Yes
Proposed Fault Location Algorithm Selected Correct Fault Type (Yes/No)	No	Yes	Yes	Yes	Yes

Table 5.13 comments: Proposed algorithm could not determine fault location with the synchrophasor data measured in frame 28. Fault started evolving when frame 28 was measured.

Table 5.14: CASE 5b results for AB fault at 40% (37.7 miles) of the line with 6 Ohms and maximum DC offset

	PMU Frame 28	PMU Frame 29	PMU Frame 30	PMU Frame 31	PMU Frame 32
Negative Sequence Algorithm Calculated Fault Location (miles)	Unable to Calculate	42.7	42.7	42.7	42.7
Negative Sequence Algorithm Fault Location Error (percent)	N/A	9.9	9.9	9.9	9.9
Positive Sequence Algorithm Calculated Fault Location (miles)	Unable to Calculate	77.5	49.5	49.2	49.3
Positive Sequence Algorithm Fault Location Error (percent)	N/A	42	12.4	12.1	12.2
Proposed Fault Location Algorithm Selected Correct Faulted Line (Yes/No)	No	Yes	Yes	Yes	Yes
Proposed Fault Location Algorithm Selected Correct Fault Type (Yes/No)	No	No	Yes	No	No

Table 5.14 comments: Proposed algorithm could not determine fault location with the synchrophasor data measured in frame 28. Fault started evolving when frame 28 was measured. Proposed algorithm was able perform fault location and determine faulted line from all frames, only synchrophasor data from frame 30 was useful to determine the fault type.

Table 5.15: CASE 5c results for ABC fault at 50% (47.2 miles) of the line with 10 Ohms and maximum DC offset

	PMU Frame 28	PMU Frame 29	PMU Frame 30	PMU Frame 31	PMU Frame 32
Negative Sequence Algorithm Calculated Fault Location (miles)	N/A	N/A	N/A	N/A	N/A
Negative Sequence Algorithm Fault Location Error (percent)	N/A	N/A	N/A	N/A	N/A
Positive Sequence Algorithm Calculated Fault Location (miles)	79.15	51.9	50.4	49.8	50.4
Positive Sequence Algorithm Fault Location Error (percent)	33.8	4.9	3.3	2.7	3.3
Proposed Fault Location Algorithm Selected Correct Faulted Line (Yes/No)	Yes	Yes	Yes	Yes	Yes
Proposed Fault Location Algorithm Selected Correct Fault Type (Yes/No)	No	Yes	Yes	Yes	Yes

Table 5.15 comments: For three phase fault, negative sequence algorithm was not used because the fault does not produce significant negative sequence component quantities.

Table 5.16: CASE 6a results for CG fault at 30% (28.3 miles) of the line with 75% series capacitor compensation inserted

	PMU Frame 28	PMU Frame 29	PMU Frame 30	PMU Frame 31	PMU Frame 32
Negative Sequence Algorithm Calculated Fault Location (miles)	Unable to Calculate	48.2	18.4	46.6	Unable to Calculate
Negative Sequence Algorithm Fault Location Error (percent)	N/A	21	21.2	19.3	N/A
Positive Sequence Algorithm Calculated Fault Location (miles)	Unable to Calculate	Unable to Calculate	15.5	48	Unable to Calculate
Positive Sequence Algorithm Fault Location Error (percent)	N/A	N/A	24.8	20.8	N/A
Proposed Fault Location Algorithm Selected Correct Faulted Line (Yes/No)	No	Yes	Yes	Yes	No
Proposed Fault Location Algorithm Selected Correct Fault Type (Yes/No)	No	Yes	Yes	Yes	No

Table 5.16 comments: Proposed algorithm could not determine fault location with the synchrophasor data measured in frame 28 and 32. MOV non-linearities in SLG fault caused errors in fault location.

Table 5.17: CASE 6b results for AB fault at 40% (35.7miles) of the line with 75% series capacitor compensation inserted

	PMU Frame 28	PMU Frame 29	PMU Frame 30	PMU Frame 31	PMU Frame 32
Negative Sequence Algorithm Calculated Fault Location (miles)	16.4	18.79	18.4	20.9	19.5
Negative Sequence Algorithm Fault Location Error (percent)	21.5	18.89	21.2	16.5	18
Positive Sequence Algorithm Calculated Fault Location (miles)	31	16.79	15.5	16.9	17
Positive Sequence Algorithm Fault Location Error (percent)	5.1	17.8	24.8	21	20
Proposed Fault Location Algorithm Selected Correct Faulted Line (Yes/No)	Yes	Yes	Yes	Yes	Yes
Proposed Fault Location Algorithm Selected Correct Fault Type (Yes/No)	No	Yes	Yes	Yes	Yes

Table 5.17 comments: Proposed algorithm was able to perform fault location, determine the faulted line and the fault type with synchrophasor data from each frame

Table 5.18: CASE 6c results for ABC fault at 60% (48.5miles) of the line with 75% series capacitor compensation inserted

	PMU Frame 28	PMU Frame 29	PMU Frame 30	PMU Frame 31	PMU Frame 32
Negative Sequence Algorithm Calculated Fault Location (miles)	N/A	N/A	N/A	N/A	N/A
Negative Sequence Algorithm Fault Location Error (percent)	N/A	N/A	N/A	N/A	N/A
Positive Sequence Algorithm Calculated Fault Location (miles)	74.8	77.5	16.9	19.7	19.7
Positive Sequence Algorithm Fault Location Error (percent)	32.5	35.8	39	35.5	35.5
Proposed Fault Location Algorithm Selected Correct Faulted Line (Yes/No)	Yes	Yes	Yes	Yes	Yes
Proposed Fault Location Algorithm Selected Correct Fault Type (Yes/No)	Yes	Yes	Yes	Yes	Yes

Table 5.18 comments: For three phase fault, negative sequence algorithm was not used because the fault does not produce significant negative sequence component quantities.

Table 5.19: CASE 7a results for CG fault at 40% (37.7miles) of the line with weak source on one end of the line

	PMU Frame 28	PMU Frame 29	PMU Frame 30	PMU Frame 31	PMU Frame 32
Negative Sequence Algorithm Calculated Fault Location (miles)	47.3	47.3	47.3	47.3	47.3
Negative Sequence Algorithm Fault Location Error (percent)	10.4	10.4	10.4	10.4	10.4
Positive Sequence Algorithm Calculated Fault Location (miles)	49.4	49.9	49.6	49.8	49.7
Positive Sequence Algorithm Fault Location Error (percent)	12.7	13.1	12.8	13	12.9
Proposed Fault Location Algorithm Selected Correct Faulted Line (Yes/No)	Yes	Yes	Yes	Yes	Yes
Proposed Fault Location Algorithm Selected Correct Fault Type (Yes/No)	Yes	Yes	Yes	Yes	Yes

Table 5.19 comments: Proposed algorithm was able to perform fault location, determine the faulted line and the fault type with synchrophasor data from each frame

Table 5.20: CASE 7b results for AC fault at 50% (44.7miles) of the line with weak source on one end of the line

	PMU Frame 28	PMU Frame 29	PMU Frame 30	PMU Frame 31	PMU Frame 32
Negative Sequence Algorithm Calculated Fault Location (miles)	19.7	19.8	18.7	19.9	19.9
Negative Sequence Algorithm Fault Location Error (percent)	27.9	27.7	29.9	27.9	27.9
Positive Sequence Algorithm Calculated Fault Location (miles)	53.4	23.5	17.8	18.9	17.8
Positive Sequence Algorithm Fault Location Error (percent)	9.7	23.6	30.09	29.9	30.09
Proposed Fault Location Algorithm Selected Correct Faulted Line (Yes/No)	Yes	Yes	Yes	Yes	Yes
Proposed Fault Location Algorithm Selected Correct Fault Type (Yes/No)	Yes	No	Yes	No	Yes

Table 5.20 comments: Proposed algorithm was able perform fault location and determine faulted line from all frames, synchrophasor data from frame 29 and 31 was not able to determine the fault type.

Table 5.21: CASE 7c results for ABC fault at 70% (56.5miles) of the line with weak source on one end of the line

	PMU Frame 28	PMU Frame 29	PMU Frame 30	PMU Frame 31	PMU Frame 32
Negative Sequence Algorithm Calculated Fault Location (miles)	N/A	N/A	N/A	N/A	N/A
Negative Sequence Algorithm Fault Location Error (percent)	N/A	N/A	N/A	N/A	N/A
Positive Sequence Algorithm Calculated Fault Location (miles)	49.8	33.3	17.03	19.9	19.9
Positive Sequence Algorithm Fault Location Error (percent)	8.3	28.7	48.9	45.3	45.3
Proposed Fault Location Algorithm Selected Correct Faulted Line (Yes/No)	Yes	Yes	Yes	Yes	Yes
Proposed Fault Location Algorithm Selected Correct Fault Type (Yes/No)	No	No	Yes	Yes	Yes

Table 5.21 comments: For three phase fault, negative sequence algorithm was not used because the fault does not produce significant negative sequence component quantities. Proposed algorithm was able perform fault location and determine faulted line from all frames, synchrophasor data from frame 28 and 29 was not useful to determine the fault type.

Table 5.22: CASE 8a results for CG fault at 40% (37.7miles) of the line with line overload condition and 5 Ohm impedance fault

	PMU Frame 28	PMU Frame 29	PMU Frame 30	PMU Frame 31	PMU Frame 32
Negative Sequence Algorithm Calculated Fault Location (miles)	47.1	47.1	47.1	45.3	Unable to Calculate
Negative Sequence Algorithm Fault Location Error (percent)	9.8	9.8	9.8	7.9	N/A
Positive Sequence Algorithm Calculated Fault Location (miles)	49.8	49.8	49.7	50.7	Unable to Calculate
Positive Sequence Algorithm Fault Location Error (percent)	12.7	12.7	12.6	13.7	N/A
Proposed Fault Location Algorithm Selected Correct Faulted Line (Yes/No)	Yes	Yes	Yes	Yes	No
Proposed Fault Location Algorithm Selected Correct Fault Type (Yes/No)	Yes	Yes	Yes	Yes	No

Table 5.22 comments: Proposed algorithm could not determine fault location with the synchrophasor data measured in frame 32. Fault was decaying after breaker opening when frame 28 was measured.

Table 5.23: CASE 8b results for AC fault at 50% (47.2miles) of the line with line overload condition and 10 Ohm impedance fault

	PMU Frame 28	PMU Frame 29	PMU Frame 30	PMU Frame 31	PMU Frame 32
Negative Sequence Algorithm Calculated Fault Location (miles)	47.2	47.2	47.2	47.2	47.2
Negative Sequence Algorithm Fault Location Error (percent)	0	0	0	0	0
Positive Sequence Algorithm Calculated Fault Location (miles)	7.8	7.7	49.2	7.7	7.8
Positive Sequence Algorithm Fault Location Error (percent)	41	41.8	2.1	41.8	41
Proposed Fault Location Algorithm Selected Correct Faulted Line (Yes/No)	Yes	Yes	Yes	Yes	Yes
Proposed Fault Location Algorithm Selected Correct Fault Type (Yes/No)	Yes	Yes	Yes	Yes	Yes

Table 5.23 comments: Proposed algorithm was able to perform fault location, determine the faulted line and the fault type with synchrophasor data from each frame.

Table 5.24: CASE 8c results for ABC fault at 70% (66.1miles) of the line with line overload condition and 5 Ohm impedance fault

	PMU Frame 28	PMU Frame 29	PMU Frame 30	PMU Frame 31	PMU Frame 32
Negative Sequence Algorithm Calculated Fault Location (miles)	N/A	N/A	N/A	N/A	N/A
Negative Sequence Algorithm Fault Location Error (percent)	N/A	N/A	N/A	N/A	N/A
Positive Sequence Algorithm Calculated Fault Location (miles)	Unable to Calculate	52.7	50.3	49.8	50.4
Positive Sequence Algorithm Fault Location Error (percent)	N/A	14.9	16.7	17.2	16.6
Proposed Fault Location Algorithm Selected Correct Faulted Line (Yes/No)	No	Yes	Yes	Yes	Yes
Proposed Fault Location Algorithm Selected Correct Fault Type (Yes/No)	No	No	Yes	Yes	Yes

Table 5.24 comments: For three phase fault, negative sequence algorithm was not used because the fault does not produce significant negative sequence component quantities. Proposed algorithm could not determine fault location with the synchrophasor data measured in frame 28. Fault started evolving when frame 28 was measured.

Table 5.25: CASE 9a results for CG fault at 40% (37.7miles) of the line with maximum DC offset and weak source on one end of the line

	PMU Frame 28	PMU Frame 29	PMU Frame 30	PMU Frame 31	PMU Frame 32
Negative Sequence Algorithm Calculated Fault Location (miles)	Unable to Calculate	47.1	47.1	47.1	47.1
Negative Sequence Algorithm Fault Location Error (percent)	N/A	9.8	9.8	9.8	9.8
Positive Sequence Algorithm Calculated Fault Location (miles)	Unable to Calculate	Unable to Calculate	49.9	49.5	49.8
Positive Sequence Algorithm Fault Location Error (percent)	N/A	N/A	12.8	12.4	12.8
Proposed Fault Location Algorithm Selected Correct Faulted Line (Yes/No)	No	Yes	Yes	Yes	Yes
Proposed Fault Location Algorithm Selected Correct Fault Type (Yes/No)	No	Yes	Yes	Yes	Yes

Table 5.25 comments: Proposed algorithm could not determine fault location with the synchrophasor data measured in frame 28. Fault started evolving when frame 28 was measured.

Table 5.26: CASE 9b results for AC fault at 10% (8.8miles) of the line with maximum DC offset and weak source on one end of the line

	PMU Frame 28	PMU Frame 29	PMU Frame 30	PMU Frame 31	PMU Frame 32
Negative Sequence Algorithm Calculated Fault Location (miles)	20	20	18.8	20	20
Negative Sequence Algorithm Fault Location Error (percent)	12.4	12.4	11.2	12.4	12.4
Positive Sequence Algorithm Calculated Fault Location (miles)	19.6	19	17.8	19.01	18.9
Positive Sequence Algorithm Fault Location Error (percent)	11.2	11.3	9.9	11.3	11.3
Proposed Fault Location Algorithm Selected Correct Faulted Line (Yes/No)	Yes	Yes	Yes	Yes	Yes
Proposed Fault Location Algorithm Selected Correct Fault Type (Yes/No)	Yes	Yes	Yes	yes	Yes

Table 5.26 comments: Proposed algorithm was able to perform fault location, determine the faulted line and the fault type with synchrophasor data from each frame.

Table 5.27: CASE 9c results for ABC fault at 50% (40.4miles) of the line with maximum DC offset and weak source on one end of the line

	PMU Frame 28	PMU Frame 29	PMU Frame 30	PMU Frame 31	PMU Frame 32
Negative Sequence Algorithm Calculated Fault Location (miles)	N/A	N/A	N/A	N/A	N/A
Negative Sequence Algorithm Fault Location Error (percent)	N/A	N/A	N/A	N/A	N/A
Positive Sequence Algorithm Calculated Fault Location (miles)	64.5	62.8	72.95	61.16	61.16
Positive Sequence Algorithm Fault Location Error (percent)	29.9	27.7	40.2	25.6	25.6
Proposed Fault Location Algorithm Selected Correct Faulted Line (Yes/No)	Yes	Yes	Yes	Yes	Yes
Proposed Fault Location Algorithm Selected Correct Fault Type (Yes/No)	Yes	Yes	Yes	Yes	Yes

Table 5.27 comments: For three phase fault, negative sequence algorithm was not used because the fault does not produce significant negative sequence component quantities.

Table 5.28: CASE 10a results for CG fault at 40% (37.7miles) of the line with 75% series capacitor compensation inserted and 3 Ohm fault resistance

	PMU Frame 28	PMU Frame 29	PMU Frame 30	PMU Frame 31	PMU Frame 32
Negative Sequence Algorithm Calculated Fault Location (miles)	Unable to Calculate	Unable to Calculate	48.4	49	Unable to Calculate
Negative Sequence Algorithm Fault Location Error (percent)	N/A	N/A	11.7	11.9	N/A
Positive Sequence Algorithm Calculated Fault Location (miles)	Unable to Calculate	Unable to Calculate	47.2	47.8	Unable to Calculate
Positive Sequence Algorithm Fault Location Error (percent)	N/A	N/A	10.42	10.6	N/A
Proposed Fault Location Algorithm Selected Correct Faulted Line (Yes/No)	No	No	Yes	Yes	No
Proposed Fault Location Algorithm Selected Correct Fault Type (Yes/No)	No	No	Yes	Yes	No

Table 5.28 comments: Proposed algorithm could not determine fault location with the synchrophasor data measured in frame 28, 29 and 32. MOV non-linearities in SLG fault caused errors in fault location.

Table 5.29: CASE 10b results for AC fault at 50% (44.7miles) of the line with 75% compensation series capacitor inserted and 6 Ohm fault resistance

	PMU Frame 28	PMU Frame 29	PMU Frame 30	PMU Frame 31	PMU Frame 32
Negative Sequence Algorithm Calculated Fault Location (miles)	21.5	20.6	16.9	16.9	19.4
Negative Sequence Algorithm Fault Location Error (percent)	25.8	26.8	30	30	28.2
Positive Sequence Algorithm Calculated Fault Location (miles)	46.3	17.07	31.98	29.2	39.9
Positive Sequence Algorithm Fault Location Error (percent)	1.9	30.8	14.09	17.2	5.1
Proposed Fault Location Algorithm Selected Correct Faulted Line (Yes/No)	Yes	Yes	Yes	Yes	Yes
Proposed Fault Location Algorithm Selected Correct Fault Type (Yes/No)	No	No	Yes	No	No

Table 5.29 comments: Proposed algorithm was able perform fault location and determine faulted line from all frames.

Table 5.30: CASE 10c results for ABC fault at 70% (56.5miles) of the line with 75% series capacitor compensation inserted and 9 Ohm fault resistance

	PMU Frame 28	PMU Frame 29	PMU Frame 30	PMU Frame 31	PMU Frame 32
Negative Sequence Algorithm Calculated Fault Location (miles)	N/A	N/A	N/A	N/A	N/A
Negative Sequence Algorithm Fault Location Error (percent)	N/A	N/A	N/A	N/A	N/A
Positive Sequence Algorithm Calculated Fault Location (miles)	61.4	61.2	72.9	63	65.03
Positive Sequence Algorithm Fault Location Error (percent)	6.0	6.0	20.2	8.0	10.5
Proposed Fault Location Algorithm Selected Correct Faulted Line (Yes/No)	Yes	Yes	Yes	Yes	Yes
Proposed Fault Location Algorithm Selected Correct Fault Type (Yes/No)	Yes	Yes	Yes	Yes	No

Table 5.30 comments: For three phase fault, negative sequence algorithm was not used because the fault does not produce significant negative sequence component quantities. Proposed algorithm was able perform fault location and determine faulted line from all frames, but synchrophasor data from frame 32 was not useful to determine the fault type.

5.6.1 Fault Location Performance Evaluation

In general terms fault location accuracy using synchronized phasor data performed well. In each case, fault location was provided at least with one frame. Both the modified Takagi (positive sequence) and negative sequence two-ended fault location equations were able to provide fault location when there was sufficient negative sequence current and the main fault location algorithm used for the thesis was able to provide the correct faulted line and fault type. Fault location provided by two-ended negative sequence fault location equation was more accurate than the fault location provided by two-ended Takagi modified (positive sequence) fault location equations. For this thesis, a fault location with less than five percent of error will be considered excellent performance. Fault location error between five to fifteen percent will be considered decent performance. More than fifteen percent will be considered bad performance.

For analysis, the fault location accuracy performance will be analyzed using the following cases: Case 1, Case 2, and Case 3. These cases were selected because they represent the most common system conditions during faults.

Case 1a, a CG line fault was applied at 50% of the line with the normal system configuration. The two-ended negative sequence method obtained a fault location error average percentage of 0%. Therefore, the performance was excellent. The two-ended modified Takagi (positive sequence) method obtained a fault location average percentage error of 2.5%. The accuracy of performance can be considered excellent which means fault location is reliable as a basis to send field crews to that specific location for equipment repair. For the positive sequence algorithm, all the frames varied a little in fault location due to change in phase current magnitude during the fault window. Frame 28 was unable to calculate fault location because synchrophasor data was created when the fault started. Thus, fault location error percentage for frame 28 was ignored. Finally, the proposed algorithm was able to determine faulted line and the fault type for all frames.

Case 1b, an ABC line fault was applied at 20% of the line with normal system. The two-ended Modified Takagi (positive sequence) method obtained a fault location error percentage average of 3.9%. The accuracy performance can be considered excellent. The proposed algorithms could determine the proper faulted line and fault type for all frames.

Case 1c, an BC line fault was applied at 50% of the line with normal system. The two-ended negative sequence method obtained a fault location error percentage average of 4.8%. Therefore, the performance was excellent. The two-ended modified Takagi (positive sequence) method obtained a fault location error percentage average of 12.6%. The accuracy performance can be considered decent. The proposed algorithm could determine the fault line for all frames, but not the fault type. Only frame 28 was able to determine the fault type.

Case 2a, an BCG line fault was applied at 40% of the line with a line overload condition. The two-ended negative sequence method obtained a fault location error percentage average of 6.2%. Therefore, the performance was decent. The two-ended modified Takagi (positive sequence) method obtained a fault location error percentage average of 9.2%. The accuracy performance can be considered decent. In this case the positive sequence fault location equation had more error than the negative sequence fault location equation due to the line overload effect that causes a decrease in the impedance of fault location equation. In this case, the proposed algorithm could determine the faulted line and fault type for all frames.

Case 2b, CG line fault was applied at 25% of the line with line overloading condition. The two-ended negative sequence method obtained a fault location error percentage average of 2.1%. Therefore, the performance was excellent. The two-ended Takagi modified (positive sequence) method obtained a fault location error percentage average of 3.5%. The accuracy performance can also be considered excellent. In this case, the proposed algorithm could determine the faulted line and fault type for all frames.

Case 2c, an ABC line fault was applied at 50% of the line with a line overload condition. The two-ended modified Takagi (positive sequence) method obtained an average fault location error of 10.5%. The accuracy performance can be considered decent. Frame 28 was unable to calculate fault location because synchrophasor data was created when the fault start evolving. Thus, fault location result for frame 28 was ignored.

Case 3a, a CG line fault was applied at 60% of the line with a fault impedance of 10 ohms. The two-ended negative sequence method obtained a fault location error percentage average of 26%. Therefore, the performance was poor. After analyzing the data, I observed that there was a little time misalignment on the synchrophasor data taken at both ends of the line during this fault. Even

though in theory the negative sequence fault location equation should be immune to fault resistance, the little time misalignment can cause errors in fault location. The two-ended modified Takagi (positive sequence) method obtained a fault location error percentage average of 25.3%. The accuracy performance also was poor.

Case 3b, AB line fault was applied at 20% of the line with a fault impedance of 20 ohms. The two-ended negative sequence method obtained a fault location error percentage average of 13.4%. Therefore, the performance was decent. Same problem as case 3b, a little time misalignment caused errors in the fault location. The two-ended Takagi modified (positive sequence) method obtained a fault location error percentage average of 15%. The accuracy performance can be considered also decent.

Case 3c, ABC line fault was applied at 40% of the line with a fault impedance of 30 ohms. The two-ended Takagi modified (positive sequence) method obtained a fault location error percentage average of 3.5%. The accuracy performance can be considered excellent.

The cases 4 to 9 results are not going to be discussed because the system conditions on these cases are cases difficult to see real life, but for the purpose of the thesis they were tested. For cases 4 to 9, the fault location algorithm was able to determine a decent fault location.

In Case 10, series compensated lines introduced non-linearities to the fault location with high impedance faults when calculation was performed using the two-ended impedance based fault location equations. Both the negative sequence method and modified Takagi (positive sequence) method performed very poorly. The explanation of this poor performance is because series capacitors have MOV for overvoltage protection and when the MOVs conduct during fault causes non-linearities affecting fault location. As an example, in case 10a, a SLG fault was applied and the fault location ranged from 11.7% to 11.9% for negative sequence fault location method and 10.42%

to 10.6% for modified Takagi (positive sequence) fault location method. In case 10b, a line-to-line fault was applied and the fault location error for negative sequence fault location method ranged from 25.8% to 30% and fault location error for modified Takagi (positive sequence) ranged from 5.1% to 30.8%. In case 10c, a 3ph fault was applied and the fault location error ranged from 5.25% to 15.7% for Takagi modified (positive sequence) fault location method.

In terms of fault type selection and faulted line selection, 95% of the synchronized phasor frames perform well. In a few cases, the synchronized phasor did not help to select the correct line or fault type.

In summary, fault location accuracy performance using impedance based fault location method was overall decent and in some cases excellent as long the system faults do not trigger non-linearities. This means that impedance based fault location method using synchronized phasor data can be implemented for non-compensated lines. Having synchrophasor data available brings two big advantages. The first advantage is that fault location promises to be more accurate because faulted data can be collected from both ends of the line and the second advantage is that synchronized phasor data can provide real time fault location. The only disadvantage is that even though synchronized phasor measurements provide very accurate measurement in real time, installing synchrophasor technology can be costly.

5.6.2 Lessons Learned

During this investigation, there were software and hardware failures. These failures allowed me to learn more about the implementation of the equipment. The first failure was a software failure where RTDS modeled system was not performing as intended. The problem was that when faults were applied on the lines, the RTDS applied the wrong fault. As an example, when a LG fault was

applied in any line, sometimes the software applied a three phase fault instead of the LG fault. This forced me to look for the personnel in charge of the RTDS programing to troubleshoot it and at the same time learn how the modules were programmed in RTDS. The second failure was a hardware failure. In this case one RTDS module failed and the power system model could not be ran. In this case, the RTDS Company got involved to solve this issue. After the RTDS Company replaced the failed hardware with a new part, more issues arose regarding compatibility and interoperability with the rest of the lab equipment. Since the newly installed RTDS hardware contained the latest firmware, the rest of the lab equipment was not compatible with the new hardware. So the power system model software had to be upgraded to the new version so it could communicate with the new installed RTDS hardware. Adding the new RTDS hardware also caused that some phasor data concentrators and phasor measurements units to fail to communicate with the RTDS hardware. In this case, the phasor data concentrator and phasor measurement unit manufacturers were contacted to address the problem. The solution was to upgrade all of the equipment to the latest firmware version that the manufacturer had at that moment. Addressing these issues provided me with a better prospective about how complex can be the implementation of synchrophasors can be because if any equipment fails, we need to make sure that the replacement equipment and software and hardware firmware will be compatible with the existing equipment.

Conclusions

This investigation focused in determining the fault location accuracy using synchrophasor data with two-ended fault location algorithms. Fault location accuracy is very important for utilities because accurate fault location can translate in saving millions of dollars during the repair of damaged transmission line equipment. In the past, traditional fault location was performed using only single ended methods due to the lack of communication between both ends of the line. Now with synchronized data available, fault location accuracy promises to be much better. Phasor Measurement Units represent a revolution in power systems monitoring and control. A PMU can measure current and voltage and calculate phase angle. Therefore a real-time calculation of phase angle can be achieved. Now with the satellite GPS (Global Positioning System) availability, digital measurements at different line terminals can be performed synchronously.

Since synchronization is not available with traditional measurements for fault location methods, synchronized phasor can improve fault location accuracy because it can be calculated in real time data from both ends of the faulted line.

8. Future Work

As this work concludes, the next step in this investigation is to fully implement a fault location process using synchronized phasor data as a new utility fault locating tool. However some considerations must be taken. First, in order for the algorithm to estimate the fault location, the phasor data concentrator must automatically push synchronized phasor data into the fault location algorithm. To do that, it may be necessary to work with the PDC manufacturers so they can program a PDC to push the required data into the algorithm. Second, since the algorithm needs to know specific information in regards positive and zero sequence line impedance to estimate the fault location, the PDC has to have a way for the user to enter that data.

Since the fault location algorithm used for this thesis was based on assumptions such as system impedance angles homogeneous, phase impedances equal, no effect from mutual coupling and it ignores shunt currents, the next step in this investigation is to make the algorithm more robust. To do that first the algorithm should be able to calculate fault location in bigger power systems. In this case, the algorithm must be programmed to accept many line impedances and line names from each line of the power system and also being able to receive synchronized phasor measurement from every end of each line. Second, the algorithm also needs to be improved to give fault location for series compensated lines, mutually coupled lines, and three terminal lines. Third, the fault location algorithm should be able to determine which synchrophasor frame can be best used to provide proper fault location information such as correct fault type and fault location.

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Appendix A: Thesis Fault Location Algorithm

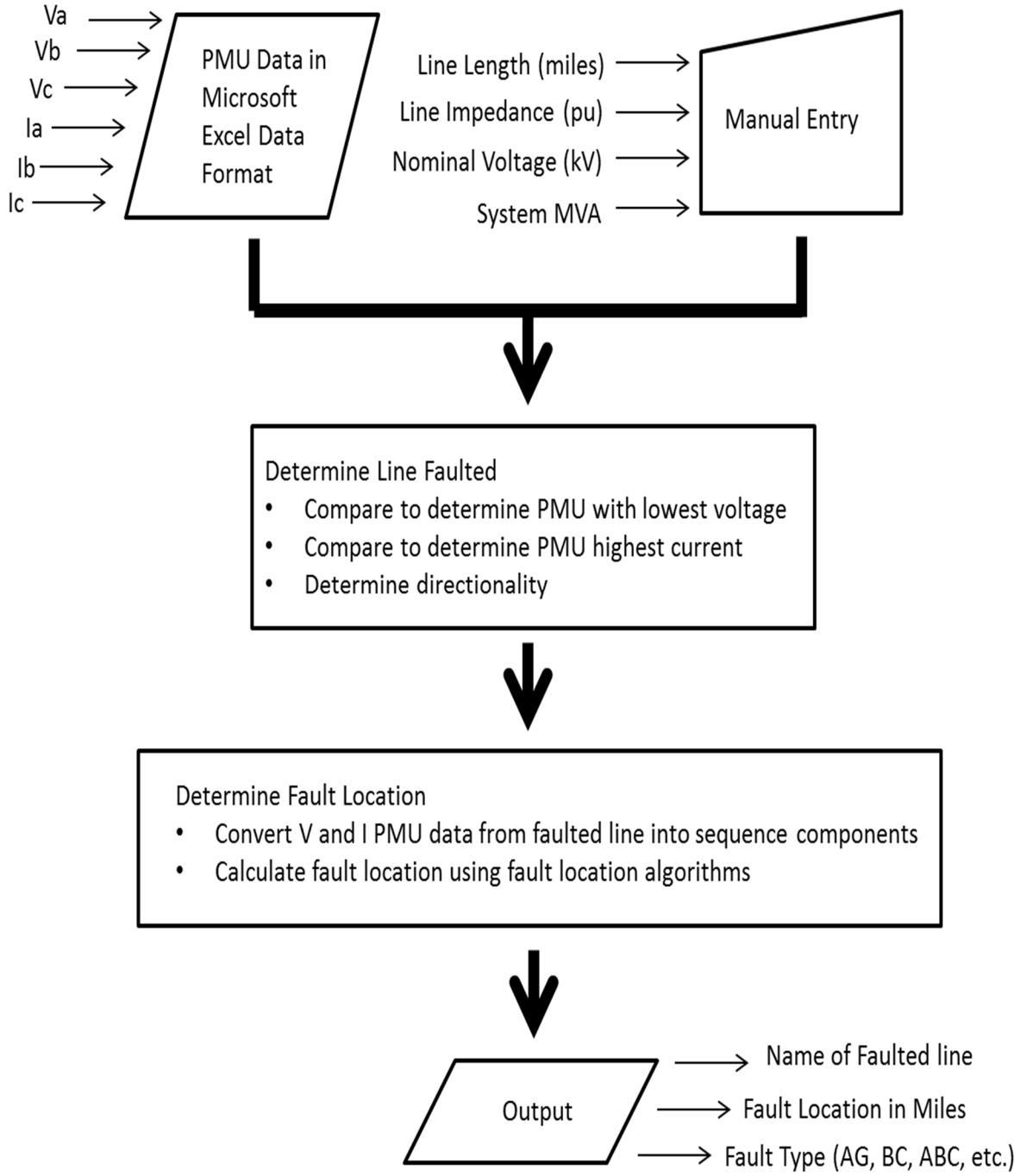


Figure 1 - Block diagram of the proposed fault location algorithm

MathCAD Implementation

$j := j \qquad pu := 1 \qquad MVA := 1000kW \qquad a := 1 \cdot e^{j \cdot 120deg} \qquad Vf := 1pu$

$\angle(magnitude, angle) := magnitude\cos(angle) + j \cdot magnitude\sin(angle)$

- **PHASOR DATA CONCENTRATOR DATA (P-CLASS)**

PMU1 - MLN

$VA_{pmu1} := (297386V) \angle (-55.132deg)$

$VB_{pmu1} := (314302V) \angle (179.975deg)$

$VC_{pmu1} := (283688V) \angle (59.345deg)$

$IA_{pmu1} := (1805.466 \cdot A) \angle (-136.146deg)$

$IB_{pmu1} := (2165.176A) \angle (-179.909deg)$

$IC_{pmu1} := (3467.892A) \angle (15.048deg)$

PMU2 - RM #1

$VA_{pmu2} := (192391V) \angle (-59.77deg)$

$VB_{pmu2} := (301156V) \angle (157.018deg)$

$VC_{pmu2} := (187221V) \angle (15.137deg)$

$IA_{pmu2} := (1967 \cdot A) \angle (43.657deg)$

$IB_{pmu2} := (2175.713A) \angle (-18.895deg)$

$IC_{pmu2} := (3540.954A) \angle (-169.362deg)$

PMU3 - RM #2

$VA_{pmu3} := (192146.1V) \angle (-59.643deg)$

$VB_{pmu3} := (301217.7V) \angle (157.08deg)$

$VC_{pmu3} := (187218.2V) \angle (15.205deg)$

$IA_{pmu3} := (10045 \cdot A) \angle (159.937deg)$

$IB_{pmu3} := (610.824A) \angle (166.372deg)$

$IC_{pmu3} := (10618.27A) \angle (-19.641deg)$

PMU4 - TM

$VA_{pmu4} := (221163.8V) \angle (-78.087deg)$

$VB_{pmu4} := (302999.1V) \angle (150.448deg)$

$VC_{pmu4} := (230412V) \angle (169.81deg)$

$IA_{pmu4} := (4210.908 \cdot A) \angle (149.465deg)$

$IB_{pmu4} := (588.445A) \angle (-31.979deg)$

$IC_{pmu4} := (3617.253A) \angle (-30.337deg)$

PMU5 - LB

$VA_{pmu5} := (311830V) \angle (-94.36deg)$

$VB_{pmu5} := (312770.9V) \angle (145.582deg)$

$VC_{pmu5} := (312028.8V) \angle (25.462deg)$

$IA_{pmu5} := (159.494 \cdot A) \angle (-95.759deg)$

$IB_{pmu5} := (163.408A) \angle (149.967deg)$

$IC_{pmu5} := (175.248A) \angle (26.029deg)$

PMU6 - GAT

$VA_{pmu6} := (307089.1V) \angle (-95.747deg)$

$VB_{pmu6} := (308799.2V) \angle (144.164deg)$

$VC_{pmu6} := (307535.6V) \angle (23.932deg)$

$IA_{pmu6} := (238.57 \cdot A) \angle (36.791deg)$

$IB_{pmu6} := (229.411A) \angle (-80.051deg)$

$IC_{pmu6} := (245.193A) \angle (160.193deg)$

PMU7 - MWY

$VA_{pmu7} := (313703.8V) \angle (-96.479deg)$

$VB_{pmu7} := (314154.3V) \angle (143.492deg)$

$VC_{pmu7} := (313804V) \angle (23.435deg)$

$IA_{pmu7} := (662.741 \cdot A) \angle (-81.234deg)$

$IB_{pmu7} := (661.267A) \angle (158.44deg)$

$IC_{pmu7} := (659.367A) \angle (38.782deg)$

PMU8 - VCN

$VA_{pmu8} := (319617.2V) \angle (-105.475deg)$

$VB_{pmu8} := (319786.3V) \angle (134.517deg)$

$VC_{pmu8} := (319664.9V) \angle (134.517deg)$

$IA_{pmu8} := (624.059 \cdot A) \angle (78.258deg)$

$IB_{pmu8} := (623.031A) \angle (-42.138deg)$

$IC_{pmu8} := (619.814A) \angle (-161.857deg)$

- **PHASOR DATA CONCENTRATOR SETTINGS**

Manually entered by the user

$V_{nom} := 500kV$ $MVA_{base} := 100MVA$

Line 1 Name: 500kV RM-MLN # 1 **PMU:** 1,2

$Rpu_{line1} := 0.00103pu$ $R0pu_{line1} := 0.01028pu$

$Xpu_{line1} := 0.02136pu$ $X0pu_{line1} := 0.07251pu$

$LL_{line1\_miles} := 94.42$

Line 2 Name: 500kV RM-TM # 2 **PMU:** 3,4

$Rpu_{line2} := 0.00097pu$ $R0pu_{line2} := 0.00952pu$

$Xpu_{line2} := 0.02167pu$ $X0pu_{line2} := 0.06294pu$

$LL_{line2\_miles} := 89.06$

Line 3 Name: 500kV GAT - LB # 1 **PMU:** 5,6

$Rpu_{line3} := 0.00pu$ $R0pu_{line3} := 0.00pu$

$Xpu_{line3} := 0.0186pu$ $X0pu_{line3} := 0.0582pu$

$LL_{line3\_miles} := 80.85$

Line 4 Name: 500kV MWY - VCN # 1 **PMU:** 7,8

$Rpu_{line4} := 0.00097pu$ $R0pu_{line4} := 0.01264pu$

$Xpu_{line4} := 0.02434pu$ $X0pu_{line4} := 0.08735pu$

$LL_{line4\_miles} := 112.6$

- **PHASOR DATA CONCENTRATOR ALGORITHM INTERNAL CALCULATIONS**

$$V_{base} := V_{nom} \qquad A_{012} := \begin{pmatrix} 1 & 1 & 1 \\ 1 & a^2 & a \\ 1 & a & a^2 \end{pmatrix}$$

$$I_{base500} := \frac{MVA_{base}}{\sqrt{3} \cdot V_{base}} = 115.47\,A \qquad Z_{base} := \frac{V_{base}^{\,2}}{MVA_{base}} = 2.5 \times 10^3\,ohm$$

$$Z1_{line1} := \left(Rpu_{line1} + j \cdot Xpu_{line1}\right) \cdot Z_{base} = (2.575 + 53.4i) \cdot ohm$$

$$Z0_{line1} := \left(R0pu_{line1} + j \cdot X0pu_{line1}\right) \cdot Z_{base} = (25.7 + 181.275i) \cdot ohm$$

$$Z1_{line2} := \left(Rpu_{line2} + j \cdot Xpu_{line2}\right) \cdot Z_{base} = (2.425 + 54.175i) \cdot ohm$$

$$Z0_{line2} := \left(R0pu_{line2} + j \cdot X0pu_{line2}\right) \cdot Z_{base} = (23.8 + 157.35i) \cdot ohm$$

$$Z1_{line3} := \left(Rpu_{line3} + j \cdot Xpu_{line3}\right) \cdot Z_{base} = 46.5i \cdot ohm$$

$$Z0_{line3} := \left(R0pu_{line3} + j \cdot X0pu_{line3}\right) \cdot Z_{base} = 145.5i \cdot ohm$$

$$Z1_{line4} := \left(Rpu_{line4} + j \cdot Xpu_{line4}\right) \cdot Z_{base} = (2.425 + 60.85i) \cdot ohm$$

$$Z0_{line4} := \left(R0pu_{line4} + j \cdot X0pu_{line4}\right) \cdot Z_{base} = (31.6 + 218.375i) \cdot ohm$$

- **SYMMETRICAL COMPONENTS CALCULATION OF EACH PMU**

PMU1 Voltage and Current Sequence Components

$$\begin{pmatrix} IA0_{pmu1} \\ IA1_{pmu1} \\ IA2_{pmu1} \end{pmatrix} := A_{012}^{-1} \cdot \begin{pmatrix} IA_{pmu1} \\ IB_{pmu1} \\ IC_{pmu1} \end{pmatrix} \qquad \begin{pmatrix} VA0_{pmu1} \\ VA1_{pmu1} \\ VA2_{pmu1} \end{pmatrix} := A_{012}^{-1} \cdot \begin{pmatrix} VA_{pmu1} \\ VB_{pmu1} \\ VC_{pmu1} \end{pmatrix}$$

$$|IA0_{pmu1}| = 124.38\,A \qquad \arg(IA0_{pmu1}) = -108.457 \cdot deg$$

$$|IA1_{pmu1}| = 2.19 \times 10^{3}\,A \qquad \arg(IA1_{pmu1}) = -99.738 \cdot deg$$

$$|IA2_{pmu1}| = 1.359 \times 10^{3}\,A \qquad \arg(IA2_{pmu1}) = 131.027 \cdot deg$$

$$|VA0_{pmu1}| = 132.746 \cdot V \qquad \arg(VA0_{pmu1}) = 27.504 \cdot deg$$

$$|VA1_{pmu1}| = 2.982 \times 10^{5} \cdot V \qquad \arg(VA1_{pmu1}) = -58.6 \cdot deg$$

$$|VA2_{pmu1}| = 1.791 \times 10^{4} \cdot V \qquad \arg(VA2_{pmu1}) = 35.728 \cdot deg$$

- **PMU2 Voltage and Current Sequence Components**

$$\begin{pmatrix} IA0_{pmu2} \\ IA1_{pmu2} \\ IA2_{pmu2} \end{pmatrix} := A_{012}^{-1} \cdot \begin{pmatrix} IA_{pmu2} \\ IB_{pmu2} \\ IC_{pmu2} \end{pmatrix} \qquad \begin{pmatrix} VA0_{pmu2} \\ VA1_{pmu2} \\ VA2_{pmu2} \end{pmatrix} := A_{012}^{-1} \cdot \begin{pmatrix} VA_{pmu2} \\ VB_{pmu2} \\ VC_{pmu2} \end{pmatrix}$$

$$|IA0_{pmu2}| = 0.504\,A \qquad \arg(IA0_{pmu2}) = -13.2 \cdot deg$$

$$|IA1_{pmu2}| = 2.391 \times 10^{3}\,A \qquad \arg(IA1_{pmu2}) = 72.322 \cdot deg$$

$$|IA2_{pmu2}| = 1.154 \times 10^{3}\,A \qquad \arg(IA2_{pmu2}) = -52.863 \cdot deg$$

$$|VA0_{pmu2}| = 138.598 \cdot V \qquad \arg(VA0_{pmu2}) = 36.028 \cdot deg$$

$$|VA1_{pmu2}| = 2.172 \times 10^{5} \cdot V \qquad \arg(VA1_{pmu2}) = -82.45 \cdot deg$$

$$|VA2_{pmu2}| = 8.401 \times 10^{4} \cdot V \qquad \arg(VA2_{pmu2}) = 35.723 \cdot deg$$

- **PMU3 Voltage and Current Sequence Components**

$$\begin{pmatrix} IA0_{pmu3} \\ IA1_{pmu3} \\ IA2_{pmu3} \end{pmatrix} := A_{012}^{-1} \cdot \begin{pmatrix} IA_{pmu3} \\ IB_{pmu3} \\ IC_{pmu3} \end{pmatrix} \qquad \begin{pmatrix} VA0_{pmu3} \\ VA1_{pmu3} \\ VA2_{pmu3} \end{pmatrix} := A_{012}^{-1} \cdot \begin{pmatrix} VA_{pmu3} \\ VB_{pmu3} \\ VC_{pmu3} \end{pmatrix}$$

$$|IA0_{pmu3}| = 11.788\,A \qquad \arg(IA0_{pmu3}) = 143.937 \cdot deg$$

$$|IA1_{pmu3}| = 5.938 \times 10^{3}\,A \qquad \arg(IA1_{pmu3}) = -166.97 \cdot deg$$

$$|IA2_{pmu3}| = 6.007 \times 10^{3}\,A \qquad \arg(IA2_{pmu3}) = 127.311 \cdot deg$$

$$|VA0_{pmu3}| = 231.741 \cdot V \qquad \arg(VA0_{pmu3}) = 61.103 \cdot deg$$

$$|VA1_{pmu3}| = 2.172 \times 10^{5} \cdot V \qquad \arg(VA1_{pmu3}) = -82.377 \cdot deg$$

$$|VA2_{pmu3}| = 8.411 \times 10^{4} \cdot V \qquad \arg(VA2_{pmu3}) = 35.834 \cdot deg$$

- **PMU4 Voltage and Current Sequence Components**

$$\begin{pmatrix} IA0_{pmu4} \\ IA1_{pmu4} \\ IA2_{pmu4} \end{pmatrix} := A_{012}^{-1} \cdot \begin{pmatrix} IA_{pmu4} \\ IB_{pmu4} \\ IC_{pmu4} \end{pmatrix} \qquad \begin{pmatrix} VA0_{pmu4} \\ VA1_{pmu4} \\ VA2_{pmu4} \end{pmatrix} := A_{012}^{-1} \cdot \begin{pmatrix} VA_{pmu4} \\ VB_{pmu4} \\ VC_{pmu4} \end{pmatrix}$$

$$|IA0_{pmu4}| = 1.966\,A \qquad \arg(IA0_{pmu4}) = 172.719 \cdot deg$$

$$|IA1_{pmu4}| = 2.272 \times 10^{3}\,A \qquad \arg(IA1_{pmu4}) = 172.094 \cdot deg$$

$$|IA2_{pmu4}| = 2.286 \times 10^{3}\,A \qquad \arg(IA2_{pmu4}) = 126.97 \cdot deg$$

$$|VA0_{pmu4}| = 1.485 \times 10^{5} \cdot V \qquad \arg(VA0_{pmu4}) = -176.629 \cdot deg$$

$$|VA1_{pmu4}| = 1.319 \times 10^{5} \cdot V \qquad \arg(VA1_{pmu4}) = -60.192 \cdot deg$$

$$|VA2_{pmu4}| = 1.586 \times 10^{5} \cdot V \qquad \arg(VA2_{pmu4}) = -35.995 \cdot deg$$

- **PMU5 Voltage and Current Sequence Components**

$$\begin{pmatrix} IA0_{pmu5} \\ IA1_{pmu5} \\ IA2_{pmu5} \end{pmatrix} := A_{012}^{-1} \cdot \begin{pmatrix} IA_{pmu5} \\ IB_{pmu5} \\ IC_{pmu5} \end{pmatrix} \qquad \begin{pmatrix} VA0_{pmu5} \\ VA1_{pmu5} \\ VA2_{pmu5} \end{pmatrix} := A_{012}^{-1} \cdot \begin{pmatrix} VA_{pmu5} \\ VB_{pmu5} \\ VC_{pmu5} \end{pmatrix}$$

$$|IA0_{pmu5}| = 8.852 \times 10^{-5}\,A \qquad \arg(IA0_{pmu5}) = -27.479 \cdot deg$$

$$|IA1_{pmu5}| = 165.909\,A \qquad \arg(IA1_{pmu5}) = -93.252 \cdot deg$$

$$|IA2_{pmu5}| = 9.581\,A \qquad \arg(IA2_{pmu5}) = 133.479 \cdot deg$$

$$|VA0_{pmu5}| = 1.269 \cdot V \qquad \arg(VA0_{pmu5}) = 98.513 \cdot deg$$

$$|VA1_{pmu5}| = 3.122 \times 10^{5} \cdot V \qquad \arg(VA1_{pmu5}) = -94.439 \cdot deg$$

$$|VA2_{pmu5}| = 571.804 \cdot V \qquad \arg(VA2_{pmu5}) = 37.036 \cdot deg$$

- **PMU6 Voltage and Current Sequence Components**

$$\begin{pmatrix} IA0_{pmu6} \\ IA1_{pmu6} \\ IA2_{pmu6} \end{pmatrix} := A_{012}^{-1} \cdot \begin{pmatrix} IA_{pmu6} \\ IB_{pmu6} \\ IC_{pmu6} \end{pmatrix} \qquad \begin{pmatrix} VA0_{pmu6} \\ VA1_{pmu6} \\ VA2_{pmu6} \end{pmatrix} := A_{012}^{-1} \cdot \begin{pmatrix} VA_{pmu6} \\ VB_{pmu6} \\ VC_{pmu6} \end{pmatrix}$$

$$|IA0_{pmu6}| = 8.953 \times 10^{-4}\,A \qquad \arg(IA0_{pmu6}) = 58.951 \cdot deg$$

$$|IA1_{pmu6}| = 237.637\,A \qquad \arg(IA1_{pmu6}) = 38.977 \cdot deg$$

$$|IA2_{pmu6}| = 9.13\,A \qquad \arg(IA2_{pmu6}) = -46.26 \cdot deg$$

$$|VA0_{pmu6}| = 1.103 \cdot V \qquad \arg(VA0_{pmu6}) = -23.703 \cdot deg$$

$$|VA1_{pmu6}| = 3.078 \times 10^{5} \cdot V \qquad \arg(VA1_{pmu6}) = -95.884 \cdot deg$$

$$|VA2_{pmu6}| = 1.026 \times 10^{3} \cdot V \qquad \arg(VA2_{pmu6}) = 38.633 \cdot deg$$

- **PMU7 Voltage and Current Sequence Components**

$$\begin{pmatrix} IA0_{pmu7} \\ IA1_{pmu7} \\ IA2_{pmu7} \end{pmatrix} := A_{012}^{-1} \cdot \begin{pmatrix} IA_{pmu7} \\ IB_{pmu7} \\ IC_{pmu7} \end{pmatrix} \qquad \begin{pmatrix} VA0_{pmu7} \\ VA1_{pmu7} \\ VA2_{pmu7} \end{pmatrix} := A_{012}^{-1} \cdot \begin{pmatrix} VA_{pmu7} \\ VB_{pmu7} \\ VC_{pmu7} \end{pmatrix}$$

$$|IA0_{pmu7}| = 0.333\,A \qquad \arg(IA0_{pmu7}) = 89.97 \cdot deg$$

$$|IA1_{pmu7}| = 661.122\,A \qquad \arg(IA1_{pmu7}) = -81.337 \cdot deg$$

$$|IA2_{pmu7}| = 2.259\,A \qquad \arg(IA2_{pmu7}) = -50.872 \cdot deg$$

$$|VA0_{pmu7}| = 4.134 \cdot V \qquad \arg(VA0_{pmu7}) = 17.035 \cdot deg$$

$$|VA1_{pmu7}| = 3.139 \times 10^{5} \cdot V \qquad \arg(VA1_{pmu7}) = -96.517 \cdot deg$$

$$|VA2_{pmu7}| = 274.903 \cdot V \qquad \arg(VA2_{pmu7}) = 34.918 \cdot deg$$

- **PMU8 Voltage and Current Sequence Components**

$$\begin{pmatrix} IA0_{pmu8} \\ IA1_{pmu8} \\ IA2_{pmu8} \end{pmatrix} := A_{012}^{-1} \cdot \begin{pmatrix} IA_{pmu8} \\ IB_{pmu8} \\ IC_{pmu8} \end{pmatrix} \qquad \begin{pmatrix} VA0_{pmu8} \\ VA1_{pmu8} \\ VA2_{pmu8} \end{pmatrix} := A_{012}^{-1} \cdot \begin{pmatrix} VA_{pmu8} \\ VB_{pmu8} \\ VC_{pmu8} \end{pmatrix}$$

$$|IA0_{pmu8}| = 2.419 \times 10^{-3}\,A \qquad \arg(IA0_{pmu8}) = -108.456 \cdot deg$$

$$|IA1_{pmu8}| = 622.299\,A \qquad \arg(IA1_{pmu8}) = 78.088 \cdot deg$$

$$|IA2_{pmu8}| = 2.557\,A \qquad \arg(IA2_{pmu8}) = 124.594 \cdot deg$$

$$|VA0_{pmu8}| = 1.846 \times 10^{5} \cdot V \qquad \arg(VA0_{pmu8}) = 164.506 \cdot deg$$

$$|VA1_{pmu8}| = 1.846 \times 10^{5} \cdot V \qquad \arg(VA1_{pmu8}) = -75.483 \cdot deg$$

$$|VA2_{pmu8}| = 1.846 \times 10^{5} \cdot V \qquad \arg(VA2_{pmu8}) = -75.464 \cdot deg$$

- **SELECTING PMUS INVOLVED IN THE FAULTED LINE**

CURRENT NEGATIVE SEQUENCE

$$Ipos1 := \begin{cases} 1 & \text{if } |IA2_{pmu1}| = \max(|IA2_{pmu1}|, |IA2_{pmu2}|, |IA2_{pmu3}|, |IA2_{pmu4}|, |IA2_{pmu5}|, |IA2_{pmu6}|, \\ 0 & \text{otherwise} \end{cases}$$

$$Ipos2 := \begin{cases} 1 & \text{if } |IA2_{pmu2}| = \max(|IA2_{pmu1}|, |IA2_{pmu2}|, |IA2_{pmu3}|, |IA2_{pmu4}|, |IA2_{pmu5}|, |IA2_{pmu6}|, \\ 0 & \text{otherwise} \end{cases}$$

$$Ipos3 := \begin{cases} 1 & \text{if } |IA2_{pmu3}| = \max(|IA2_{pmu1}|, |IA2_{pmu2}|, |IA2_{pmu3}|, |IA2_{pmu4}|, |IA2_{pmu5}|, |IA2_{pmu6}|, \\ 0 & \text{otherwise} \end{cases}$$

$$Ipos4 := \begin{cases} 1 & \text{if } |IA2_{pmu4}| = \max(|IA2_{pmu1}|, |IA2_{pmu2}|, |IA2_{pmu3}|, |IA2_{pmu4}|, |IA2_{pmu5}|, |IA2_{pmu6}|, \\ 0 & \text{otherwise} \end{cases}$$

$$Ipos5 := \begin{cases} 1 & \text{if } |IA2_{pmu5}| = \max(|IA2_{pmu1}|, |IA2_{pmu2}|, |IA2_{pmu3}|, |IA2_{pmu4}|, |IA2_{pmu5}|, |IA2_{pmu6}|, \\ 0 & \text{otherwise} \end{cases}$$

$$Ipos6 := \begin{cases} 1 & \text{if } |IA2_{pmu6}| = \max(|IA2_{pmu1}|, |IA2_{pmu2}|, |IA2_{pmu3}|, |IA2_{pmu4}|, |IA2_{pmu5}|, |IA2_{pmu6}|, \\ 0 & \text{otherwise} \end{cases}$$

$$Ipos7 := \begin{cases} 1 & \text{if } |IA2_{pmu7}| = \max(|IA2_{pmu1}|, |IA2_{pmu2}|, |IA2_{pmu3}|, |IA2_{pmu4}|, |IA2_{pmu5}|, |IA2_{pmu6}|, \\ 0 & \text{otherwise} \end{cases}$$

$$Ipos8 := \begin{cases} 1 & \text{if } |IA2_{pmu8}| = \max(|IA2_{pmu1}|, |IA2_{pmu2}|, |IA2_{pmu3}|, |IA2_{pmu4}|, |IA2_{pmu5}|, |IA2_{pmu6}|, \\ 0 & \text{otherwise} \end{cases}$$

$Ipos1 = 0$ $Ipos2 = 0$ $Ipos3 = 1$ $Ipos4 = 0$

$Ipos5 = 0$ $Ipos6 = 0$ $Ipos7 = 0$ $Ipos8 = 0$

VOLTAGE SEQUENCES

A PHASE VOLTAGE

$$VAPH_{pmu1} := \begin{cases} 1 & \text{if } |VA_{pmu1}| = \min(|VA_{pmu1}|, |VA_{pmu2}|, |VA_{pmu3}|, |VA_{pmu4}|, |VA_{pmu5}|, |VA_{pm} \\ 0 & \text{otherwise} \end{cases}$$

$$VAPH_{pmu2} := \begin{cases} 1 & \text{if } |VA_{pmu2}| = \min(|VA_{pmu1}|, |VA_{pmu2}|, |VA_{pmu3}|, |VA_{pmu4}|, |VA_{pmu5}|, |VA_{pm} \\ 0 & \text{otherwise} \end{cases}$$

$$VAPH_{pmu3} := \begin{cases} 1 & \text{if } |VA_{pmu3}| = \min(|VA_{pmu1}|, |VA_{pmu2}|, |VA_{pmu3}|, |VA_{pmu4}|, |VA_{pmu5}|, |VA_{pm} \\ 0 & \text{otherwise} \end{cases}$$

$$VAPH_{pmu4} := \begin{cases} 1 & \text{if } |VA_{pmu4}| = \min(|VA_{pmu1}|, |VA_{pmu2}|, |VA_{pmu3}|, |VA_{pmu4}|, |VA_{pmu5}|, |VA_{pm} \\ 0 & \text{otherwise} \end{cases}$$

$$VAPH_{pmu5} := \begin{cases} 1 & \text{if } |VA_{pmu5}| = \min(|VA_{pmu1}|, |VA_{pmu2}|, |VA_{pmu3}|, |VA_{pmu4}|, |VA_{pmu5}|, |VA_{pm} \\ 0 & \text{otherwise} \end{cases}$$

$$VAPH_{pmu6} := \begin{cases} 1 & \text{if } |VA_{pmu6}| = \min(|VA_{pmu1}|, |VA_{pmu2}|, |VA_{pmu3}|, |VA_{pmu4}|, |VA_{pmu5}|, |VA_{pm} \\ 0 & \text{otherwise} \end{cases}$$

$$VAPH_{pmu7} := \begin{cases} 1 & \text{if } |VA_{pmu7}| = \min(|VA_{pmu1}|, |VA_{pmu2}|, |VA_{pmu3}|, |VA_{pmu4}|, |VA_{pmu5}|, |VA_{pm} \\ 0 & \text{otherwise} \end{cases}$$

$$VAPH_{pmu8} := \begin{cases} 1 & \text{if } |VA_{pmu8}| = \min(|VA_{pmu1}|, |VA_{pmu2}|, |VA_{pmu3}|, |VA_{pmu4}|, |VA_{pmu5}|, |VA_{pm} \\ 0 & \text{otherwise} \end{cases}$$

B PHASE VOLTAGE

$$VBPH_{pmu1} := \begin{cases} 1 & \text{if } |VB_{pmu1}| = \min(|VB_{pmu1}|, |VB_{pmu2}|, |VB_{pmu3}|, |VB_{pmu4}|, |VB_{pmu5}|, |VB_{pm} \\ 0 & \text{otherwise} \end{cases}$$

$$VBPH_{pmu2} := \begin{cases} 1 & \text{if } |VB_{pmu2}| = \min(|VB_{pmu1}|, |VB_{pmu2}|, |VB_{pmu3}|, |VB_{pmu4}|, |VB_{pmu5}|, |VB_{pm} \\ 0 & \text{otherwise} \end{cases}$$

$$VBPH_{pmu3} := \begin{cases} 1 & \text{if } |VB_{pmu3}| = \min(|VB_{pmu1}|, |VB_{pmu2}|, |VB_{pmu3}|, |VB_{pmu4}|, |VB_{pmu5}|, |VB_{pm} \\ 0 & \text{otherwise} \end{cases}$$

$$VBPH_{pmu4} := \begin{cases} 1 & \text{if } |VB_{pmu4}| = \min(|VB_{pmu1}|, |VB_{pmu2}|, |VB_{pmu3}|, |VB_{pmu4}|, |VB_{pmu5}|, |VB_{pm} \\ 0 & \text{otherwise} \end{cases}$$

$$VBPH_{pmu5} := \begin{cases} 1 & \text{if } |VB_{pmu5}| = \min(|VB_{pmu1}|, |VB_{pmu2}|, |VB_{pmu3}|, |VB_{pmu4}|, |VB_{pmu5}|, |VB_{pm} \\ 0 & \text{otherwise} \end{cases}$$

$$VBPH_{pmu6} := \begin{cases} 1 & \text{if } |VB_{pmu6}| = \min(|VB_{pmu1}|, |VB_{pmu2}|, |VB_{pmu3}|, |VB_{pmu4}|, |VB_{pmu5}|, |VB_{pm} \\ 0 & \text{otherwise} \end{cases}$$

$$VBPH_{pmu7} := \begin{cases} 1 & \text{if } |VB_{pmu7}| = \min(|VB_{pmu1}|, |VB_{pmu2}|, |VB_{pmu3}|, |VB_{pmu4}|, |VB_{pmu5}|, |VB_{pm} \\ 0 & \text{otherwise} \end{cases}$$

$$VBPH_{pmu8} := \begin{cases} 1 & \text{if } |VB_{pmu8}| = \min(|VB_{pmu1}|, |VB_{pmu2}|, |VB_{pmu3}|, |VB_{pmu4}|, |VB_{pmu5}|, |VB_{pm} \\ 0 & \text{otherwise} \end{cases}$$

C PHASE VOLTAGE

$$VCPH_{pmu1} := \begin{cases} 1 & \text{if } |VC_{pmu1}| = \min(|VC_{pmu1}|, |VC_{pmu2}|, |VC_{pmu3}|, |VC_{pmu4}|, |VC_{pmu5}|, \\ 0 & \text{otherwise} \end{cases}$$

$$VCPH_{pmu2} := \begin{cases} 1 & \text{if } |VC_{pmu2}| = \min(|VC_{pmu1}|, |VC_{pmu2}|, |VC_{pmu3}|, |VC_{pmu4}|, |VC_{pmu5}|, \\ 0 & \text{otherwise} \end{cases}$$

$$VCPH_{pmu3} := \begin{cases} 1 & \text{if } |VC_{pmu3}| = \min(|VC_{pmu1}|, |VC_{pmu2}|, |VC_{pmu3}|, |VC_{pmu4}|, |VC_{pmu5}|, \\ 0 & \text{otherwise} \end{cases}$$

$$VCPH_{pmu4} := \begin{cases} 1 & \text{if } |VC_{pmu4}| = \min(|VC_{pmu1}|, |VC_{pmu2}|, |VC_{pmu3}|, |VC_{pmu4}|, |VC_{pmu5}|, \\ 0 & \text{otherwise} \end{cases}$$

$$VCPH_{pmu5} := \begin{cases} 1 & \text{if } |VC_{pmu5}| = \min(|VC_{pmu1}|, |VC_{pmu2}|, |VC_{pmu3}|, |VC_{pmu4}|, |VC_{pmu5}| \\ 0 & \text{otherwise} \end{cases}$$

$$VCPH_{pmu6} := \begin{cases} 1 & \text{if } |VC_{pmu6}| = \min(|VC_{pmu1}|, |VC_{pmu2}|, |VC_{pmu3}|, |VC_{pmu4}|, |VC_{pmu5}| \\ 0 & \text{otherwise} \end{cases}$$

$$VCPH_{pmu7} := \begin{cases} 1 & \text{if } |VC_{pmu7}| = \min(|VC_{pmu1}|, |VC_{pmu2}|, |VC_{pmu3}|, |VC_{pmu4}|, |VC_{pmu5}| \\ 0 & \text{otherwise} \end{cases}$$

$$VCPH_{pmu8} := \begin{cases} 1 & \text{if } |VC_{pmu8}| = \min(|VC_{pmu1}|, |VC_{pmu2}|, |VC_{pmu3}|, |VC_{pmu4}|, |VC_{pmu5}| \\ 0 & \text{otherwise} \end{cases}$$

$VAPH_{pmu1} = 0$ $VAPH_{pmu2} = 0$ $VAPH_{pmu3} = 1$ $VAPH_{pmu4} = 0$ $VAPH_{pmu5} = 0$

$VBPH_{pmu1} = 0$ $VBPH_{pmu2} = 1$ $VBPH_{pmu3} = 0$ $VBPH_{pmu4} = 0$ $VBPH_{pmu5} = 0$

$VCPH_{pmu1} = 0$ $VCPH_{pmu2} = 0$ $VCPH_{pmu3} = 1$ $VCPH_{pmu4} = 0$ $VCPH_{pmu5} = 0$

$$Vpos1 := \begin{cases} 1 & \text{if } \left(VAPH_{pmu1} = 1 \vee VBPH_{pmu1} = 1 \vee VCPH_{pmu1} = 1\right) \\ 0 & \text{otherwise} \end{cases}$$

$$Vpos2 := \begin{cases} 1 & \text{if } \left(VAPH_{pmu2} = 1 \vee VBPH_{pmu2} = 1 \vee VCPH_{pmu2} = 1\right) \\ 0 & \text{otherwise} \end{cases}$$

$$Vpos3 := \begin{cases} 1 & \text{if } \left(VAPH_{pmu3} = 1 \vee VBPH_{pmu3} = 1 \vee VCPH_{pmu3} = 1\right) \\ 0 & \text{otherwise} \end{cases}$$

$$Vpos4 := \begin{cases} 1 & \text{if } \left(VAPH_{pmu4} = 1 \vee VBPH_{pmu4} = 1 \vee VCPH_{pmu4} = 1\right) \\ 0 & \text{otherwise} \end{cases}$$

$$Vpos5 := \begin{cases} 1 & \text{if } \left(VAPH_{pmu5} = 1 \vee VBPH_{pmu5} = 1 \vee VCPH_{pmu5} = 1\right) \\ 0 & \text{otherwise} \end{cases}$$

$$Vpos6 := \begin{cases} 1 & \text{if } \left(VAPH_{pmu6} = 1 \vee VBPH_{pmu6} = 1 \vee VCPH_{pmu6} = 1\right) \\ 0 & \text{otherwise} \end{cases}$$

$$Vpos7 := \begin{cases} 1 & \text{if } \left(VAPH_{pmu7} = 1 \vee VBPH_{pmu7} = 1 \vee VCPH_{pmu7} = 1\right) \\ 0 & \text{otherwise} \end{cases}$$

$$Vpos8 := \begin{cases} 1 & \text{if } \left(VAPH_{pmu8} = 1 \vee VBPH_{pmu8} = 1 \vee VCPH_{pmu8} = 1\right) \\ 0 & \text{otherwise} \end{cases}$$

$Vpos1 = 0$ $Vpos2 = 1$ $Vpos3 = 1$ $Vpos4 = 0$

$Vpos5 = 0$ $Vpos6 = 0$ $Vpos7 = 0$ $Vpos8 = 0$

Directionality

Line 1

$$L1_{APH} := \left|\arg\left(IA_{pmu1}\right) - \arg\left(IA_{pmu2}\right)\right| = 179.803 \cdot deg$$

$$L1_{BPH} := \left|\arg\left(IB_{pmu1}\right) - \arg\left(IB_{pmu2}\right)\right| = 161.014 \cdot deg$$

$$L1_{CPH} := \left|\arg\left(IC_{pmu1}\right) - \arg\left(IC_{pmu2}\right)\right| = 184.41 \cdot deg$$

Line 2

$$L2_{APH} := \left|\arg\left(IA_{pmu3}\right) - \arg\left(IA_{pmu4}\right)\right| = 10.472 \cdot deg$$

$$L2_{BPH} := \left|\arg\left(IB_{pmu3}\right) - \arg\left(IB_{pmu4}\right)\right| = 198.351 \cdot deg$$

$$L2_{CPH} := \left|\arg\left(IC_{pmu3}\right) - \arg\left(IC_{pmu4}\right)\right| = 10.696 \cdot deg$$

Line 3

$$L3_{APH} := \left|\arg\left(IA_{pmu5}\right) - \arg\left(IA_{pmu6}\right)\right| = 132.55 \cdot deg$$

$$L3_{BPH} := \left|\arg\left(IB_{pmu5}\right) - \arg\left(IB_{pmu6}\right)\right| = 230.018 \cdot deg$$

$$L3_{CPH} := \left|\arg\left(IC_{pmu5}\right) - \arg\left(IC_{pmu6}\right)\right| = 134.164 \cdot deg$$

Line 4

$$L4_{APH} := \left|\arg\left(IA_{pmu7}\right) - \arg\left(IA_{pmu8}\right)\right| = 159.492 \cdot deg$$

$$L4_{BPH} := \left|\arg\left(IB_{pmu7}\right) - \arg\left(IB_{pmu8}\right)\right| = 200.578 \cdot deg$$

$$L4_{CPH} := \left|\arg\left(IC_{pmu7}\right) - \arg\left(IC_{pmu8}\right)\right| = 200.639 \cdot deg$$

$$Dir_{L1} := \begin{cases} 1 & \text{if } (L1_{APH} < 50deg \vee L1_{BPH} < 50deg \vee L1_{CPH} < 50deg) \\ 0 & \text{otherwise} \end{cases}$$

$$Dir_{L2} := \begin{cases} 1 & \text{if } (L2_{APH} < 50deg \vee L2_{BPH} < 50deg \vee L2_{CPH} < 50deg) \\ 0 & \text{otherwise} \end{cases}$$

$$Dir_{L3} := \begin{cases} 1 & \text{if } (L3_{APH} < 50deg \vee L3_{BPH} < 50deg \vee L3_{CPH} < 50deg) \\ 0 & \text{otherwise} \end{cases}$$

$$Dir_{L4} := \begin{cases} 1 & \text{if } (L4_{APH} < 50deg \vee L4_{BPH} < 50deg \vee L4_{CPH} < 50deg) \\ 0 & \text{otherwise} \end{cases}$$

$Dir_{L1} = 0$ $Dir_{L2} = 1$ $Dir_{L3} = 0$ $Dir_{L4} = 0$

$$LINE\_NAME := \begin{cases} out \leftarrow \text{"500kV MNL-RM 500kV \# 1"} \text{ if } [(Ipos1 = 1 \vee Ipos2 = 1) \vee (Vpos1 = 1 \vee Vpos2 \\ out \leftarrow \text{"500kV RM - TM \# 2"} \text{ if } [(Ipos3 = 1 \vee Ipos4 = 1) \vee (Vpos3 = 1 \vee Vpos4 = 1)] \\ out \leftarrow \text{"500kV GAT - LB \# 2"} \text{ if } [(Ipos5 = 1 \vee Ipos6 = 1) \vee (Vpos5 = 1 \vee Vpos6 = 1)] \\ out \leftarrow \text{"500kV VCN - MWY \# 1"} \text{ if } [(Ipos7 = 1 \vee Ipos8 = 1) \vee (Vpos7 = 1 \vee Vpos8 = \end{cases}$$

- **LOCAL (PMUX) AND REMOTE (PMUY) PMUS INVOLVED IN THE FAULT**

$$I012_{PMUX} := \begin{cases} \text{return} \begin{pmatrix} IA0_{pmu1} \\ IA1_{pmu1} \\ IA2_{pmu1} \end{pmatrix} & \text{if } Ipos1 = 1 \\ \text{return} \begin{pmatrix} IA0_{pmu2} \\ IA1_{pmu2} \\ IA2_{pmu2} \end{pmatrix} & \text{if } Ipos2 = 1 \\ \text{return} \begin{pmatrix} IA0_{pmu3} \\ IA1_{pmu3} \\ IA2_{pmu3} \end{pmatrix} & \text{if } Ipos3 = 1 \\ \text{return} \begin{pmatrix} IA0_{pmu4} \\ IA1_{pmu4} \\ IA2_{pmu4} \end{pmatrix} & \text{if } Ipos4 = 1 \\ \text{return} \begin{pmatrix} IA0_{pmu5} \\ IA1_{pmu5} \\ IA2_{pmu5} \end{pmatrix} & \text{if } Ipos5 = 1 \\ \text{return} \begin{pmatrix} IA0_{pmu6} \\ IA1_{pmu6} \\ IA2_{pmu6} \end{pmatrix} & \text{if } Ipos6 = 1 \\ \text{return} \begin{pmatrix} IA0_{pmu7} \\ IA1_{pmu7} \\ IA2_{pmu7} \end{pmatrix} & \text{if } Ipos7 = 1 \\ \text{return} \begin{pmatrix} IA0_{pmu8} \\ IA1_{pmu8} \\ IA2_{pmu8} \end{pmatrix} & \text{if } Ipos8 = 1 \end{cases}$$

$$I012_{PMUY} := \begin{cases} \text{return} \begin{pmatrix} IA0_{pmu2} \\ IA1_{pmu2} \\ IA2_{pmu2} \end{pmatrix} & \text{if } Ipos1 = 1 \\ \text{return} \begin{pmatrix} IA0_{pmu1} \\ IA1_{pmu1} \\ IA2_{pmu1} \end{pmatrix} & \text{if } Ipos2 = 1 \\ \text{return} \begin{pmatrix} IA0_{pmu4} \\ IA1_{pmu4} \\ IA2_{pmu4} \end{pmatrix} & \text{if } Ipos3 = 1 \\ \text{return} \begin{pmatrix} IA0_{pmu3} \\ IA1_{pmu3} \\ IA2_{pmu3} \end{pmatrix} & \text{if } Ipos4 = 1 \\ \text{return} \begin{pmatrix} IA0_{pmu6} \\ IA1_{pmu6} \\ IA2_{pmu6} \end{pmatrix} & \text{if } Ipos5 = 1 \\ \text{return} \begin{pmatrix} IA0_{pmu5} \\ IA1_{pmu5} \\ IA2_{pmu5} \end{pmatrix} & \text{if } Ipos6 = 1 \\ \text{return} \begin{pmatrix} IA0_{pmu8} \\ IA1_{pmu8} \\ IA2_{pmu8} \end{pmatrix} & \text{if } Ipos7 = 1 \\ \text{return} \begin{pmatrix} IA0_{pmu7} \\ IA1_{pmu7} \\ IA2_{pmu7} \end{pmatrix} & \text{if } Ipos8 = 1 \end{cases}$$

$$V012_{PMUX} := \begin{cases} \text{return} \begin{pmatrix} VA0_{pmu1} \\ VA1_{pmu1} \\ VA2_{pmu1} \end{pmatrix} & \text{if } Ipos1 = 1 \\ \text{return} \begin{pmatrix} VA0_{pmu2} \\ VA1_{pmu2} \\ VA2_{pmu2} \end{pmatrix} & \text{if } Ipos2 = 1 \\ \text{return} \begin{pmatrix} VA0_{pmu3} \\ VA1_{pmu3} \\ VA2_{pmu3} \end{pmatrix} & \text{if } Ipos3 = 1 \\ \text{return} \begin{pmatrix} VA0_{pmu4} \\ VA1_{pmu4} \\ VA2_{pmu4} \end{pmatrix} & \text{if } Ipos4 = 1 \\ \text{return} \begin{pmatrix} VA0_{pmu5} \\ VA1_{pmu5} \\ VA2_{pmu5} \end{pmatrix} & \text{if } Ipos5 = 1 \\ \text{return} \begin{pmatrix} VA0_{pmu6} \\ VA1_{pmu6} \\ VA2_{pmu6} \end{pmatrix} & \text{if } Ipos6 = 1 \\ \text{return} \begin{pmatrix} VA0_{pmu7} \\ VA1_{pmu7} \\ VA2_{pmu7} \end{pmatrix} & \text{if } Ipos7 = 1 \\ \text{return} \begin{pmatrix} VA0_{pmu8} \\ VA1_{pmu8} \\ VA2_{pmu8} \end{pmatrix} & \text{if } Ipos8 = 1 \end{cases}$$

$$V012_{PMUY} := \begin{cases} \text{return} \begin{pmatrix} VA0_{pmu2} \\ VA1_{pmu2} \\ VA2_{pmu2} \end{pmatrix} & \text{if } Ipos1 = 1 \\ \text{return} \begin{pmatrix} VA0_{pmu1} \\ VA1_{pmu1} \\ VA2_{pmu1} \end{pmatrix} & \text{if } Ipos2 = 1 \\ \text{return} \begin{pmatrix} VA0_{pmu4} \\ VA1_{pmu4} \\ VA2_{pmu4} \end{pmatrix} & \text{if } Ipos3 = 1 \\ \text{return} \begin{pmatrix} VA0_{pmu3} \\ VA1_{pmu3} \\ VA2_{pmu3} \end{pmatrix} & \text{if } Ipos4 = 1 \\ \text{return} \begin{pmatrix} VA0_{pmu6} \\ VA1_{pmu6} \\ VA2_{pmu6} \end{pmatrix} & \text{if } Ipos5 = 1 \\ \text{return} \begin{pmatrix} VA0_{pmu5} \\ VA1_{pmu5} \\ VA2_{pmu5} \end{pmatrix} & \text{if } Ipos6 = 1 \\ \text{return} \begin{pmatrix} VA0_{pmu8} \\ VA1_{pmu8} \\ VA2_{pmu8} \end{pmatrix} & \text{if } Ipos7 = 1 \\ \text{return} \begin{pmatrix} VA0_{pmu7} \\ VA1_{pmu7} \\ VA2_{pmu7} \end{pmatrix} & \text{if } Ipos8 = 1 \end{cases}$$

$$IABC_{PMUX} := \begin{cases} \text{return } \begin{pmatrix} IA_{pmu1} \\ IB_{pmu1} \\ IC_{pmu1} \end{pmatrix} & \text{if } Ipos1 = 1 \\ \text{return } \begin{pmatrix} IA_{pmu2} \\ IB_{pmu2} \\ IC_{pmu2} \end{pmatrix} & \text{if } Ipos2 = 1 \\ \text{return } \begin{pmatrix} IA_{pmu3} \\ IB_{pmu3} \\ IC_{pmu3} \end{pmatrix} & \text{if } Ipos3 = 1 \\ \text{return } \begin{pmatrix} IA_{pmu4} \\ IB_{pmu4} \\ IC_{pmu4} \end{pmatrix} & \text{if } Ipos4 = 1 \\ \text{return } \begin{pmatrix} IA_{pmu5} \\ IB_{pmu5} \\ IC_{pmu5} \end{pmatrix} & \text{if } Ipos5 = 1 \\ \text{return } \begin{pmatrix} IA_{pmu6} \\ IB_{pmu6} \\ IC_{pmu6} \end{pmatrix} & \text{if } Ipos6 = 1 \\ \text{return } \begin{pmatrix} IA_{pmu7} \\ IB_{pmu7} \\ IC_{pmu7} \end{pmatrix} & \text{if } Ipos7 = 1 \\ \text{return } \begin{pmatrix} IA_{pmu8} \\ IB_{pmu8} \\ IC_{pmu8} \end{pmatrix} & \text{if } Ipos8 = 1 \end{cases}$$

$$IABC_{PMUY} := \begin{cases} \text{return } \begin{pmatrix} IA_{pmu2} \\ IB_{pmu2} \\ IC_{pmu2} \end{pmatrix} & \text{if } Ipos1 = 1 \\ \text{return } \begin{pmatrix} IA_{pmu1} \\ IB_{pmu1} \\ IC_{pmu1} \end{pmatrix} & \text{if } Ipos2 = 1 \\ \text{return } \begin{pmatrix} IA_{pmu4} \\ IB_{pmu4} \\ IC_{pmu4} \end{pmatrix} & \text{if } Ipos3 = 1 \\ \text{return } \begin{pmatrix} IA_{pmu3} \\ IB_{pmu3} \\ IC_{pmu3} \end{pmatrix} & \text{if } Ipos4 = 1 \\ \text{return } \begin{pmatrix} IA_{pmu6} \\ IB_{pmu6} \\ IC_{pmu6} \end{pmatrix} & \text{if } Ipos5 = 1 \\ \text{return } \begin{pmatrix} IA_{pmu5} \\ IB_{pmu5} \\ IC_{pmu5} \end{pmatrix} & \text{if } Ipos6 = 1 \\ \text{return } \begin{pmatrix} IA_{pmu8} \\ IB_{pmu8} \\ IC_{pmu8} \end{pmatrix} & \text{if } Ipos7 = 1 \\ \text{return } \begin{pmatrix} IA_{pmu7} \\ IB_{pmu7} \\ IC_{pmu7} \end{pmatrix} & \text{if } Ipos8 = 1 \end{cases}$$

$$VABC_{PMUX} := \left| \begin{array}{ll} \text{return} \begin{pmatrix} VA_{pmu1} \\ VB_{pmu1} \\ VC_{pmu1} \end{pmatrix} & \text{if } Ipos1 = 1 \\ \text{return} \begin{pmatrix} VA_{pmu2} \\ VB_{pmu2} \\ VC_{pmu2} \end{pmatrix} & \text{if } Ipos2 = 1 \\ \text{return} \begin{pmatrix} VA_{pmu3} \\ VB_{pmu3} \\ VC_{pmu3} \end{pmatrix} & \text{if } Ipos3 = 1 \\ \text{return} \begin{pmatrix} VA_{pmu4} \\ VB_{pmu4} \\ VC_{pmu4} \end{pmatrix} & \text{if } Ipos4 = 1 \\ \text{return} \begin{pmatrix} VA_{pmu5} \\ VB_{pmu5} \\ VC_{pmu5} \end{pmatrix} & \text{if } Ipos5 = 1 \\ \text{return} \begin{pmatrix} VA_{pmu6} \\ VB_{pmu6} \\ VC_{pmu6} \end{pmatrix} & \text{if } Ipos6 = 1 \\ \text{return} \begin{pmatrix} VA_{pmu7} \\ VB_{pmu7} \\ VC_{pmu7} \end{pmatrix} & \text{if } Ipos7 = 1 \\ \text{return} \begin{pmatrix} VA_{pmu8} \\ VB_{pmu8} \\ VC_{pmu8} \end{pmatrix} & \text{if } Ipos8 = 1 \end{array} \right.$$

$$VABC_{PMUY} := \left| \begin{array}{ll} \text{return} \begin{pmatrix} VA_{pmu2} \\ VB_{pmu2} \\ VC_{pmu2} \end{pmatrix} & \text{if } Ipos1 = 1 \\ \text{return} \begin{pmatrix} VA_{pmu1} \\ VB_{pmu1} \\ VC_{pmu1} \end{pmatrix} & \text{if } Ipos2 = 1 \\ \text{return} \begin{pmatrix} VA_{pmu4} \\ VB_{pmu4} \\ VC_{pmu4} \end{pmatrix} & \text{if } Ipos3 = 1 \\ \text{return} \begin{pmatrix} VA_{pmu3} \\ VB_{pmu3} \\ VC_{pmu3} \end{pmatrix} & \text{if } Ipos4 = 1 \\ \text{return} \begin{pmatrix} VA_{pmu6} \\ VB_{pmu6} \\ VC_{pmu6} \end{pmatrix} & \text{if } Ipos5 = 1 \\ \text{return} \begin{pmatrix} VA_{pmu5} \\ VB_{pmu5} \\ VC_{pmu5} \end{pmatrix} & \text{if } Ipos6 = 1 \\ \text{return} \begin{pmatrix} VA_{pmu8} \\ VB_{pmu8} \\ VC_{pmu8} \end{pmatrix} & \text{if } Ipos7 = 1 \\ \text{return} \begin{pmatrix} VA_{pmu7} \\ VB_{pmu7} \\ VC_{pmu7} \end{pmatrix} & \text{if } Ipos8 = 1 \end{array} \right.$$

LOCAL ABC VOLTAGES AND CURRENTS OF THE FAULTED LINE

VOLTAGES

$$VABC_{PMUX} = \begin{pmatrix} 9.711 \times 10^4 - 1.658i \times 10^5 \\ -2.774 \times 10^5 + 1.173i \times 10^5 \\ 1.807 \times 10^5 + 4.91i \times 10^4 \end{pmatrix} \cdot V$$

A – PHASE $\left|VABC_{PMUX_0}\right| = 1.921 \times 10^5 \cdot V$

B – PHASE $\left|VABC_{PMUX_1}\right| = 3.012 \times 10^5 \cdot V$

C – PHASE $\left|VABC_{PMUX_2}\right| = 1.872 \times 10^5 \cdot V$

CURRENTS

$$IABC_{PMUX} = \begin{pmatrix} -9.435 \times 10^3 + 3.446i \times 10^3 \\ -593.627 + 143.921i \\ 1 \times 10^4 - 3.569i \times 10^3 \end{pmatrix} A$$

A – PHASE $\left|IABC_{PMUX_0}\right| = 1.004 \times 10^4 A$

B – PHASE $\left|IABC_{PMUX_1}\right| = 610.824 A$

C – PHASE $\left|IABC_{PMUX_2}\right| = 1.062 \times 10^4 A$

LOCAL 0,1,2 VOLTAGE AND CURRENT SEQUENCE COMPONENTS OF THE FAULTED LINE

VOLTAGES

$$V012_{PMUX} = \begin{pmatrix} 111.986 + 202.887i \\ 2.881 \times 10^4 - 2.152i \times 10^5 \\ 6.819 \times 10^4 + 4.924i \times 10^4 \end{pmatrix} \cdot V$$

ZERO SEQ $\left|V012_{PMUX_0}\right| = 231.741 \cdot V$

POS SEQ $\left|V012_{PMUX_1}\right| = 2.172 \times 10^5 \cdot V$

NEG SEQ $\left|V012_{PMUX_2}\right| = 8.411 \times 10^4 \cdot V$

CURRENTS

$$I012_{PMUX} = \begin{pmatrix} -9.529 + 6.939i \\ -5.785 \times 10^3 - 1.339i \times 10^3 \\ -3.641 \times 10^3 + 4.778i \times 10^3 \end{pmatrix} A$$

ZERO SEQ $\left|I012_{PMUX_0}\right| = 11.788\,A$

POS SEQ $\left|I012_{PMUX_1}\right| = 5.938 \times 10^3\,A$

NEG SEQ $\left|I012_{PMUX_2}\right| = 6.007 \times 10^3\,A$

REMOTE ABC VOLTAGES AND CURRENTS OF THE FAULTED LINE

VOLTAGES

$$VABC_{PMUY} = \begin{pmatrix} 4.565 \times 10^4 - 2.164i \times 10^5 \\ -2.636 \times 10^5 + 1.494i \times 10^5 \\ -2.268 \times 10^5 + 4.076i \times 10^4 \end{pmatrix} \cdot V$$

A – PHASE $\left|VABC_{PMUY_0}\right| = 2.212 \times 10^5 \cdot V$

B – PHASE $\left|VABC_{PMUY_1}\right| = 3.03 \times 10^5 \cdot V$

C – PHASE $\left|VABC_{PMUY_2}\right| = 2.304 \times 10^5 \cdot V$

CURRENTS

$$IABC_{PMUY} = \begin{pmatrix} -3.627 \times 10^3 + 2.139i \times 10^3 \\ 499.144 - 311.645i \\ 3.122 \times 10^3 - 1.827i \times 10^3 \end{pmatrix} A$$

A – PHASE $\left|IABC_{PMUY_0}\right| = 4.211 \times 10^3\,A$

B – PHASE $\left|IABC_{PMUY_1}\right| = 588.445\,A$

C – PHASE $\left|IABC_{PMUY_2}\right| = 3.617 \times 10^3\,A$

REMOTE 0,1 2 VOLTAGE AND CURRENT SEQUENCE COMPONENTS OF THE FAULTED LINE

VOLTAGES

$$V012_{PMUY} = \begin{pmatrix} -1.482 \times 10^5 - 8.731i \times 10^3 \\ 6.557 \times 10^4 - 1.145i \times 10^5 \\ 1.283 \times 10^5 - 9.321i \times 10^4 \end{pmatrix} \cdot V$$

ZERO SEQ $\left|V012_{PMUY_0}\right| = 1.485 \times 10^5 \cdot V$

POS SEQ $\left|V012_{PMUY_1}\right| = 1.319 \times 10^5 \cdot V$

NEG SEQ $\left|V012_{PMUY_2}\right| = 1.586 \times 10^5 \cdot V$

CURRENTS

$$I012_{PMUY} = \begin{pmatrix} -1.95 + 0.249i \\ -2.25 \times 10^3 + 312.446i \\ -1.375 \times 10^3 + 1.827i \times 10^3 \end{pmatrix} A$$

ZERO SEQ $\left|I012_{PMUY_0}\right| = 1.966\ A$

POS SEQ $\left|I012_{PMUY_1}\right| = 2.272 \times 10^3\ A$

NEG SEQ $\left|I012_{PMUY_2}\right| = 2.286 \times 10^3\ A$

- **POSITIVE AND ZERO SEQUENCE IMPEDANCES OF THE FAULTED LINE**

$$Z1_{line} := \begin{cases} \text{return } Z1_{line1} \text{ if } [(Ipos1 = 1 \vee Ipos2 = 1) \vee (Vpos1 = 1 \vee Vpos2 = 1)] \wedge (Dir_{L1} = 1) \\ \text{return } Z1_{line2} \text{ if } [(Ipos3 = 1 \vee Ipos4 = 1) \vee (Vpos3 = 1 \vee Vpos4 = 1)] \wedge (Dir_{L2} = 1) \\ \text{return } Z1_{line3} \text{ if } [(Ipos5 = 1 \vee Ipos6 = 1) \vee (Vpos5 = 1 \vee Vpos6 = 1)] \wedge (Dir_{L3} = 1) \\ \text{return } Z1_{line4} \text{ if } [(Ipos7 = 1 \vee Ipos8 = 1) \vee (Vpos7 = 1 \vee Vpos8 = 1)] \wedge (Dir_{L4} = 1) \end{cases}$$

$$Z0_{line} := \begin{cases} \text{return } Z0_{line1} \text{ if } [(Ipos1 = 1 \vee Ipos2 = 1) \vee (Vpos1 = 1 \vee Vpos2 = 1)] \wedge (Dir_{L1} = 1) \\ \text{return } Z0_{line2} \text{ if } [(Ipos3 = 1 \vee Ipos4 = 1) \vee (Vpos3 = 1 \vee Vpos4 = 1)] \wedge (Dir_{L2} = 1) \\ \text{return } Z0_{line3} \text{ if } [(Ipos5 = 1 \vee Ipos6 = 1) \vee (Vpos5 = 1 \vee Vpos6 = 1)] \wedge (Dir_{L3} = 1) \\ \text{return } Z0_{line4} \text{ if } [(Ipos7 = 1 \vee Ipos8 = 1) \vee (Vpos7 = 1 \vee Vpos8 = 1)] \wedge (Dir_{L4} = 1) \end{cases}$$

Positive Sequence Impedance

$$Z1_{line} = (2.425 + 54.175i) \cdot ohm$$

$$\left|Z1_{line}\right| = 54.229 \cdot ohm$$

$$\arg\left(Z1_{line}\right) = 87.437 \cdot deg$$

Zero Sequence Impedance

$$Z0_{line} = (23.8 + 157.35i) \cdot ohm$$

$$\left|Z0_{line}\right| = 159.14 \cdot ohm$$

$$\arg\left(Z0_{line}\right) = 81.399 \cdot deg$$

- **SELECTING TYPE OF FAULT USING LOCAL PMU (PMUX)**

$$\arg\left(I012_{PMUX_0}\right) = 143.937 \cdot \text{deg} \qquad \arg\left(I012_{PMUX_2}\right) = 127.311 \cdot \text{deg}$$

$$\theta_{0\_2} := \arg\left(I012_{PMUX_0}\right) - \arg\left(I012_{PMUX_2}\right) \qquad \theta_{0\_2} = 16.627 \cdot \text{deg}$$

$$I0\_I2ang := \begin{cases} \left(\theta_{0\_2} + 360\text{deg}\right) & \text{if } \theta_{0\_2} < -180\text{deg} \\ \left(\theta_{0\_2} - 360\text{deg}\right) & \text{if } \theta_{0\_2} > 180\text{deg} \\ \theta_{0\_2} & \text{otherwise} \end{cases}$$

$$I0\_I2ang = 16.627 \cdot \text{deg}$$

$$FSA := \begin{cases} 1 & \text{if } (-60\text{deg} \le I0\_I2ang \le 60\text{deg}) \\ 0 & \text{otherwise} \end{cases}$$

$$FSA = 1 \qquad \text{AG or BC or BCG}$$

$$FSB := \begin{cases} 1 & \text{if } (60\text{deg} \le I0\_I2ang \le 180\text{deg}) \\ 0 & \text{otherwise} \end{cases}$$

$$FSB = 0 \qquad \text{BG or CA or CAG}$$

$$FSC := \begin{cases} 1 & \text{if } (-180\text{deg} \le I0\_I2ang \le -60\text{deg}) \\ 0 & \text{otherwise} \end{cases}$$

$$FSC = 0 \qquad \text{CG or AB or ABG}$$

- **CALCULATION OF PHASE TO GROUND FAULT LOCATION USING LOCAL PMU (PMUX) AND REMOTE PMU (PMUY) DATA AND MULTI-ENDED FAULT LOCATION METHOD WITH TOTAL NEGATIVE SEQUENCE CURRENT**

$$I2Ta := I012_{PMUX_2} + I012_{PMUY_2}$$

$$I2Tb := a \cdot I2Ta$$

$$I2Tc := a^2 \cdot I2Ta$$

$$IG := 3 \cdot I012_{PMUX_0}$$

$$K_0 := \frac{Z0_{line} - Z1_{line}}{3 \cdot Z1_{line}} = 0.639 - 0.103i$$

$$mAG := \frac{Im\left(VABC_{PMUX_0} \cdot \overline{I2Ta}\right)}{Im\left[Z1_{line} \cdot \left(IABC_{PMUX_0} + K_0 \cdot IG\right) \cdot \overline{I2Ta}\right]} = 0.049$$

$$mBG := \frac{Im\left[VABC_{PMUX_1} \cdot \overline{(I2Tb)}\right]}{Im\left[Z1_{line1} \cdot \left(IABC_{PMUX_1} + K_0 \cdot IG\right) \cdot \overline{(I2Tb)}\right]} = -96.669$$

$$mCG := \frac{Im\left(VABC_{PMUX_2} \cdot \overline{I2Tc}\right)}{Im\left[Z1_{line1} \cdot \left(IABC_{PMUX_2} + K_0 \cdot IG\right) \cdot \overline{I2Tc}\right]} = 0.053$$

- **CALCULATION OF PHASE TO PHASE FAULT LOCATION USING LOCAL PMU (PMUX) AND REMOTE PMU (PMUY) DATA AND MULTI-ENDED FAULT LOCATION METHOD WITH TOTAL NEGATIVE SEQUENCE CURRENT**

LINE TO LINE PHASE VOLTAGES AND CURRENTS FROM LOCAL PMU (PMUX) OF THE FAULTED LINE

$$VAB_{PMUX} := VABC_{PMUX_0} = \left(9.711 \times 10^4 - 1.658i \times 10^5\right) \cdot V$$

$$VBC_{PMUX} := VABC_{PMUX_1} = \left(-2.774 \times 10^5 + 1.173i \times 10^5\right) \cdot V$$

$$VCA_{PMUX} := VABC_{PMUX_2} = \left(1.807 \times 10^5 + 4.91i \times 10^4\right) \cdot V$$

$$IAB_{PMUX} := IABC_{PMUX_0} = \left(-9.435 \times 10^3 + 3.446i \times 10^3\right) A$$

$$IBC_{PMUX} := IABC_{PMUX_1} = (-593.627 + 143.921i)\,A$$

$$ICA_{PMUX} := IABC_{PMUX_2} = \left(1 \times 10^4 - 3.569i \times 10^3\right) A$$

LINE TO LINE PHASE VOLTAGES AND CURRENTS FROM REMOTE PMU (PMUY) OF THE FAULTED LINE

$$VAB_{PMUY} := VABC_{PMUY_0} \cdot \sqrt{3} = \left(7.908 \times 10^4 - 3.748i \times 10^5\right) \cdot V$$

$$VBC_{PMUY} := VABC_{PMUY_1} \cdot \sqrt{3} = \left(-4.565 \times 10^5 + 2.588i \times 10^5\right) \cdot V$$

$$VCA_{PMUY} := VABC_{PMUY_2} \cdot \sqrt{3} = \left(-3.928 \times 10^5 + 7.06i \times 10^4\right) \cdot V$$

$$IAB_{PMUY} := IABC_{PMUY_0} = \left(-3.627 \times 10^3 + 2.139i \times 10^3\right) A$$

$$IBC_{PMUY} := IABC_{PMUY_1} = (499.144 - 311.645i)\,A$$

$$ICA_{PMUY} := IABC_{PMUY_2} = \left(3.122 \times 10^3 - 1.827i \times 10^3\right) A$$

$$mAB := \frac{Im\left[VAB_{PMUX} \cdot \overline{(j \cdot I2Tc)}\right]}{Im\left[Z1_{line} \cdot \left(IAB_{PMUX}\right) \cdot \overline{(j \cdot I2Tc)}\right]} = -0.279$$

$$mBC := \frac{Im\left[VBC_{PMUX} \cdot \overline{(j \cdot I2Ta)}\right]}{Im\left[Z1_{line} \cdot \left(IBC_{PMUX}\right) \cdot \overline{(j \cdot I2Ta)}\right]} = -13.229$$

$$mCA := \frac{Im\left[VCA_{PMUX} \cdot \overline{(j \cdot I2Tb)}\right]}{Im\left[Z1_{line} \cdot \left(ICA_{PMUX}\right) \cdot \overline{(j \cdot I2Tb)}\right]} = 0.2$$

- **CALCULATION OF 3 PHASE FAULT LOCATION USING LOCAL PMU (PMUX) AND REMOTE PMU (PMUY) DATA AND MULTI-ENDED FAULT LOCATION METHOD**

$$VA_{LG} := VABC_{PMUX_0} = \left(9.711 \times 10^4 - 1.658i \times 10^5\right) \cdot V$$

$$IA_L := IABC_{PMUX_0} = \left(-9.435 \times 10^3 + 3.446i \times 10^3\right) A$$

$$ITOTAL := IABC_{PMUX_0} + IABC_{PMUY_0}$$

$$m3P := \frac{Im\left[VA_{LG} \cdot \overline{(ITOTAL)}\right]}{Im\left[Z1_{line} \cdot \left(IA_L\right) \cdot \overline{(ITOTAL)}\right]} = 0.21$$

- **CALCULATION OF FAULT LOCATION USING NEGATIVE SEQUENCE LOCAL PMU (PMUX) AND REMOTE PMU (PMUY) DATA AND MULTI-ENDED FAULT LOCATION METHOD**

$$\text{Double\_End\_2} := \operatorname{Re}\left(\frac{V012_{PMUX_2} - V012_{PMUY_2} + I012_{PMUY_2}\cdot Z1_{line}}{I2Ta\cdot Z1_{line}}\right) = 0.206$$

$$\text{FAULT_TYPE} := \begin{cases}
\text{out} \leftarrow \text{"AG"} \text{ if } (FSA = 1 \wedge 0 < mAG < 1) \wedge \left(\left|IABC_{PMUX_0}\right| > \left|IABC_{PMUX_1}\right|\right) \wedge \left(\left|\right.\right. \\
\text{out} \leftarrow \text{"BG"} \text{ if } (FSB = 1 \wedge 0 < mBG < 1) \wedge \left(\left|IABC_{PMUX_1}\right| > \left|IABC_{PMUX_0}\right|\right) \wedge \left(\left|\right.\right. \\
\text{out} \leftarrow \text{"CG"} \text{ if } (FSC = 1 \wedge 0 < mCG < 1) \wedge \left(\left|IABC_{PMUX_2}\right| > \left|IABC_{PMUX_0}\right|\right) \wedge \left(\left|\right.\right. \\
\text{out} \leftarrow \text{"AB"} \text{ if } (FSC = 1 \vee 0 < mAB < 1) \wedge \left(\left|I012_{PMUX_0}\right| < 0.2\left|I012_{PMUX_1}\right|\right) \wedge \left(\\
\text{out} \leftarrow \text{"BC"} \text{ if } (FSA = 1 \vee 0 < mBC < 1) \wedge \left(\left|I012_{PMUX_0}\right| < 0.2\left|I012_{PMUX_1}\right|\right) \wedge \left(\\
\text{out} \leftarrow \text{"CA"} \text{ if } (FSB = 1 \vee 0 < mCA < 1) \wedge \left(\left|I012_{PMUX_0}\right| < 0.2\left|I012_{PMUX_1}\right|\right) \wedge \left(\\
\text{out} \leftarrow \text{"ABG"} \text{ if } FSC = 1 \wedge (0 < mAB < 1) \wedge \left[\left|I012_{PMUX_0}\right| > \left(0.2\left|I012_{PMUX_1}\right|\right)\right] \\
\text{out} \leftarrow \text{"BCG"} \text{ if } FSA = 1 \wedge (0 < mBC < 1) \wedge \left[\left|I012_{PMUX_0}\right| > \left(0.2\left|I012_{PMUX_1}\right|\right)\right] \\
\text{out} \leftarrow \text{"CAG"} \text{ if } \left[FSB = 1 \wedge (0 < mCA < 1) \wedge \left[\left|I012_{PMUX_0}\right| > \left(0.2\left|I012_{PMUX_1}\right|\right)\right.\right. \\
\text{out} \leftarrow \text{"ABC"} \text{ if } (0 < m3P < 1) \wedge \left[\left[\left|I012_{PMUX_0}\right| < \left(0.05\cdot\left|I012_{PMUX_1}\right|\right)\right] \vee \left[\left|I012\right.\right.
\end{cases}$$

$$\text{LINE_FAULT_PERCENTAGE} := \begin{cases}
\text{return (mAG)} \text{ if } (FSA = 1 \wedge 0 < mAG < 1) \wedge \left(\left|IABC_{PMUX_0}\right| > 2\right| \\
\text{return (mBG)} \text{ if } (FSB = 1 \wedge 0 < mBG < 1) \wedge \left(\left|IABC_{PMUX_1}\right| > 2\cdot \right. \\
\text{return (mCG)} \text{ if } (FSC = 1 \wedge 0 < mCG < 1) \wedge \left(\left|IABC_{PMUX_2}\right| > 2\cdot \right. \\
\text{return (mAB)} \text{ if } (0 < mAB < 1) \wedge \left|I012_{PMUX_2}\right| > 0.2\cdot\left|I012_{PMUX_1}\right. \\
\text{return (mBC)} \text{ if } (0 < mBC < 1) \wedge \left|I012_{PMUX_2}\right| > 0.2\cdot\left|I012_{PMUX_1}\right. \\
\text{return (mCA)} \text{ if } (0 < mCA < 1) \wedge \left|I012_{PMUX_2}\right| > 0.2\cdot\left|I012_{PMUX_1}\right. \\
\text{return (mAB)} \text{ if } (FSC = 1 \wedge 0 < mAB < 1) \wedge \left|I012_{PMUX_0}\right| > 0.2\left|I\right. \\
\text{return (mBC)} \text{ if } (FSA = 1 \wedge 0 < mBC < 1) \wedge \left|I012_{PMUX_0}\right| > 0.2\cdot \\
\text{return (mCA)} \text{ if } (FSB = 1 \wedge 0 < mCA < 1) \wedge \left|I012_{PMUX_0}\right| > 0.2\cdot \\
\text{return (m3P)} \text{ if } (0 < m3P < 1) \wedge \left(\left|I012_{PMUX_0}\right| < 0.1\left|I012_{PMUX_1}\right|\right)
\end{cases}$$

$DISTANCE_{miles} := LINE\_FAULT\_PERCENTAGE \cdot LL_{line1\_miles}$

NEG_SEQ_PERCENTAGE:= Double_End_2

$NEG\_SEQ\_DISTANCE_{miles} := Double\_End\_2 \cdot LL_{line1\_miles}$

- **RESULTS**

LINE_NAME = "500kV RM - TM # 2"

FAULT_TYPE= "CA"

LINE_FAULT_PERCENTAGE= 20.013 · % NEG_SEQ_PERCENTAGE= 20.557 · %

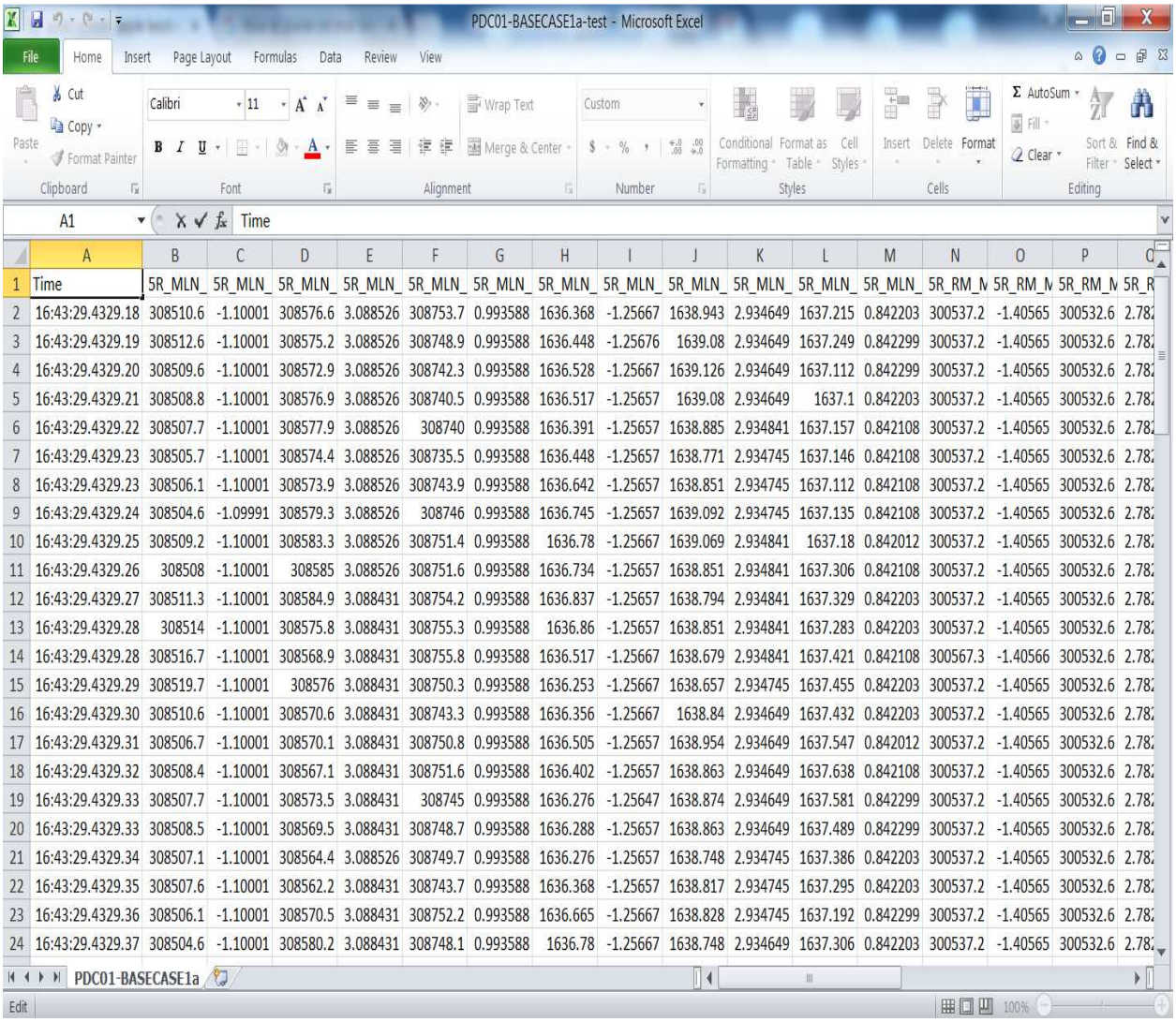
$DISTANCE_{miles}$ = 18.896 miles $NEG\_SEQ\_DISTANCE_{miles}$ = 19.41 miles

Notes:

LINE_FAULT_PERCENTAGE result shows the fault calculation in line percentage using the Modified Takagi Fault Impedance method. NEG_SEQ_PERCENTAGE result shows the fault calculation in line percentage using Negative Sequence Fault Impedance method.

Appendix B: Synchrophasor Data Format

Synchrophasor data was downloaded in the Microsoft Excel format from the Phasor Data Concentrator (PDC) and then run through the thesis fault location algorithm in MathCAD to obtain the calculated fault location. Each Microsoft Excel data row represents one PMU frame with the following column information: time, Va, Vb, Vc, Ia, Ib and Ic for each PMU. See the figure below.



	A	B	C	D	E	F	G	H	I	J	K	L	M	N	O	P	Q
1	Time	5R_MLN_	5R_MLN_	5R_MLN_	5R_MLN_	5R_MLN_	5R_MLN_	5R_MLN_	5R_MLN_	5R_MLN_	5R_MLN_	5R_MLN_	5R_MLN_	5R_RM_M	5R_RM_M	5R_RM_M	5R_R
2	16:43:29.4329.18	308510.6	-1.10001	308576.6	3.088526	308753.7	0.993588	1636.368	-1.25667	1638.943	2.934649	1637.215	0.842203	300537.2	-1.40565	300532.6	2.782
3	16:43:29.4329.19	308512.6	-1.10001	308575.2	3.088526	308748.9	0.993588	1636.448	-1.25676	1639.08	2.934649	1637.249	0.842299	300537.2	-1.40565	300532.6	2.782
4	16:43:29.4329.20	308509.6	-1.10001	308572.9	3.088526	308742.3	0.993588	1636.528	-1.25667	1639.126	2.934649	1637.112	0.842299	300537.2	-1.40565	300532.6	2.782
5	16:43:29.4329.21	308508.8	-1.10001	308576.9	3.088526	308740.5	0.993588	1636.517	-1.25657	1639.08	2.934649	1637.1	0.842203	300537.2	-1.40565	300532.6	2.782
6	16:43:29.4329.22	308507.7	-1.10001	308577.9	3.088526	308740	0.993588	1636.391	-1.25657	1638.885	2.934841	1637.157	0.842108	300537.2	-1.40565	300532.6	2.782
7	16:43:29.4329.23	308505.7	-1.10001	308574.4	3.088526	308735.5	0.993588	1636.448	-1.25657	1638.771	2.934745	1637.146	0.842108	300537.2	-1.40565	300532.6	2.782
8	16:43:29.4329.23	308506.1	-1.10001	308573.9	3.088526	308743.9	0.993588	1636.642	-1.25657	1638.851	2.934745	1637.112	0.842108	300537.2	-1.40565	300532.6	2.782
9	16:43:29.4329.24	308504.6	-1.09991	308579.3	3.088526	308746	0.993588	1636.745	-1.25657	1639.092	2.934745	1637.135	0.842108	300537.2	-1.40565	300532.6	2.782
10	16:43:29.4329.25	308509.2	-1.10001	308583.3	3.088526	308751.4	0.993588	1636.78	-1.25667	1639.069	2.934841	1637.18	0.842012	300537.2	-1.40565	300532.6	2.782
11	16:43:29.4329.26	308508	-1.10001	308585	3.088526	308751.6	0.993588	1636.734	-1.25657	1638.851	2.934841	1637.306	0.842108	300537.2	-1.40565	300532.6	2.782
12	16:43:29.4329.27	308511.3	-1.10001	308584.9	3.088431	308754.2	0.993588	1636.837	-1.25657	1638.794	2.934841	1637.329	0.842203	300537.2	-1.40565	300532.6	2.782
13	16:43:29.4329.28	308514	-1.10001	308575.8	3.088431	308755.3	0.993588	1636.86	-1.25657	1638.851	2.934841	1637.283	0.842203	300537.2	-1.40565	300532.6	2.782
14	16:43:29.4329.28	308516.7	-1.10001	308568.9	3.088431	308755.8	0.993588	1636.517	-1.25667	1638.679	2.934841	1637.421	0.842108	300567.3	-1.40566	300532.6	2.782
15	16:43:29.4329.29	308519.7	-1.10001	308576	3.088431	308750.3	0.993588	1636.253	-1.25667	1638.657	2.934745	1637.455	0.842203	300537.2	-1.40565	300532.6	2.782
16	16:43:29.4329.30	308510.6	-1.10001	308570.6	3.088431	308743.3	0.993588	1636.356	-1.25667	1638.84	2.934649	1637.432	0.842203	300537.2	-1.40565	300532.6	2.782
17	16:43:29.4329.31	308506.7	-1.10001	308570.1	3.088431	308750.8	0.993588	1636.505	-1.25657	1638.954	2.934649	1637.547	0.842012	300537.2	-1.40565	300532.6	2.782
18	16:43:29.4329.32	308508.4	-1.10001	308567.1	3.088431	308751.6	0.993588	1636.402	-1.25657	1638.863	2.934649	1637.638	0.842108	300537.2	-1.40565	300532.6	2.782
19	16:43:29.4329.33	308507.7	-1.10001	308573.5	3.088431	308745	0.993588	1636.276	-1.25647	1638.874	2.934649	1637.581	0.842299	300537.2	-1.40565	300532.6	2.782
20	16:43:29.4329.33	308508.5	-1.10001	308569.5	3.088431	308748.7	0.993588	1636.288	-1.25657	1638.863	2.934649	1637.489	0.842299	300537.2	-1.40565	300532.6	2.782
21	16:43:29.4329.34	308507.1	-1.10001	308564.4	3.088526	308749.7	0.993588	1636.276	-1.25657	1638.748	2.934745	1637.386	0.842203	300537.2	-1.40565	300532.6	2.782
22	16:43:29.4329.35	308507.6	-1.10001	308562.2	3.088431	308743.7	0.993588	1636.368	-1.25657	1638.817	2.934745	1637.295	0.842203	300537.2	-1.40565	300532.6	2.782
23	16:43:29.4329.36	308506.1	-1.10001	308570.5	3.088431	308752.2	0.993588	1636.665	-1.25667	1638.828	2.934745	1637.192	0.842299	300537.2	-1.40565	300532.6	2.782
24	16:43:29.4329.37	308504.6	-1.10001	308580.2	3.088431	308748.1	0.993588	1636.78	-1.25667	1638.748	2.934649	1637.306	0.842203	300537.2	-1.40565	300532.6	2.782

Figure 2 – Synchrophasor Data

Appendix C: Synchrophasor Frame Organization

Table C.1: Detailed Data Frame Organization

No.	Field	Size(bytes)	Comments
1	SYNC	2	Sync word provides synchronization and frame identification First byte: AA HEX Second byte: frame type and version, divided as follows: Bit 7: must be 0 for this version Bits 6-4: 000: Data Frame type 001: Header Frame 010: Configuration Frame 1 011: Configuration Frame 2 101: Configuration Frame 3 100: Command Frame (received message) Bits 3-0: Version Number, in binary (1-15) Version 1 (0001) for messages defined in IEEE C37.118-2005 Version 2 (0010) for messages added in IEEE C37.118-2011
2	FRAMESIZE	2	Number of bytes in frame 16-bit unsigned number Range = maximum 65535
3	IDCODE	2	PMU/PDC stream source ID number. This identifies the destination data stream for commands and source data stream for other messages. A stream will be hosted by a device that can be physical or virtual. If a device only hosts one data stream, the IDCODE identifies the device as well as the data stream. If a device hosts more than one data stream, it will be different IDCODE for each stream. Data stream ID number 16-bit integer (1- 65534)
4	SOC	4	Second of Century Time stamp, 32-bit unsigned number SOC count start at midnight 01-jan-1970 (UNIX base time) Range is 136 years, rolls over after 2106 AD Leap seconds are not counted in count, so each year has the same number of seconds except leap years, which have an extra day (84600 sec)
5	FRASEC	4	Fraction of Second and Time Quality, time of measurement for data frames or time of frames transmission for non-data frames. The time of measurement or data transmission for non-data frames is the SOC time stamp, which fixes the integer second plus fractional time. The fractional time is determined by dividing the 24-bit integer FRACSEC by the TIME_BASE integer given in configuration frame. Time = SOC + FRASEC / TIME_BASE. When divided by TIME_BASE yields the actual fractional second. FRACSEC used in all messages to and from given PMU shall use the same TIME_BASE provided that it is provided in the configuration message from that PMU. Time Quality indicates the quality of the time being reported as well as the indication of leap second status. FRACSEC is divided into two components: Time Quality Bits 31-24: Message Time Quality Flag Bit 7: Reserved Bit 6: Leap Second Direction – 0 for add, 1 for delete Bit 5: Leap Second Occurred – set in the first second after the leap second occurs and remains set for 24 h Bit 4: Leap Second Pending – shall be set not more than 60s Nor less than 1 s before a leap second occurs and cleared in the second after the leap second occurs Bit 3-0: Message Time Quality indicator for maximum time error. 0000 normal operation, clock looked to UTC

			traceable source. 1111 fault – clock failure, time not reliable. Anything between 0000 and 1111 indicates time deviation from UTC. Fraction of Second Bits 23-00: FRACSEC, 24-bit integer number
6	STAT	2	Bit-mapped flags Bit 15-14: Data error indicator 00 = good measurement data, no errors 01 = PMU error. No information about data 10 = PMU in test mode or absent data tags inserted (do not use values) 11 = PMU error. (do not use values) Bit 13: PMU sync. 0 when in sync with a UTC traceable time source Bit 12: Data sorting, 0 by time stamp, 1 by arrival Bit 11: PMU trigger detected. 0 when no trigger Bit 10: Configuration change Set 1 for 1 min to advise configuration change Clear to 0 when change effected Bit 9: Data modified, 1 if data modified by post processing, 0 otherwise Bit 08-06: PMU Time Quality Bit 05-04: Unlock time 00 = sync locked or unlocked < 10 s (best quality) 01 = 10 s < unlocked time < 100 s 10 = 100 < unlock time < 1000 s 11 = unlocked time > 1000 s Bit 03-00: Trigger reason 1111-1000: Available for user definition 0111: Digital 0101: df/dt 0011: Phase angle difference 0001: Magnitude low 0110: Reserved 0100: Frequency high or low 0010: Magnitude high 0000: Manual
7	PHASORS	4xPHNMR or 8xPHNMR	Phasor estimates. Data type indicated by FORMAT field in configuration 1, 2, and 3 frames Rectangular format (16-bit integer values): - real and imaginary, real value first - 16-bit signed integer, range -32 767 to +32 767 Polar format (16-bit integer value): -magnitude and angle, magnitude first -magnitude 16-bit unsigned integer range 0 to 65535 -angle 16-bit signed integer, in radiansx10^4, range -31 416 to +31 416 32-bit values in IEEE floating-point format: Rectangular format: -real and imaginary, in engineering units, real value first Polar format -magnitude and angle, magnitude first and in engineering units -angle in radians, range –π to +π
8	FREQ	2/4	Frequency deviation from nominal, in mHz Data type indicated by the FORMAT field in configuration 1, 2, and 3 frames Range-nominal (50Hz or 60Hz) -32.767 to +32.767 16-bit integer; 16-bit signed integers, range -32 767 to +32 767 32-bit integer floating point: actual frequency value in IEEE format
9	DFREQ	2/4	ROCOF, in Hertz per second times 100 Data type indicated by the FORMAT field in configuration 1, 2, and 3 frames Range - 327.67 to + +327.67 Hz per second

			16-bit integer or IEEE 32-bit integer floating point
10	ANALOG	2xANNMR or 4xNNMR	Analog word. Values and ranges defined by the user. It could be sample data such as control signal or transducer value. Data type indicated by the FORMAT field in configuration 1, 2, and 3 frames. 16-bit integer or IEEE floating point
11	DIGITAL	2xDGNMR	Digital Status word. It is a bit mapped as status or flag. Values are defined by user.
	Repeat 6 to 11		Fields 6 to 11 are repeated for as many PMUs as in NUM_PMU field in configuration frame.
12+	CHK	2	CRC-CCTITT. 16-bit unsigned integer CRC-CCITT uses the generating polynomial X^16+X^12+X^5+1 with an initial value of -1 (hex FFFF) and no final mask

Table C.2: Detailed Configuration Frame CFG-1 and CFG-2 Organization

No	Field	Size (bytes)	Comments
1	SYNC	2	First byte: AA hex Second byte: 21 hex for configuration 1 31 hex for configuration 2 Both frames are version 1 (IEEE C37.118-2005)
2	FRAMESIZE	2	Same as FRAMESIZE field in the data Frame
3	IDCODE	2	Same as IDCODE field in the Data Frame
4	SOC	4	Same as SOC field in the Data Frame
5	FRACSEC	4	Same as FRACSEC field in the data frame
6	TIME_BASE	4	Resolution of the fractional second time stamp (FREASEC) in all frames Bits: 31-24: Reserved for flags (high 8-bits) Bits 23-0: 24-bit unsigned integer The actual “fractional second of the data frame” = FRASEC / TIME_BASE
7	NUM_PMU	2	The number of PMU included in the frame. Limit of 65535 bytes in one frame per FRAMESIZE field
8	STN	16	Station name - 16 bytes in ASCII format
9	IDCODE	2	Data stream ID number identifies source of each block. Specifically identifies the data stream in field 3 and the data source in field 9
10	FORMAT	2	Data format in data frames. 16-bit flag Bits 15-4: Unused Bit 3: 0 = FREQ/DFREQ 16-bit integer, 1 = floating point Bit 2: 0 = analogs 16-bit integer, 1 = floating point Bit 1: 0 = phasors 16-bit integer, 1 = floating point Bit 0: 0 = phasor real and imaginary (rectangular), 1 = magnitude and angle (polar)
11	PHNMR	2	Number of phasors – 2 byte integer
12	ANNMR	2	Number of analog values – 2 byte integer
13	DGNMR	2	Number of digital status words – 2 byte integer. Digital status words are normally 16-bit Boolean numbers with each bit representing a digital status channel measured by a PMU
14	CHNAM	16x(PHNAM+ ANNMR+ 16xDGNMR)	Phasor and channel names 16 bytes for each phasor, analog and each digital channel (16 channels in each digital word) in ASCII format in the same order as they are transmitted. For digital channels, the channel name order will be from the least significant to the most significant.
15	PHUNIT	4xPHNMR	Conversion factor for phasor channels. 4 bytes for each phasor. Most significant byte: 0 – voltage, 1 – Current Least significant byte: An unsigned 24-bit word in 10^-5 Volts or

			Amps per bit to scale 16-bit integer
16	ANUNIT	4xANNMR	Conversion factor for analog channels. 4 bytes for analog value. Most significant byte: 0 – single point on the wave, 1 - rms of analog Input, 2 - peak of analog input, 5-65 – reserved for future definition Least significant byte: A signed 24-bit word
17	DIGUNIT	4xDGNMR	Mask words for status words. Two 16-bit words are provided foreach digital word. First word indicates normal status of the digital status Second word indicates the current valid inputs to the PMU
18	FNOM	2	Nominal line frequency code (16-bit unsigned integer) Bits 15-1: Reserved Bit 0: 1 – Fundamental frequency at 50Hz 0 – Fundamental frequency at 60Hz
19	CFGCNT	2	Configuration change count. Incremented each time a change is made in the PMU configuration.
		Repeat 8-19	Fields 8 to 19 are repeated for as many PMUs as in NUM_PMU field in configuration frame.
20	DATA_RATE	2	Rate of data transmission If DATA_RATE > 0, rate is number of frames per second If DATA_RATE < 0, rate is negative seconds per frame
21	CHK	2	CRC-CCITT same as in the Data Frame

Table C.3: Detailed Configuration Frame CFG-3 Organization

No	Field	Size (bytes)	Comments
1	SYNC	2	First byte: AA hex Second byte: 52 hex for configuration 3 Frame is version 2 (IEEE std. C37.118-2011)
2	FRAMESIZE	2	Same as FRAMESIZE field in Data Frame
3	IDCODE	2	Same as IDCODE field in Data Frame
4	SOC	4	Same as SOC field in Data Frame
5	FRACSEC	4	Same as FRACSEC field in Data Frame
6	CONT_IDX	2	Continuation index for fragmented frames: 0: only frame in configuration, no further frames 1: first frame in series, more to follow 2-65534: number of each succeeding frame, in order 65534 (hex FFFF): last frame in series
7	TIME_BASE	4	Same as TIME_BASE field in configuration 1 and 2 frame
8	NUM_PMU	2	Same as NUM_PMU field in configuration 1 and 2 frame
9	STN	1-256	Station name – in UTF-8 format, up to 255 bytes
10	IDCODE	2	Same as IDCODE field in configuration 1 and 2 frame
11	G_PMU_ID	16	128-bit PMU ID. It allows uniquely identifying PMUs in a system that has more than 65535 PMUs
12	FORMAT	2	Same as FORMAT field in configuration 1 and 2 frame
13	PHNMR	2	Same as PHNMR field in configuration 1 and 2 frame
14	ANNMR	2	Same as ANNMR field in configuration 1 and 2 frame
15	DGNMR	2	Same as DGNMR field in configuration 1 and 2 frame
16	CHNAM	1-256 per Name	Channel names One name for each phasor, analog, and digital channel in UTC-8 Names appear in the same order as they are transmitted: All phasor followed by all analogs followed by all digitals For digitals, the orders is the same as the configuration 1 and 2 frames
17	PHSCALE	12xPHNMR	Magnitude and angle scaling for phasor with data flags. This has three 4-byte long words.

			First byte word: bit mapped flags Second byte: magnitude scale factor Bit 0: No used reserved Bit 1: Up sampled with interpolation Bit 2: Up sampled with extrapolation Bit 3: Down sampled by reselection Bit 4: Down sampled with FIR filter Bit 5: Down sampled with non-FIR filter Bit 6: Filtered without changing sampling Bit 7: Phasor magnitude adjusted for calibration Bit 8: Phasor phase adjusted for calibration Bit 9: Phasor adjusted for rotation Bit 10: Pseudo-phasor value Bit 11-14: Reserved for future assignment Bit 15: Modification applied Third byte: phasor type indication Bits 07-04: Reserved for future use Bit 03: 0 – voltage; 1 – current Bits 02-00: Phasor component code 111: Reserved 110: Phase C 101: Phase B 100: Phase A 011: Reserved 010: Negative Sequence 001: Positive Sequence 000: Zero Sequence
18	ANSCALE	8xANNMR	Linear scaling for Analog channels. For analog value X, this defines scale M and offset B for X'=M x X + B
19	DIGUNIT	4xDGNMR	Same as DIGUNIT field in configuration 1 and 2 frames
20	PMU_LAT	4	PMU latitude in degrees, range -90 to +90 Positive values are N of equator. WGS 84 datum
21	PMU_LON	4	PMU longitude in degrees, range -179.9999 to +180 Positive values are E of prime meridian. WGS 84 datum
22	PMU_ELEV	4	PMU Elevation in meters Positive values are above mean sea level. WGS 84 datum
23	SVC_CLASS	1	Service class M or P. A single ASCII character
24	WINDOW	4	Phasor measurement window length including all filters and estimation windows in effect
25	GRP_DLY	4	Phasor measurement group delay including all filters and estimation windows in effect
26	FNOM	2	Same as FNOM field in configuration 1 and 2 frames
27	CFGCNT	2	Same as CFGCNT field in configuration 1 and 2 frames
	Repeat 9-27		Fields 9 to 27 are repeated for as many PMUs as in NUM_PMU field in configuration frame.
28	DATA_RATE	2	Same as DATA_RATE field in configuration 1 and 2 frames
29	CHK	2	Same as CHK field in data frame

Table C.4: Detailed Header Frame Message Organization

No	Field	Size (bytes)	Comments
1	SYNC	2	Sync byte followed by frame type and version number (AA11 hex)
2	FRAMESIZE	2	Same as FRAMESIZE field in data frame
3	IDCODE	2	Same as IDCODE field in data frame
4	SOC	4	Same as SOC field in data frame
5	FRACSEC	4	Same as FRACSEC field in data frame
6	DATA 1	1	ASCII character, first byte
K+6	DATA K	1	ASCII character, kth byte, K > 0 is an integer
K+7	CHK	2	Same as CHK field in data frame

Table C.5: Detailed Command Frame Message Organization

No	Field	Size (bytes)	Comments
1	SYNC	2	Sync byte followed by frame type and version number (AA41 hex)
2	FRAMESIZE	2	Same as FRAMESIZE field in data frame
3	IDCODE	2	Same as IDCODE field in data frame
4	SOC	4	Same as SOC field in data frame
5	FRACSEC	4	Same as FRACSEC field in data frame
6	CMD	2	Command being send to PMU/PDC (0) Bit 15-0: 0000 0000 0000 0001 – Turn off transmission of data frames 0000 0000 0000 0001 – Turn off transmission of data frames 0000 0000 0000 0010 – Turn on transmission of data frames 0000 0000 0000 0011 – Send header frame 0000 0000 0000 0100 – Send configuration 1 frame 0000 0000 0000 0101 – Send configuration 2 frame 0000 0000 0000 0110 – Send configuration 3 frame (optional) 0000 0000 0000 1000 – Extended frame 0000 0000 xxxx xxxx – All undersigned codes reserved 0000 yyyy xxxx xxxx – All codes where yyyy ≠ 0 available for user designation zzzz xxxx xxxx xxxx – All codes where zzzz ≠ 0 reserved
7	EXTFRAME	0-65518	Extended frame data, 16-bit words
8	CHK	2	Same as CHK field in data frame

Appendix D: 500 kV Test System (Only lines used for thesis)

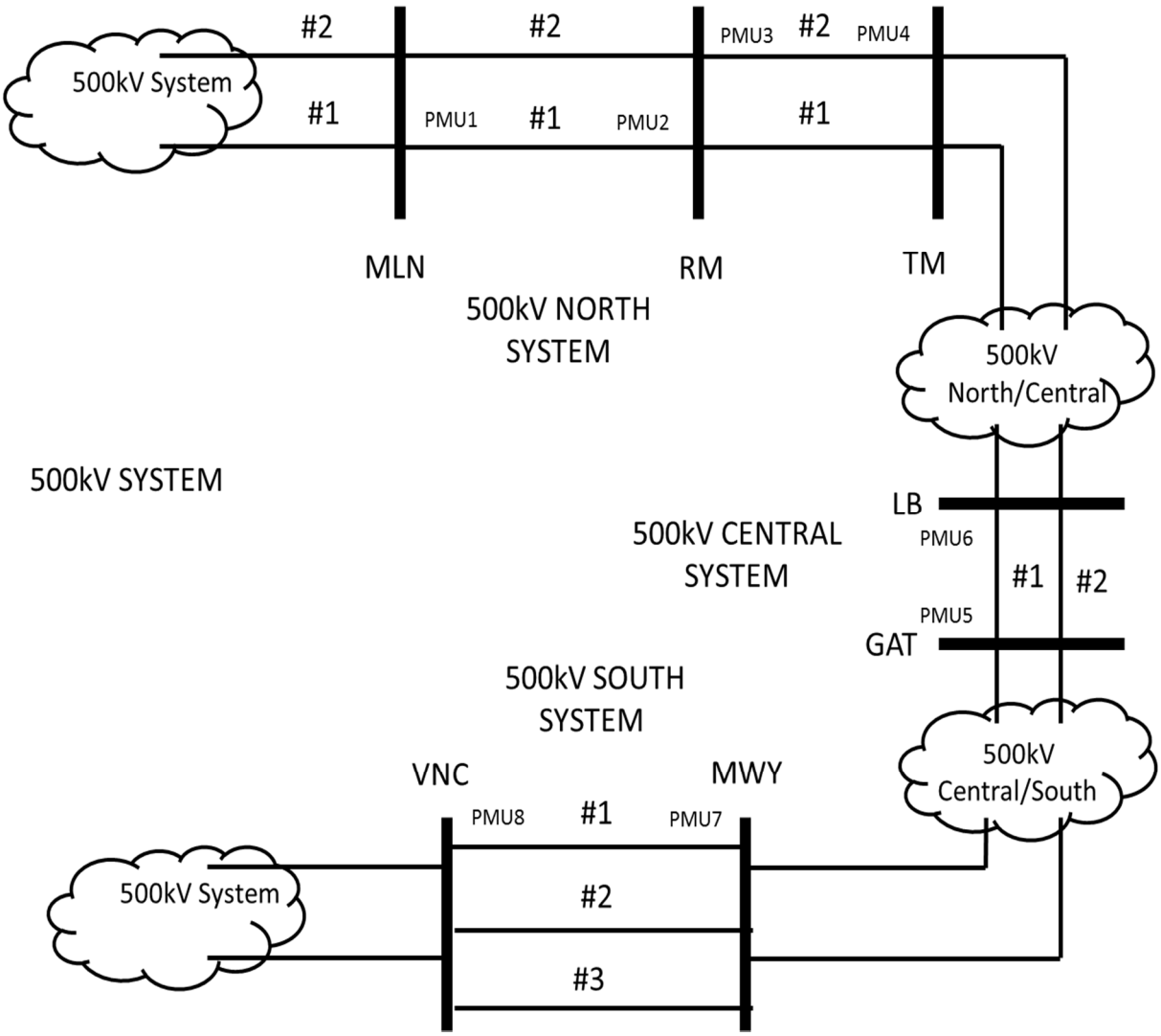


Figure 3 – 500 kV Test System

Appendix E: Synchrophasor Proof of Concept (POC) Lab

Lab Topology

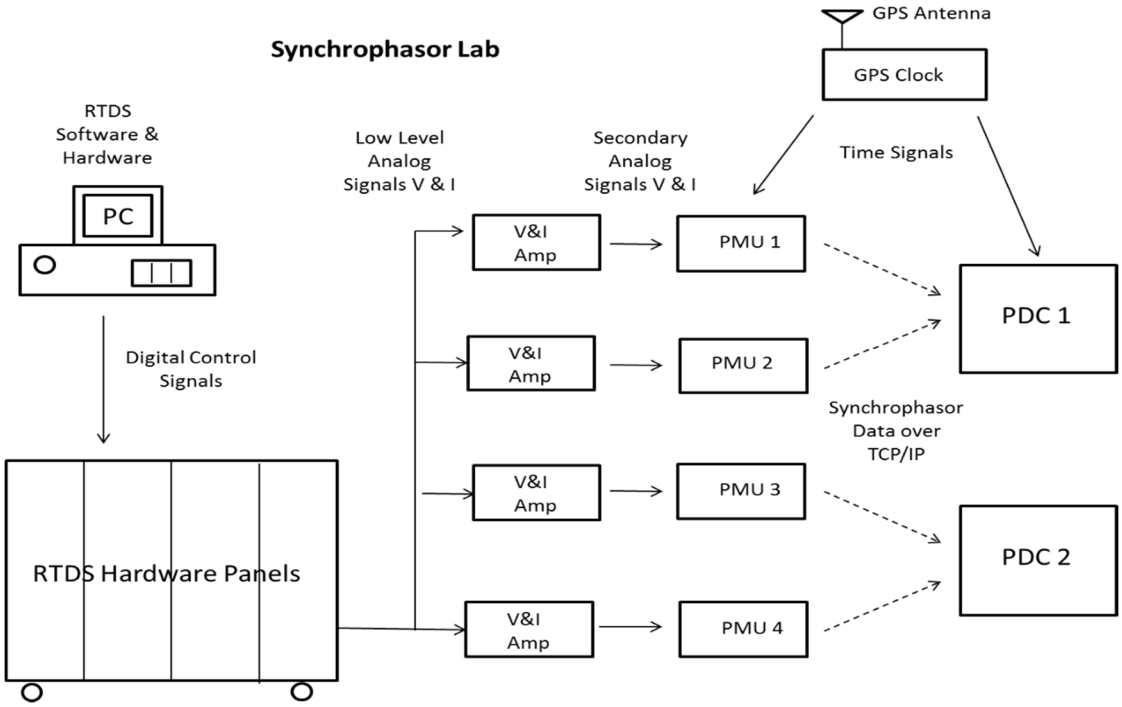


Figure 4 – Synchrophasor POC Lab Topology

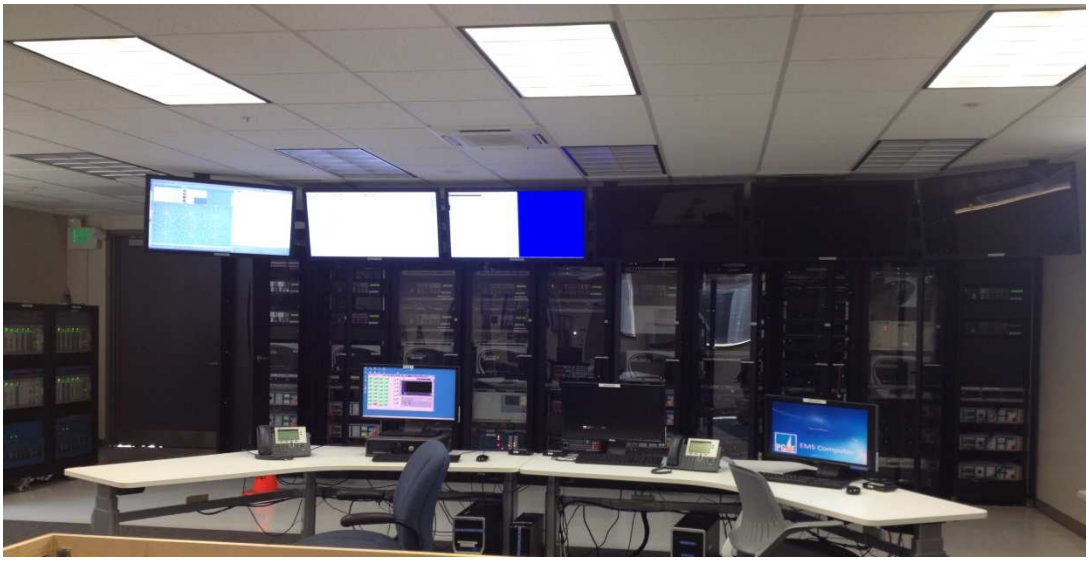


Figure 5 – Synchrophasor POC Lab