An Analysis of Short Channel effects in Gate All Around FET devices

a TCAD Simulation

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Abstract

The Gate All Around (GAA) Field Effect Transistor (FET) is a type of MOS (Metal Oxide Semiconductor) device that circumvents the problem of the existing FinFET devices and produces effective results on scaling up to 7nm technology node and beyond. The significant benefits of this transistor design are size reduction and increased potential for channel length scaling, which attributes to increased transistor density. However, there are some major challenges, like Short Channel Effects (SCE), which include Subthreshold Slope (SS), Drain Induced Barrier lowering (DIBL), and Gate Induced Drain Leakage (GIDL), that are involved in scaling. This paper mainly focuses on reviewing those challenges by analyzing the TCAD simulation results of two different types of GAA FET devices, Nanosheet (NS) and Nanowire (NW), along with the summary of the effect of the width and radius of NS and NW on the above-mentioned short channel effects. A comparative overview of the impact on a single and stacked device is also discussed.

Acknowledgements

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Dedication

To my husband, without whom this journey would not have been possible

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CHAPTER 1

Introduction

1.1 TRANSISTORS AND THEIR SIZE

Scaling of the transistors became necessary to keep up with the demand for ultra-low-power and high-performance computational devices. The traditional planar MOSFETs have xbeen scaled from 65nm nodes to FinFETs, which work effectively up to 12nm nodes [Iannaccone *et al*. (2018)]. Beyond which its performance degraded, it led to the emergence of GAA FETs that work effectively even when scaled beyond 7nm nodes [Hu and Li (2021)]. However, reducing the device's size further impacts its performance, modeling, and reliability due to Short Channel Effects (SCEs). It became essential to reduce these to have better electrostatic control over the device.

The goal of my project involves two primary analyses: first is to understand the effect of adding a substrate to the GAA-FET device and is done by comparing the simulation results of various GAA structures with and without substrate. The next is to comprehend the effect of process parameters on various SCEs. It is achieved by comparing the simulation results by changing the widths or the radii of the NS and NW structures, respectively.

As we are dealing with short-channel devices, it is critical to understand the leakage that occurs due to various phenomena. This project aims to understand such effects on four different Nanosheet and Nanowire GAA FETs structures each. A comparative analysis helps to understand the impact of these short-channel effects.

In addition to Subthreshold slope (SS) and Drain Induced Barrier Lowering (DIBL), a reduction in the channel length causes overlap between the device's Gate and the Drain region. When the device is OFF, a voltage applied to the drain results in a large band bending at the overlapped portion of the drain. This band bending activates the Band to Band Tunneling (BTBT) of electrons, causing it to sweep to the drain and the substrate regions Rai *et al*. (2022). A high electric field at this overlapped region results in leakage current to flow, resulting in Gate induced Drain Leakage (GIDL). This GIDL current is one of

the dominant reasons for submicron CMOS circuits degradation Semenov *et al*. (2001). A detailed analysis of this GIDL is performed and discussed.

CHAPTER 2

Background

2.1 TRANSISTOR TREND

Moore predicted that the number of transistors in an integrated circuit would double every two years, which means that the channel length of the transistor would reduce by half every six years. The possibility for growth became the driving force for semiconductor technology leading to the development of computers and other electronic devices [James (2023)].

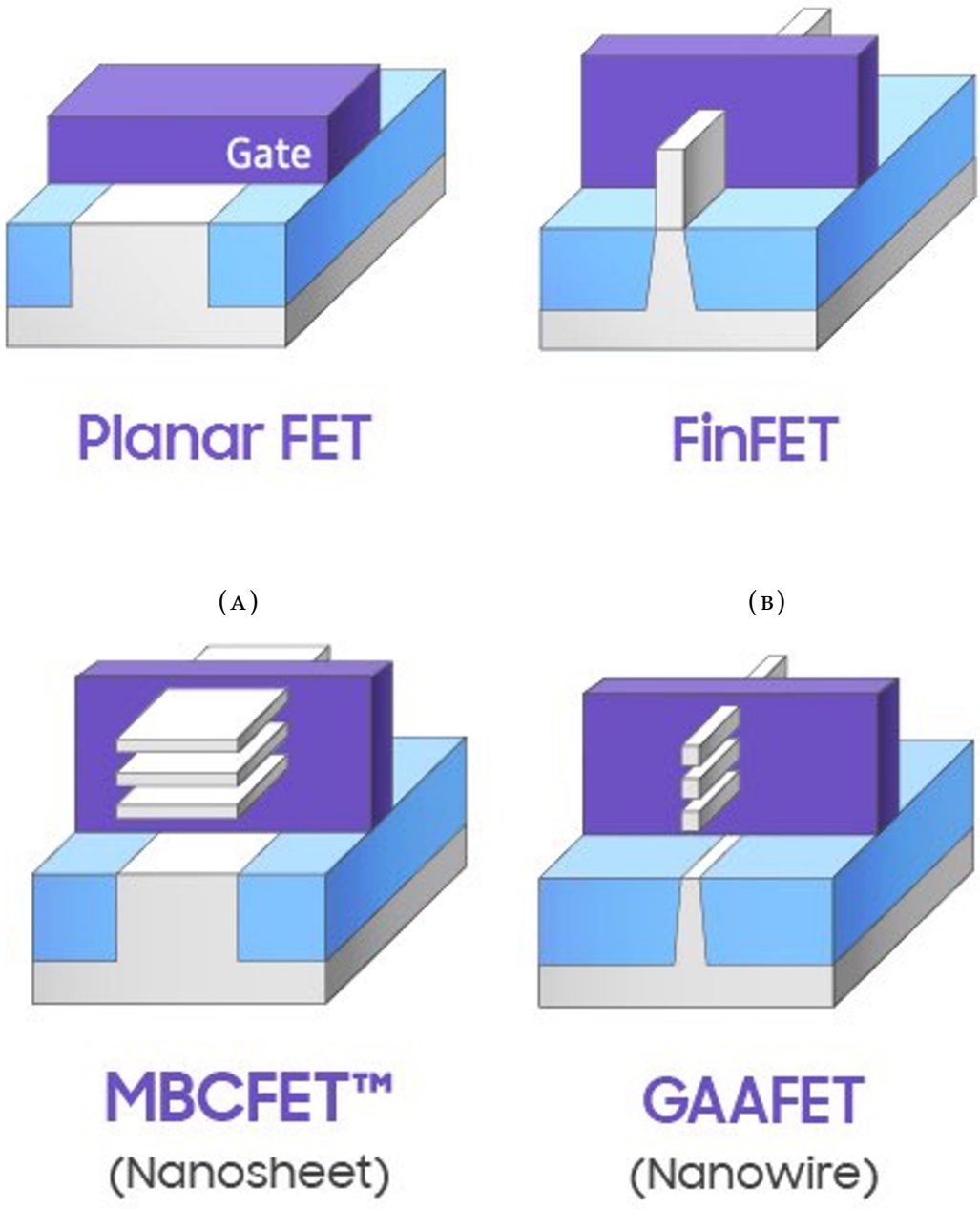
Moore's Law: . *It is the principle that the speed and capability of computers can be expected to double every two years due to increases in the number of transistors a microchip can contain [James (2023)].*

However, there is an increase in the doubling interval, causing Moore's law to slow down, owing to the development of advanced technologies. At present, the density of the chips is not doubling every two years but rather at a slow pace [James (2023)].

It has been observed that reducing the channel length of the transistors has resulted in improved device speed and reduced power; however, it inhibited the performance of the complementary metal-oxide-semiconductor (CMOS) devices when reduced below 14 nm [Ionescu and Riel (2011)] and these are called Short Channel Effects (SCEs).

A three-dimensional configuration was formulated to overcome these problems and to shrink the transistors further. These are called FinFETs, as shown in Fig 2.1b, with the gate on three sides of the channel, giving it more surface area to control the channel electrostatically. The structure worked effectively with reduced leakage and the SCE's up to 3nm process node [Bohr and Young (2017)].

New technologies are required to reduce the size beyond the 3nm node, which led to Gate-All-Around FET (GAAFET) with a channel surrounded by the gate on all four sides [Newsroom (2019)]. It was developed in two forms: Nanowires and Nanosheets as in Fig 2.1c and 2.1d.



(A) (B)

(C) (D)

FIGURE 2.1: Evolution of FET Devices [Newsroom (2019)]

The Nanosheet and Nanowire structures can also be stacked laterally or vertically, as shown in Fig 2.2 to have improved performance [Veloso *et al.* (2016)]. The significant advantages of this method include improved speed without increasing the area and, therefore, no change in the device's footprint [Mari (2020)].

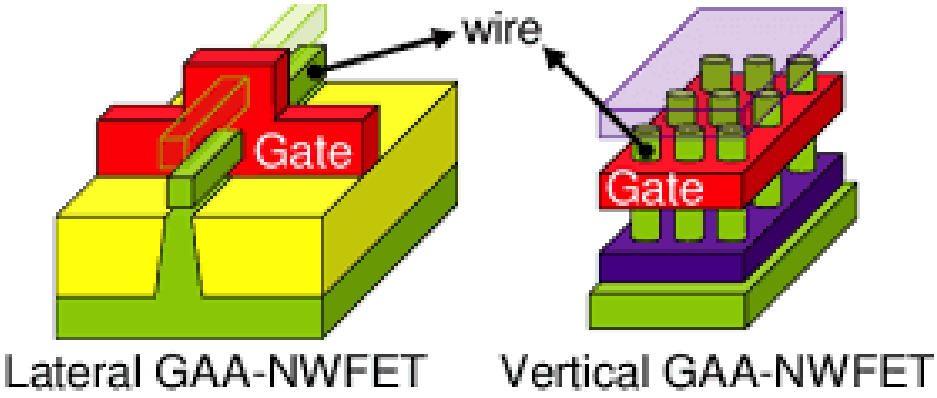


FIGURE 2.2: Lateral and Vertical NWFET [Veloso *et al.* (2016)]

2.1.1 *Challenges in scaling the transistors*

According to the international technology roadmap for semiconductors (ITRS), the primary aim is to decrease the MOSFET dimensions. Even though there are many advantages to decreased size, like area efficiency, increased speed, and performance, when MOSFET enters the nanometer scale, some significant issues, including the Short channel effects (SCEs), come into effect.

2.2 SHORT CHANNEL EFFECTS

Some of the significant SCEs are:

1. Threshold Voltage Roll-off (Vt Rolloff)

2. Subthreshold Swing (SS)

3. Drain Induced Barrier Lowering (DIBL)

4. Gate Induced Drain Leakage (GIDL)

2.2.1 *Threshold Voltage Roll-off (Vt Rolloff)*

As the channel length reduces, the number of depletion charge carriers decreases; hence the energy band changes. The channel's Conduction band (Ec) is pulled lower and closer to the Ec of the source; this lowered barrier makes it easier for the charge carriers to flow into the channel to form the inversion layer, which results in a reduced threshold voltage as shown in the Fig 2.3. The phenomenon is called Vt roll-off. As we shrink the devices further, there is a significant drop in the threshold voltage, and Ioff becomes unacceptable. Hence it is essential to design the device such that the Vt roll-off does not prevent using the targeted minimum length [Hu (2010)].

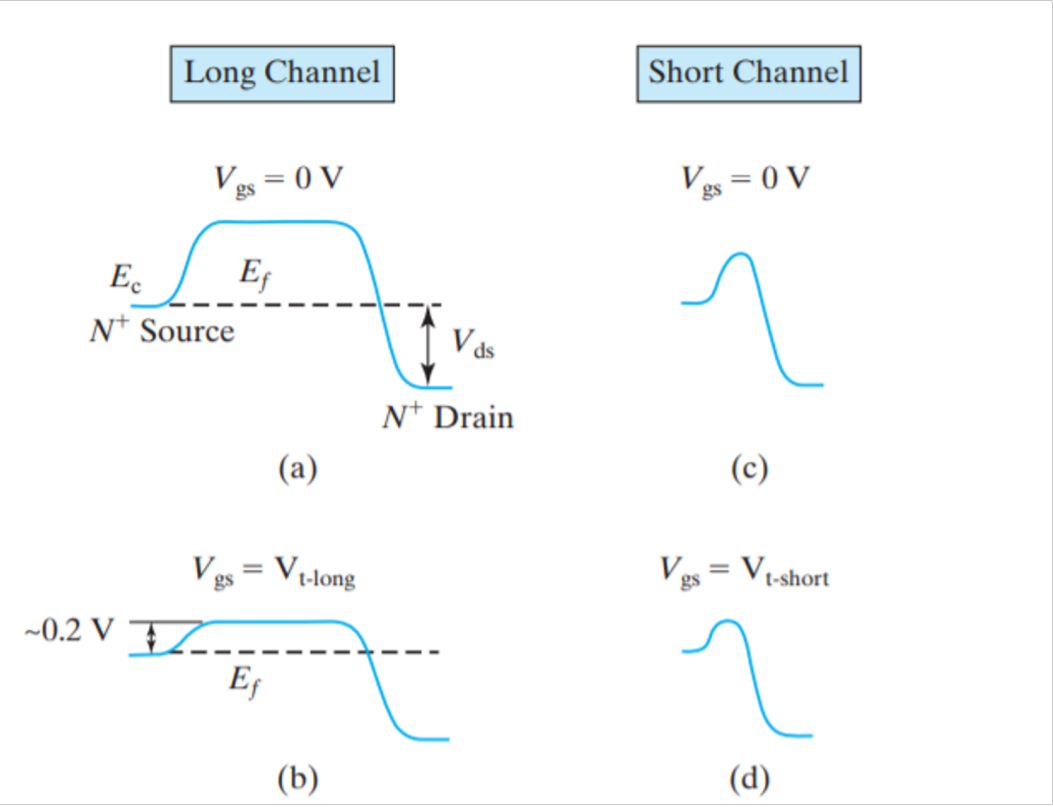


FIGURE 2.3: Threshold Voltage Roll-off [Hu (2010)]

2.2.2 *Subthreshold Slope*

In an ideal MOSFET operation, the transistor is said to be in an OFF state when the gate-to-source voltage (Vgs) is lower than the threshold voltage (Vt). However, the current does not abruptly cut off below threshold voltage, but a small amount of leakage current flows between the source and drain, as shown in Fig 2.4. This region where Vgs < Vt is called the weak inversion region, and the subthreshold leakage current that flows increases exponentially as Vt decreases [Harris and Weste (2010)].

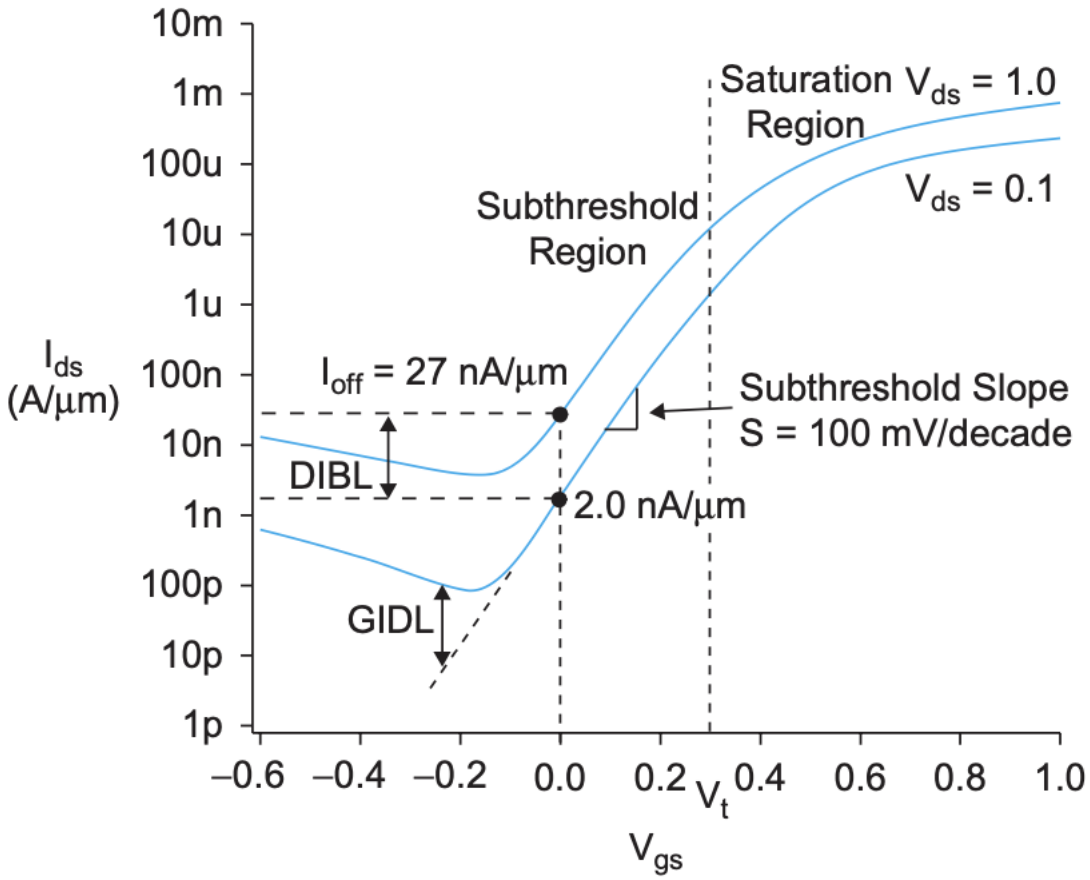


FIGURE 2.4: IV Characteristics of a transistor describing SCE's [Harris and Weste (2010)]

The subthreshold leakage is measured by the subthreshold slope (SS) as the change in gate voltage (Vgs) per decade of drain current (Ids) in the units of mV/dec. The subthreshold slope is an essential factor of consideration as it indicates how much the gate voltage must drop to decrease the leakage current by order of magnitude.

2.2.3 *Drain Induced Barrier Lowering*

In short channel devices, when the voltage applied between drain and source junctions is increased, the drain depletion region extends to the source, forming a unique depletion region called a punch-through. Because of this, the potential barrier is lowered, and the phenomenon is called Drain-induced barrier Lowering (DIBL). A high drain voltage can open the bottleneck and contribute to turning on the transistor as a gate would. Here, the flow of charge carriers is controlled more by drain voltage than gate voltage, and the electrons flow from source to drain even if the gate-to-source voltage (Vgs) is not present. As a result, the saturation current increases with a more positive slope in the Id-Vds curve since the current is inversely proportional to the channel length 'L' [Harris and Weste (2010)].

2.2.4 *Gate Induced Drain Lowering*

The gate-induced Drain Leakage (GIDL) is another leakage mechanism that occurs when the drain is at a higher voltage than the gate resulting in a deep-depletion region forming underneath the gate-to-drain overlap region [Harris and Weste (2010)] GIDL is mainly due to the band-to-band tunneling process in the overlap region. The electrons in the valence band tunnel through the band gap to the conduction band, causing leakage. This leakage current increases with an increase in Vd and a decrease in Vg. GIDL current is one of the dominant reasons for sub-micron CMOS circuit degradation; hence, it is essential to control it [Rai *et al*. (2022)]

2.3 PURPOSE OF THE THESIS

My thesis aims to perform a technology computer-aided design (TCAD) assessment to study the impact of device dimensions on the short-channel effects over various structures of the GAA FET. These simulations would compare the different configurations of the device and provide insight into the GAA structure that provides the most promising performance. Further, it would lay a foundation for future research toward implementing different approaches to build better-performing devices.

CHAPTER 3

Literature Review

3.1 Device Structure

Many developments in the fabrication of the transistors have been proposed, with various strategies to make them excellent candidates for advanced technology nodes - specifically, better electrostatic control, improved performance, and energy saving. One such development is stacking. Experiments prove that stacking at such scale paves the way for a significant increase in the effective width and current density and substantial savings in device footprint [Gaben *et al*. (2016)].

3.1.1 *Nanowire*

The GAA FETs can be stacked vertically or Laterally, as shown in Fig 3.1 to replace finFETs in sub-10nm technology nodes.

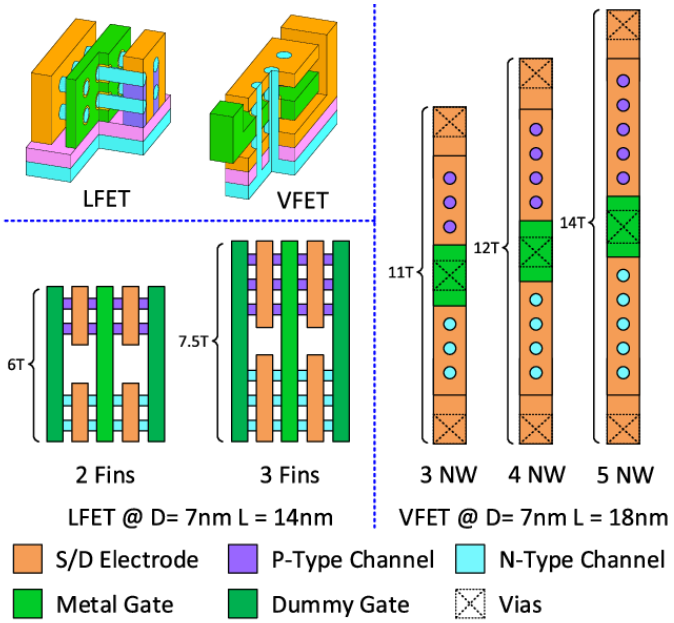


FIGURE 3.1: Lateral and Vertical configurations of a NW FET [Pan *et al*. (2015)]

The Lateral NW structures are fabricated similarly to the conventional replacement metal gate finFETs. The simulation results show a reduced current

density per layout width compared to the FinFET structure [Lauer *et al*. (2015)]. While the device's footprint confines the gate length and spacer thickness of lateral NWs, these structures have an increased channel mobility leading to a higher ON current [Pan *et al*. (2015)].

The Vertical NW structure consists of horizontally stacked NWs with the Source and Drain on the top and bottom of the gate, another topology considered for improving scalability.[Pan *et al*. (2015)] These structures reduce the effect of parasitic elements due to higher device density without scaling down physical gate lengths.[Fahad and Hussain (2012)]

3.1.2 *Nanosheet*

Like Nanowires, Nanosheet structures can be stacked laterally or vertically, as shown in Fig 3.2. Laterally /Horizontally stacked Nanosheets have their channels in the horizontal direction and are stacked vertically. These structures have a higher on-state current than the nanowires due to sizeable effective width, Weff [Hu and Li (2021)]. Vertically stacked Nanosheet devices can perform better beyond 7nm technology nodes due to their superior short-channel effects. They also allow optimizing the sheet widths to increase the effective device width (Weff) compared with FinFETs while maintaining short-channel control. [Lee *et al*. (2017)]

The major limitation in the lateral structures' scaling is the contacted gate pitch (CGP) [Thean *et al*. (2015)]. To overcome this, Vertical NS FETs are fabricated such that the channel is not formed horizontally but vertically. This feature helps relax the gate length and the spacer while reducing the device's footprint, taking advantage of the 3D space. Because of this, quantum confinement effects are reduced.

3.2 BAND TO BAND TUNNELING

3.2.1 *BTBT in Nanowire Structure*

The Tunneling of electrons occurs in two ways: Transverse band-to-band tunneling (T-BTBT) and Longitudinal band-to-band tunneling (L-BTBT). The T-BTBT is significant at the high gate to source voltage (Vgs) and is less severe for

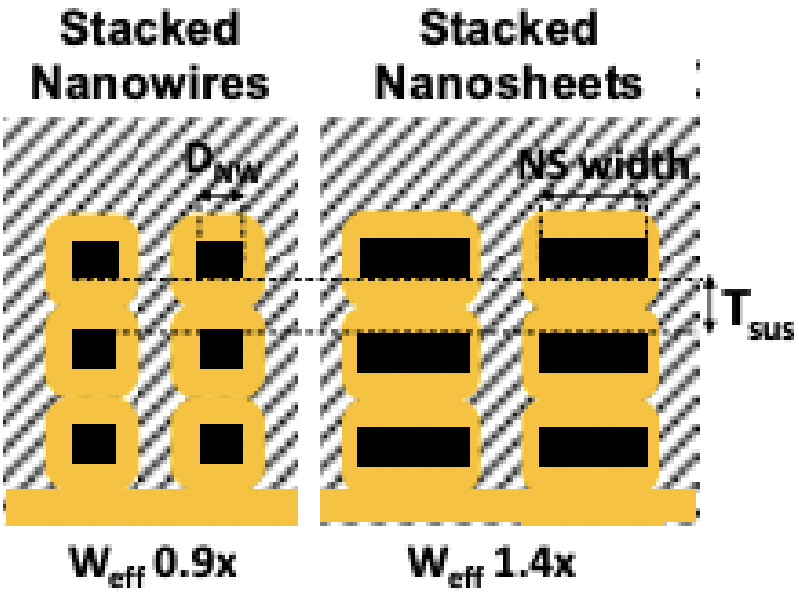


FIGURE 3.2: Stacked configurations of GAA FET [Lee *et al*. (2017)]

the Nanowire due to its GAA structure and small diameter of the channel [Fan *et al*. (2014)]. Fig 3.3 shows the schematic diagram of GIDL Induced by a) T-BTBT and b) L-BTBT in an n-type GAA Nanowire FET. The gate controllability to the body/drain junction will exhibit a much more significant impact on the longitudinal energy band. Hence, it is expected that in the small channel NW device, L-BTBT will increase substantially, resulting in unexpectedly large GIDL at low Vgs [Rai *et al*. (2022)].

The NW structure used for the analysis is fabricated, as demonstrated in [Fan *et al*. (2013)]. The experimental results show that at low Vgd, an enhanced L-BTBT produces a higher GIDL current, as shown in Fig 3.4

Simulating the structure over different radii (Fig 3.5) shows that as we increase the radius from 3 to 7 nm, the GIDL current increases, implying that BTBT depends on the channel area because it occurs at the body/drain junction area [Kim *et al*. (2018)].

Increasing the number of NWs in the lateral direction helps increase the drive current but at the cost of increased silicon consumption. Vertical stacking of NWs yields a much higher drive current without increasing the device's footprint [Singh *et al*. (2008)].

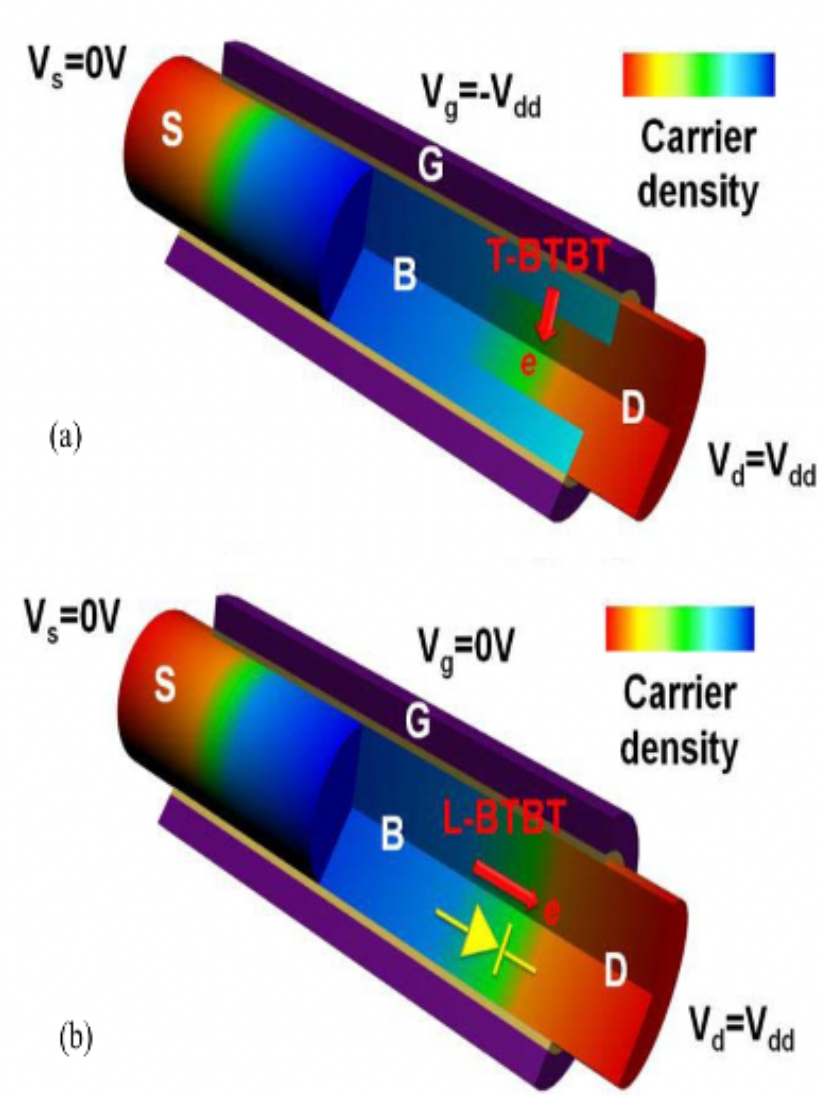


FIGURE 3.3: Schematic diagram of GIDL induced by a) T-BTBT and B) L-BTBT in an N type GAA NW FET [Fan *et al*. (2014)]

Here the analysis is done on Stacked NW FET in two operating modes, an inversion mode (IM) and a junctionless mode (JM). The stacked NW structure of the device with its dimensions are shown in Fig 3.6

We determine the GIDL current at low Vgs, and we can see from the graph Fig 3.7 that IM-FET has a higher GIDL current than JM-FET, which is attributed to the high doping concentration of IM-FET as it results in smaller tunneling width. This aligns with the results of the single NW device, as seen before [Fan *et al*. (2014)].

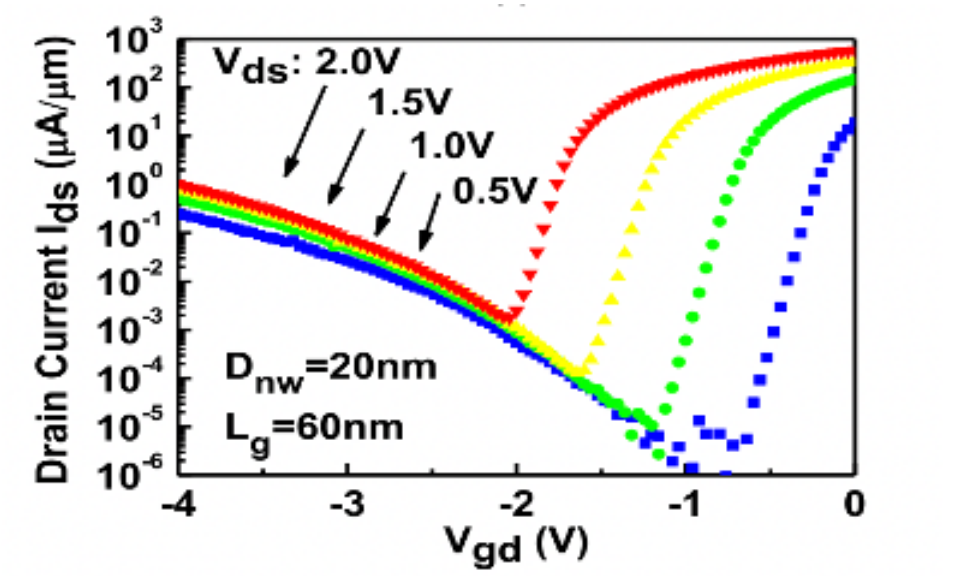


FIGURE 3.4: GIDL current of the NW device as a function of Vgd with different Vds [Fan *et al.* (2014)]

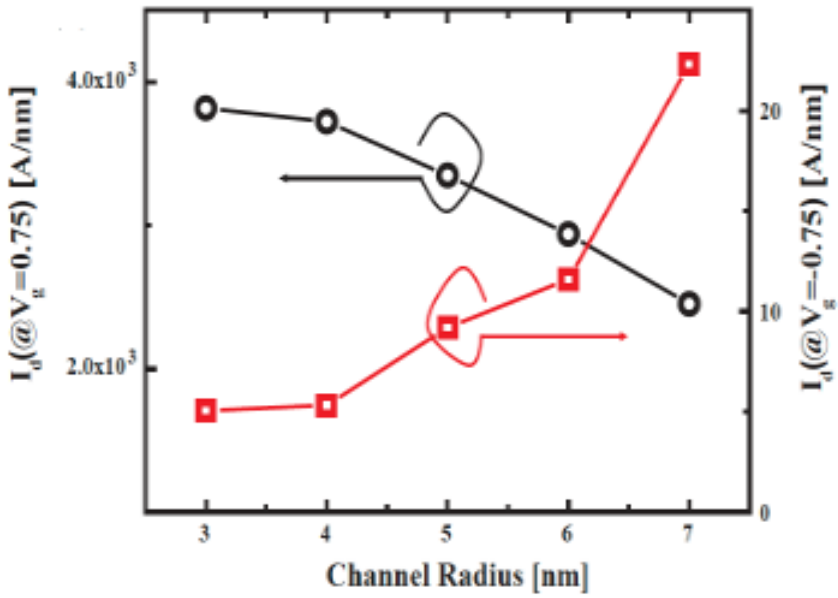


FIGURE 3.5: Comparison of ON current and GIDL current with different radii from 3 to 7 nm [Kim *et al.* (2018)]

3.2.2 *BTBT in Nanosheet Structure*

Like Nanowires, Nanosheets (NS) are stacked to overcome the issue of low overdrive current. Multiple sheets can be stacked to realize a device, resulting in larger effective widths per unit footprint area [Pundir *et al.* (2020)]. The GAA Stacked NS structure analyzed is shown in Fig 3.8

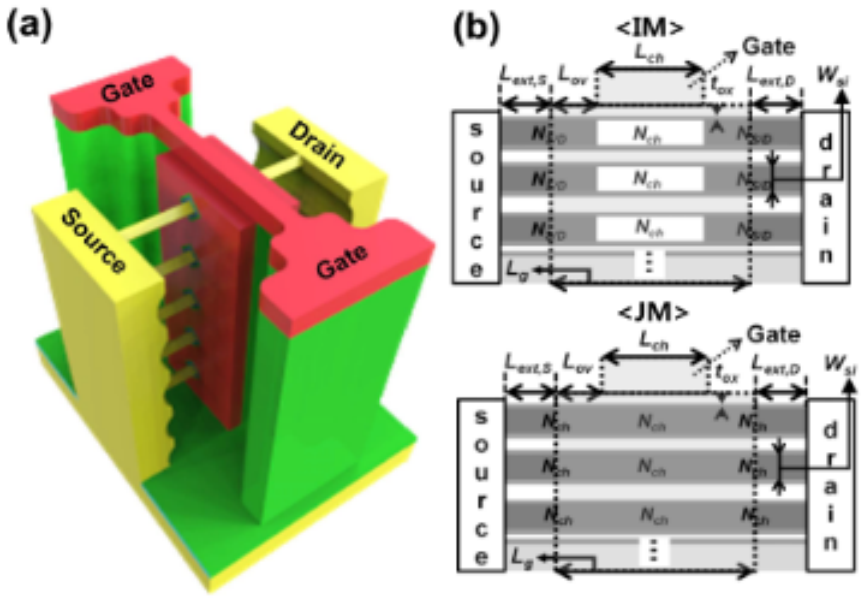


FIGURE 3.6: a) Schematic of the Vertically Stacked NW, and (b) front view of the IM-FET and the JM-FET respectively [Hur *et al*. (2016)]

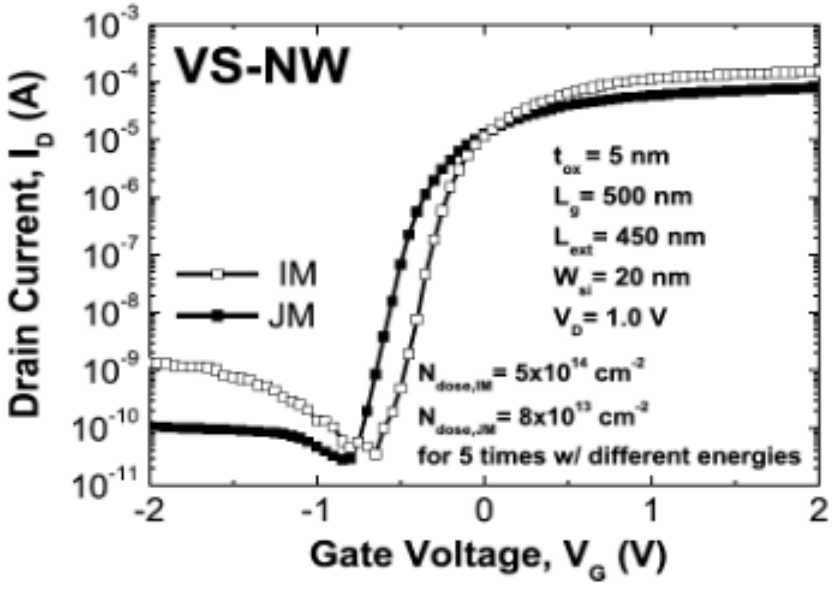


FIGURE 3.7: Transfer characteristics of the Vertically Stacked NW of IM-FET and the JM-FET [Hur *et al*. (2016)]

The parameters used in the simulation are referred to by IRDS 2020 [Hoefflinger (2020)] and the experimental data [Loubet *et al*. (2017)]. The I-V characteristics of the same are shown in Fig 3.9 [Gu *et al*. (2021)].

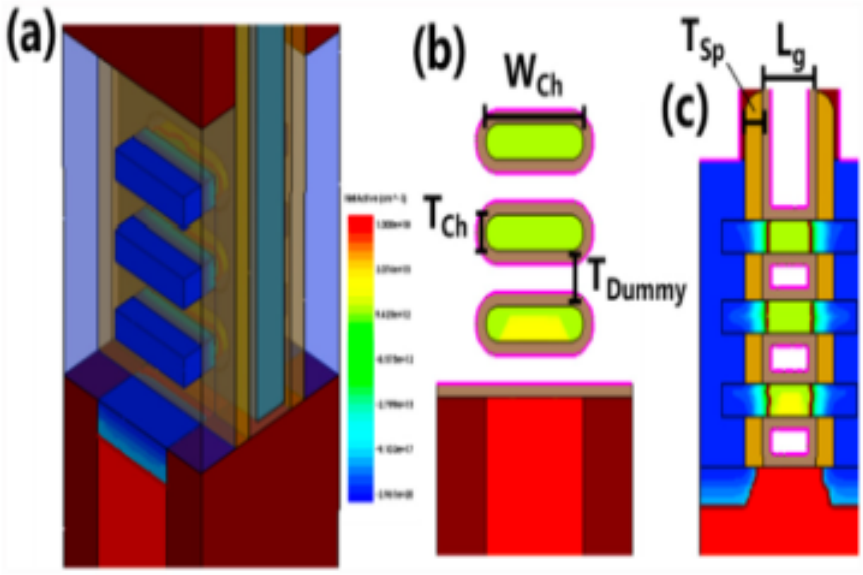


FIGURE 3.8: Schematic of the simulated NS-FET cross section (b) perpendicular to and (c) along with the channel direction, respectively [Pundir *et al.* (2020)]

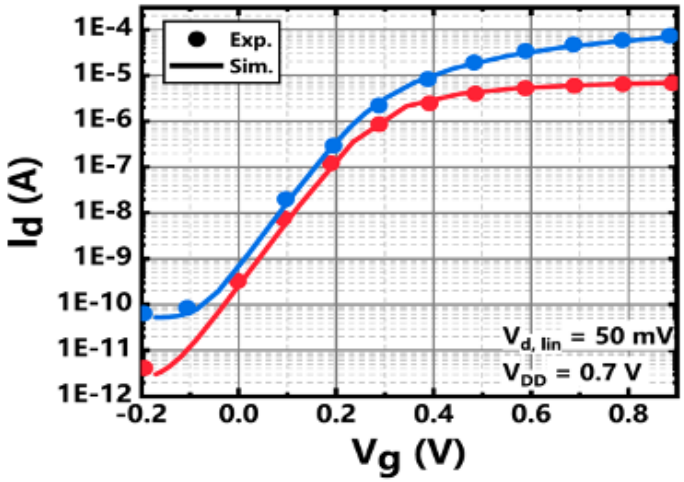


FIGURE 3.9: Comparison of Id-Vg characteristics with the experimental results [Gu *et al.* (2021)],[Loubet *et al.* (2017)]

Another type of NS fabrication involves forming a doped ultra-thin (DUT) layer, epitaxially grown on the starting wafer before the stack formation. This NS structure with the DUT layer is shown in Fig 3.10 [Lee and Park (2022)].

The device's simulation results with different DUT layer thicknesses show that with a thicker DUT, a p-n diode is formed between the drain and the DUT layer. In the off-state, this reverse-biased p-n diode triggers the BTBT of electrons and increases the Off current (Ioff). As the thickness increases, there

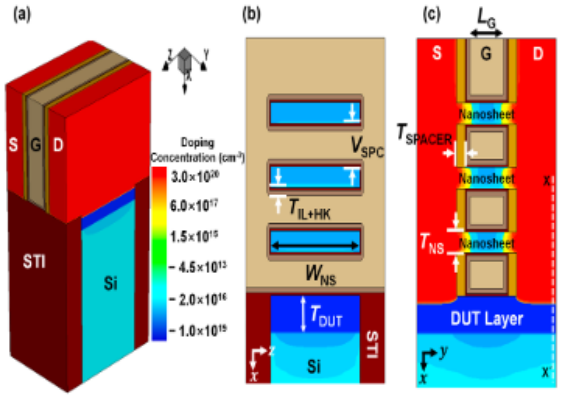


FIGURE 3.10: a) NS FET device structure including the epitaxially–grown DUT layer on the starting wafer. Cross–sectional view of the proposed NS FET with a cut along the (b) gate and (c) channel directions, respectively [Lee and Park (2022)]

is a significant increase in electron generation by the BTBT. Thus, the thickness of the DUT layer should be smaller to avoid unwanted increasing Ioff [Lee and Park (2022)].

Further, Fig 3.11 shows that with low Vgs, the hole-current component is the dominant one in producing gate-induced drain leakage (GIDL) [Jegadheesan *et al*. (2020)]. This is because the negative bias at the gate terminal leads to band bending at the channel, which causes tunneling of the electrons, causing GIDL current to flow through the device. However, this can be controlled by increasing the tunnel barrier width, thereby decreasing the electric field at the junction [Jegadheesan *et al*. (2020)], [Gundapaneni *et al*. (2012)].

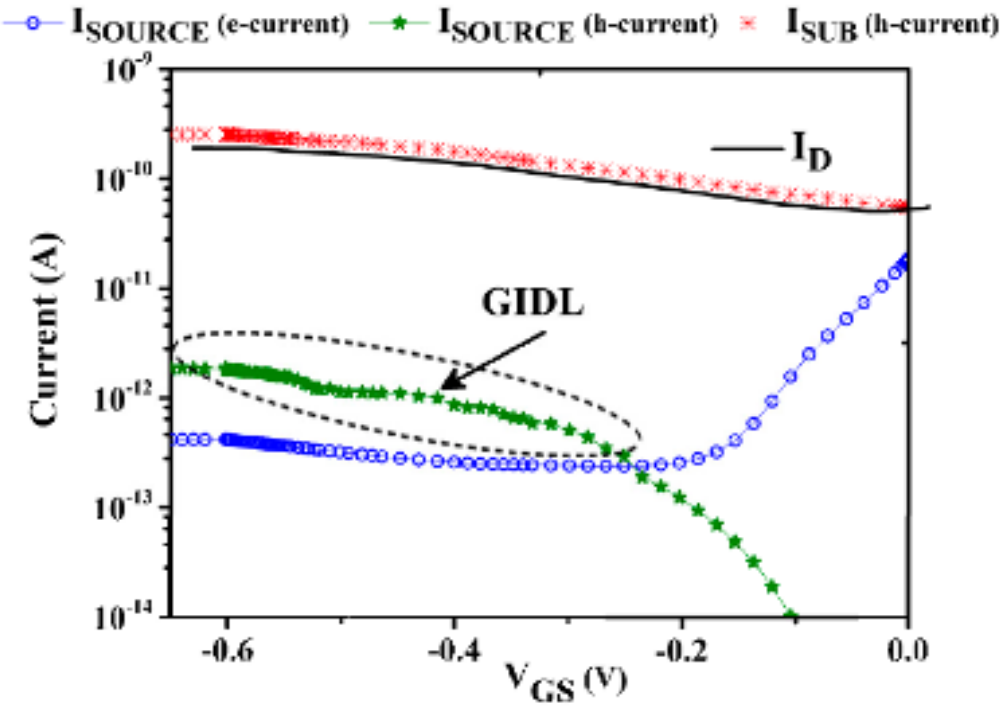


FIGURE 3.11: e-current and h-current components of the source and substrate terminal of NS-FET for different VGS [Jegadheesan *et al.* (2020)]

CHAPTER 4

Methodology

4.1 RESEARCH OBJECTIVES

My project analyzes how various parametric modifications of different GAA structures affect their performance. The base of my work comes from the model structure developed previously by the students of the 3D nanoscale IC research group under the guidance of Dr. Li. I adapted the model to suit the requirements of this project and performed the analysis on the same.

The GAA Device structures: Nanosheet (NS) and Nanowire (NW) as a single and stacked device in both lateral (NS_L and NS_LS) and vertical (NW_L and NW_LS) directions were constructed in a Sentaurus Technology Computer-Aided Design (TCAD) simulation tool, as discussed in the sections below.

The preliminary analysis is a comparative assessment of On current (Ion), Off current (Ioff), Threshold Voltage (Vt), Subthreshold Slope (SS), and Drain Induced Barrier Lowering (DIBL) with and without substrate over various widths (in the case of NS) and radii (in the case of NW).

The analysis of the substrate's impact is significant because the doping concentration of the substrate inversely affects the drain current while favoring the threshold voltage (Vt) [Saha and Goswami (2018)]. Thus, an increase in substrate concentration increases Vt, negatively impacting the device characteristics.

Following this, we analyzed the device dimensions' impact on Band to Band Tunneling (BTBT), a significant contributor to the Gate Induced Drain Leakage (GIDL) current. We have included the Kinetic Velocity Model (KVM) available in TCAD that incorporates ballistic effects as the default model does not account for these effects, which strongly overestimate the drain current and produce a pronounced threshold voltage shift due to the overestimated channel mobility [Penzin *et al.* (2017)].

Furthermore, the source and the drain regions are doped with a Gaussian doping profile instead of uniform doping as there are studies that confirm

better control of ON state current [Charmi *et al*. (2013)] and reduction in SS and DIBL with Gaussian doping [Hossain and Chowdhury (2016)]. The simulation model is then calibrated to match the experimental results of [Fan *et al*. (2014)].

4.2 DEVICE PARAMETERS

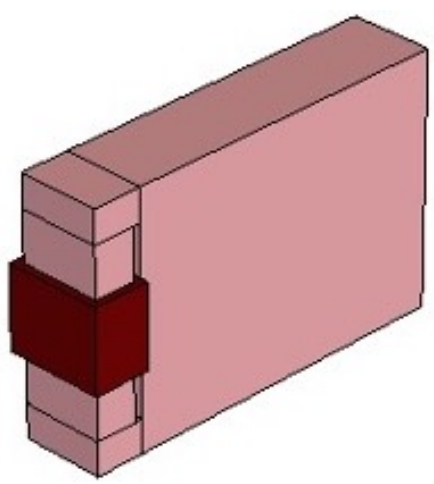
The GAA FET structures for the simulations were created using the Sentaurus device (sdevice) tool, and the parameters of each structure are projected based on [Das and Bhattacharyya (2020)]. The gate length (Lg) is 10nm, and the contact gate pitch (CGP) is set to be 24 nm for lateral GAA FET. These values are increased by 20% for vertical devices as their parameters can be relaxed due to the vertical deployment of the channel [Thean *et al*. (2015)]. The parameters for lateral and vertical GAA structures are listed in the table 4.1 below.

Setup	LGAA	VGAA
CGP(nm)	24	28.8
LG(nm)	10	12
TOX(nm)	1	1
Spacer(nm)	6	7.2
Contact(nm)	4	4.8
Stack Spacer (nm)	4	4
Channel Doping (cm-3)	1.00E+17	1.00E+17
SD Doping (cm-3)	1.00E+20	1.00E+20
WK (eV)	4.52/4.4	4.52/4.4
Nanosheet Width (nm)	10 to 20	10 to 20
Nanosheet thickness (nm)	5 to 10	5 to 10
Nanowire Radius (nm)	5 to 10	5 to 10

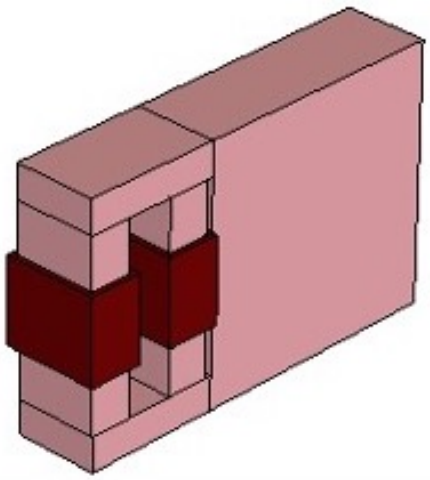
TABLE 4.1: Parameter Setup.

The 3D and cross-sectional views of all different GAA FET structures are shown in Fig 4.1 and Fig 4.2, respectively.

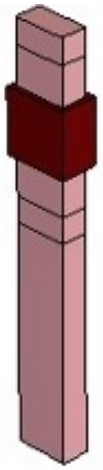
We have considered single and stacked structures to study the preliminary analysis: I-V characteristics, Vt, SS, and DIBL, and just the single structures to understand the GIDL mechanism, which can be implemented for the stacked structures in the future. The stacked structures possess two channels separated by a stack spacer of 4 nm sharing the same S/D contact, as shown in Fig 4.1b, Fig 4.1d, Fig 4.2b and Fig 4.2d. We have assumed the width (W) of NS to be



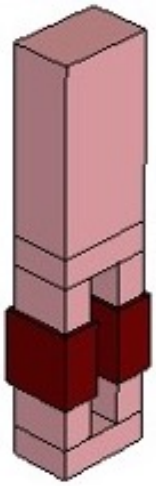
(A) Nanosheet Lateral (NS_L)



(B) Nanosheet Lateral Stacked(NS_LS)

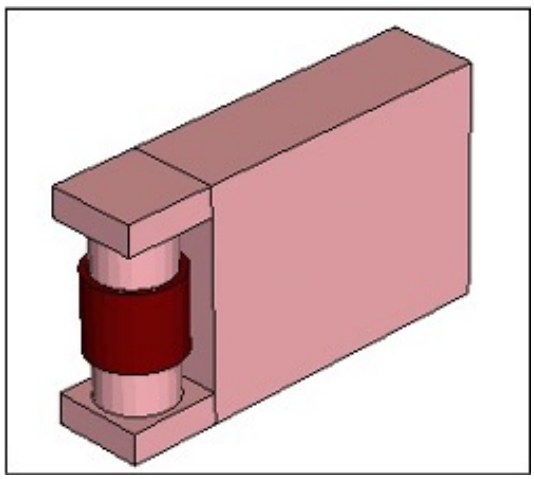


(C) Nanosheet Vertical (NS_V)

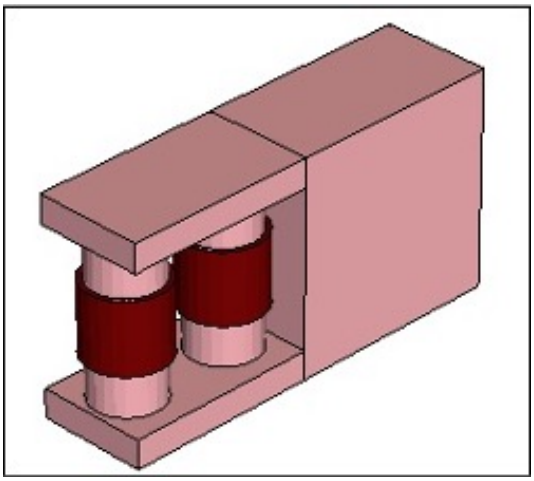


(D) Nanosheet Vertical (NS_VS)

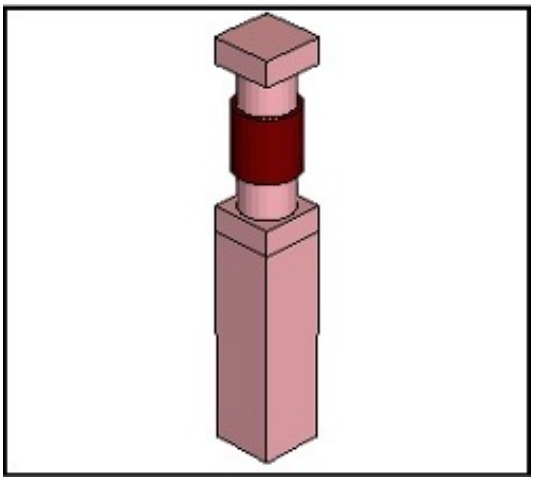
FIGURE 4.1: Nanosheet Structures



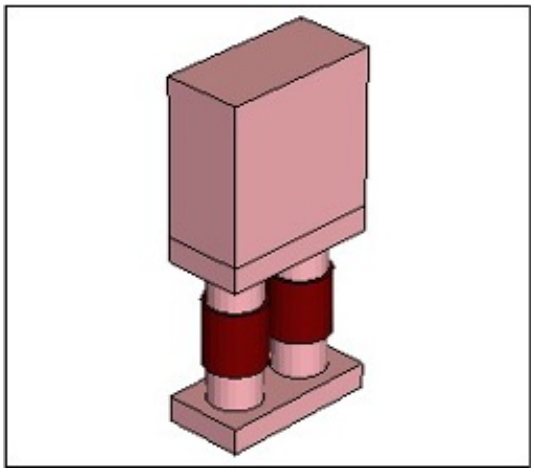
(A) Nanowire Lateral (NW_L)



(B) Nanowire Lateral Stacked(NW_LS)



(C) Nanowire Vertical (NW_V)



(D) Nanowire Vertical (NW_VS)

FIGURE 4.2: Nanowire Structures

twice its thickness, while the effective width (Weff) is considered the perimeter (2 * (width + height)). For NW, Weff is the circumference (2 * π * radius) of the cross-section. The analyses are performed by sweeping the NS width from 10 to 20 nm and the NW radius from 5 to 20 nm.

It may be noted that the work function of the gate material is set as 4.52 eV (Tungsten) for the preliminary analysis and is altered to 4.4eV to match the experimental data for the GIDL study where the source and the drain regions are modeled as a gaussian doping profile with a maximum doping of 1e20 cm-3 at S/D and a minimum doping of 1e17 cm-3 at the channel interface.

The GIDL simulation model is then calibrated to match the experimental results of [Fan *et al*. (2014)]

4.3 SIMULATION SETUP

The 3D device simulations were performed using the Sentaurus Device editor (SDE) in TCAD. The ballistic mobility and High field saturation models were activated to consider both doping dependence and field-dependent mobility. A nonlocal BTBT model based on the Wentzel–Kramers–Brillouin approximation was included for band-to-band tunneling. Fermi–Dirac statistics, Shockley–Read–Hall, and Auger recombination model were also included. The effective density of states of electrons (gc) and holes (gv) were default values, and the tunneling masses of the electrons (me) and holes (mh) were tuned in the parameter file to match the experimental results of [Fan *et al*. (2014)].

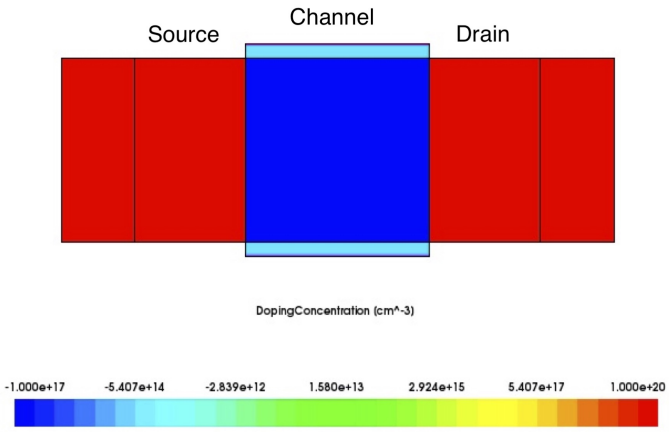
The Sentaurus TCAD Suite constitutes the tools that help us create and simulate semiconductor devices in 2D and 3D. The Sentaurus Workbench (SWB) is a GUI that allows us to create projects to generate and simulate electronic devices.

The Sentaurus Device (SDevice) tool [Guide (2020)] is used to simulate the electrical characteristics by providing necessary commands in the sdevice_des.cmd file. The models for accounting for the effects of mobility, recombination, and tunneling are included in the Physics section. The parameters of these models can be modified in the sdevice.par file. The Solve section contains

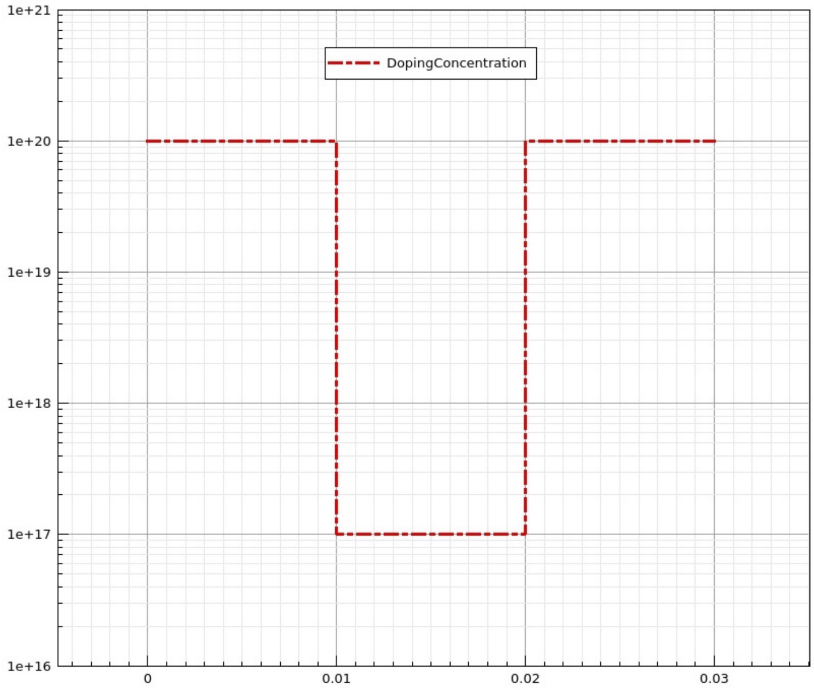
the required equations that are to be solved. Finally, the data saved at the end of the simulation are plotted in the file specified in the File section.

The NS and NW and all their structures in both orientations are built using the Sentaurus Structure editor or by providing commands in the sde_dvs.cmd file [Synopsys (2020)]. The design parameters and the doping profiles mentioned earlier in the section are defined in this file. The 3D view of all the structures is shown in Fig 4.1 and Fig 4.2

The doping profiles considered for the preliminary analysis (uniform) and the GIDL analysis (Gaussian) are as shown in Fig 4.3a and Fig 4.4a.

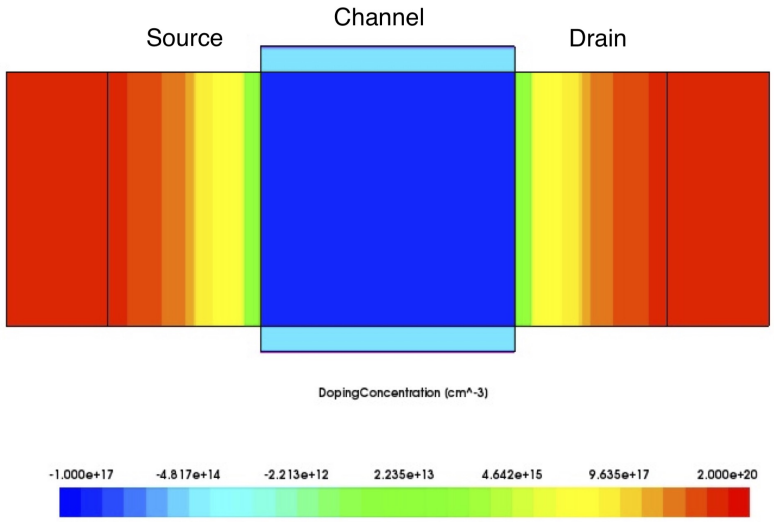


(A) Doping Concentration visualized in the Nanosheet structure.

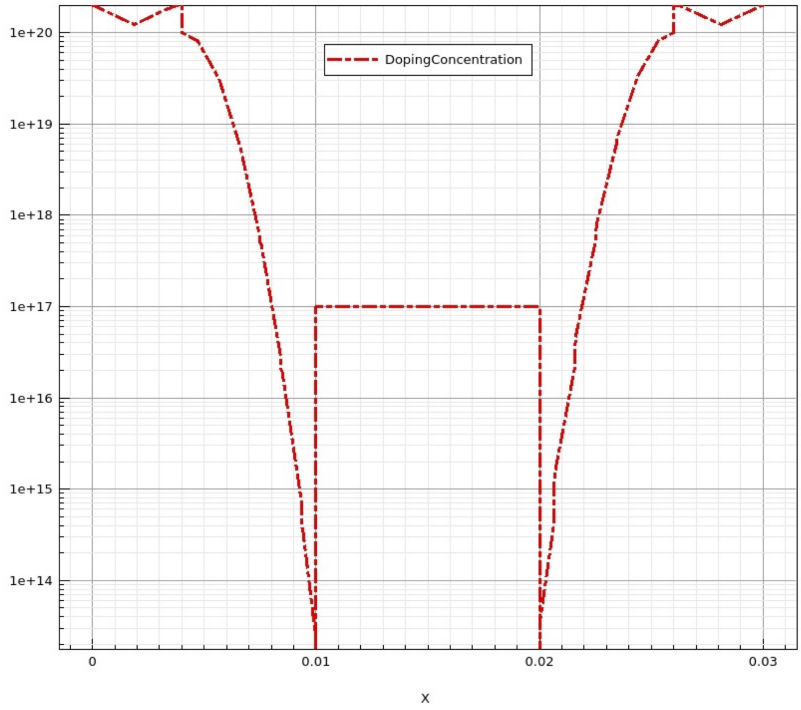


(B) Doping Concentration along X-axis

FIGURE 4.3: Uniform Doping Profile



(A) Doping Concentration visualized in the Nanosheet structure.



(B) Doping Concentration along X-axis

FIGURE 4.4: Gaussian Doping Profile

CHAPTER 5

Results and Discussion

5.1 SUMMARY

The device structures modeled are simulated in the SWB by creating new experiments for different widths and radii. Each experiment can specify the values for a Work function (WK), Gate Voltage (Vg), and Drain voltage (Vd) as required for the analysis.

5.2 EFFECT OF ADDING SUBSTRATE

The preliminary analysis of the project is to understand the effect of adding a substrate on the ON current. As expected, adding a substrate will account for the leakage currents and hence a reduced current. From the IV characteristics shown in Fig 5.1a and Fig 5.1b, the NS structures have a reduced ON current with the substrate as expected, while the NW structures have an opposite effect. The ON current of all four NW structures is higher after adding the substrate.

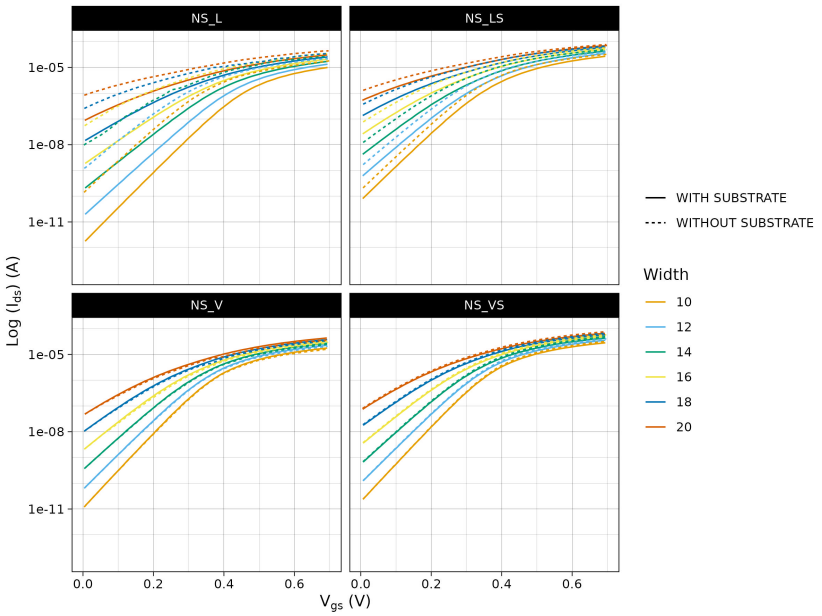
5.3 DEPENDENCE OF SCE'S ON WIDTH AND RADII

5.3.1 *Threshold Voltage (Vt)*

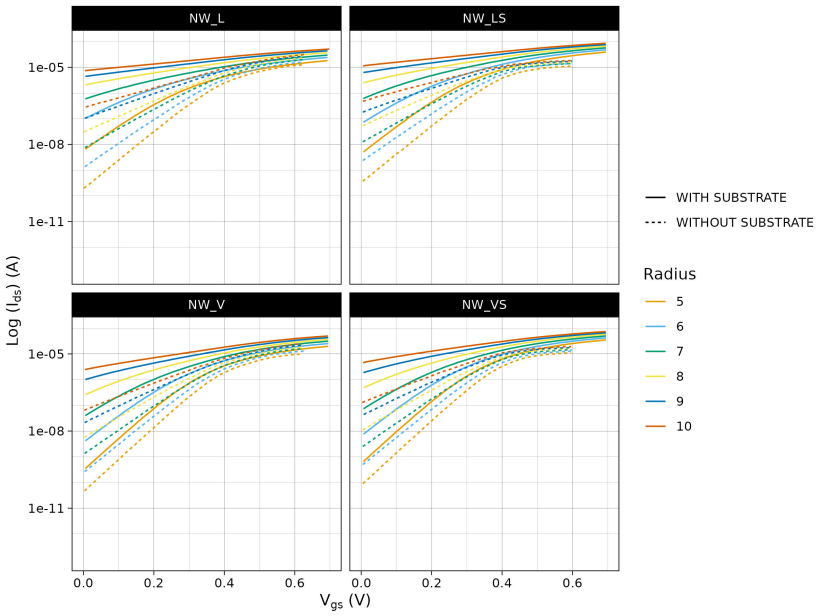
The Vt results are obtained using the Sentaurus Inspect tool of the TCAD software. The tool can extrapolate parameters from the graphs, such as threshold voltage and the Subthreshold slope. It can be run by adding commands in the inspect_ins.cmd file.

As we simulate by sweeping the width and radii, the inspect tool calculates the threshold voltage from the IV characteristics and displays it on the workbench. Fig 5.2a and Fig 5.2b shows the Vt results obtained for various structures of the GAA FET, and it is clear that as the width and radii increase, the Vt value decreases.

Also, as we can expect, the Vt values with the substrate are higher than those obtained without the substrate. It is the same in all cases. The primary

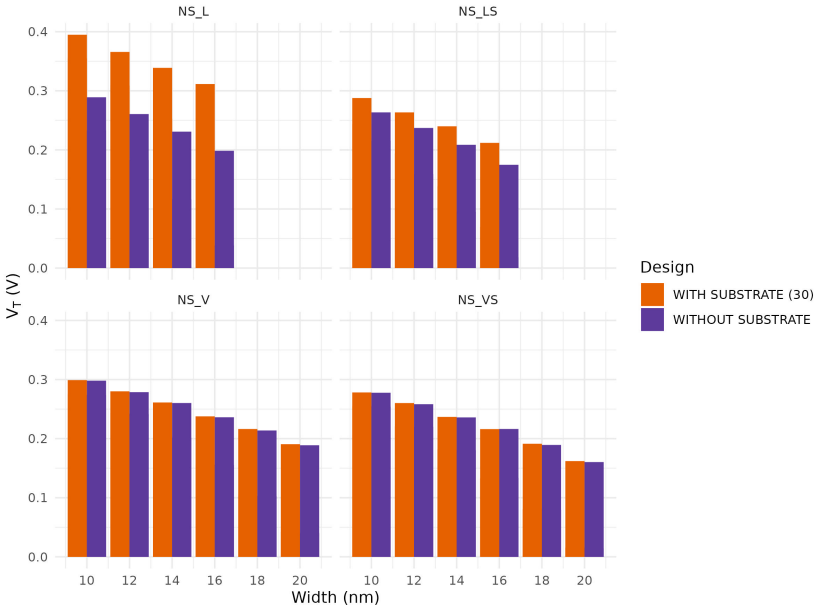


(A) IV Characteristics for Different Widths of Nanosheet

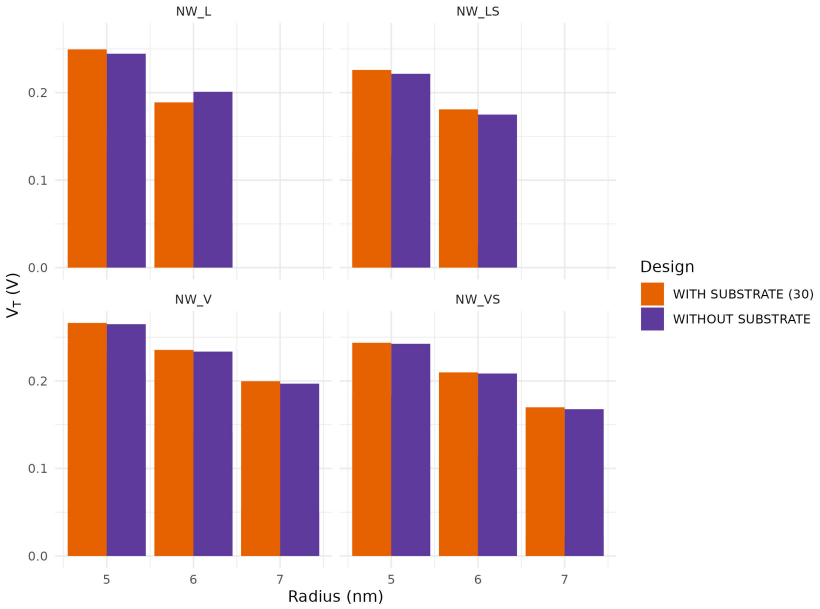


(B) IV Characteristics for Different Radii of Nanowire

FIGURE 5.1: Effect of adding Substrate on IV characteristics



(A) Threshold Voltage over different widths of Nanosheet.



(B) Threshold Voltage over different radii of Nanowire.

FIGURE 5.2: Effect of addition of substrate on threshold voltage.

reason for this decrease in Vt can be understood from the energy band diagram shown in Fig 5.3a and Fig 5.3b.

As the width increases, the barrier height between the source and the channel decreases, and hence the electrons from the source easily move to the drain region, requiring less threshold voltage to turn on the device.

5.3.2 *Subthreshold Slope (SS)*

Like Vt, SS is also obtained from the Inspect tool. Here, the IV linear curve is first transformed into a log curve, and the first derivative is calculated. Finally, the reciprocal number of the maximum of the values is found. The results from the simulation over different structures with changes in width and radii are shown in Fig 5.4a and Fig 5.4b.

From the graphs, we can understand that the SS worsens with the increase in width and radii. Moreover, adding substrate has significantly reduced the SS in NS and NW Lateral structures.

5.3.3 *Drain Induced Barrier lowering (DIBL)*

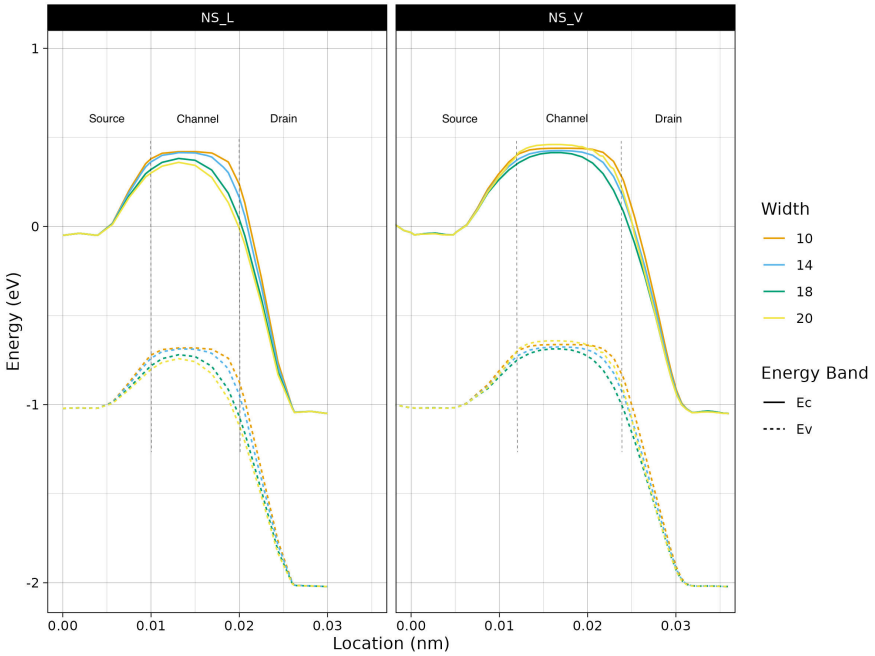
Like SS, DIBL also increases with an increase in width and radii. This is because the NW device with smaller width has enhanced control of the gate over the channel region; therefore, the drain control of the channel is reduced, resulting in a small DIBL. The results from the simulation over different structures with changes in width and radii are shown in Fig 5.5a and Fig 5.5b.

In comparison, the DIBL values without substrate are higher than with substrate meaning the addition of substrate reduced the DIBL effect.

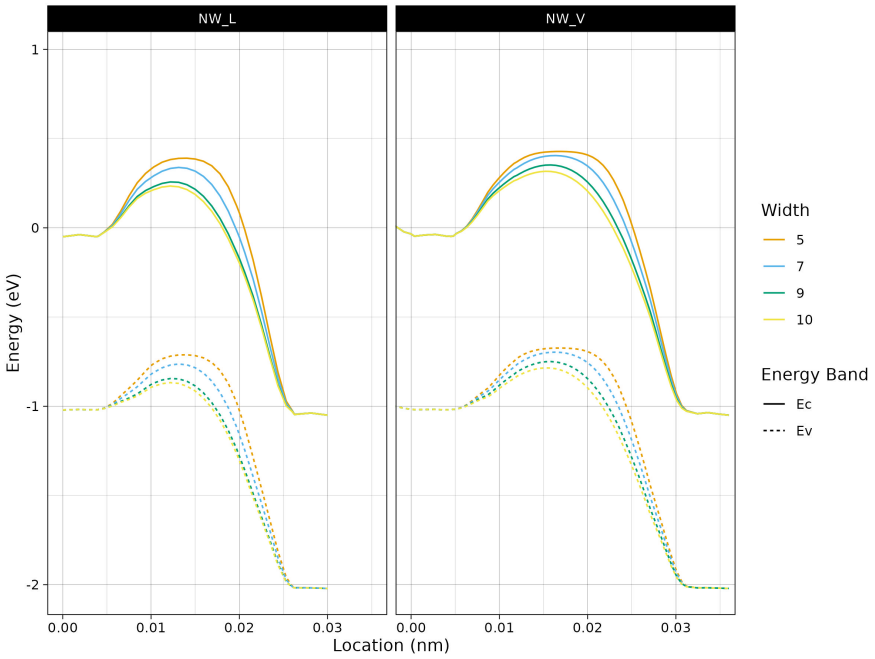
The summarised results of On and off currents, Vt, SS, and DIBL for all structures are described in the table 5.1 and 5.2.

5.3.4 *GIDL*

To perform the GIDL analysis, the simulation model is calibrated by reproducing the experimental results of [Fan *et al*. (2014)] by fine-tuning the parameters, as shown in Fig.5.6.

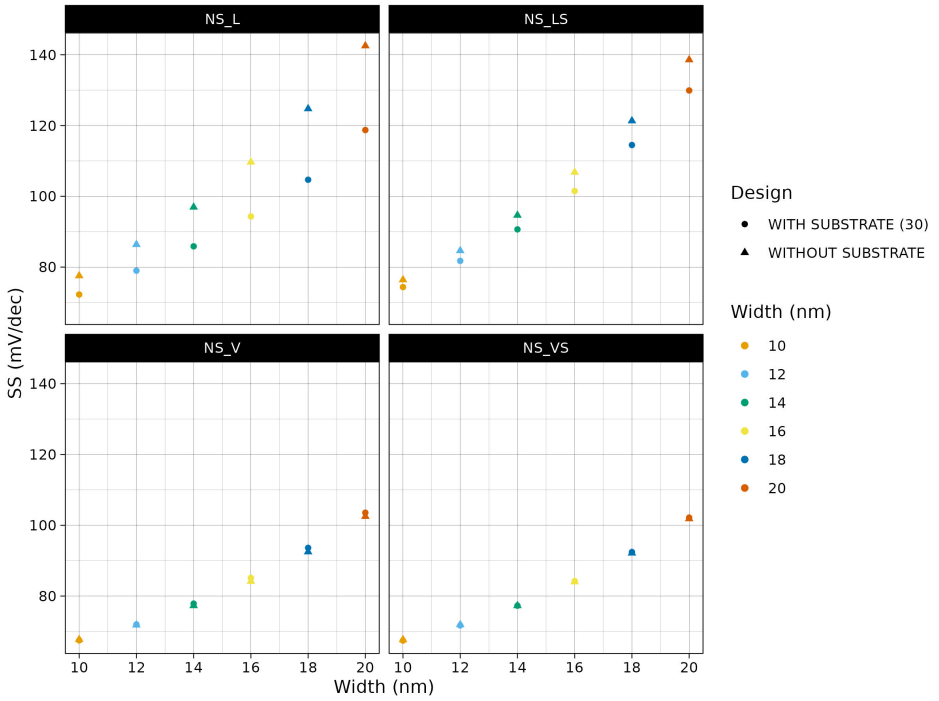


(A)

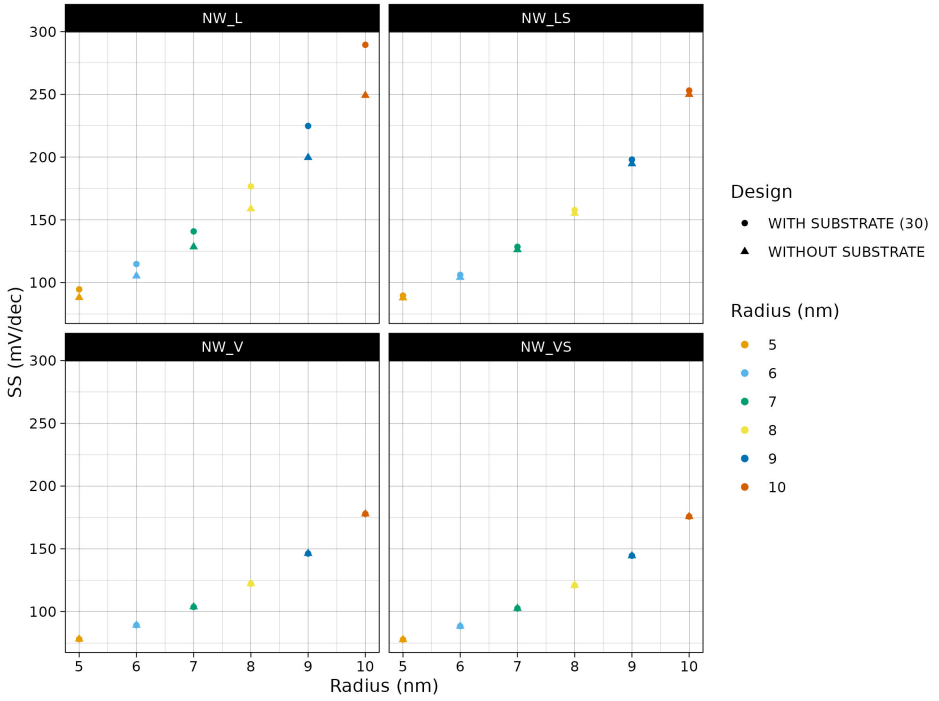


(B)

FIGURE 5.3: Energy Band Profile over different widths and radii for lateral and vertical Nanosheet and Nanowire respectively.

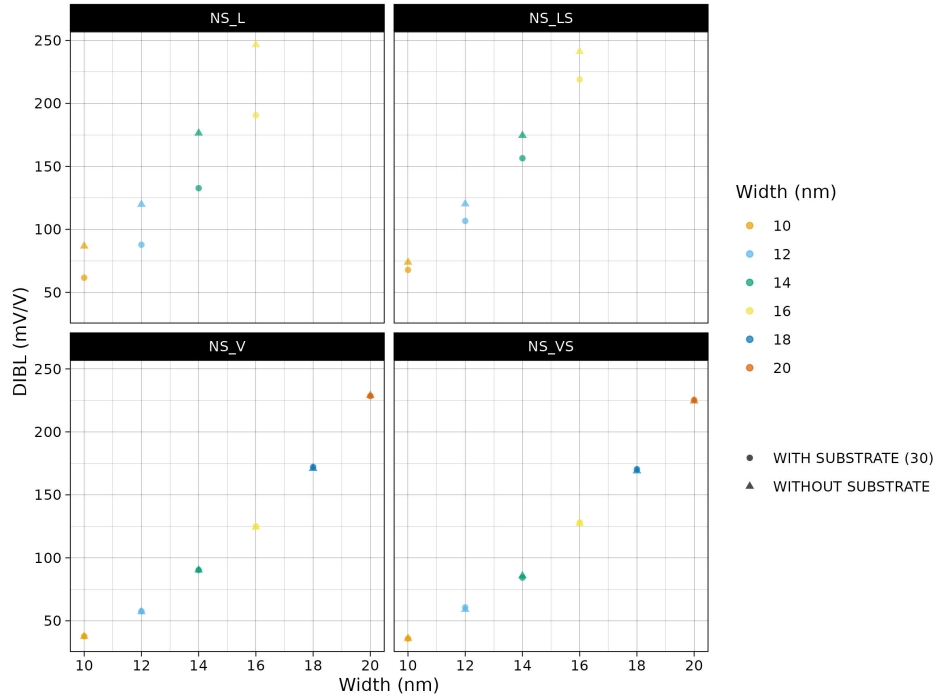


(A)

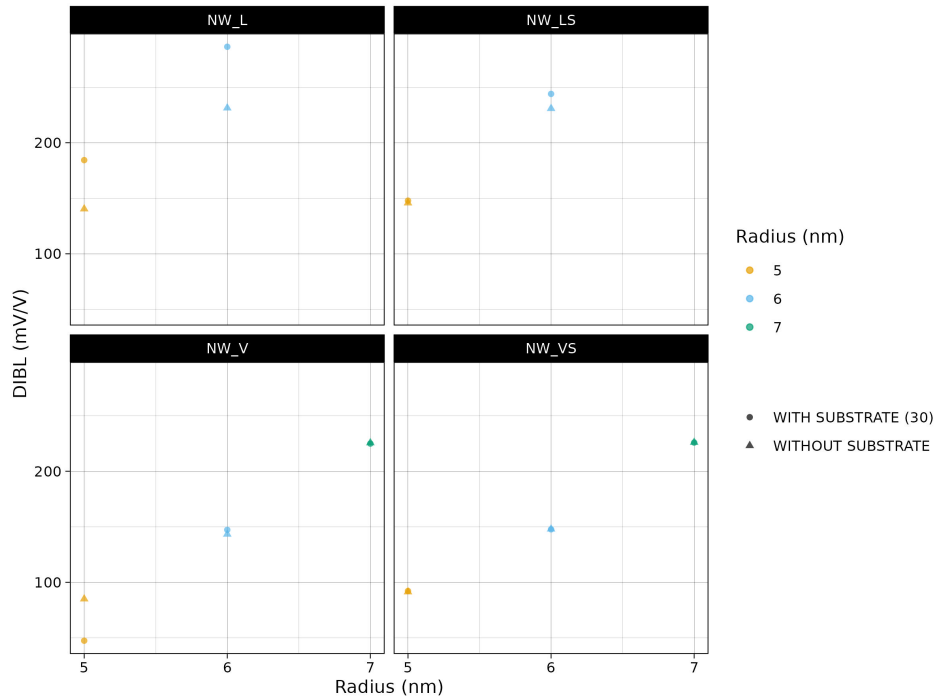


(B)

FIGURE 5.4: Subthreshold Slope over different widths and radii.



(A)



(B)

FIGURE 5.5: Drain Induced Barrier lowering (DIBL) across different widths and radii

Single	NS_L	NW_L	NS_V	NW_V
Weff(nm)	30	31	30	31
Vt (V)	0.394	0.249	0.299	0.266
Ion (μ A)	10.81	19.12	18.24	20.22
Ioff (pA)	1.465	5940	10.94	292.2
SS (mV/dec)	72.26	94.66	67.48	78.05
DIBL (mV/V)	61.60	184.36	37.74	47.43

TABLE 5.1: Comparison of Simulation Results of Single structures.

Stacked	NS_LS	NW_LS	NS_VS	NW_VS
Weff(nm)	60	63	60	63
Vt (V)	0.288	0.226	0.278	0.244
Ion (μ A)	27.91	38.59	31.14	34.11
Ioff (pA)	67.99	4441	20.54	534.5
SS (mV/dec)	74.36	89.69	67.42	77.74
DIBL (mV/V)	67.80	147.88	35.81	92.18

TABLE 5.2: Comparison of Simulation Results of Stacked structures.

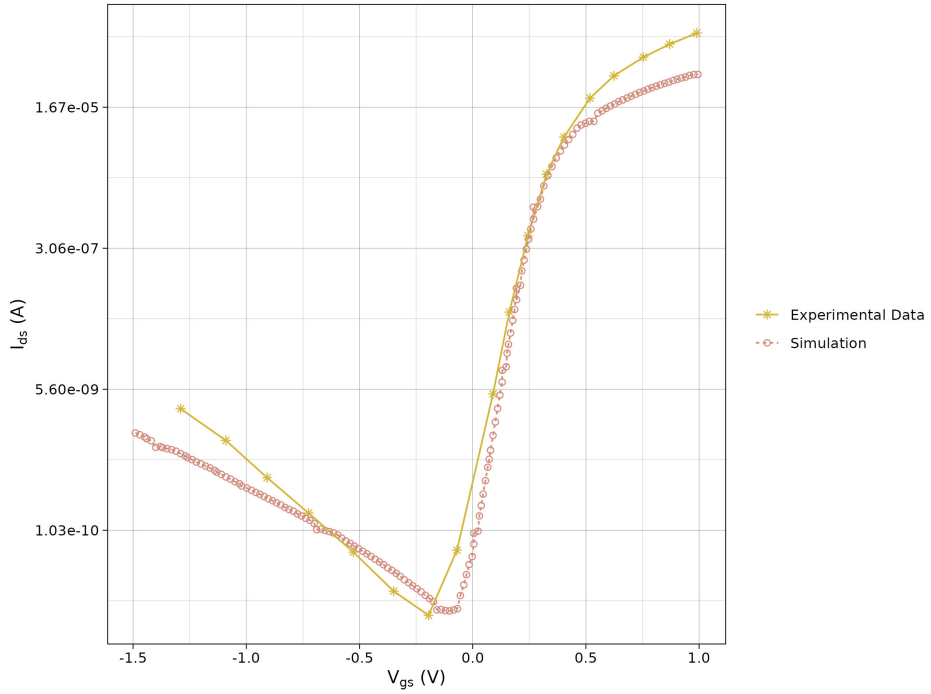


FIGURE 5.6: IV characteristics comparing experimental Fan *et al*. (2014) and simulated data

The calibration is done by sweeping Vgs from -1.5 to 1V in the NW structure with Lg set to 60nm and radii 10nm. The results obtained are comparable with the experimental data, so we proceeded with the GIDL analysis.

The GIDL phenomena can be observed by viewing the energy band profile or the leakage current with negative gate bias. A negative voltage at the gate leads to band bending at the channel leading to the movement of electrons from the channel's valance band into the drain's conduction band. Due to this electron movement, the concentration of holes in the source and the substrate regions increases; hence, the leakage current is mainly the hcurrent component of the source [Chan *et al*. (1987)]. The results from the simulation over different structures with change in width are shown in Fig 5.7.

The GIDL current for all the structures at gate voltages -1.5 and 0V are shown in the figures. It is clear from the results that at Vgs = -1.5V, the GIDL current increases as the width of the NS is swept from 10 to 20 nm. This can be proved by observing the energy band profile shown in Fig 5.8a and Fig 5.8b., the smaller W causes smaller band bending, i.e., large tunneling width as and hence less tunneling of electrons.

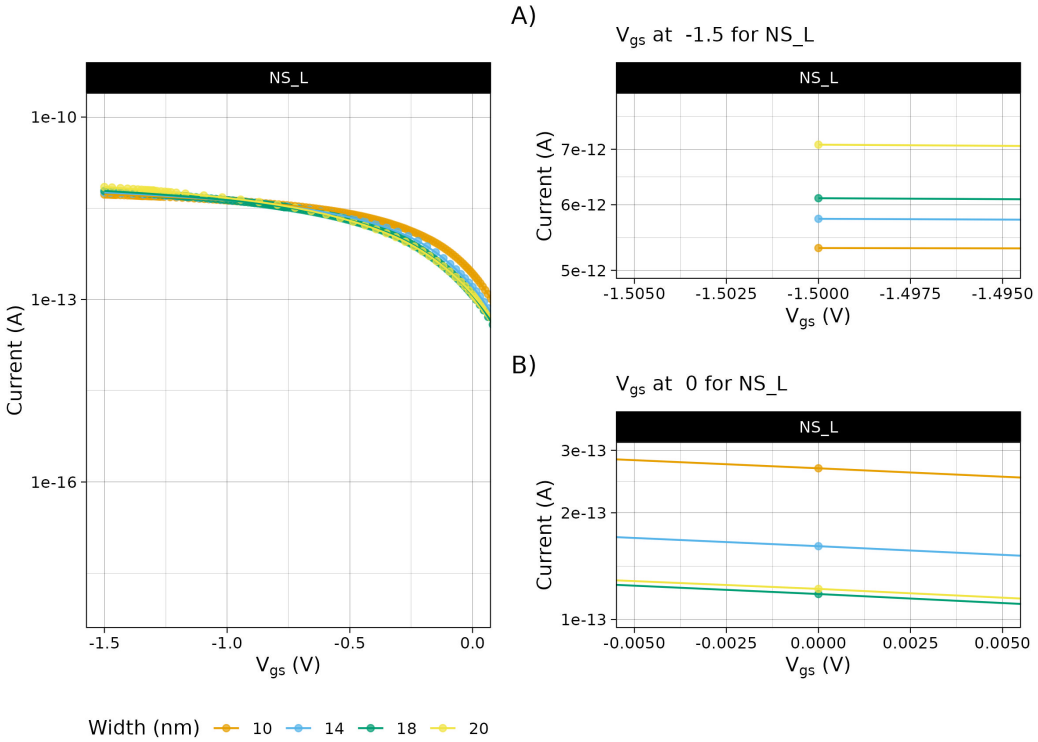
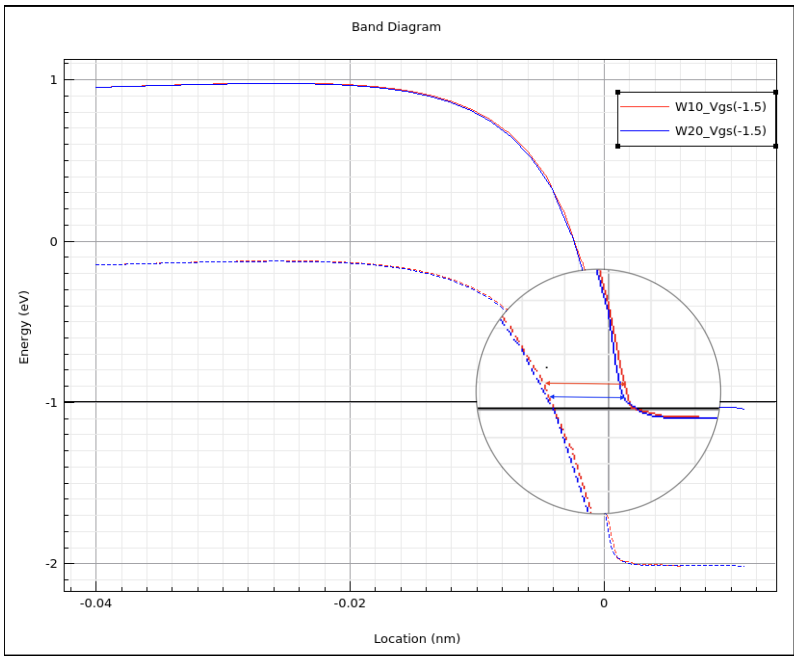
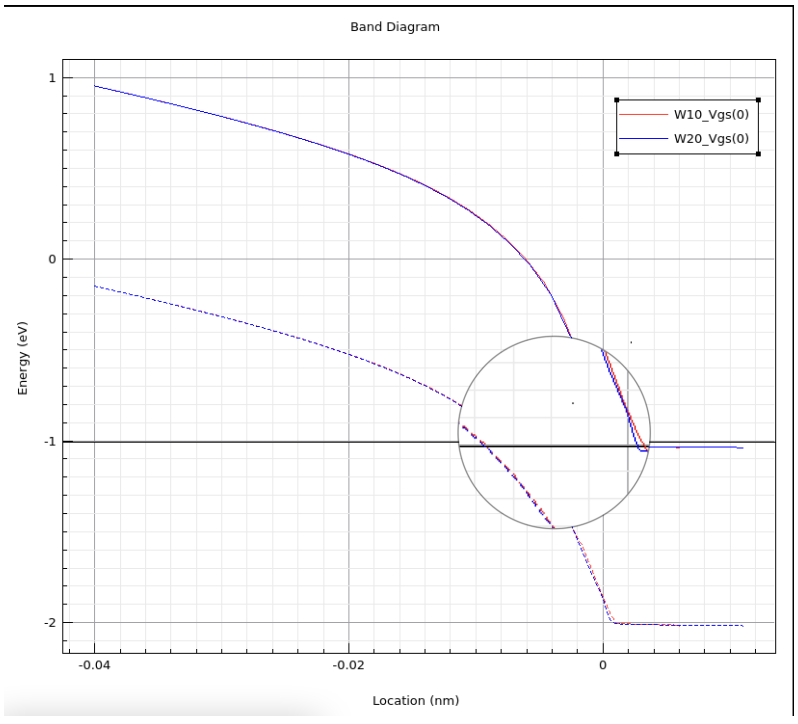


FIGURE 5.7: GIDL Current Characteristics. A and B sub plot depicts the GIDL characteristics at Vgs = -1.5V and Vgs = 0 respectively.

At Vgs = 0V, the NS with larger width experiences weak gate controllability, so there is not much of a band bending. However, as the width decreases, the gate coupling gets stronger; hence, higher tunneling occurs at smaller widths. A similar result is observed in the other NS and NW structures, which are summarised in Fig 5.9a and Fig 5.9b.

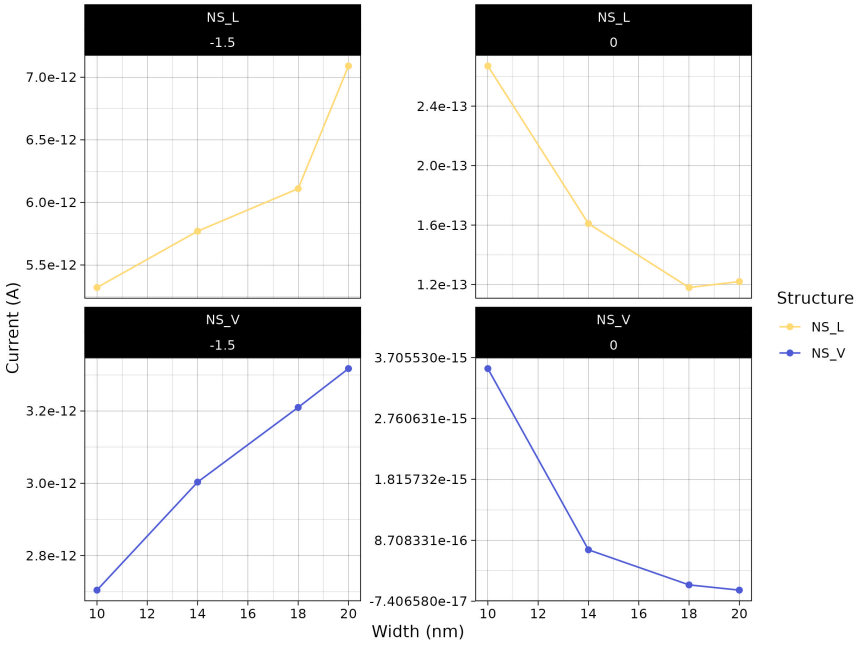


(A) Energy Band Diagram of Drain Substrate Interface at Vgs = -1.5V

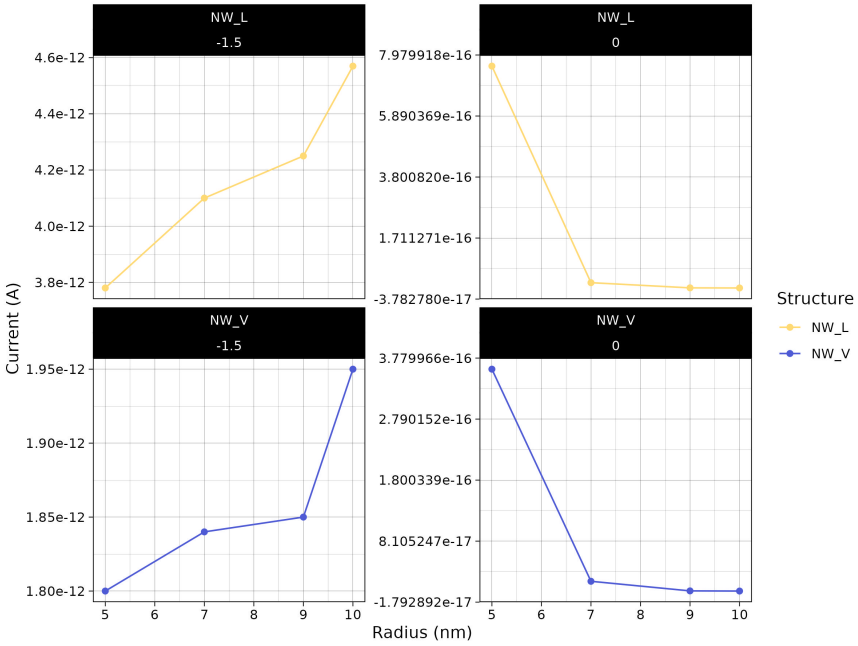


(B) Energy Band Diagram of Drain Substrate Interface at Vgs = 0

FIGURE 5.8: Energy Band Diagram of Drain Substrate Interface at different Vgs values.



(A) GIDL Current for different widths of Nanosheet at specific gate voltages.



(B) GIDL Current for different radii of Nanowire at specific gate voltages.

FIGURE 5.9: GIDL Current characteristics.

CHAPTER 6

Conclusion

6.1 SUMMARY

My thesis work involves two significant analyses. The first is the comparative analysis of ON current, Vt, SS, and DIBL with and without adding substrate. The second is the effect of process parameters like width and radii over short-channel effects like SS, DIBL, and GIDL.

Comparing the results, we can conclude that the threshold voltage values of NW are less than the NS, which implies that the Ion of NW is higher than the NS, and the results verify the same. It can be noted that Ioff for NW_L is huge and also has the worst control of SCEs with the highest values of SS and DIBL.

Overall, among the eight structures, NS_VS performs better with lower SCEs (SS and DIBL) and a comparable Ion current. Compared to Lateral GAAs, Vertical GAAs perform better, and the stacked structures can improve the Ion without increasing SCEs.

A detailed analysis of the effects of BTBT on various GAA FET devices to study the GIDL current infers that scaling down the width will help to reduce the GIDL current at high Vgs, whereas it worsens it at negative Vgs.

In the future, the GAA structures can be improved by adding spacer material and optimizing the channel material to improve performance. The capacitance effect can also be added to the analysis to extract more parameters and simulate more practical and real devices. Also, the GIDL analysis can be done on stacked structures to know more about their performance characteristics.

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APPENDIX A

Supplementary Information to Chapter 4

A.1 TCAD code for nanosheet definition

```
; Sentaurus SDE Command File
; Date: April 06, 2023
; Description:
;-------------------------------------------------;
; This cmd file makes a 3D gate-all-around Nanosheet device.
; Modifications for uniform and Gaussian doping are mentioned in
   ↪ the comments
; Structure Definitions of Lateral and Vertical NS are mentioned
   ↪ separately
; Modifications for single and stacked devices are also provided
;-------------------------------------------------;

;-------------- Parameter setup -------------------;
(define W @W@)
(define H (/ W 2))
(define tox 1)
(define tpoly 2)
;---------------------------------;
;--- Parameters for Lateral NS ---;
(define Lg 10)
(define LSDC 4)
(define LSD 6)
;--- Parameters Modified for Vertical NS ---;
(define Lg 12)
(define LSDC 4.8)
(define LSD 7.2)
```

```
;--------------------------------;
(define C_Doping 1e17)
(define SD_Doping 1e20)
(define B_Doping 1e17)
(define nm 1e-3)
(define x1 LSDC)
(define x2 (+ x1 LSD))
(define x3 (+ x2 Lg))
(define x4 (+ x3 LSD))
(define x5 (+ x4 LSDC))
(define x6 (+ x5 40))

(define y1 tox)
(define y2 (+ y1 W))
(define y3 (+ y2 tox))

(define z1 tox)
(define z2 (+ z1 H))
(define z3 (+ z2 tox))
(define z4 (+ z3 spacer))
(define z6 (+ z4 tox))
(define z7 (+ z6 H))
(define z8 (+ z7 tox))

(define b1 (- y1 0))
(define b2 (+ y2 0))
(define spacer 4)

;--------------- Structure for Lateral Nanosheet ---------------;

;--- Source Contact and Source ---;
"ABA"
```

```
(sdegeo:create-cuboid (position 0 y1 z1 ) (position x1 y2 z2 ) "
   ↪ Silicon" "SourceC")
(sdegeo:create-cuboid (position x1 y1 z1 ) (position x2 y2 z2 ) "
   ↪ Silicon" "Source")
;--- Stacked Source ---;
(sdegeo:create-cuboid (position x1 y1 z6 ) (position x2 y2 z7 ) "
   ↪ Silicon" "Source2")


;--- Gate oxide ---;
(sdegeo:create-cuboid (position x2 0 0 ) (position x3 y3 z3 ) "SiO2
   ↪ " "Gateoxide")
;--- Stacked Gate oxide ---;
(sdegeo:create-cuboid (position x2 0 z4 ) (position x3 y3 z8 ) "
   ↪ SiO2" "Gateoxide2")

;--- Channel ---;
 (sdegeo:create-cuboid (position x2 y1 z1 ) (position x3 y2 z2 ) "
    ↪ Silicon" "Channel")
;--- Stacked Channel ---;
 (sdegeo:create-cuboid (position x2 y1 z6 ) (position x3 y2 z7 ) "
    ↪ Silicon"
"Channel2")

;--- Drain Contact and Drain ---;
(sdegeo:create-cuboid (position x3 y1 z1 ) (position x4 y2 z2 ) "
   ↪ Silicon" "Drain")
(sdegeo:create-cuboid (position x4 y1 z1 ) (position x5 y2 z2 ) "
   ↪ Silicon" "DrainC")
;--- Stacked Drain ---;
(sdegeo:create-cuboid (position x3 y1 z6 ) (position x4 y2 z7 ) "
   ↪ Silicon" "Drain2")
```

```
;--- Body ---;
(sdegeo:create-cuboid (position x6 b1 z1 ) (position x5 b2 z2 ) "
   ↪ Silicon" "Body")

;--------------- Structure for Vertical Nanosheet ---------------;

;--- Source ---;
"ABA"
(sdegeo:create-cuboid (position 0 y1 z1 ) (position x1 y2 z2 ) "
   ↪ Silicon" "SourceC")
(sdegeo:create-cuboid (position x1 y1 z1 ) (position x2 y2 z2 ) "
   ↪ Silicon" "Source")
;--- Stacked Source ---;
(sdegeo:create-cuboid (position x1 y1 z6 ) (position x2 y2 z7 ) "
   ↪ Silicon" "Source2")

;--- Gate oxide ---;
(sdegeo:create-cuboid (position x2 0 0 ) (position x3 y3 z3 ) "SiO2
   ↪ " "Gateoxide")
;--- Stacked Gate Oxide ---;
(sdegeo:create-cuboid (position x2 0 z4 ) (position x3 y3 z8 ) "
   ↪ SiO2" "Gateoxide2")

;--- Channel ---;
 (sdegeo:create-cuboid (position x2 y1 z1 ) (position x3 y2 z2 ) "
    ↪ Silicon" "Channel")
 ;--- Stacked Channel ---;
(sdegeo:create-cuboid (position x2 y1 z6 ) (position x3 y2 z7 ) "
   ↪ Silicon"
"Channel2")

;--- Drain ---;
```

```
(sdegeo:create-cuboid (position x3 y1 z1 ) (position x4 y2 z2 ) "
   ↪ Silicon" "Drain")
(sdegeo:create-cuboid (position x4 y1 z1 ) (position x5 y2 z2 ) "
   ↪ Silicon" "DrainC")
;--- Stacked Drain ---;
(sdegeo:create-cuboid (position x3 y1 z6 ) (position x4 y2 z7 ) "
   ↪ Silicon" "Drain2")

;--- Si Body ---;
(sdegeo:create-cuboid (position x6 b1 z1 ) (position x5 b2 z2 ) "
   ↪ Silicon" "Body")

;--------------- Contact Definition ---------------;

;----- Gate -----;
(sdegeo:define-contact-set "G" 4.0 (color:rgb 1.0 0.0 0.0 ) "||" )
(sdegeo:set-current-contact-set "G")
(sdegeo:set-contact-faces (find-face-id (position (+ x2 1) (+ y1 1)
   ↪  z3 )))

(sdegeo:define-contact-set "G" 4.0 (color:rgb 1.0 0.0 0.0 ) "||" )
(sdegeo:set-current-contact-set "G")
(sdegeo:set-contact-faces (find-face-id (position (+ x2 1) (+ y1 1)
   ↪  0 )))

(sdegeo:define-contact-set "G" 4.0 (color:rgb 1.0 0.0 0.0 ) "||" )
(sdegeo:set-current-contact-set "G")
(sdegeo:set-contact-faces (find-face-id (position (+ x2 1) 0 z1 )))

(sdegeo:define-contact-set "G" 4.0 (color:rgb 1.0 0.0 0.0 ) "||" )
(sdegeo:set-current-contact-set "G")
(sdegeo:set-contact-faces (find-face-id (position (+ x2 1) y3 z1 ))
   ↪ )
```

```
;----- Stacked Gate -----;
(sdegeo:define-contact-set "G" 4.0 (color:rgb 1.0 0.0 0.0 ) "||" )
(sdegeo:set-current-contact-set "G")
(sdegeo:set-contact-faces
(find-face-id (position (+ x2 1) (+ y1 1) z8 )))

(sdegeo:define-contact-set "G" 4.0 (color:rgb 1.0 0.0 0.0 ) "||" )
(sdegeo:set-current-contact-set "G")
(sdegeo:set-contact-faces
(find-face-id (position (+ x2 1) (+ y1 1) z4 )))

(sdegeo:define-contact-set "G" 4.0 (color:rgb 1.0 0.0 0.0 ) "||" )
(sdegeo:set-current-contact-set "G")
(sdegeo:set-contact-faces
(find-face-id (position (+ x2 1) 0 z7 )))

(sdegeo:define-contact-set "G" 4.0 (color:rgb 1.0 0.0 0.0 ) "||" )
(sdegeo:set-current-contact-set "G")
(sdegeo:set-contact-faces
(find-face-id (position (+ x2 1) y3 z7 )))

;----- Drain -----;
(sdegeo:define-contact-set "D" 4.0 (color:rgb 1.0 0.0 0.0 ) "##" )
(sdegeo:set-current-contact-set "D")
(sdegeo:set-contact-faces (find-face-id (position (+ x4 (/ LSDC 2))
   ↪  (- y2 1) z2 )))

;----- Source -----;
(sdegeo:define-contact-set "S" 4.0 (color:rgb 1.0 0.0 0.0 ) "##" )
(sdegeo:set-current-contact-set "S")
(sdegeo:set-contact-faces (find-face-id (position (- x1 1) (- y2 1)
   ↪  z2 )))
```

```
;----- Body -----;
(sdegeo:define-contact-set "B" 4.0 (color:rgb 1.0 1.0 0.0 ) "##" )
(sdegeo:set-current-contact-set "B")
(sdegeo:set-contact-faces (find-face-id (position x6 (- b2 1) (- z2
   ↪  1))))

;--------------- Doping ---------------;

;----- Channel -----;
(sdedr:define-constant-profile "dopedC" "BoronActiveConcentration"
   ↪ C_Doping )
(sdedr:define-constant-profile-region "RegionC" "dopedC" "Channel"
   ↪ )
;----- Stacked Channel -----;
(sdedr:define-constant-profile "dopedC2" "BoronActiveConcentration"
   ↪  C_Doping)
(sdedr:define-constant-profile-region "RegionC2" "dopedC2" "
   ↪ Channel2" )

;----- Source (Uniform Doping - preliminary analysis) -----;
(sdedr:define-constant-profile "dopedS" "ArsenicActiveConcentration
   ↪ " SD_Doping )
(sdedr:define-constant-profile-region "RegionS" "dopedS" "Source" )
;----- Stacked Source -----;
(sdedr:define-constant-profile "dopedS2" "
   ↪ ArsenicActiveConcentration" SD_Doping )
(sdedr:define-constant-profile-region "RegionS2" "dopedS2" "Source2
   ↪ " )

;----- Source (Gaussian Doping - GIDL analysis) -----;
(sdedr:define-refeval-window "B.Source" "Cuboid" (position 0 y1 z1
   ↪ ) (position x1 y2 z2 ))
```

```
(sedr:define-gaussian-profile "Gauss.Source" "
   ↪ ArsenicActiveConcentration" "PeakPos" 0 "PeakVal" SD_Doping
"ValueAtDepth" C_Doping "Depth" spacer "Gauss" "Factor" 0.08)
(sedr:define-analytical-profile-placement "AP.Source" "Gauss.
   ↪ Source" "B.Source" "Positive" "NoReplace" "Eval")

;----- Source Contact -----;
(sedr:define-constant-profile "dopedSC" "
   ↪ ArsenicActiveConcentration" SD_Doping )
(sedr:define-constant-profile-region "RegionSC" "dopedSC" "SourceC
   ↪ " )

;----- Drain (Uniform Doping - preliminary analysis) ------;
(sedr:define-constant-profile "dopedD" "ArsenicActiveConcentration
   ↪ " SD_Doping )
(sedr:define-constant-profile-region "RegionD" "dopedD" "Drain" )
;----- Stacked Drain -----;
(sedr:define-constant-profile "dopedD2" "
   ↪ ArsenicActiveConcentration" SD_Doping )
(sedr:define-constant-profile-region "RegionD2" "dopedD2" "Drain2"
   ↪  )

;----- Drain (Gaussian Doping - GIDL analysis) -----;
(sedr:define-refeval-window "B.Drain" "Cuboid" (position x4 y1 z1
   ↪ ) (position x5 y2 z2 ))
(sedr:define-gaussian-profile "Gauss.Drain" "
   ↪ ArsenicActiveConcentration" "PeakPos" 0 "PeakVal" SD_Doping
"ValueAtDepth" C_Doping "Depth" spacer "Gauss" "Factor" 0.08)
 sedr:define-analytical-profile-placement "AP.Drain" "Gauss.Drain"
    ↪  "B.Drain" "Positive" "NoReplace" "Eval")

;----- Drain Contact -----;
```

```
(sdedr:define-constant-profile "dopedDC" "
   ↪ ArsenicActiveConcentration" SD_Doping )
(sdedr:define-constant-profile-region "RegionDC" "dopedDC" "DrainC"
   ↪  )

;----- Body -----;
(sdedr:define-constant-profile "dopedB" "BoronActiveConcentration"
   ↪ B_Doping )
(sdedr:define-constant-profile-region "RegionB" "dopedB" "Body" )

;--------------- Mesh ---------------;
;--- AllMesh ---;
(sdedr:define-refinement-size "Cha_Mesh" 2 2 2 2 2 2)
(sdedr:define-refinement-material "channel_RF" "Cha_Mesh" "Silicon"
   ↪  )
;--- ChannelMesh ---;
(sdedr:define-refinement-window "multiboxChannel" "Cuboid" (
   ↪ position 30 y1 z1) (position (+ 30 Lg) y2 z2) )
(sdedr:define-multibox-size "multiboxSizeChannel" 1 1 1 0.1 0.1
   ↪ 0.1)
(sdedr:define-multibox-placement "multiboxPlacementChannel"
"multiboxSizeChannel" "multiboxChannel")
(sdedr:define-refinement-function "multiboxPlacementChannel"
"DopingConcentration" "MaxTransDiff" 1)

;--- Mest for Stack structure ---;
(sdedr:define-refinement-window "multiboxChannel2" "Cuboid"
(position 30 y1 z6)
(position (+ 30 Lg) y2 z7) )
(sdedr:define-multibox-size "multiboxSizeChannel2" 1 1 1 0.1 0.1
   ↪ 0.1)
(sdedr:define-multibox-placement "multiboxPlacementChannel2"
"multiboxSizeChannel2" "multiboxChannel2")
```

```
(sdedr:define-refinement-function "multiboxPlacementChannel2"
"DopingConcentration" "MaxTransDiff" 1)

;--------------- Save BND and CMD and rescale to nm
   ↪ ---------------;

(sde:assign-material-and-region-names (get-body-list) )
(sdeio:save-tdr-bnd (get-body-list) "n@node@_nm.tdr")
(sdedr:write-scaled-cmd-file "n@node@_msh.cmd" nm) (define sde:
   ↪ scale-tdr-bnd (lambda (tdrin sf tdrout)
(sde:clear)
(sdegeo:set-default-boolean "XX")
(sdeio:read-tdr-bnd tdrin) (entity:scale (get-body-list) sf)
(sdeio:save-tdr-bnd (get-body-list) tdrout) ))
(sde:scale-tdr-bnd "n@node@_nm.tdr" nm "n@node@_bnd.tdr")

;--------------- END ---------------;



% Text enclosed inside \texttt{verbatim} environment
% is printed directly
% and all \LaTeX{} commands are ignored.
```

A.2 TCAD CODE FOR NANOWIRE DEFINITION

```
; Sentaurus SDE Command File
; Date: April 06, 2023
; Description:
;-------------------------------------------------;
; This cmd file makes a 3D gate-all-around Nanowire device.
```

```
; Modifications for uniform and Gaussian doping are mentioned in
   ↪ the comments
; Structure Definitions of Lateral and Vertical NW are mentioned
   ↪ separately
; Modifications for single and stacked devices are also provided
;-------------------------------------------------;

;-------------- Parameter setup -------------------;
(define r @r@)
(define tox 1)
(define tpoly 2)
;--------------------------------;
;--- Parameters for Lateral NW ---;
(define Lg 10)
(define LSDC 4)
(define LSD 6)
;--- Parameters Modified for Vertical NW ---;
(define Lg 12)
(define LSDC 4.8)
(define LSD 7.2)
;--------------------------------;
(define C_Doping 1e17)
(define B_Doping 1e17)
(define SD_Doping 1e20)
(define nm 1e-3)
(define x1 LSDC)
(define x2 (+ x1 LSD))
(define x3 (+ x2 Lg))
(define x4 (+ x3 LSD))
(define x5 (+ x4 LSDC))
(define r1 (+ r tox))

(define edge 2)
```

```
(define spacer 4)

(define y1 tox)
(define y2 (+ y1 r))
(define y3 (+ y2 tox))

(define z1 (+ r1 spacer))
(define z2 (+ z1 r1))
(define z3 (+ z2 r1))
(define z4 (+ z3 edge))
(define z5 (- 0 r1))
(define z6 (- z5 edge))
(define z7 (+ z1 tox))
(define z8 (+ 0 r1))
(define z9 (- z5 20))

(define y4 (- 0 r1))
(define y5 (- y1 tpoly))
(define y6 (+ 0 r1))
(define y7 (+ y3 tpoly))

(define b1 (- y4 0))
(define b2 (+ y2 0))

;--------------- Structure for Lateral Nanowire ---------------;

;--- Source Contact and Source ---;
(sdegeo:create-cuboid (position 0 y4 z5) (position x1 y2 z8) "
   ↪ Silicon" "SourceC")
(sdegeo:create-cylinder (position x1 0 0) (position x2 0 0) r "
   ↪ Silicon" "Source")

;--- Channel ---;
```

```
(sdegeo:create-cylinder (position x2 0 0) (position x3 0 0) r "
   ↪ Silicon" "Channel" )

;--- Gate Oxide ---;
(sdegeo:set-default-boolean "BAB")
(sdegeo:create-cylinder (position x2 0 0) (position x3 0 0) r1 "
   ↪ SiO2" "GateOxide" )

;--- Drain Contact and Drain ---;
(sdegeo:create-cylinder (position x3 0 0) (position x4 0 0) r "
   ↪ Silicon" "Drain")
(sdegeo:create-cuboid (position x4 y4 z5) (position x5 y2 z8) "
   ↪ Silicon" "DrainC")

;--- Body ---;
(sdegeo:create-cuboid (position 0 y2 z5 ) (position x5 y4 (- z5 40)
   ↪ ) "Silicon" "Body")

;--------------- Structure for Vertical Nanowire ---------------;

;--- Source Contact and Source ---;
(sdegeo:create-cuboid (position 0 y2 z6) (position x1 y4 z4 ) "
   ↪ Silicon" "SourceC")
(sdegeo:create-cylinder (position x1 0 0) (position x2 0 0) r "
   ↪ Silicon" "Source1")
;--- Stacked Source ---;
(sdegeo:create-cylinder (position x1 0 z2) (position x2 0 z2) r "
   ↪ Silicon" "Source2")

;--- Channel ---;
(sdegeo:create-cylinder (position x2 0 0) (position x3 0 0) r "
   ↪ Silicon" "Channel1" )
;--- Stacked Channel ---;
```

```
(sdegeo:create-cylinder (position x2 0 z2) (position x3 0 z2) r "
   ↪ Silicon" "Channel2" )
(sdegeo:set-default-boolean "BAB")

;--- Gate Oxide ---;
(sdegeo:create-cylinder (position x2 0 0) (position x3 0 0) r1 "
   ↪ SiO2" "GateOxide1" )
;--- Stacked Gate Oxide ---;
(sdegeo:create-cylinder (position x2 0 z2) (position x3 0 z2) r1 "
   ↪ SiO2" "GateOxide2" )

;--- Drain Contact and Drain ---;
(sdegeo:create-cylinder (position x3 0 0) (position x4 0 0) r "
   ↪ Silicon" "Drain1")
;--- Stacked Drain ---;
(sdegeo:create-cylinder (position x3 0 z2) (position x4 0 z2) r "
   ↪ Silicon" "Drain2")
(sdegeo:create-cuboid (position x4 y2 z6) (position x5 y4 z4 ) "
   ↪ Silicon" "DrainC")

;--- Body ---;
(sdegeo:create-cuboid (position -30 y2 z6 ) (position 0 y4 z4 ) "
   ↪ Silicon" "Body")

;--------------- Doping ---------------;

;----- Channel -----;
(sdedr:define-constant-profile "dopedC" "BoronActiveConcentration"
   ↪ C_Doping )
(sdedr:define-constant-profile-region "RegionC" "dopedC" "Channel"
   ↪ )
;----- Stacked Channel -----;
```

```
(sdedr:define-constant-profile "dopedC2" "BoronActiveConcentration"
   ↪  C_Doping )
(sdedr:define-constant-profile-region "RegionC2" "dopedC2" "
   ↪ Channel2" )

;----- Source (Uniform Doping - preliminary analysis) -----;
(sdedr:define-constant-profile "dopedS" "ArsenicActiveConcentration
   ↪ " SD_Doping )
(sdedr:define-constant-profile-region "RegionS" "dopedS" "Source" )
(sdedr:define-constant-profile "dopedSC" "
   ↪ ArsenicActiveConcentration" SD_Doping )
(sdedr:define-constant-profile-region "RegionSC" "dopedSC" "SourceC
   ↪ " )
;----- Stacked Source -----;
(sdedr:define-constant-profile "dopedS2" "
   ↪ ArsenicActiveConcentration" SD_Doping )
(sdedr:define-constant-profile-region "RegionS2" "dopedS2" "Source2
   ↪ " )

;----- Source (Gaussian Doping - GIDL analysis) -----;
(sdedr:define-refeval-window "B.Source" "Cuboid" (position 0 y4 z5)
   ↪  (position x1 y2 z8))
(sdedr:define-gaussian-profile "Gauss.Source" "
   ↪ ArsenicActiveConcentration" "PeakPos" 0 "PeakVal" SD_Doping
"ValueAtDepth" C_Doping "Depth" spacer "Gauss" "Factor" 0.08)
(sdedr:define-analytical-profile-placement "AP.Source" "Gauss.
   ↪ Source" "B.Source" "Positive" "NoReplace" "Eval")

;----- Drain (Uniform Doping - preliminary analysis) -----;
(sdedr:define-constant-profile "dopedD" "ArsenicActiveConcentration
   ↪ " SD_Doping )
(sdedr:define-constant-profile-region "RegionD" "dopedD" "Drain" )
```

```
(sdedr:define-constant-profile "dopedDC" "
   ↪ ArsenicActiveConcentration" SD_Doping )
(sdedr:define-constant-profile-region "RegionDC" "dopedDC" "DrainC"
   ↪  )
;----- Stacked Drain -----;
(sdedr:define-constant-profile "dopedD2" "
   ↪ ArsenicActiveConcentration" SD_Doping )
(sdedr:define-constant-profile-region "RegionD2" "dopedD2" "Drain2"
   ↪  )

;----- Drain (Gaussian Doping - GIDL analysis) -----;
(sdedr:define-refeval-window "B.Drain" "Cuboid" (position x4 y4 z5)
   ↪  (position x5 y2 z8))
(sdedr:define-gaussian-profile "Gauss.Drain" "
   ↪ ArsenicActiveConcentration" "PeakPos" 0 "PeakVal" SD_Doping
"ValueAtDepth" C_Doping "Depth" spacer "Gauss" "Factor" 0.08)
(sdedr:define-analytical-profile-placement "PlaceAP.Drain" "Gauss.
   ↪ Drain" "B.Drain" "Positive" "NoReplace" "Eval")

;----- Body -----;
(sdedr:define-constant-profile "dopedB" "BoronActiveConcentration"
   ↪ B_Doping )
(sdedr:define-constant-profile-region "RegionB" "dopedB" "Body" )

;--------------- Contact Definition ---------------;

;----- Source -----;
(sdegeo:define-contact-set "S" 4.0 (color:rgb 1.0 0.0 0.0 ) "##" )
(sdegeo:set-current-contact-set "S")
(sdegeo:set-contact(find-face-id (position (/ x1 2) 0 z8 )))

;----- Gate -----;
(sdegeo:define-contact-set "G" 4.0 (color:rgb 1.0 0.0 0.0 ) "##" )
```

```
(sdegeo:set-current-contact-set "G")
(sdegeo:define-3d-contact(list(car(find-face-id (position (+ x2 (/
   ↪ Lg 2)) (+ r tox) 0 ))))"G")
;----- Stacked Gate -----;
(sdegeo:define-contact-set "G" 4.0 (color:rgb 1.0 0.0 0.0 ) "##" )
(sdegeo:set-current-contact-set "G")
(sdegeo:define-3d-contact(list(car(find-face-id (position (+ x2 (/
   ↪ Lg 2)) (+ r tox)
z9 ))))"G")

;----- Drain -----;
(sdegeo:define-contact-set "D" 4.0 (color:rgb 1.0 0.0 0.0 ) "##" )
(sdegeo:set-current-contact-set "D")
(sdegeo:set-contact(find-face-id (position (+ x4 (/ LSDC 2)) 0
z8 )))

;----- Body -----;
(sdegeo:define-contact-set "B" 4.0 (color:rgb 1.0 1.0 0.0 ) "##" )
(sdegeo:set-current-contact-set "B")
(sdegeo:set-contact-faces (find-face-id (position (* 0.5 x5) 5 (-
   ↪ z5 40) )))

;--------------- Mesh ---------------;

;--- AllMesh ---;
(sdedr:define-refinement-size "Cha_Mesh" 2 2 2 1 1 1)
(sdedr:define-refinement-material "channel_RF" "Cha_Mesh" "Silicon"
   ↪  )
;--- ChannelMesh ---;
(sdedr:define-refinement-window "multiboxChannel" "Cuboid"
(position x1 r r) (position x4 (- r) (- r)) )
(sdedr:define-multibox-size "multiboxSizeChannel" 1 1 1 1 1 1)
(sdedr:define-multibox-placement "multiboxPlacementChannel"
```

```
"multiboxSizeChannel" "multiboxChannel")
(sdedr:define-refinement-function "multiboxPlacementChannel"
"DopingConcentration" "MaxTransDiff" 1)

;--- Stacked ChannelMesh ---;
(sdedr:define-refinement-window "multiboxChannel2" "Cuboid"
(position x1 r z7)
(position x4 (- r) z8 ))
(sdedr:define-multibox-size "multiboxSizeChannel2" 1 1 1 1 1 1)
(sdedr:define-multibox-placement "multiboxPlacementChannel2"
"multiboxSizeChannel2" "multiboxChannel2")



;--------------- Save BND and CMD and rescale to nm
   ↪ ---------------;

(sde:assign-material-and-region-names (get-body-list) )
(sdeio:save-tdr-bnd (get-body-list) "n@node@_nm.tdr")
(sdedr:write-scaled-cmd-file "n@node@_msh.cmd" nm)
(define sde:scale-tdr-bnd(lambda (tdrin sf tdrout)
(sde:clear)
(sdegeo:set-default-boolean "XX")
(sdeio:read-tdr-bnd tdrin)
(entity:scale (get-body-list) sf)
(sdeio:save-tdr-bnd (get-body-list) tdrout)
))
(sde:scale-tdr-bnd "n@node@_nm.tdr" nm "n@node@_bnd.tdr")
;--------------- END ---------------;

% Text enclosed inside \texttt{verbatim} environment
% is printed directly
% and all \LaTeX{} commands are ignored.
```

A.3 SENTAURUS DEVICE SETTINGS

```
* Sentaurus Device Command File
* Date: April 06, 2023
* Description:
;-------------------------------------------------;
; This cmd file is used to add equations to model the
   ↪ characteristics and solve them.
; Common for all the structures
;-------------------------------------------------;
;--------------- File Section ---------------;
File{
Grid="@tdr@"
Plot="@tdrdat@"
Current="@plot@"
Output="@log@"
Parameter = "sdevice.par"
}

Electrode {
{ name="S" Voltage=0.0 }
{ name="D" Voltage=0.0 }
{ name="G" Voltage=0 WorkFunction=@WK@}
{ name="B" Voltage=0.0 }
}

;--------------- Physics section ---------------;
Physics{
Mobility( DopingDep HighFieldSaturation Enormal BalMob(KVM Fermi
   ↪ Frensley))
EffectiveIntrinsicDensity( OldSlotboom )
Recombination ( SRH( DopingDep ) Auger Band2BandTunneling(
   ↪ NonlocalPath1) )
}
```

```
;--------------- Math Section ---------------;
Math {
Method= ILS(set=24) ILSrc= "set (24) {iterative (gmres(150), tolrel
    ↪ =1e-10, maxit=300);preconditioning(ilut(1e-5,-1),left);
    ↪ ordering(symmetric=nd, nonsymmetric=mpsilst);options(verbose
    ↪ =0, refineresidual=10, prep=1, pdeg=2);};"}

Math{
-ExitOnUnknownParameterRegion
Extrapolate
Derivatives
RelErrControl
Digits=5
ErRef(electron)=1.e10
ErRef(hole)=1.e10
Notdamped=50
Iterations=10
Directcurrent
Parallel= 4
Number_of_Threads = 4
Number_of_Assembly_Threads = 4
Number_of_Solver_Threads = 4
NaturalBoxMethod
Stacksize=200000000
}

;--------------- Plot Section ---------------;
Plot{
eDensity hDensity
eCurrent hCurrent
TotalCurrent/Vector eCurrent/Vector hCurrent/Vector
eMobility hMobility
```

```
eVelocity hVelocity
eBarrierTunneling hBarrierTunneling
eEnormal hEnormal
ElectricField/Vector Potential SpaceCharge
eQuasiFermi hQuasiFermi
Potential Doping SpaceCharge
SRH Auger eBand2BandGeneration hBand2BandGeneration
    ↪ Band2BandGeneration
AvalancheGeneration
DonorConcentration AcceptorConcentration
Doping
eGradQuasiFermi/Vector hGradQuasiFermi/Vector
eEparallel hEparalllel
BandGap
BandGapNarrowing
Affinity
ConductionBand ValenceBand
}

 ;--------------- Solve Section ---------------;
Solve
{
* EQUILIBRIUM
Coupled ( Iterations =100 LineSearchDamping =1e-4) { Poisson
    ↪ hQuantumPotential }
Coupled ( Iterations =100) { Poisson hQuantumPotential }
* TURN -ON
* increasing VDS to goal
quasistationary ( InitialStep = 0.010 MaxStep = 0.05 MinStep =1e-6
    ↪ Increment= 1.4 Decrement= 2
Goal { name = "D" voltage = @Vd@ }
)
{ coupled { poisson electron hole hQuantumPotential } }
```

```
* increasing VGS to goal
quasistationary ( InitialStep = 0.010 MaxStep = 0.05 MinStep =1e-6
    ↪ Increment= 1.4 Decrement= 2
Goal { name = "G" voltage = @Vg@ }
)
{ coupled { poisson electron hole hQuantumPotential } }
}

;--------------- END ---------------;
```

APPENDIX B

Publication

Li, F., Raveendran, S. (2022, May). Wirebonding based 3-D SiC IC stacks for high temperature applications. In 2022 IEEE 72nd Electronic Components and Technology Conference (ECTC) (pp. 2023-2027). IEEE.