Overlapping Soft Comparators for High-Speed and Accurate ADCs

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Abstract

Comparators are one of the main building blocks in ADCs and there are quite a few techniques for designing high-quality Comparators. Nevertheless, when two inputs of a comparator are very close to each other, perfect device-matching is required to reduce offset. Noise can also cause meta-stability and degrades the precision, and it takes a very long time for the comparator to settle down, which adversely impacts the conversion time and throughput of the ADCs. Furthermore, designing a large number of high quality comparators is not affordable, which explains why high-resolution Flash ADCs are not common. To address the aforementioned problem, in this work a new comparator design is proposed, named as the Soft Comparator. In the proposed Soft Comparator, the settling time is exploited to generate multiple bits instead of only one bit. This allows reducing the number of comparators in designing high resolution Flash ADCs by a big factor. It is capable of alleviating meta-stability and offset problems by relying on adjacent comparators that overlap with each other. Ultimately, it can speed up the data conversion time as the longest settling time will not be relevant anymore.

Acknowledgements

I wish to thank my major professor Dr. Saied Hemati for providing me the opportunity to conduct my Masters research under his supervision, for guiding and supporting me throughout my graduate research work, for providing me the laboratory facilities, for giving technical advices and finally for having patience on my abilities.
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I would also like to thank Ph.D. student Hossein Mani for helping me in Soft Comparator Noise Analysis.
Finally, I would like to thank my mother for her prayers, constant mental support and encouragement throughout my life.

Dedication

This work is dedicated to my parents,
Md. Tajul Islam and Dilruba Islam, who have provided me constant support and encouragement during difficult periods of my graduate school and life.
This work is also dedicated to all the freedom fighters of Liberation War in 1971, who sacrificed their lives for my beloved motherland Bangladesh.

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CHAPTER 1

Introduction

A comparator is a circuit which detects whether a signal is larger or smaller than another signal, or larger than zero or not. It is the second most widely used electronic circuit after operational amplifier (OpAmp). The principle application of comparators lie in designing analog-to-digital converter (ADC) circuits. Among others, data transmission, switching power regulators, threshold & zero crossing detectors, relaxation oscillators, level shifters are some of the most important applications. Thus to meet different application requirements, comparators must meet different key specifications like offset, noise, speed, power, hysteresis to name a few. A good comparator should possess good decision making speed, low error, low power consumption, and be easy to design.

1.1 MOTIVATION AND BACKGROUND

Analog-to-digital converters (ADCs) have different important applications in communications, sensors, music technology, microcontrollers, software defined radios, medical fields, etc. Comparators are one of the main building blocks in analog-to-digital converters (ADCs). A comparator compares two analog input signals, or compares a single analog signal to zero and produces a single bit output (hard comparators), which is one or zero. Comparators perform better when the difference between the inputs is large. This makes the comparator fast and reduces error and as a result ADCs can also be fast. There are some reasons behind this fact. First of all, the positive feedback builds up quickly that increases the comparator speed. Secondly, the small offset voltages due to device mismatch will not change the final decision and thirdly, the likelihood of meta-stability due to noise will be negligible. Unfortunately, in high resolution ADCs the voltage difference between the inputs is very small which is why the comparator needs a long settling time. It is a fundamental challenge to design a comparator which can be capable of comparing two very close signals

without meta-stability, with good speed and accuracy. Also to build a high resolution Flash ADC, it is necessary to design a large number of accurate comparators, which is the reason behind difficulties in designing high resolution Flash ADCs.

1.2 CONTRIBUTIONS

There are different types of comparator circuits available. All these comparators compares two signals and produce only one single bit output – either 1 or 0. These comparators can be called *Hard Comparator* as they produce a hard decision output by telling whether the signal is larger or smaller than the other one. But comparator's decision making time is long and these circuits suffer from offset errors and meta-stabilities. Being slow in decision making, the comparators cannot be used in very high speed applications easily. Being affected by offset errors, their accuracy will be low and can generate unstable outputs because of meta-stability. To address these problems, a new comparator scheme has been proposed in this thesis. This new comparator circuit is designed with a latched comparator, some delay circuits, memory circuits, and an encoder module. In this design, the comparator settling time has been exploited to generate multiple bits per comparison, which is thus called a *Soft Comparator*. By using multiple overlapping soft comparators, reliable outputs can be generated. This also improves the accuracy and speed of ADCs (SAR, Flash, etc.). Especially for high resolution Flash ADCs, a large number of comparators are needed, which is the reason high resolution Flash ADCs are not common in general. For example, for a 5-bit Flash ADC, $(2^5 - 1)$ traditional comparators will be needed. But using only one of our proposed Soft Comparators, up to 4 bits can be generated. Thus ideally by using only 4 of these Soft Comparators, a 5-bit Flash ADC can be designed, resulting in less power consumption, better accuracy, and high speed operation.

1.3 THESIS ORGANIZATION

The thesis is organized in six chapters. Chapter 1 introduces the applications of comparators and analog-to-digital converters. It describes the background and motivation

of the research work and also the problems in designing comparators in general. It also briefly describes the research contributions of this thesis. At the end, it discusses the thesis organization.

Chapter 2 discusses comparator voltage transfer characteristics and comparator static characteristics, such as voltage gain, input offset, input resolution, noise, input common mode voltage range, and output high and low states. It also goes over comparator dynamic characteristics, such as propagation delay and slew rate. At the end, it goes through comparator classifications, continuous comparators, and dynamic latched comparators. It also reviews literature regarding different state-of-art comparator designs. This chapter also includes one continuous comparator and one dynamic latched comparator design regeneration and input-output simulations.

Chapter 3 starts with briefing the importance of analog to digital data conversion and why it is so challenging to work in analog domain. It describes various applications of analog-to-digital converters (ADCs) and relates different types of ADCs to their specific applications. Major portions of this chapter then reviews the literature by discussing various ADC designs published in Journal of Solid-State Circuit (JSSC) from 2010 to 2015. It studies and focuses ADC designs from different perspectives and summarizes their changes over time. It then discusses high speed and high resolution ADCs and their design challenges, then investigates the reason behind the lesser number of high resolution, high speed ADCs. At the end, it focuses on some specific design challenges of Successive Approximation Register (SAR) ADCs and Flash ADCs.

Chapter 4 explains the soft comparator architecture and working principle. It starts with explaining soft and hard decision decoding, the concept of hard comparator and soft comparator, and the relation between them. It overviews the designing of a soft comparator architecture and its different sub-modules including a dynamic latched comparator, delay line circuits, memory circuits, and encoder circuits and their working flow in different stages. Then it summarizes the working principle of soft comparators. At the end of this chapter, soft comparator noise analysis is briefly discussed. It also shows how using multiple soft comparators can improve the input voltage value detection, which is helpful for designing high speed and accurate

analog-to-digital converters (ADCs).

Chapter 5 shows the circuit layout design. It discusses the initial layout plan for the soft comparator chip, then breaks down into different sub-module layout designs. It covers the layout of dynamic comparator, XOR gate, buffer circuit, delay line circuit, memory circuit, and the encoder circuit. It then discusses the analog, digital, power, and ground pad layout design, pad frame creation, image bevel, metal filling, and usage of capacitors and their layout design. It also focuses on the chip evaluation and power, speed, and voltage of the designed chip.

Chapter 6 briefly summarizes the accomplishments and applications of the soft comparator design, some alternative soft comparator design approaches as the future ideas, and some design challenges while working on the soft comparator.

CHAPTER 2

Comparator Overview

A comparator compares two analog input signals - one is the reference signal and the other is the input signal. It compares them and produces a binary output - one or zero. Thus, a comparator acts as a single bit analog to digital converter (ADC). For an ideal comparator, it takes zero amount of time to compare and produce the output. But for all practical comparators, there is a transition time which is needed to compare the signals and produce the output. Thus, for every comparator, output voltage changes with different input signals and creates a comparator voltage transfer characteristic. This chapter covers characteristics related to comparators designed with open-loop operational amplifiers (Op-Amps).

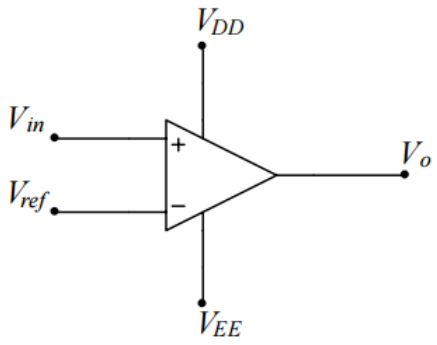


Figure 2.1: Non-inverting Comparator [1]

2.1 Comparator Voltage Transfer Characteristics

A simple comparator can be designed with the help of an OpAmp with open loop configuration. If the open loop gain of the OpAmp is A then the comparator output equation will be:

$$V_O = A(V_+ - V_-) \tag{2.1}$$

Where V_+ and V_- represent the non-inverting and inverting input of the OpAmp circuit and output V_O can be anything within the upper voltage limit V_{DD} and lower

voltage limit V_{EE}. In this case, V_+ is the input analog signal V_{in} and V_- is the reference voltage signal V_{ref}. The voltage transfer characteristics represents how the output voltage V_O changes with the input voltage V_{in}.
If V_{in} is greater than V_{ref}, the output signal V_O should be equal to V_{DD}. On the other hand, if V_{in} is less than V_{ref}, the output signal V_O should be equal to V_{EE}. This is an ideal comparator case, where the assumption is that the comparator doesn't need any transition or settling time. Thus, it can instantly change levels without any delay.

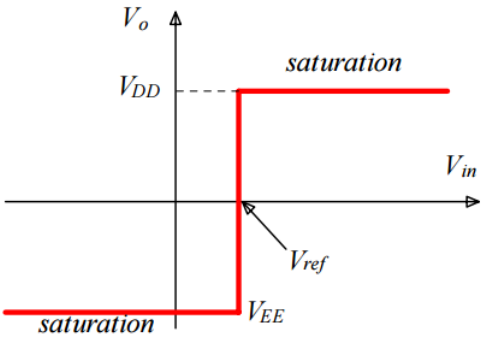


FIGURE 2.2: Voltage transfer characteristic (Ideal) [1]

But a real comparator does not follow the ideal voltage transfer characteristics. Here, the comparator needs some transition or decision settling time to make a decision. If V_{in} is greater than $V_{\delta+}$ then the output signal V_O will be equal to V_{DD}. On the other hand, if V_{in} is less than $V_{\delta-}$ then the output signal V_O will be equal to V_{EE}. If the V_{in} is in between $V_{\delta+}$ and $V_{\delta-}$, then the output signal can be anything between V_{DD} and V_{EE}.

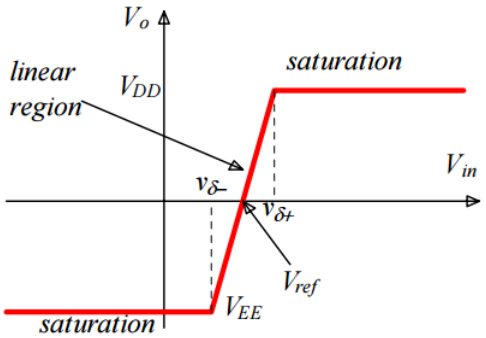


FIGURE 2.3: Voltage transfer characteristic (Non-ideal) [1]

Generally, in many comparators, the analog input signal is compared against the ground level that is the zero reference voltage. In that case, V_{ref} will be 0 and the voltage transition will go through the zero reference voltage point. Fig. 2.4 is showing the case where V_{ref} = 0 and the comparator is non-ideal.

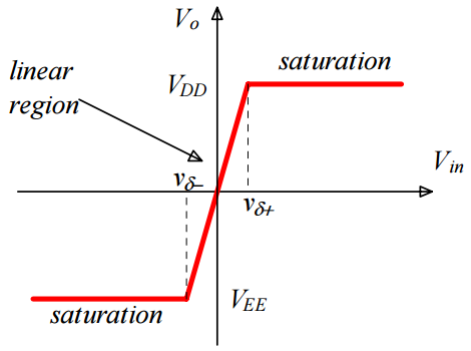


FIGURE 2.4: Voltage transfer characteristic (Non-ideal, zero reference) [1]

Thus, for a practical comparator ($V_{\delta+}$ - $V_{\delta-}$) is the linear range and V_{DD} and V_{EE} are the saturation ranges. Here, $V_{\delta+}$ and $V_{\delta-}$ are dependent on the open loop gain of the comparator A.

$$v_{\delta+} = \frac{V_{DD}}{A} \tag{2.2}$$

$$v_{\delta-} = \frac{V_{EE}}{A} \tag{2.3}$$

For a practical comparator open loop voltage gain, A = 200000 and V_{DD} = 10V and V_{EE} = -10V. Thus, the value of $V_{\delta+}$ and $v_{\delta-}$ are very small. In other words, the operational amplifier will be saturated very quickly.

2.2 COMPARATOR STATIC CHARACTERISTICS

Comparators can have both static and dynamic characteristics. Static characteristics don't change with time where dynamic characteristics change with time progress. Also, static characteristics are mainly related to device sizes and parameters. On the other hand, dynamic characteristics are related to randomness of circuit. The main static characteristics of comparators are:

1. Voltage gain
2. Input offset
3. Input resolution
4. Noise
5. Input common mode voltage range
6. Output high and low states

2.2.1 *Voltage Gain*

Voltage gain represents the overall device of the comparator. It is the ratio of the output voltage change to the input voltage change. Output voltage normally changes from a low saturation to a high saturation voltage level. Thus, if the low saturation level is V_{OL} and high saturation level is V_{OH}, and input voltage changes from V_{IL} to V_{IH} (or, vice versa) then voltage gain (A_v) of the comparator would be

$$A_v = \frac{V_{OH} - V_{OL}}{V_{IH} - V_{IL}} \tag{2.4}$$

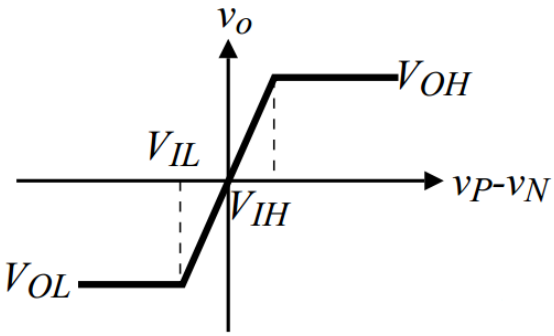


FIGURE 2.5: Voltage Gain of a Comparator [2]

Here, V_{IH} denotes the smallest input voltage for which the output rises to V_{OH} and V_{IL} denotes the largest amount of input voltage for which the output remains at V_{OL}. If the voltage gain is high for the comparator, then it can work well with small voltage changes. In other words, the resolution will also be better for that comparator.

2.2.2 *Input offset*

Comparators can suffer from an input offset voltage issue. When both inputs of the comparators are equal, ideally, there should not be any high or low output states. But due to input offset, output can have either a high or low state even if both inputs are equal. The input offset of a comparator is the input at which the output is equally likely to be high or low. Noise determines how the output statistics vary as a function of input [7]. Input offset can be modeled or represented by a series voltage source applied at either of the comparator inputs.

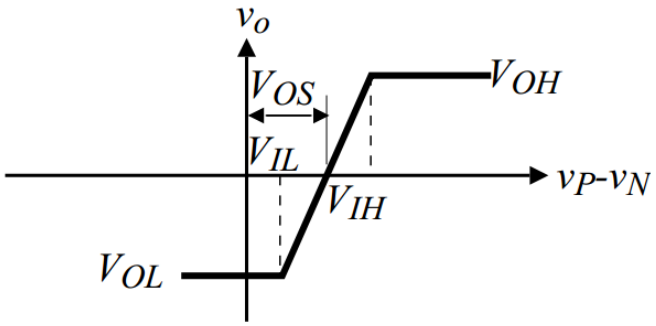


FIGURE 2.6: Input Offset of a Comparator [2]

Thus, input offset voltage V_{OS} is the amount of voltage needed to apply at the input to make the output voltage level equal to $\frac{V_{OH}+V_{OL}}{2}$ when both comparator inputs are equal. The source of input offset can be the transistor size mismatch. Mismatch in threshold voltage of the transistors and transistor trans-conductance parameters can be other sources. Input offset can degrade the comparator resolution.

2.2.3 *Input resolution*

Comparator input resolution can be described as the amount of voltage change in the input of a comparator to make a state change at the output, that is from low to high state or vice versa. Thus, it is the smallest voltage difference between the input and the reference voltage responsible for binary digit change at the comparator output.

2.2.4 *Noise*

Noise is an important issue when the comparator has high resolution. Random circuit noise can cause the output of a comparator to change from one logic state to the other, even when the comparator input is held constant. Hence, in order to measure the input-offset voltage in the presence of circuit noise, the input voltage is measured that results in the output state of the comparator being high or low with equal likelihood. The input-referred noise is then observed by changing the input around this value and observing how the output statistics vary as a function of the input voltage around this dc offset [7].

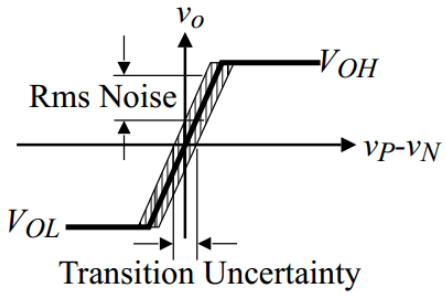


FIGURE 2.7: Comparator Noise [2]

2.2.5 *Input Common Mode Voltage Range*

Input common mode voltage range is the voltage range within which the comparator performs the comparison without any problem. It is abbreviated as ICMR. Within ICMR, all the transistors in the comparator will be in saturation. Thus, to ensure the normal operation of comparator, ICMR is very important. ICMR can be affected by noise voltage which can hamper the differential performance of the comparators.

2.2.6 *Output High and Low States*

The output high and low states are also important static characteristics. The output high state V_{OH} is the amount of voltage which can represent binary level '1' and output low state V_{OL} is the voltage level which represents the output binary level '0'.

Normally, output can have only these two states as the state transition time is very short for general comparators.

2.3 COMPARATOR DYNAMIC CHARACTERISTICS

Comparators also possess dynamic characteristics. Some of the characteristics of comparators change with time advancement. Due to their time varying nature, they are considered as dynamic characteristics. The major dynamic characteristics of comparators are:

1. Slew rate
2. Propagation delay

2.3.1 *Slew Rate*

If a pulse signal is applied to one input of a comparator to compare with the other input signal or reference signal, then due to the internal compensation capacitor and depending on the frequency of the input pulse signal, the comparator might not follow the signal properly. Thus, the ability of any comparator to change the output voltage with time can be defined as slew rate of that comparator. The slew rate comes from the capacitor voltage and current relationship as below,

$$i = C\frac{dV}{dt} \tag{2.5}$$

Where i is the capacitor current and V is the voltage across the capacitor. If the rising and/or, falling voltage of comparator becomes high very large, the comparator output signal might be limited by slew rate. From this current-voltage relationship, if current becomes limited, then voltage also becomes limited and deteriorates the signal.

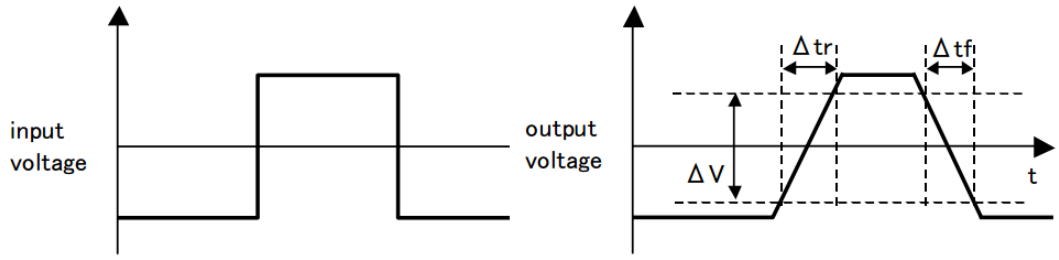


FIGURE 2.8: Slew Rate of a Comparator [3]

Comparator rising edge slew rate and falling edge slew rate are different. From the figure, rising and falling edge slew rate are expressed as,

$$SR_+ = \frac{\Delta V}{\Delta t_r} \tag{2.6}$$

$$SR_- = \frac{\Delta V}{\Delta t_f} \tag{2.7}$$

$$\tag{2.8}$$

Where Δt_r and Δt_f are measured for 10% and 90% of maximum voltage swing and ΔV is the voltage difference between output high voltage state and output low voltage state.

2.3.2 *Propagation delay*

Propagation delay is one of the most important parameter of any comparator. It directly relates to the input signal frequency range. When a comparator compares two input signals, it needs some time to make the comparison decision. This time is the propagation delay. In a more specific way, it can be said, when the input analog signal crosses the reference signal, to the time when the comparator makes a decision and changes the output states is expressed as propagation delay. Propagation delay can happen in rising edge or falling edge of the signal. Thus, the overall propagation delay is calculated by averaging the rising edge delay and falling edge delay.

Propagation delay time in fact varies with the input analog signal amplitude, which is also related to the slew rate of the comparator. Thus, propagation delay is indirectly related to the slew rate. So for a slew rate limited comparator, the

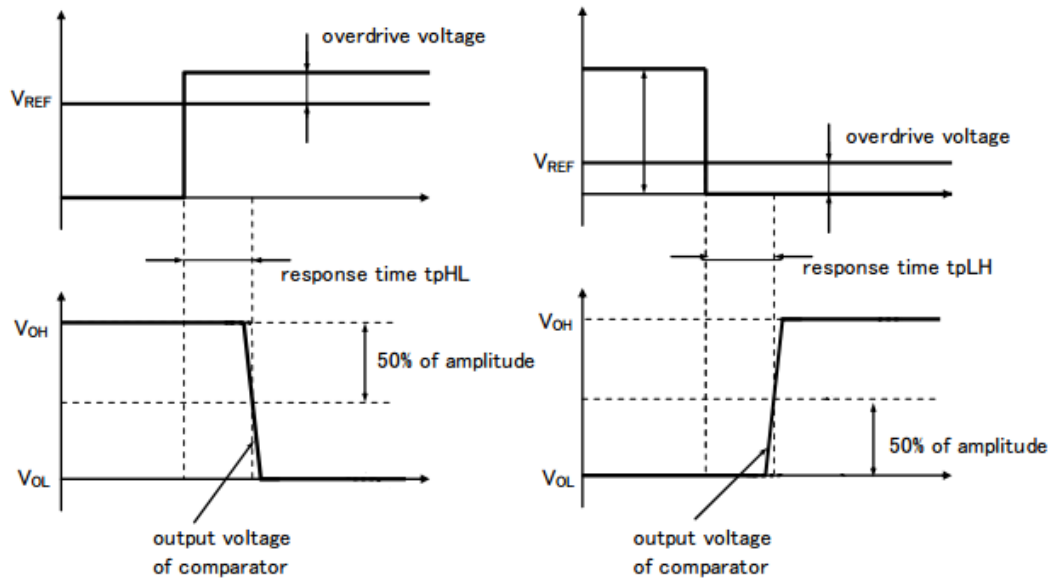


FIGURE 2.9: Propagation Delay of Comparator [3]

propagation delay t_p can be expressed as,

$$t_p = \Delta T = \frac{\Delta V}{SR} = \frac{(V_{OH} - V_{OL})}{2 \cdot SR} \tag{2.9}$$

Where slew rate SR is,

$$SR = \frac{dV_O}{dt} = \frac{\Delta V}{t_p} \tag{2.10}$$

2.4 COMPARATOR TYPES

There are various types of comparator circuits. Each comparator circuit has advantages and disadvantages of its own. Based on different types of applications and requirements, comparators are designed differently. But in general, almost all comparators can be categorized into two basic types −

1. Continuous Comparator
2. Clocked, Dynamic, or Latched Comparator

2.4.1 *Continuous Comparator*

Continuous comparators are very fast. Normally, they can have output logic states either at '1' or '0' all the time, given that there is higher or lower analog input signal compared to the reference signal. As this comparator has continuous operation, it can change the output state immediately with the change of the input signal. But as it is working continuously, it is also consuming power all the time. Thus, it is a power hungry and energy inefficient comparator type.

Continuous comparators can be built using both CMOS and BiCMOS circuits. One design comprises of BiCMOS which is of high speed and also of high precision is shown in Fig. 2.10. For this design, offset voltage is compensated sacrificing the total timing of comparison.

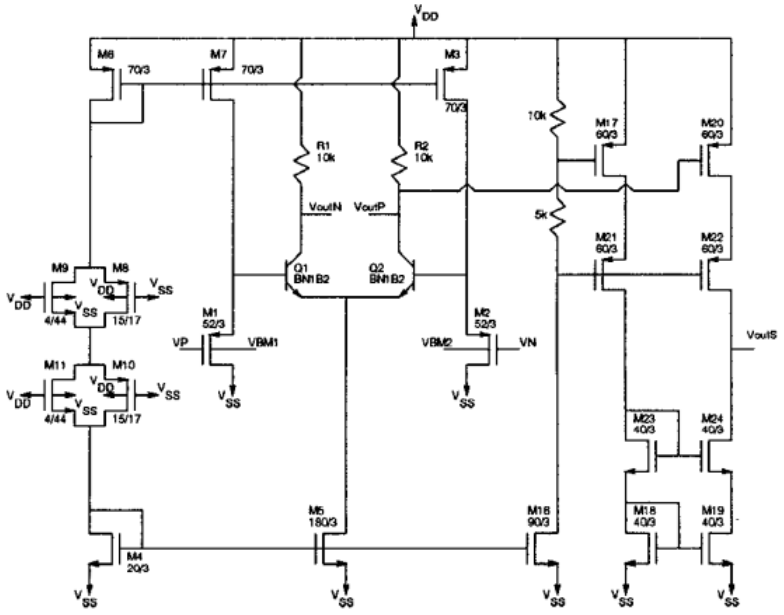


FIGURE 2.10: A BiCMOS Continuous-time comparator [4]

Here, both inputs of the differential amplifier are disconnected, input mismatched are stored in a capacitor and then this offset is subtracted from the original measurement. The inputs can be tied together and then output can be measured, which gives the offset measurement. The offset can then be subtracted from the original output measurement during normal operation of the comparator.

Fig. 2.11 shows another design comprised of two comparators, which are connected together to form a comparator [5]. Here, the input stage is designed by 3 PMOS transistors and they are connected through diode connections.

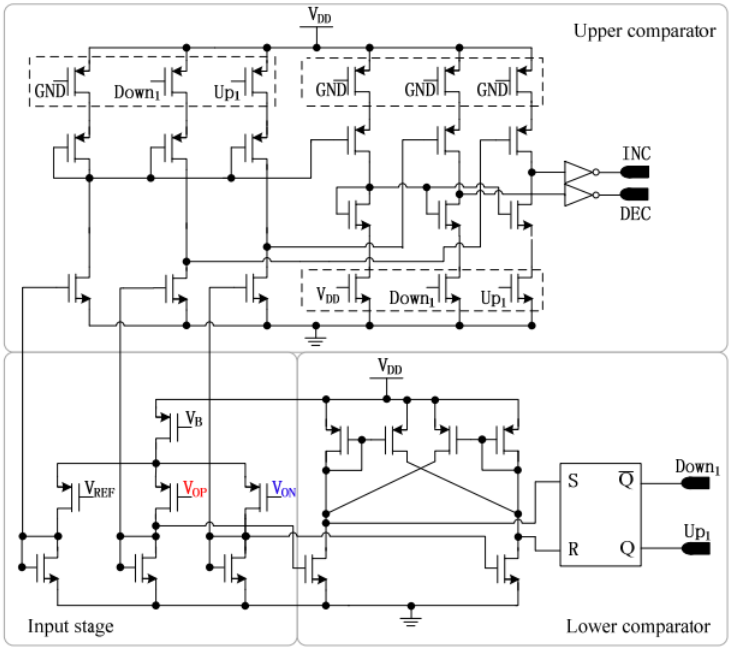


FIGURE 2.11: Continuous-time Comparator with two comparison part [5]

Upper stage and lower stage comparators are totally different in terms of design as the lower stage also comprises a S-R latch for better gain and rail to rail performance. Only one differential input comes to the upper stage and compared against the reference voltage to detect the trigger level and the other input is idle at that time.
Fig. 2.12 shows a continuous time comparator design [6], which consists of a differential amplifier followed by a common source amplifier stage. This comparator is used in designing a 9-bit pulse position modulation based ADC design.

A ramp signal is applied as a reference signal to one of the comparator's inputs. It takes the input signal in the other input of the comparator and compares the signal amplitude with the reference ramp signal amplitude. Whenever the input signal becomes smaller than the ramp signal, *stop* signal becomes high and remains high until it is smaller than the ramp signal again. This *stop* signal is then converted to a digital bit flow using the subsequent time-to-digital circuit converter.

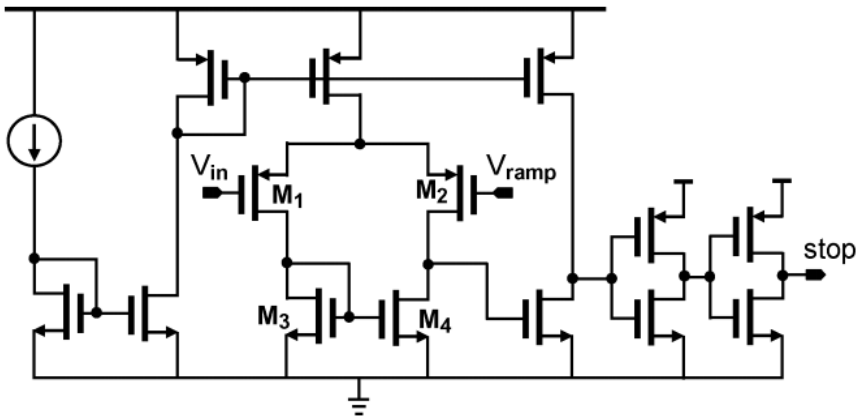


FIGURE 2.12: Continuous-time comparator with two stages [6]

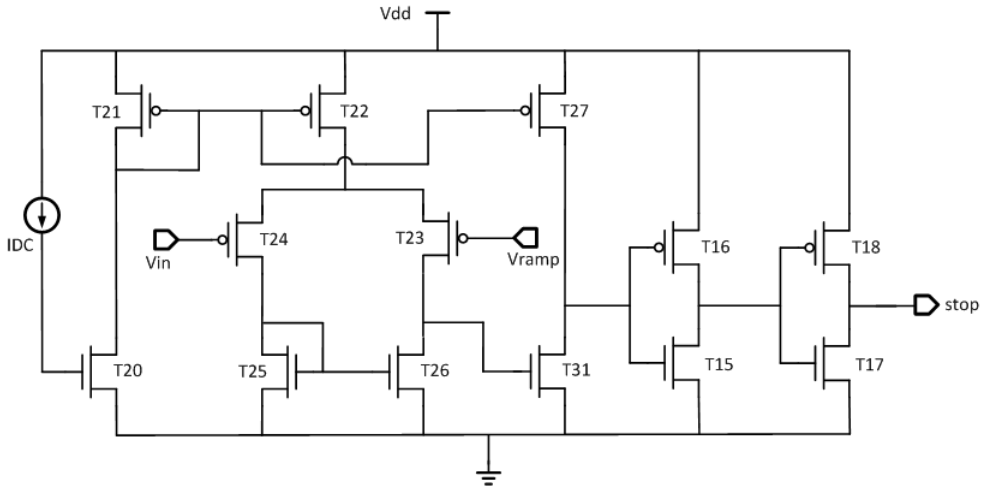


FIGURE 2.13: Regenerated Continuous-time Comparator in 130nm technology

In this thesis, the comparator in [6] was regenerated using 130nm CMOS technology with some design modifications and a 600mV supply voltage (Fig. 2.13). The regenerated comparator worked properly and produced the same output *stop* signal (Fig. 2.14). One ramp generator circuit was designed, which took the clock signal as input and produced ramp of regular intervals. Also, one current generator circuit was designed which supplied a fixed DC current for this continuous comparator circuit and generated the biasing current.

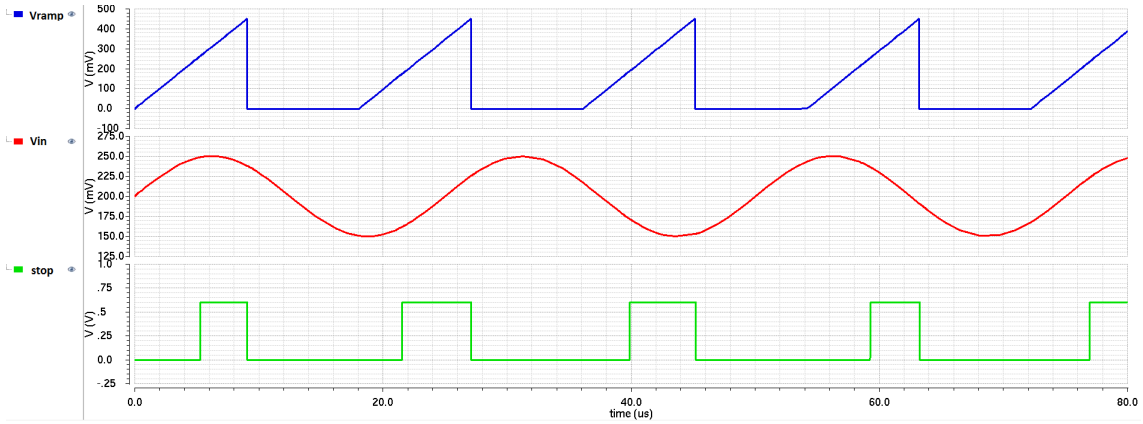


FIGURE 2.14: Regenerated Comparator input and output signals

2.4.2 *Latched Comparator*

Continuous comparators keep comparing two analog input signals all the time even when the comparison is actually not needed. Thus, it can consume unwanted power, which makes it energy inefficient. Many applications including analog-to-digital converters (ADCs) and digital memory circuit needs the comparator to compare the input signals at certain points of operation. When the comparison is done at certain intervals, greater comparison accuracy is achieved and also power management improves and results in an energy efficient comparator circuit. Thus, latched comparators need *clock signal* – with the high state of the clock, *Comparison* is done and with low state, *Reset* operation is done which eventually removes the previous comparison results stored in the comparator. This is the reason why it is also called a *Clocked Comparator*. The comparison action depends on the state of the clock and as soon as the clock changes its state, the comparator also acts. Thus, this type of comparator is also known as a *Dynamic Comparator*.

High speed dynamic latched comparators normally consist of two major stages – *Pre-amplifier* stage and *Track-and-Latch* stage [7]. The pre-amplifier stage amplifies the input analog signal thus, it gains higher resolution than the original signal. The output of the pre-amplifier is still smaller than the digital part of the comparator circuit. This also helps to minimize the kickback effect drastically. The outputs of the pre-amplifier stage go to the track and latch stage. This stage amplifies the pre-

TABLE 2.1: Design parameters for the Continuous Comparator

Transistor	(W/L) Ratio
T21	$1\mu/2\mu$
T22	$8\mu/2\mu$
T23	$10\mu/1\mu$
T24	$10\mu/1\mu$
T20	$2.4\mu/2.4\mu$
T25	$3\mu/1\mu$
T26	$3\mu/1\mu$
T27	$4\mu/2\mu$
T31	$2.8\mu/1\mu$
T16	240n/140n
T18	240n/140n
T15	240n/140n
T17	240n/140n

amplifier output both in track phase and latch phase. A positive feedback is normally enabled during the latch phase. This positive feedback ultimately generates the digital signal at the output of the comparator.

Fig. 2.16 shows a regenerative comparator design, which consists of a pre-amplifier and a latch circuit with two modes of operation − latch mode and trach mode [8]. The pre-amplifier consists of two p-type diode connected MOSFETs acting as an active load for two n-type MOSFET which are biased by a fixed tail DC current. The latch circuit is made of a cross-coupled pair of inverters. In the track mode, the difference between input signals will be amplified by the pre-amplifier. At that time, the latch circuit will be disabled. In the latch mode, latch circuit is enabled and it takes the pre-amplifier output to regeneratively amplify the difference in order to get a rail to rail voltage which in turn creates the digital output states − either a high '1' or low '0'. One advantage of using a regenerative latched comparator is that they are pretty much noise free when the comparison decision is made as the outputs will be totally disconnected from the latch circuit inputs. But this kind of latch circuit can face meta-stability issues during sampling and amplifying the voltage difference received from the pre-amplifier stage. Regeneration time which is defined as the time needed for creating a decision in logic level from the start of sampling time, is a function of

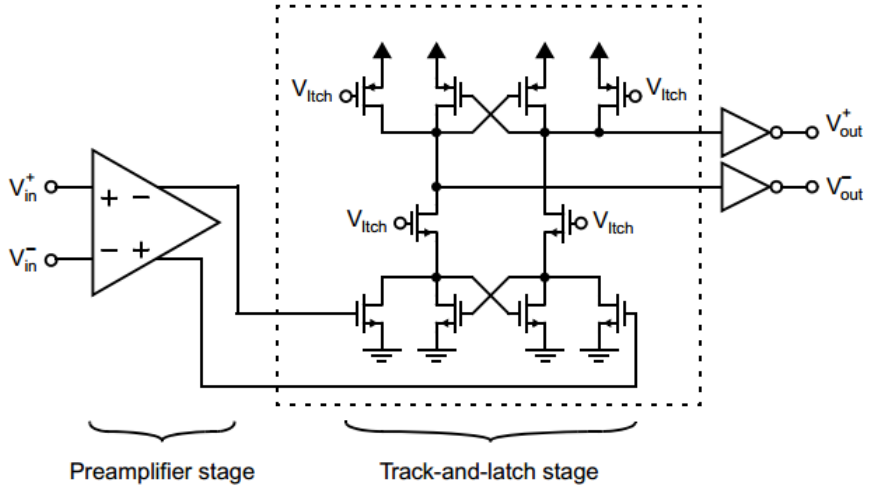


FIGURE 2.15: A typical Dynamic Latched Comparator [7]

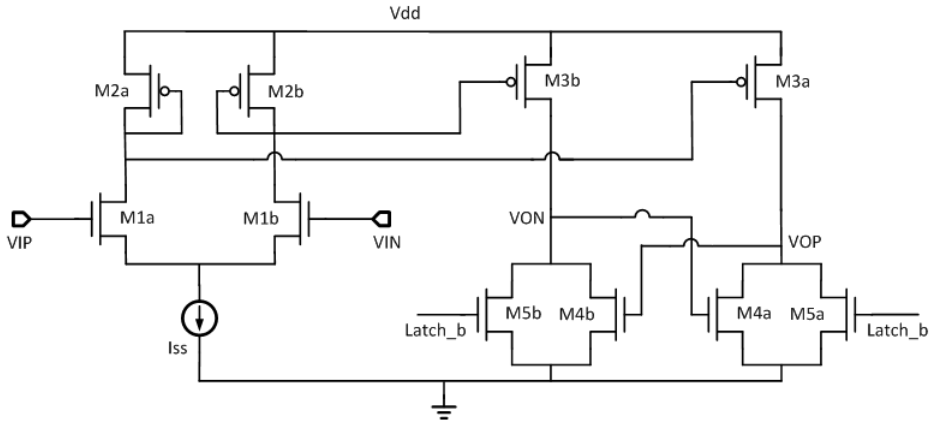


FIGURE 2.16: A Regenerative Latched Comparator [8]

initial voltage differences between the inputs and also the latch time constant which also depends on the parasitic capacitance of the circuit.

Dynamic latched comparators are fast, generally low power consuming with full rail-to-rail swing and high gain. Thus, this kind of comparator has many applications, including high speed and low power analog-to-digital converter (ADC), digital memory circuit, sense amplifier, etc. But due to parasitic capacitance output load mismatches and offset issues, they can have poor accuracy. Pre-amplifiers are normally used to minimize the offset.

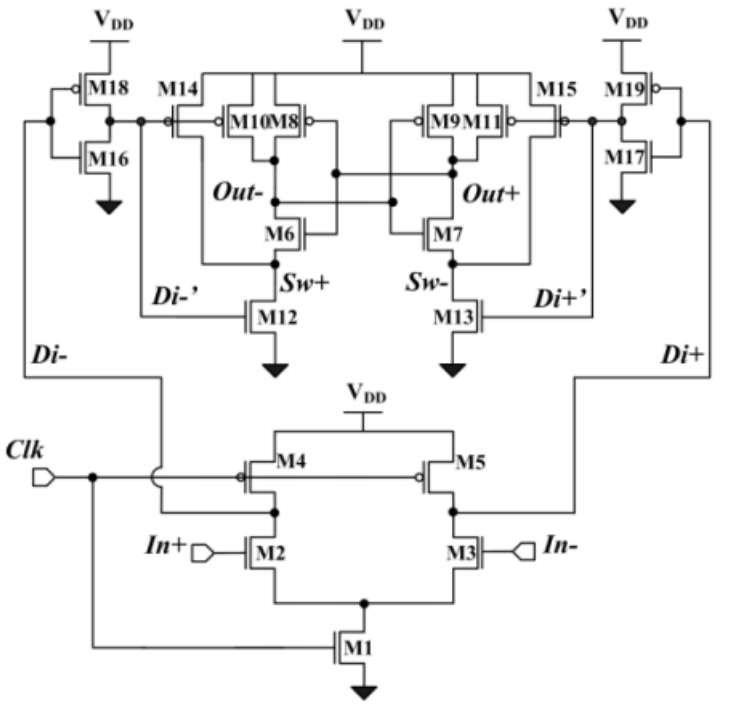


FIGURE 2.17: A Fully Dynamic Latched Comparator with Higher Gain [9]

The design in [9] introduces two inverters between the pre-amplifier and latch stage. With this extra circuitry, the gain of the latch stage improves significantly.
Fig. 2.18 shows an energy efficient dynamic two stage comparator used in a SAR ADC [10]. The first stage is the pre-amplifier and the second stage acts as another voltage amplifier and also as a positive feedback amplifier, which helps to create rail-to-rail digital output voltage. During the low state of the clock signal, FP and FN nodes parasitic capacitors will be charged. During the high state of the clock, these charged nodes will start to discharge through two n-type MOSFET to ground. Thus, the voltages of the nodes FP and FN will reduce to *gnd* from supply voltage level. As the FN and FP nodes lose their charges, in the second stage, two p-type MOSFET start to switch ON and the SN and SP node voltages will start to rise. Depending on the INP and INN values, either of SN or SP will reach to high voltage and the other one will eventually be grounded, thus, creating rail-to-rail digital voltage at the output [10].

The node voltages of the comparator, FN and FP of the first stage and SN and SP of the second stage, are also shown in Fig. 2.19. The FN and FP nodes discharge from

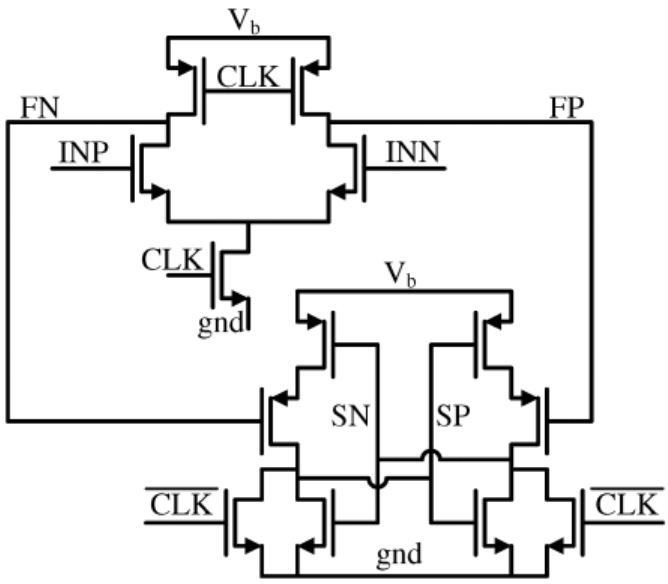


FIGURE 2.18: Energy efficient Dynamic two stage Comparator[10]

V_b supply voltage level to *gnd* level while SP and SN nodes started from the *gnd* level to reach rail-to-rail output voltage V_b and *gnd*. This design is very energy efficient. When nodes FN and FP are completely discharged, the power dissipation in the first stage stops and when the output nodes SN and SP reach a rail-to-rail voltage level, power dissipation stops in the seconds stage. Thus, when the comparator is not active or not doing any comparison, the total power dissipation is zero. Comparably, the first stage is more power efficient than the second stage, and it also amplifies more than the second stage.

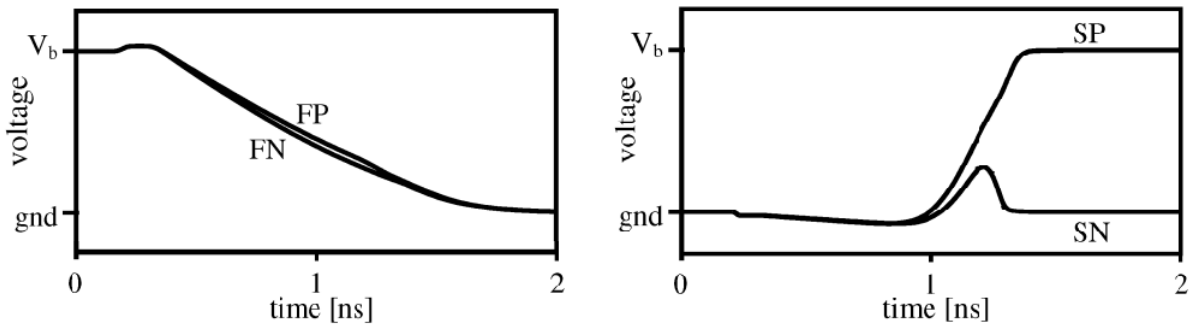


FIGURE 2.19: Comparator node voltages during comparison [10]

In this thesis, the comparator circuit in [10] is regenerated using IBM 180nm CMOS technology with supply voltage of 1V and common mode voltage of 500mV (Fig. 2.20). The regenerated comparator produced the same node voltage characteristics.

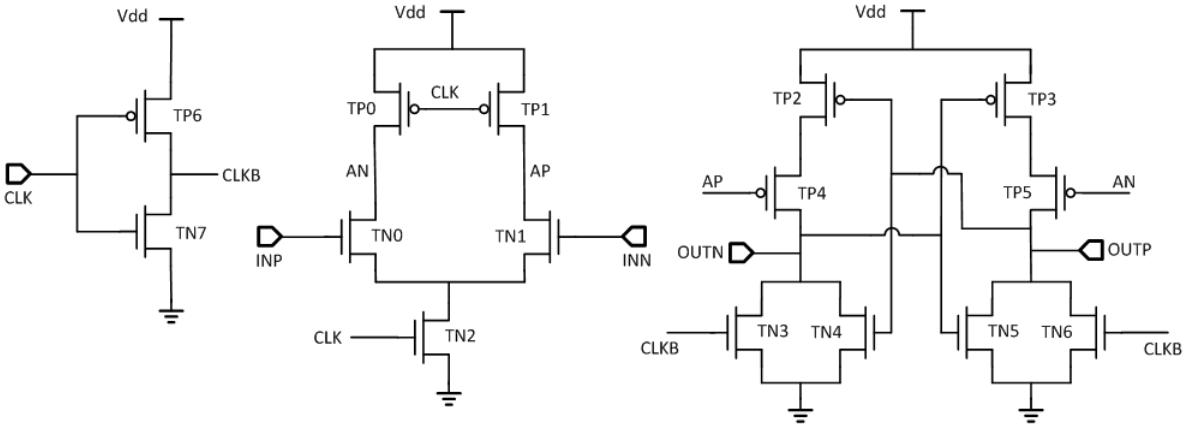


FIGURE 2.20: Regenerated Dynamic Latched Comparator in 180nm technology

Here, AN and AP node voltages represent the FN and FP nodes respectively, which show similar voltage discharge behavior (Fig. 2.21).

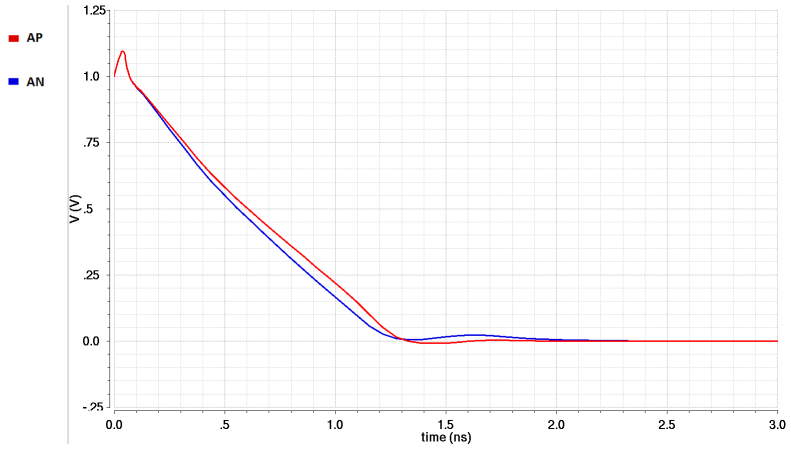


FIGURE 2.21: Comparator nodes AP and AN during comparison

The output nodes of the second stage OUTP and OUTN represent the same nodes SP and SN, respectively and behave in the same way. Here, input voltages are INNP = 850mV and INN = 500mV and the rail-to-rail output voltage is reached in less than

2ns.

Comparator is one of the main building block of designing an analog-to-digital

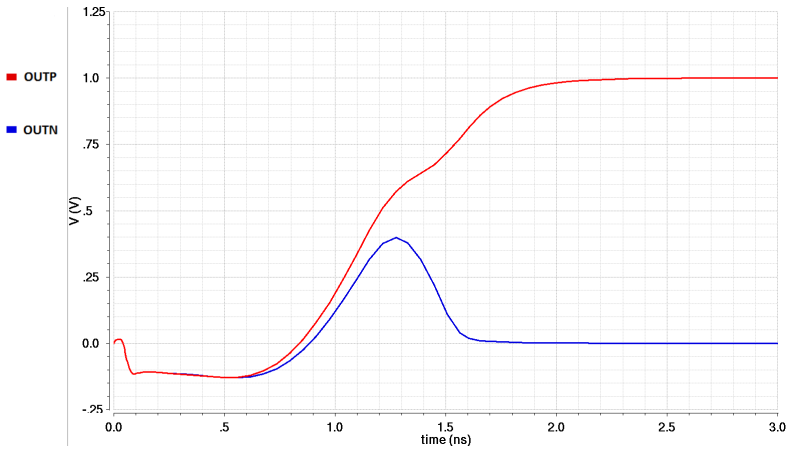


FIGURE 2.22: Comparator nodes OUTP and OUTN during comparison

TABLE 2.2: Design parameters for the Latched Comparator

Transistor	**(W/L) Ratio**
TP6	$2.4\mu/200n$
TN7	$1.2\mu/200n$
TP0	$1.2\mu/200n$
TP1	$1.2\mu/200n$
TN0	$6\mu/400n$
TN1	$6\mu/400n$
TN2	$6\mu/400n$
TN3	$1.2\mu/200n$
TN4	$1.2\mu/200n$
TN5	$1.2\mu/200n$
TN6	$1.2\mu/200n$
TP2	$2\mu/400n$
TP3	$2\mu/400n$
TP4	$2\mu/400n$
TP5	$2\mu/400n$

converter (ADC). Thus designing an comparator with less offset, meta-stability and noise will help in designing a better performing ADC, which is covered in the next chapter.

CHAPTER 3

Analog-to-Digital Converter (ADC) Overview

An analog-to-digital converter (ADC) is a device which is able to convert an analog continuous signal to discrete digital signal. By nature, analog signals are continuous in amplitude and continuous in time; for example, temperature, pressure, natural sound, etc. On the other hand, digital signals are discrete in amplitude and discrete in time. In the modern age, all the digital equipment, including personal computers, can only *understand* digital signals. The ideal digital signal can be represented with only two states - '1' and '0'.

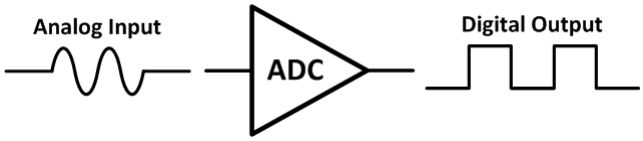


Figure 3.1: Analog to digital conversion through ADC

The analog-to-digital conversion process involves sampling and a quantization process which introduces some errors. Every ADC has a range of frequencies within which it can operate without any major distortion called ADC bandwidth. The practical bandwidth of ADC can be defined by its sampling rate. If the sampling rate is twice the amount of the signal bandwidth, that ADC is capable of regenerating the signal without any aliasing. Resolution, which is defined by the number of output levels an ADC can quantize it's analog level to, is related to dynamic range of ADC. Thus, for various applications, different resolutions and sampling rates are needed, which ultimately create the need for different types of analog-to-digital converters.

3.1 Analog-to-digital converter applications

Analog-to-digital converters are used when an analog signal needs to be converted to digital. Although all the signals in the real world are analog, easiness of storing, re-constructing, and processing digital signals have increased the demand for digital

data exponentially. Based on the required speed, power, and resolution, the ADC type is selected.

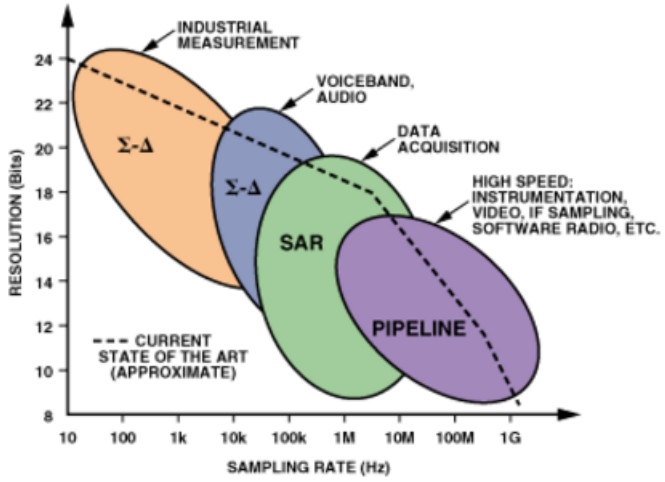


FIGURE 3.2: ADC types and applications based on speed and resolution [11]

Main applications can be categorized into: precise industrial measurements, voiceband and audio, data acquisition, high-speed instrumentation, high-speed video, and software defined radio [11]. Most of these applications can be covered with the Sigma-Delta ($\Sigma - \Delta$) ADC, Successive Approximation Register (SAR) ADC and Pipeline ADC. For fast applications, Flash ADCs are used. Thus these three type of ADCs along with Flash ADC, are the most popular ADC types for high resolution and high speed applications. Adding to these, Single Slope, Dual Slope or Integrating ADC, and Time-Interleaved ADC also have many important applications.

Industrial measurement and instrumentation need high resolution analog-to-digital converters. Typically 16 to 24 bits are necessary along with a couple of hundreds Hertz of sampling rate. Integrating ADCs, including dual slope, triple slope, etc. used to serve this purpose, were very popular. But the Sigma-Delta ($\Sigma - \Delta$) ADC slowly took their place and is now the main ADC to serve the previously mentioned purposes [11].

Data acquisition systems in measurements and process control systems have many applications. SAR ADCs are the best suited ADC type for this kind of applications [11]; especially when multiple channels are needed for multiplexing purpose. SAR

ADCs pose low to medium converting speed, accuracy is medium to high, but area is very small which made it perfect for using with sensors, or any other equipment from where data can be directly provided.

Voice band and audio systems needed very high resolution and very accurate data conversion. Adding to that, they need proper signal filtering and have specific signal-to-noise ratio (SNR) requirement. In a modern solid state memory era, all the audios need to be processed and stored in digital devices and have small areas for data conversion. Sigma-Delta ADCs are a very popular choice for these applications. They have high resolution (16 to 24 bits), very high accuracy, and do not need large area, making them perfect for these kind of applications [11].

High speed applications like digital video and display electronics need ADCs capable of converting the analog signal to digital quickly. Flash converters are a very popular choice for this purpose as they are very fast in operation. But as the requirements for high resolution ADC increased, flash converters couldn't fulfill that demand. Pipeline and SAR ADCs are fast in operation and resolution is also high [114]. Thus, these two ADCs saw lots of usage in high speed video and display electronics applications.

For software defined radio (SDR) applications, sampling rate should be very high as the radio frequency, or bandwidth used for these kind of applications are very large. Typically from 70 MHz to a couple of gigahertz of signal frequencies are used in SDR. Pipeline ADCs pose very high sampling rate, which is perfect for these kind of applications and widely used in the industry.

Flash ADCs are the fastest ADCs available. They normally work in the gigahertz range of sampling rate. Thus they have applications in radar systems, wideband radio receivers, electronic testing equipment, optical communications links, etc. But due to high power consumption, they do not have many low power and remote applications. Another disadvantage of Flash ADCs are that they offer low resolutions.

3.2 DESIGN STUDY OF ANALOG-TO-DIGITAL CONVERTERS (ADCS)

This section presents a summary of selected articles related to ADC design published in IEEE Journal of Solid-State Circuits (JSSC) between 2010 to 2014. ADC designs are categorized based on the architecture, design year, technology, resolution, sampling rate, power, and area. Fig. 3.3 maps a number of ADC types reported in JSSC in each of the years from 2010 to 2014. Pipeline ADCs were published in large numbers

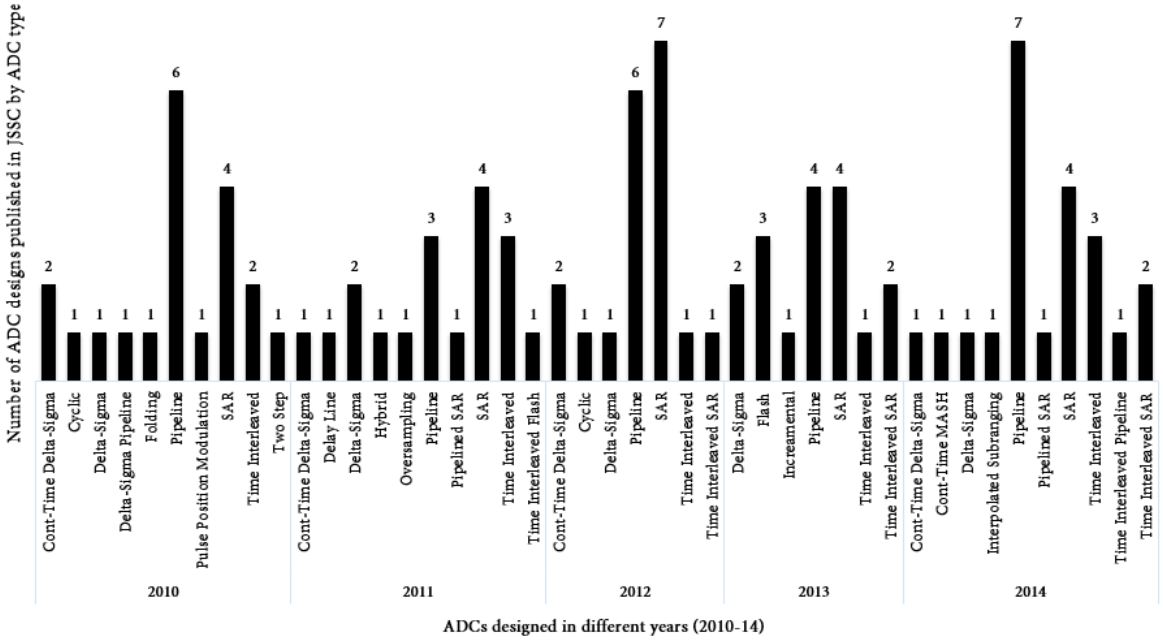


FIGURE 3.3: Number of different ADC architectures published between 2010-14

consistently. Successive approximation (SA) and Time-Interleaved (TI) ADCs were also popular during that time frame. Other types of ADCs only have 1-2 papers in each year.

3.2.1 *Different Technologies and Architectures*

Fig. 3.4 shows the number of ADCs designed with different technologies from 2010 to 2014 and published in JSSC. In 2010, the number of ADCs designed with 90nm and 180nm were large. In 2012, 40nm, 65nm, 90nm, 130nm, and 180nm technologies were equally popular. In 2011, 2013, and 2014, 65nm technologies dominated the ADC

designs published in JSSC.

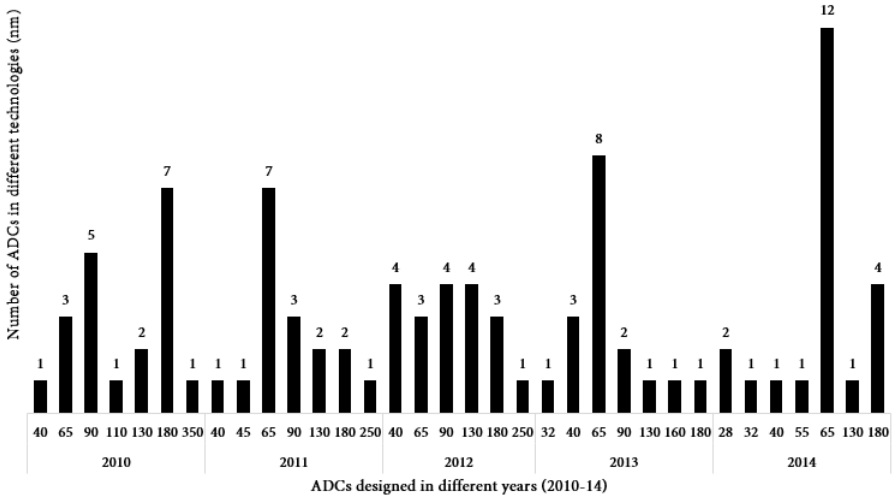


FIGURE 3.4: Number of ADCs with different technologies (nm)

Fig. 3.5 shows the number of ADCs designed with different architectures (2010-14) and published in JSSC. Pipeline and SAR ADCs were the two major architectures reported mostly. After that, Time-Interleaved and Sigma-Delta ADCs were equally popular. Other ADC design types were randomly reported.

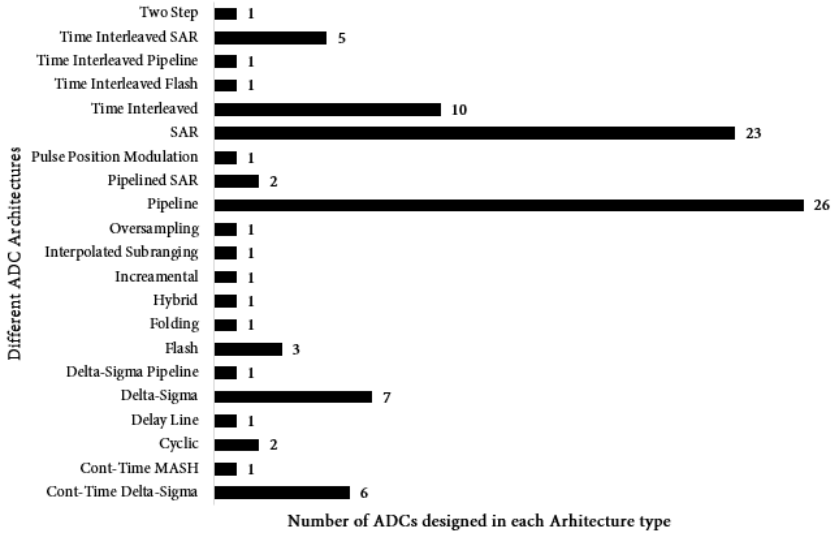


FIGURE 3.5: Number of ADCs with different Architectures

3.2.2 *Resolution and Sampling Rate*

ADC resolution depends on the number of analog levels in conversion and not related to technology. It is expected, since it is a basic design requirement. A higher resolution will mean a more precise converter. Fig. 3.6 shows the ADC resolution with different

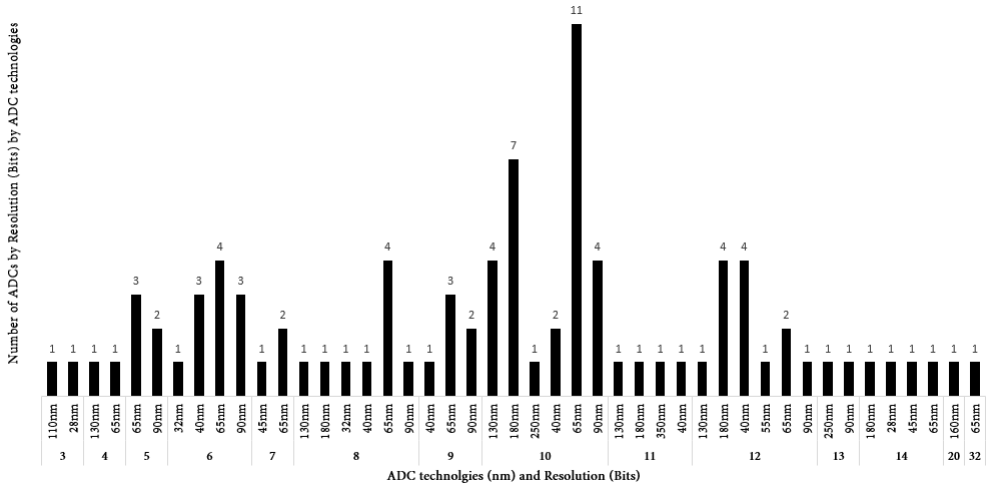


FIGURE 3.6: ADC Resolution (Bits) with different Technologies (nm)

technologies. It seems, 65nm and 180nm were used more for designing high resolution ADCs compared to other technologies. Fig. 3.7 shows the ADC resolution with

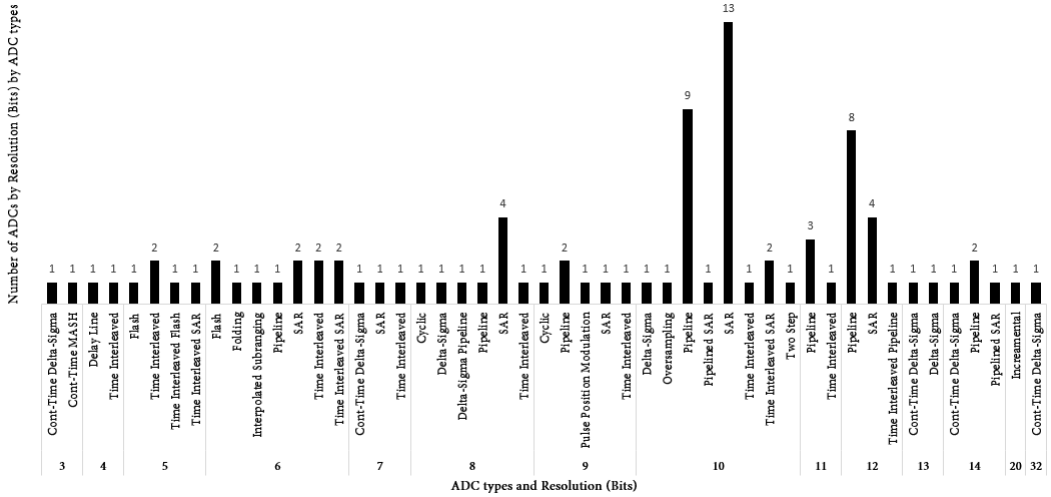


FIGURE 3.7: ADC Resolution (Bits) with different Architectures

different architectures. Pipelined and SAR architectures typically show the largest

number of bits used for resolution. High speed ADCs, like Flash and Sigma-Delta have low resolution designs. Because, with high speed architecture, it is difficult to design high resolution ADCs. The overall observation is that, ADCs with resolutions between 4 and 12 are most popular and ranges in many applications.

The sampling rate is a frequency at which analog signal is sampled while converting to digital. It is not directly related to the bandwidth. Sampling rate should be twice the Nyquist frequency of a signal in order to replicate the signal from its digital form. Fig. 3.8 shows different ADC designs sampling frequency with different architectures.

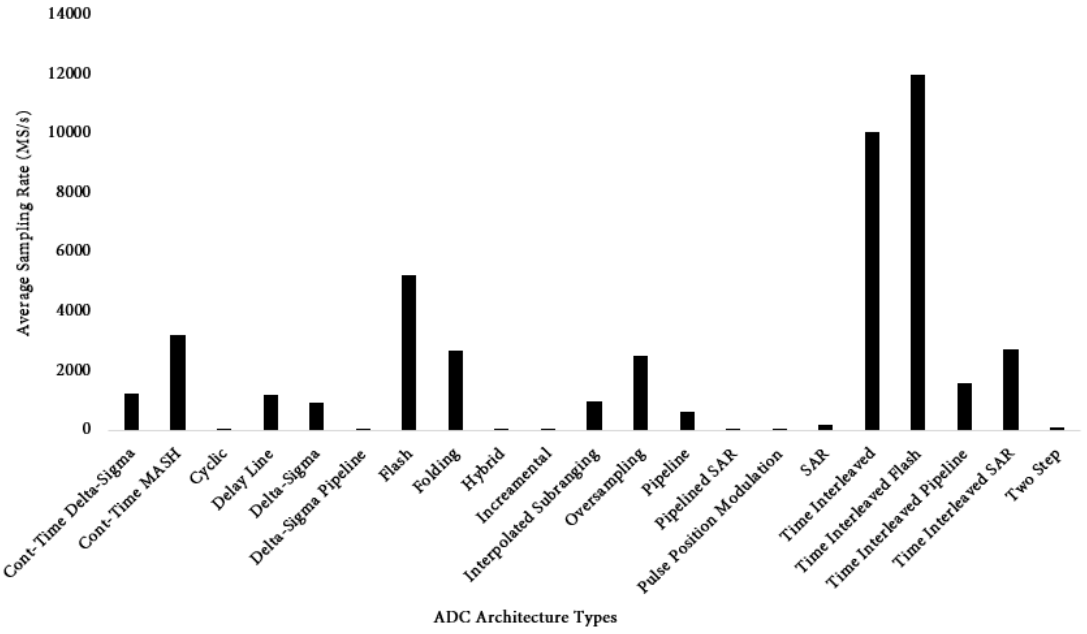


FIGURE 3.8: ADC Sampling RateResolution (Bits) with different Architectures

Time Interleaved (TI) and Flash ADC architectures have the highest speed capabilities. Thus these two types of ADC also have the higher sampling rate. Flash ADC is the fastest ADC and possesses the highest sampling rate. Pipeline and Folding architectures also show high sampling rate, as these architectures are also designed for high speed applications along with Flash and Time Interleaved (TI) ADCs. Successive Approximation (SA) ADCs are generally the slowest type. Delta Sigma ADCs can also have high speed designs. ADCs designed for high speed applications generally use small fabrication technologies which can provide inherent speed advantages.

3.2.3 *Power Consumption and Area*

ADCs used for high speed applications need more power compared to the slow applications. Fig. 3.9 shows a pie-chart where different technologies are mapped with their ADC average power consumption. Smaller technologies, like 28nm, 40nm, 45nm, and 65nm are normally used for high speed applications where power requirement is high. It is also reflecting in the pie-chart that smaller technologies have higher average power.

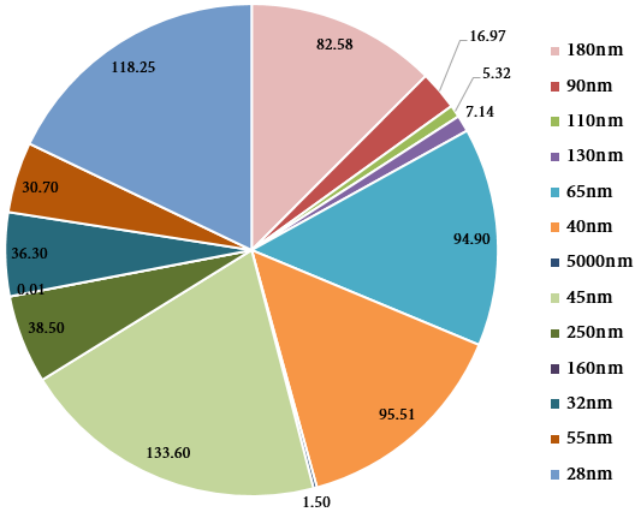


FIGURE 3.9: ADC Average Power (mW) with Technologies (nm)

High speed ADC architecture needs a high amount of power. Fig. 3.10 shows a pie-chart where different ADC architectures are mapped with their average power consumption. Time Interleaved Pipeline ADCs' average power is higher than any other ADC. Also, Flash, Pipeline, and Time Interleaved show high power consumptions. It is very much expected as these ADCs are designed for high speed applications, which require high power consumption. Pulse Position Modulation, SAR, Cyclic, Two Step, and Delta-Sigma ADCs show low power consumption as they are generally not designed for high speed applications.

ADC area is an important factor for certain applications. Remote and mobile applications look for ADCs with smaller area. Fig. 3.11 shows a pie-chart where different technologies are mapped with average ADC area, which also shows that area

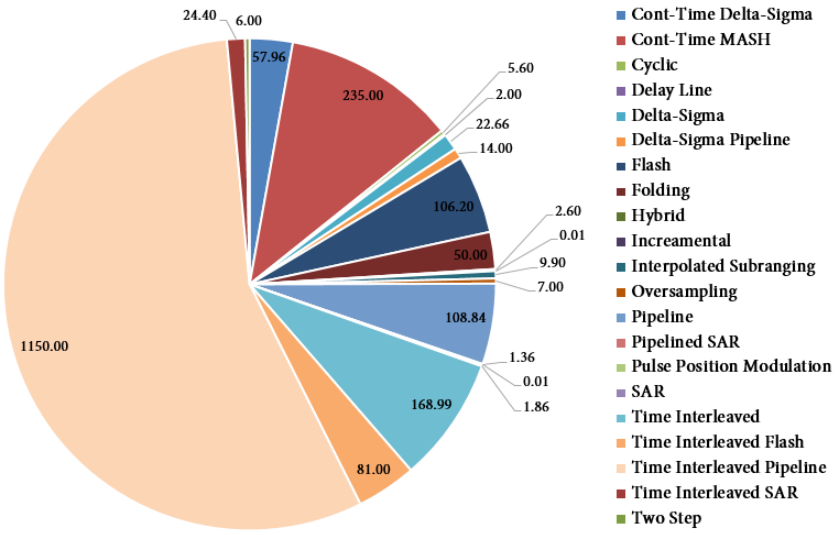


FIGURE 3.10: ADC Average Power (mW) with different Architectures

is highly process dependent. The higher the technologies (nm), the higher the active area requirement. Fig. 3.12 shows a pie-chart where different ADC architectures are

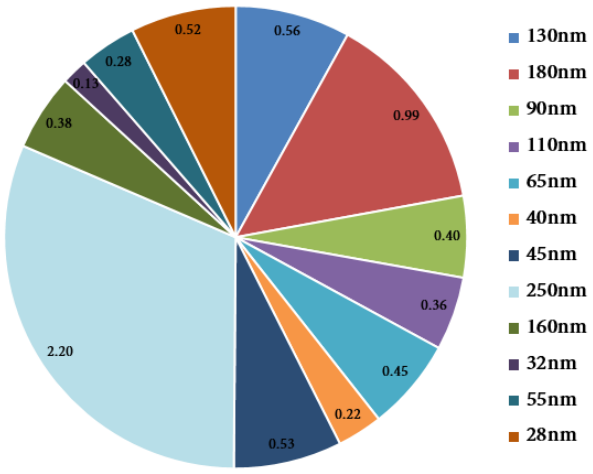


FIGURE 3.11: ADC Average area (mm^2) with Technologies (nm)

mapped with average ADC area. Hybrid ADCs and Time Interleaved Pipeline ADCs need more active area than any other architectures. It is expected as Time Interleaved architecture needs large numbers of ADCs to design which need more ADC design area.

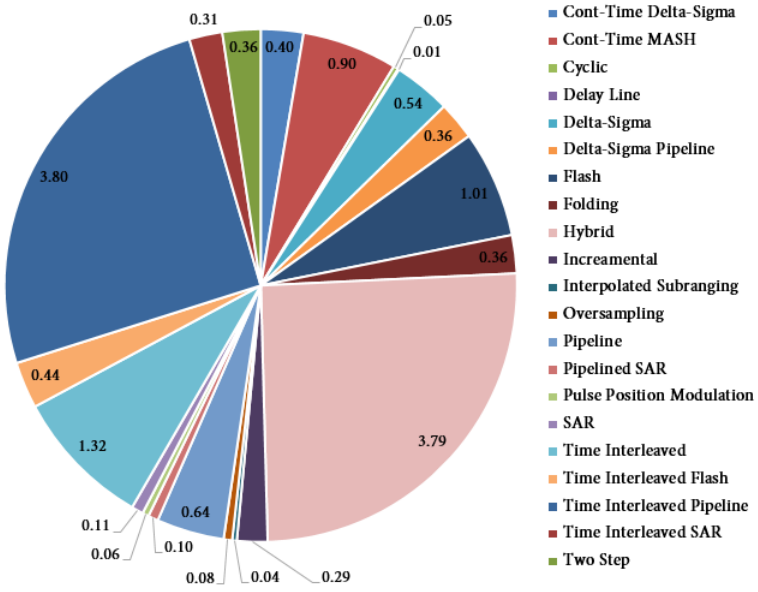


FIGURE 3.12: ADC Average area (mm^2) with different Architectures

3.2.4 *DNL and INL*

INL (Integral Nonlinearity) error and DNL (Differential Nonlinearity) error are measures of how much the input to output levels deviate from a straight line, measured in LSB. Fig. 3.13 shows the average DNL values with technology change. They do not

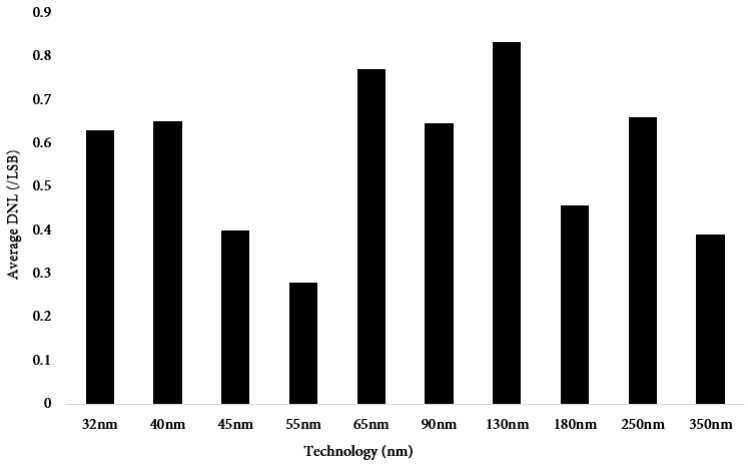


FIGURE 3.13: Average DNL values with Technologies (nm)

show significant technology dependencies. Nearly all values are less than 1. Fig. 3.14 shows the average INL values with technology change. INL values more than *1* were

shown during this survey. INL values showed more inconsistency than DNL values. DNL and INL value changes were also observed with different ADC architectures.

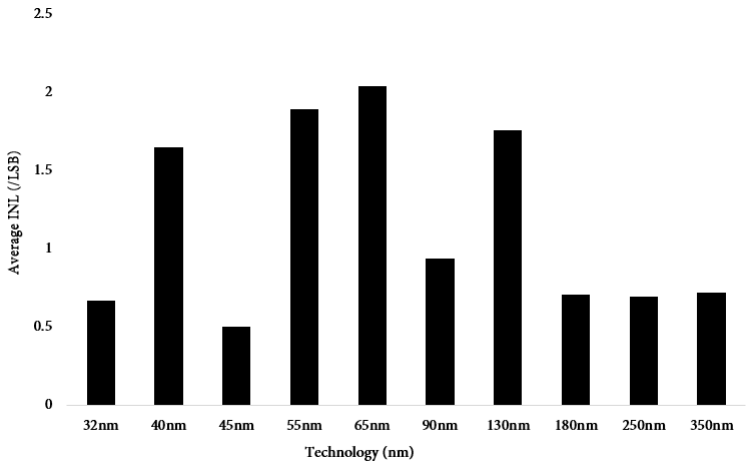


FIGURE 3.14: Average INL values with Technologies (nm)

Fig. 3.15 shows the average DNL value change with different ADC architectures. These show very little overall DNL differences. Pulse Position Modulation, Time Interleaved, and Interpolated Subranging type ADCs showed larger average DNL values compared to others, which showed fairly similar values. Fig. 3.16 shows the

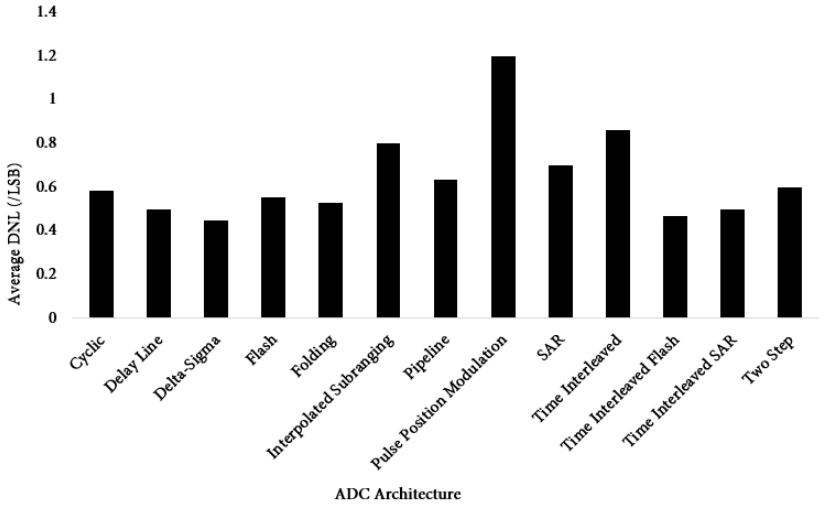


FIGURE 3.15: Average DNL values with different Architectures

average INL value change with different ADC architectures. Time Interleaved ADCs showed much larger INL values than the rest. Other designs showed comparatively

lower INL values. Flash ADCs showed lower average DNL and average INL values, which is significant.

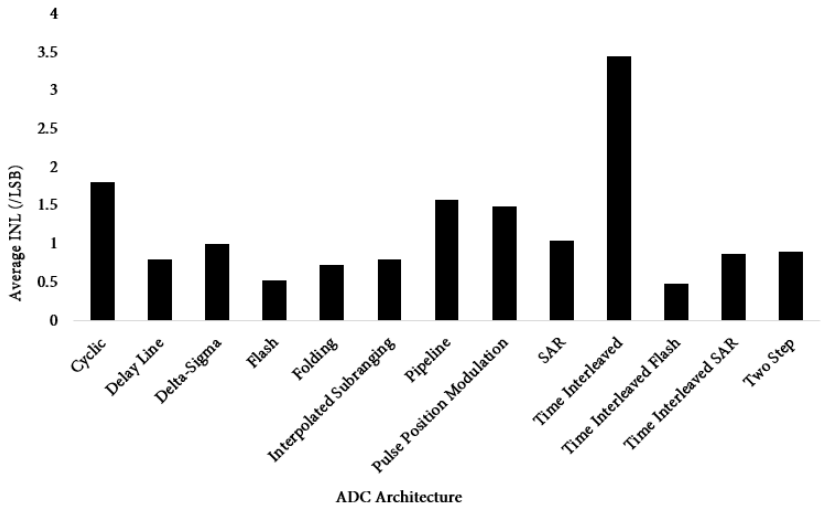


FIGURE 3.16: Average INL values with different Architectures

3.2.5 *Signal-to-Noise and Distortion Ratio (SNDR)*

SNDR (Signal to Noise and Distortion Ratio) is related to noise and the strength of the signal compared to noise and harmonics. These are important for accuracy of conversion, and ensuring ENOB is closer to the resolution. Fig. 3.17 shows the average

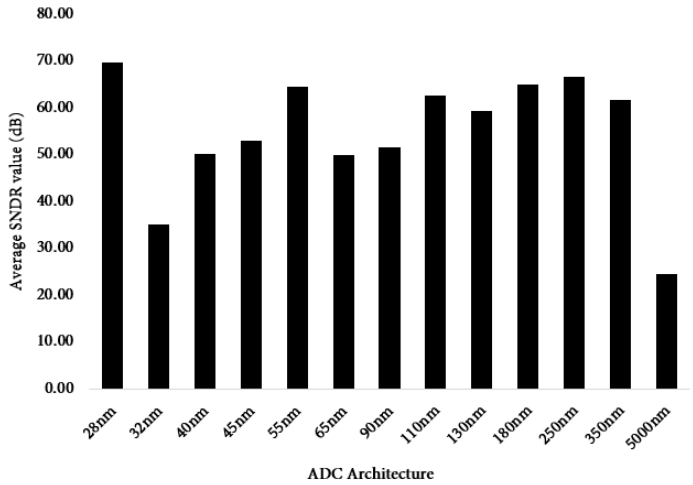


FIGURE 3.17: Average SNDR values with Technologies (nm)

SNDR values with technology change and it does not show much process dependency. Only 5000nm technology showed very low SNDR value, which is expected from a bigger technology. Fig. 3.18 shows the average SNDR values with different ADC

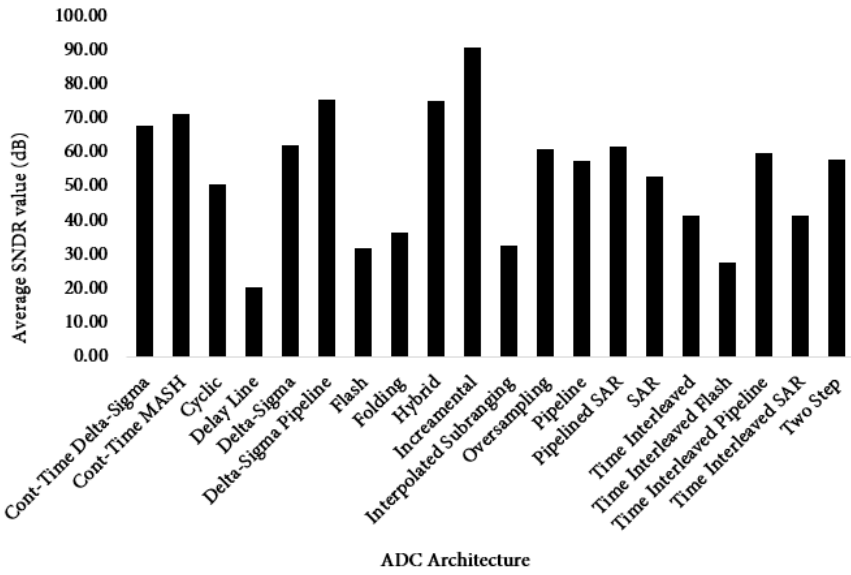


FIGURE 3.18: Average SNDR values with different Architectures

architectures. Incremental type ADCs showed the largest SNDR value. Cont-Time Delta-Sigma, Cont-Time MASH, Hybrid, and Delta-Sigma Pipeline architectures also showed reasonably good SNDR values which help noise minimization and better ENOB. Delay Line ADCs showed the smallest SNDR values which also impact ENOB harshly. Time Interleaved Flash, Flash, and Interpolated Subranging architectures also showed small SNDR values, decreasing ENOB values.

Nyquist sampling rate (f_{snyq}) is calculated by dividing sampling rate (f_s) with over-sampling ratio (OSR). And energy per Nyquist sample can be expressed as $Power/f_{snyq}$. Thus, power is directly proportional to the Nyquist sampling rate. The frequency at which SNDR is measured is expressed as $f_{in,hf}$.

ADC designs from 1997 to 2015, published in the IEEE International Solid-State Circuits Conference (ISSCC) and the IEEE Symposium on VLSI Technology Conference were studied, and Energy per Nyquist sample values are plotted against SNDR values (Fig. 3.19). Figure-of-Merit (FOM) were also plotted for all these designs which showed as an envelope for the energy values against SNDR values. From the plot, it is

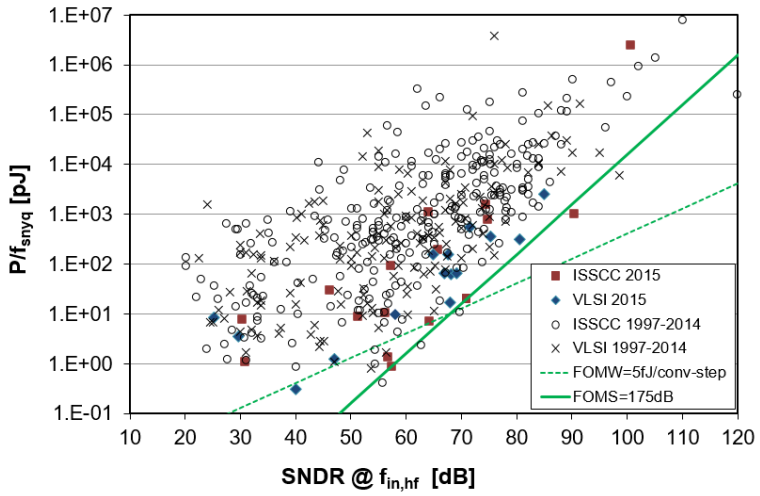


FIGURE 3.19: SNDR values against Energy per Nyquist sample [12]

clear that most of the ADCs SNDR values lie between 50dB to 85dB. Although a large group of ADCs showed their SNDR values between 25dB and 45dB. One interesting observation is, most of the ADC design from 2015 showed less energy demand with SNDR value changes. SNDR values from all these ADC designs from 1997 to 2015,

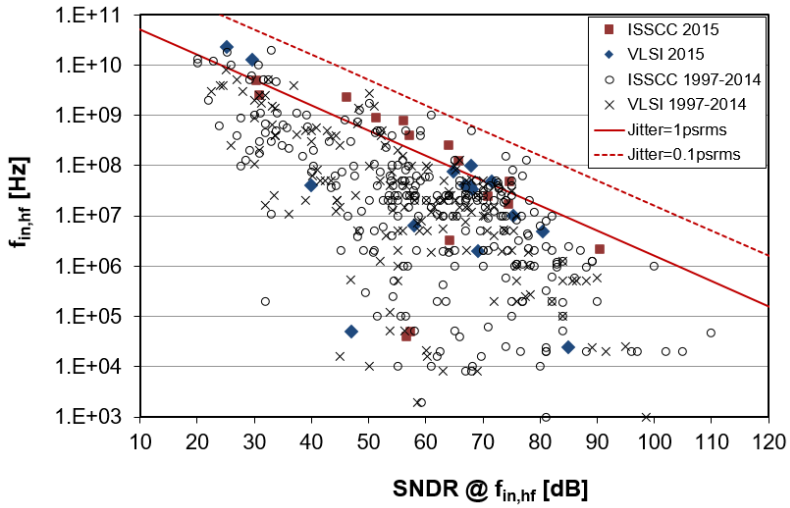


FIGURE 3.20: SNDR values against frequencies ($f_{in,hf}$) [12]

published in the IEEE International Solid-State Circuits Conference (ISSCC) and the IEEE Symposium on VLSI Technology Conference were also plotted against $f_{in,hf}$ (Fig. 3.20). Clock Jitter values were also plotted for all these designs which showed as an

envelope for the SNDR values against $f_{in,hf}$ values .
From the plot, it is shown that, if plotted against $f_{in,hf}$, most of the ADCs SNDR values lie between 45dB to 90dB. Although some ADCs showed their SNDR values between 20dB and 40dB. Adding to that, a large number of ADCs designed in 2015, showed $f_{in,hf}$ higher than average ADCs' $f_{in,hf}$ values, which are from 1997 to 2014.

3.2.6 *ADC performance summary (2010-2014)*

Table –3.1 lists a brief summary of ADCs designed in 2010 that were published in JSSC. From the table, it is clear that the Pipeline ADC dominated in 2010. The 1st design with 0.0019mW has the lowest power consumption, the 8th design is the best in terms of ENOB, the 3rd design is the best for SNDR, and 3rd and 4th designs have good DNL and INL performances. The 8th design has the highest speed.
Table –3.2 lists a brief summary of ADCs designed in 2011 that were published in JSSC. From the table, it is observed that not any single type of ADC dominated in 2011. The 1st design with 0.0013mW has the lowest power consumption, the 1st design is also the best in terms of ENOB, and it is also the best for SNDR with 57.7dB. The 7th ADC design is the overall best for DNL and INL performances with 0.47 and 0.49, respectively. The 8th design has the highest speed.
Table –3.3 lists a brief summary of ADCs designed in 2012 that were published in JSSC. It is clear that Pipeline and SAR were reported more than other ADCs. The 1st design with 0.053μW has the lowest power consumption, the 3rd design is the best in terms of ENOB with 9.83/10, the 5th design is the best for SNDR, and the 2nd design has the best DNL and INL performances with 0.25 and 0.38, respectively. The 12th design has the highest speed.
Table –3.4 lists a brief summary of ADCs designed in 2013 that were published in JSSC. From the table, it is clear that SAR ADC was more popular in 2013. The 1st design has the lowest power consumption, the 8th design is the best in terms of ENOB with 4.8/5, and the 2nd one is the best for SNDR with 63dB. The 1st ADC design is the overall best for DNL and INL performances with 0.36 and 0.44, respectively. The 9th design is the fastest one.
Table –3.5 lists a brief summary of ADCs designed in 2014 that were published in

JSSC. It is clear that Pipeline, SAR and Time Interleaved ADCs dominated in 2014. The 1st design has the lowest power consumption, the 3rd design is the best in terms of ENOB with 9.73/10, the 4th design is the best for SNDR, and the 1st design has the best DNL and INL performances with 0.09 and 0.22, respectively. The last design is the fastest.

TABLE 3.1: Brief summary of ADCs designed in 2010 published in JSSC

Technology (nm)	**Resolution (Bits)**	**Sampling Rate (MS/s)**	**Power (mW)**	**Area (mm^2)**	**Supply (V)**	**ENOB (Bits)**	**ADC Type**	**DNL (/LSB)**	**INL (/LSB)**	**SNDR (dB)**
65	10	1	0.0019	0.36	1.3	8.75	SAR	0.49	2.24	54.4
90	9	50	6.9	0.02	1	8.1	Cyclic	0.47	0.63	50.5
180	12	50	18.4	0.26	1.8	10.3	Pipeline	0.26	0.72	64
180	10	50	9.9	0.36	1.8	9.4	Pipeline	0.35	0.7	58.2
90	10	100	6	0.36	1	9.34	Two Step	0.6	0.9	58
350	11	160	594	13.3	1.8	9.9	TI	0.39	0.72	61.6
40	6	2200	2.6	0.03	1.1	5.0	Pipeline	0.8	0.8	31.6
90	6	2700	50	0.36	1	5.8	Folding	0.53	0.73	36.5

TABLE 3.2: Brief summary of ADCs designed in 2011 published in JSSC

Technology (nm)	**Resolution (Bits)**	**Sampling Rate (MS/s)**	**Power (mW)**	**Area (mm^2)**	**Supply (V)**	**ENOB (Bits)**	**ADC Type**	**DNL (/LSB)**	**INL (/LSB)**	**SNDR (dB)**
130	10	40	0.55	0.32	1.2	8.11	SAR	0.78	1.55	50.6
90	10	100	12.2	0.26	1.4	8.8	Pipeline	1	1.5	55
40	12	800	105	0.88	2.5	7.5	Pipeline	0.4	2.5	59
65	4	1200	2	0.011	1.2	3.6	Delay Line	0.5	0.8	20.4
65	8	2400	318	0.042	1	4.7	Pipeline	1.4	1.6	30.1
65	5	12000	81	0.44	1.1	4.3	TI Flash	0.47	0.49	27.5
65	6	16000	435	1.47	1.5	4.9	TI	0.6	0.7	28

TABLE 3.3: Brief summary of ADCs designed in 2012 published in JSSC

Technology (nm)	**Resolution (Bits)**	**Sampling Rate (MS/s)**	**Power (mW)**	**Area (mm^2)**	**Supply (V)**	**ENOB (Bits)**	**ADC Type**	**DNL (/LSB)**	**INL (/LSB)**	**SNDR (dB)**
130	10	0.001	0.000053	0.191	1	9.1	SAR	0.61	0.46	56.7
180	10	0.2	0.001	0.082	0.6	9.18	SAR	0.25	0.38	57.97
180	10	0.768	0.058	0.011	3.3	9.83	SAR	0.55	0.77	50.4
40	8	1.1	0.0012	0.011	0.5	7.5	SAR	1.4	1.1	46.8
90	12	30	2.95	0.36	1.2	10.4	Pipeline	0.82	1.54	64.5
250	10	80	72	4	2.5	9.4	Pipeline	0.66	0.69	58.3
65	10	200	5.37	0.19	1	9.13	Pipeline	0.38	1.36	55
40	11	300	40	0.42	1.8	9.1	Pipeline	0.3	1.5	56.6
65	8	400	4	0.028	1.2	7.1	SAR	1.6	1.5	44.5
40	6	1250	6.08	0.014	1	4.8	SAR	0.75	0.65	30.5
65	7	2200	40	0.3	1	6	TI	0.27	0.68	38
40	12	3000	500	0.4	2.5	9.3	Pipeline	0.5	2.4	58

TABLE 3.4: Brief summary of ADCs designed in 2013 published in JSSC

Technology (nm)	Resolution (Bits)	Sampling Rate (MS/s)	Power (mW)	Area (mm^2)	Supply (V)	ENOB (Bits)	ADC Type	DNL (/LSB)	INL (/LSB)	SNDR (dB)
40	9	0.02	0.00000065	0.013	0.5	8.4	SAR	0.36	0.44	50.1
65	12	0.04	0.000097	0.076	0.6	10.1	SAR	0.97	1.9	63
65	10	2	0.000053	0.212	1	8.84	SAR	0.58	0.57	55
65	10	170	2.3	0.104	1	8.8	TI SAR	0.52	0.93	54.6
65	10	300	26.6	0.36	1	8.9	Pipeline	0.52	1.65	55.4
65	10	1000	33	0.225	1.2	8.4	Pipeline	0.5	2	52.4
32	8	1200	3.1	0.0015	1	6.23	SAR	0.79	0.91	39.3
65	5	1250	0.595	0.007	1	4.8	Flash	0.67	0.47	30.7
90	6	1600	20.1	0.24	1.3	4.75	TI SAR	0.67	1.7	30.5
40	12	2100	240	0.5	2.5	10	Pipeline	0.8	6	52
90	6	4100	76	2.75	1.5	4.89	Flash	0.49	0.74	31.2
40	6	10300	242	0.27	0.9	5.35	Flash	0.5	0.4	34

TABLE 3.5: Brief summary of ADCs designed in 2014 published in JSSC

Technology (nm)	Resolution (Bits)	Sampling Rate (MS/s)	Power (mW)	Area (mm^2)	Supply (V)	ENOB (Bits)	ADC Type	DNL (/LSB)	INL (/LSB)	SNDR (dB)
180	10	0.016	0.00000058	0.12	0.6	9.73	SAR	0.09	0.22	60.5
180	10	0.1	0.00039	0.103	0.6	9.2	SAR	0.5	0.89	57.2
65	12	52	4.04	0.11	1.25	10.8	SAR	0.2	1.8	67
180	14	60	67.8	1.43	1.6	12.5	Pipeline	0.53	0.6	76.9
130	11	70	6.38	0.5	1.3	11.2	Pipeline	0.78	0.79	69.3
40	10	80	2.86	0.0656	1.1	9.15	SAR	0.7	0.7	56.85
55	12	200	30.7	0.282	1.1	10.44	Pipeline	0.28	1.89	64.4
65	10	800	19	0.18	1	8.4	Pipeline	0.9	1.8	52.2
65	6	1000	9.9	0.044	1.1	5.16	Sub ranging	0.8	0.8	32.8
65	9	1000	7.1	0.1	1	7.7	Pipeline	0.87	1.8	48
65	14	1000	1200	0.526	3.3	11.2	Pipeline	0.3	1	69
65	10	1000	18.9	0.78	1	8.2	TI SAR	1	1	51.4
65	8	4000	120	1.35	1.4	7.1	TI	0.75	1.5	44.4
65	6	10000	79.1	0.33	1.1	4.03	TI SAR	0.19	0.65	29.19
65	5	12800	162	0.23	1.2	4.6	TI	3.4	20	29.4
32	6	20000	69.5	0.25	0.9	5.49	TI	0.47	0.42	30.7

3.3 HIGH SPEED-HIGH RESOLUTION ANALOG-TO-DIGITAL CONVERTERS (ADCS)

Most of the high resolution ADCs are slow in conversion and most of the high speed ADCs feature low resolution. Flash ADCs are the fastest ADC available, but suffers from low resolution. On the other hand, Sigma-Delta ADCs have high resolution, but are very slow. SAR ADCs have moderate speed and resolution.

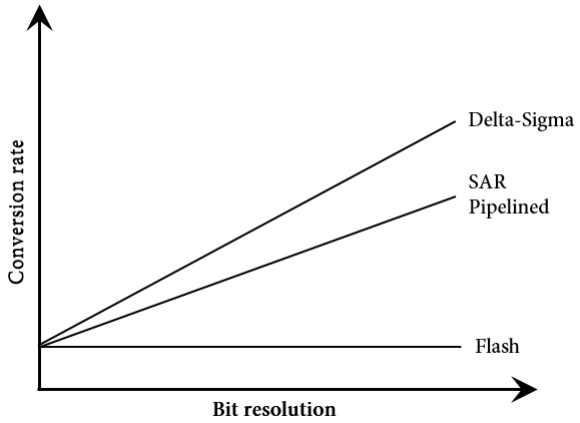


FIGURE 3.21: State-of-the-art analog-to-digital converters (ADCs)

3.3.1 *Importance of High Speed-High Resolution ADCs*

High speed ADCs have many important applications. Digital video and display electronics are two of the most widely used applications of high speed ADCs. Wideband communication systems, wireless backhaul, software defined radio (SDR), satellite applications, ultrasound and medical imaging, radar detection and sonar applications, testing, measurement and instrumentation, and wireless gigabit communications are some of the very important applications where high speed ADCs are necessary.
On the other hand, high resolution and high accuracy ADCs have also seen a wide variety of applications. Precise industrial measurements, data acquisitions, voice band and audio systems, temperature sensors, weigh scale, pressure sensors, microcontrollers, and processors are some of the most important applications of high resolution ADCs. SAR ADCs can serve for both high resolution and medium speed applications, but they have their own disadvantages including meta-stability issue.

3.3.2 *Why high resolution Flash ADCs are not common*

Flash ADCs are the fastest ADCs, capable of converting the analog to digital data in very high sampling rate. This kind of ADC is suitable for high bandwidth and fast applications. But Flash ADCs are highly power consuming, pose low resolution, and expensive. Furthermore, it also adds lot of capacitances at the input. Interpolating and folding architectures can save some power in this architecture. An n-bit Flash ADC consists of $(2^n - 1)$ comparators that are directly used to measure analog data and convert it to digital data. For a 4-bit Flash ADC, 15 comparators are needed. Analog signal is fed into 15 comparators, each of which compares the analog value with pre-defined discrete reference values.
$(2^n - 1)$ comparators also have $(2^n - 1)$ discrete digital outputs as each comparator produce either '1' or '0' after the comparison. These discrete outputs are called *Thermometer codes*. Regenerative latch at the comparator output store the results. These thermometer codes then go through a priority encoder, which encodes these data into digital out bit stream. Since all the comparators compare together, it is also called a *Parallel ADC* and has the highest sampling rate. A 5-bit Flash ADC needs 31 precise comparators, which can draw lots of power. Also, designing and fabricating a large number of highly precise comparators is a very difficult task.

When the output of a comparator cannot decide or distinguish between '1' and '0', then comparator output faces meta-stability. If meta-stability occurs, it results an incorrect thermometer code and finally incorrect digital output. Thus, due to large number of required comparators and high power consumption, high resolution flash converters are not common.

3.3.3 *Successive Approximation Register (SAR) ADC Meta-stability*

Working principle and architecture of Successive Approximation Register (SAR) ADCs are quite opposite to Flash ADCs. While in Flash ADCs, many comparators are utilized at the same time, in SAR ADCs, only one comparator is used in many cycles in a successive fashion to make the data conversion. SAR ADCs have various

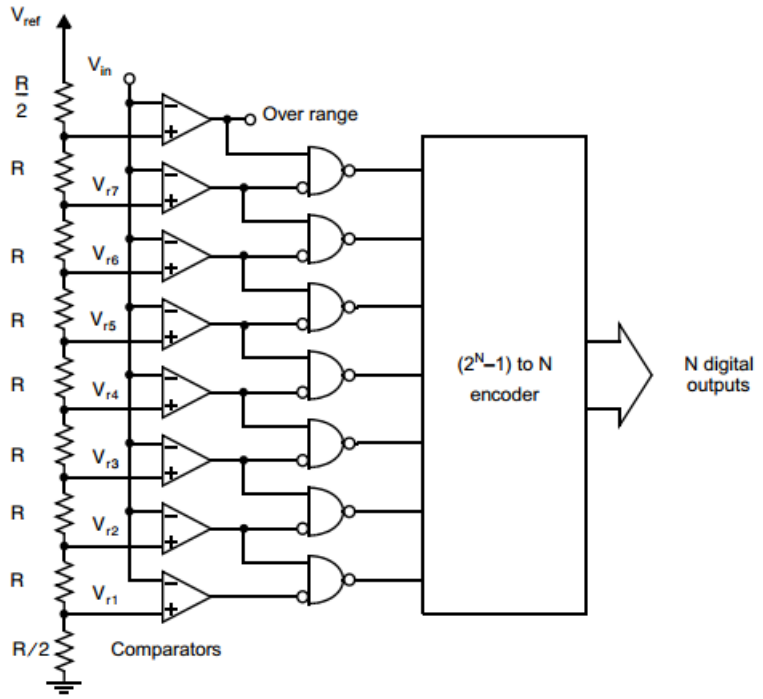


FIGURE 3.22: Typical 3-bit Flash ADC architecture [7]

applications in different sectors, as they pose medium to high resolutions, medium to high sampling rates [13], and the required area is relatively small.

Due to the balance in speed, resolution, area, and power consumption, SAR ADCs have found many applications in the area of multi-channel data acquisition, motor control, sensor interfaces, instrumentations, power factor monitoring, UPS, process control, and remote applications. SAR ADCs use binary search algorithm for data conversion which is more power efficient than Flash ADCs'. In a SAR ADC, a *sample & hold circuit* samples the input with a Nyquist rate frequency. This sampled signal level is then compared with the output of a digital-to-analog converter (DAC). This is the sequential binary search process which is initialized by setting an N-bit register to $\frac{V_{ref}}{2}$ value. If the sampled signal level is greater than $\frac{V_{ref}}{2}$, then output MSB remains at '1'. but if this sampled signal level is smaller than $\frac{V_{ref}}{2}$, then the output MSB bit is changed to '0'. This process repeats successively N-times to generate N-bits: from MSB to LSB. Thus, the resolution of this comparator is N-bits [13].

Meta-stability is a comparison issue and occurs in successive binary searching process.

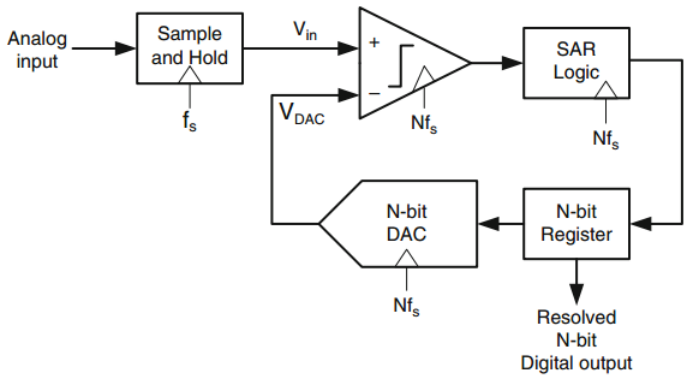


FIGURE 3.23: Typical SAR ADC architecture [13]

Although it can happen in other ADCs, SAR ADCs are the most sensitive to meta-stability. Metastable state occurs, when the output cannot decide the state as '1' or '0'. In a SAR ADC, when a metastable value is at the input of the SAR ADC algorithm, the sub-sequence steps lose their tracks. Since the time requirement is very strict, the SAR ADC conversion algorithm becomes irreversible [115].

3.4 CHALLENGES IN DESIGNING HIGH SPEED-HIGH RESOLUTION ADCS

High speed and high resolution analog-to-digital converters have many important applications. But design and implementation of these kind of ADCs are very challenging. There are many design considerations and difficulties. For example, noise, meta-stability, offset, power, ENOB, sampling rate, etc. Also, different ADC architectures have their own design challenges and restrictions.

According to the Nyquist theorem, to re-construct an analog signal from it's digital form, sampling rate should be higher than twice the bandwidth of the input signal. The faster the sampling speed in an analog to digital conversion process, the more accurate re-production of the analog signal is possible. But with high sampling rate, comes higher bandwidth requirement and power consumption, which make designing low power ADCs more challenging.

High resolution applications require high resolution ADCs. Resolution reflects how

accurate and close the digital data is, compared to its analog form. The higher the resolution, the digital form is closer to the analog form. High resolution applications like audio systems and precise instrumentations require high resolution converters, while temperature sensor and pressure sensors can work with low resolution converters.

Signal-to-noise ratio (SNR) requirements differ for various applications. Audio systems have low noise tolerance level, since it degrades the audio quality. On the other hand, temperature and pressure sensors can be more flexible in terms of noise tolerance. Since it's directly related to the resolution of the converter, signal to noise level ratio is very important.

Effective number of bits (ENOB) is an ADC performance metric. For example, due to noise and distortion, a good 12-bit ADC's ENOB can be 11.5, while for a badly affected ADC, it can be 8. Also, ENOB is a performance comparison metric for ADCs with different resolutions. For example, an 11-bit ADC with an ENOB of 10.5 is way better than a 14-bit ADC with an ENOB of 11.

Power consumption is a major concern when it comes to high speed ADC design. The more the sampling rate, the more power is needed. Thus, it's a trade-off between speed and power consumption. For low power applications, such as cellphone, high speed ADC design is a challenge.

CHAPTER 4

Soft Comparators

Traditional comparators have one common feature —they produce 1-bit digital output: either high state '1' or low state '0'. This is why these comparators can be called 1-bit analog-to-digital converter (ADC). Adding to that, the comparison decision time is usually pretty long. In this work, a unique comparator design is proposed that is capable of producing multiple bits.

4.1 SOFT AND HARD DECISION DECODING

Hard decision decoding takes a stream of binary values, for example from a threshold detector where each binary bit is either '1' or '0'. Input signal is sampled and compared with a single threshold value. If the voltage value is greater than the threshold voltage level, the binary level is labeled as '1', but if it is less than the threshold level, the binary level is labeled as '0'. In soft decision decoding, input signal is compared with different threshold levels to find the closest binary value. Thus the output is not only '0' or '1', but different combinations of '0' and '1' to represent the closest amplitude level.

For understanding soft and hard decision decoding, let's assume an even parity encoder which generates possible codewords of 000, 011, 101, and 110. Also assume the interesting transmitted message is '01' which after the parity encoder becomes '011'. Now this '011' is transmitted through a communication channel and due to noise at the output of that channel it becomes '001'. Through the transmission channel, '0' is transmitted as '0 volt' and '1' is transmitted as '1 volt' [14]. For hard decision decoding, the only threshold voltage is 0.5 volt.

But '001' is not a valid codeword according to the parity encoder. The decoder in this case compares this output with all the possible codewords and calculates the minimum *Hamming Distance* and makes a decision when it finds the minimum distance.

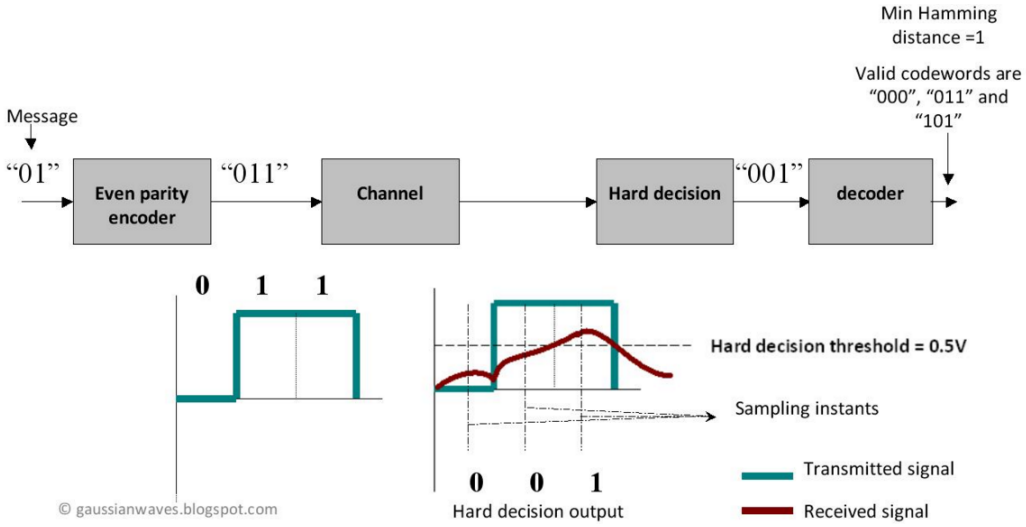


FIGURE 4.1: Hard decision decoding system setup [14]

All possible Codewords	Hard decision output	Hamming distance
000	001	1
011	001	1
101	001	1
110	001	3

FIGURE 4.2: Hard decision decoding [14]

In this case, the minimum *Hamming Distance* is '1' and for that it has three valid codewords. The decoder may choose any of these and thus the probability of picking the correct codewords is 1/3.

For soft decoding, different threshold voltage levels are used for comparison and decision making. In this case, the received information is compared with all the possible codewords and minimum *Euclidean Distance* is measured. The codeword that has the minimum Euclidean distance is taken as the correct output data [14].

In this case, three threshold voltage levels 0.7V, 0.4V and 0.2V are found as the instant voltage level of the signal. The output level is compared with all the possible codewords, Euclidean distances area measured and the minimum distance is found as 0.49 which represents the correct codeword '011'.

Thus soft decision decoder uses more information than the hard decision decoder to find the correct transmitted codewords [14].

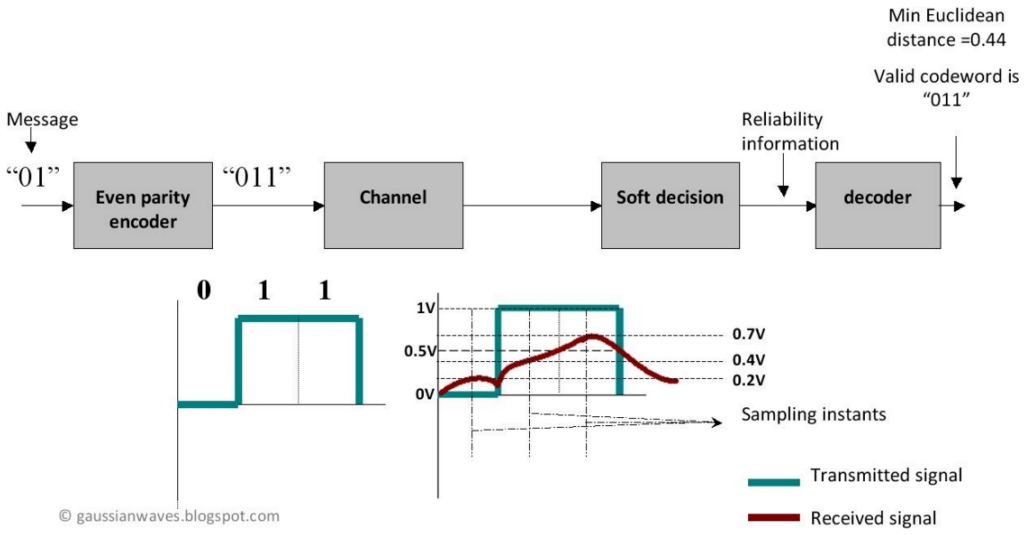


FIGURE 4.3: Soft decision decoding system setup [14]

Valid codewords	Voltage levels at each sampling instant of received waveform	Euclidean distance calculation	Euclidean distance
0 0 0 (0V 0V 0V)	0.2V 0.4V 0.7V	$(0-0.2)^2+(0-0.4)^2+(0-0.7)^2$	0.69
0 1 1 (0V 1V 1V)	0.2V 0.4V 0.7V	$(0-0.2)^2+(1-0.4)^2+(1-0.7)^2$	0.49
1 0 1 (1V 0V 1V)	0.2V 0.4V 0.7V	$(1-0.2)^2+(0-0.4)^2+(1-0.7)^2$	0.89
1 1 0 (1V 1V 0V)	0.2V 0.4V 0.7V	$(1-0.2)^2+(1-0.4)^2+(0-0.7)^2$	1.49

FIGURE 4.4: Soft decision decoding [14]

4.2 SOFT COMPARATOR AND HARD COMPARATOR CONCEPT

All the traditional comparators take two inputs to compare and produce one single bit output - either high '1' or low '0' which resembles hard decision decoding concept. Thus those comparators can be named *Hard Comparator*. In this thesis, a comparator design is proposed which resembles the soft decision decoding concept. It utilizes the comparator decision transition time and instead of one single bit output, it produces multiple bits expressing different states of the comparison process. Because of the similarities with soft decision decoding concept, this comparator is referred as *Soft*

Comparator. Thus, one comparator is capable of producing multiple bits digital output. Furthermore, traditional Flash ADCs need large numbers of comparators. For example, while designing 12-bit Flash ADC, $(2^{12} - 1)$ precise comparators are needed which require lots of power. Mismatch among the transistors can introduce offset. Using the proposed comparator, it is possible to design high resolution Flash ADCs with a smaller number of comparators. For example, if the soft comparator is capable of producing 4-bits of output, a 5-bit Flash ADC will only need 4 soft comparators, which is certainly capable of bring down the power requirements.

4.3 SOFT COMPARATOR ARCHITECTURE

The soft comparator basic structure is simple and divided into a few submodules. The heart of this circuit is a back-to-back NOT gate based dynamic latched comparator which can make the comparison decision quickly.

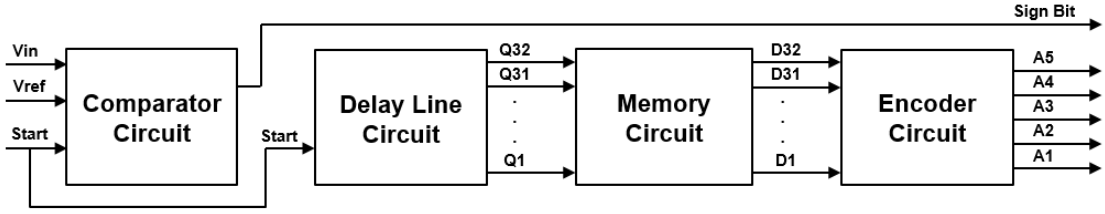


FIGURE 4.5: Soft Comparator basic block diagram

After the comparator, an XOR gate and a buffer are used followed by a delay line which is made out of tristate NOT gates, a NOT gate and a buffer circuit. The delay line is comprised of 32 delay cells connected in series. Each of these delay cells consists of a tristate NOT gate, a NOT gate and a buffer circuit. After the delay line circuit, a memory circuit is used. The memory circuit is comprised of 32 D-latches connected in parallel. Each of these D-latches is comprised of two transmission gates, a NAND gate and two NOT gates. At the end of these sub-modules, there is a 32-to-5 encoder circuit which encodes the 32 digital output from the memory circuit into 5 bit output. Fig. 4.5 shows the soft comparator basic block diagram consisting of major sub-modules.

4.3.1 *Soft Comparator schematic diagram*

The soft comparator schematic and layout are designed with Cadence Virtuoso IBM 130nm CMOS technology. Fig. 4.6 shows the soft comparator schematic diagram comprising all the sub-modules.

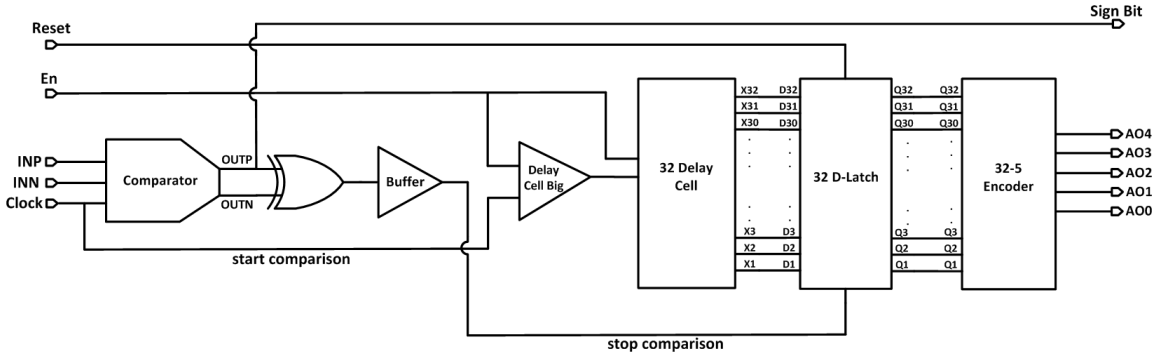


FIGURE 4.6: Soft comparator schematic diagram

Among all these sub-modules, the major sub-modules are the dynamic latched comparator, 32 delay cells or the delay line circuit, 32 D-latches in parallel or the memory circuit, and a 32-to-5 simple encoder circuit. For this soft comparator, two different supply voltages are used. The dynamic comparator uses 800mV (V_{dd1}) and the rest of the circuits use 1.2V (V_{dd}). At the comparator INN input, 600mV is used as input common mode voltage. Reset voltage is 1.2V and digital pulse source is used as Enable (En) signal.

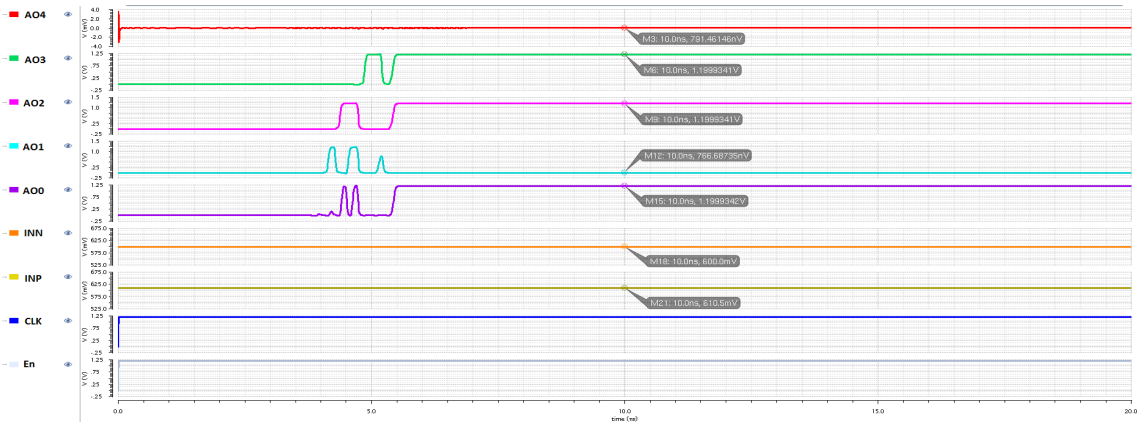


FIGURE 4.7: Soft Comparator output with INP = 610mV and INN = 600mV

This enable signal switches from V_1=0V to V_2= 1.2V, its period is 130ns, pulse width is 65ns, the rise and fall time is 15ps and zero delay time is used. Another digital pulse source is used as the Clock signal (CLK). This clock signal switches from V_1=0V to V_2= 1.2V, period is 40ns, pulse width is 20ns, the rise and fall time is 15ps and zero delay time is used. Fig. 4.7 shows a 6-bit soft comparator output, where INP=610mv and INN=600mV are used. CLK signal and Enable (EN) signal are *High*. Here, Sign Bit ='1' and 5-bit digital output is '10110', which represents AO4=1, AO3=0, AO3=1, AO2=1, and AO0=0.

4.3.2 *Dynamic Latched Comparator*

The dynamic latched comparator used in the soft comparator design, is proposed in one energy efficient SAR ADC design and it is a dynamic two stage comparator [10]. The first stage is a pre-amplifier that performs the amplification of the input signal difference. The second stage acts as another voltage amplifier and also as a positive feedback amplifier which helps to create rail-to-rail voltage as digital output. This design was first designed for IBM 180nm CMOS and then was redesigned in IBM 130nm CMOS technology. For designing and simulating this dynamic latched comparator, a clock signal with a period of 40ns and pulse width of 20ns is used. The clock switches from V_1=0V to V_2= 1.2V, and its rising and falling times are 15ps each with no delay. The supply voltage V_{dd1} was used 800mV for this comparator.

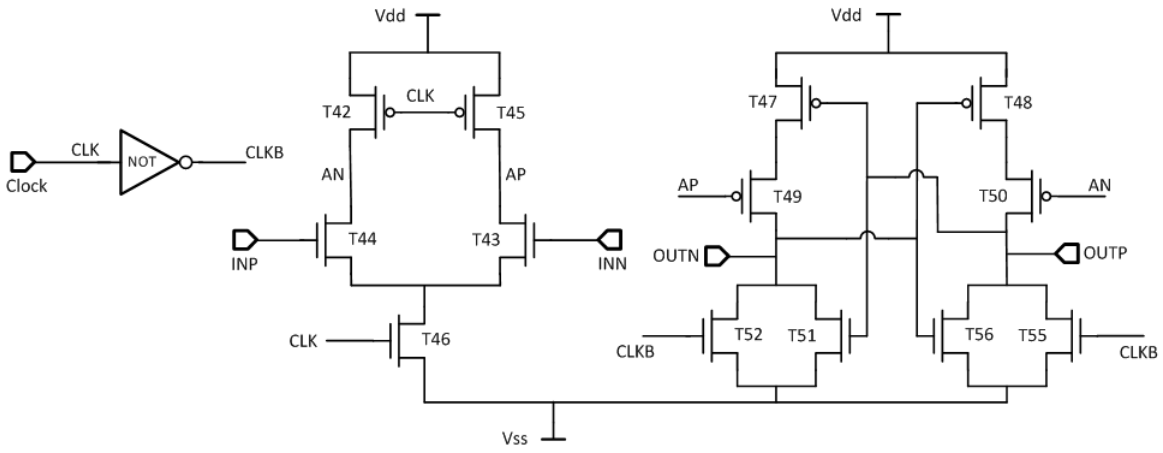


FIGURE 4.8: Dynamic Two-stage Latched Comparator

For inputs INN=600mv and INP=610mV, supply voltage of 800mV, a clock signal of 40ns period and V_1=0V to V_2= 1.2V, the output node voltages (OUTP and OUTN) during the comparison phase are observed.

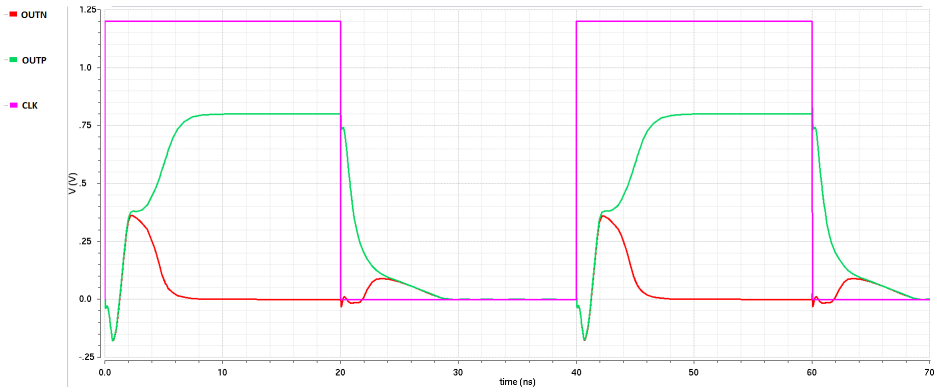


FIGURE 4.9: Comparator nodes OUTP and OUTN during comparison

The common mode voltage is 600mV which is applied at the input INN. If the input at INP now increases from 600Mv to higher values, for example up to 1.2V, the transition, decision making time, or output settling time of the dynamic comparator will be shorter. Because of bigger voltage difference between the inputs, it is easier for the comparator to make a comparison decision compared to the case when both input voltage values are very close. Here, output OUTP settling time is defined as the 95% voltage value of the maximum or, final OUTP value, which in this case is 1.2V. Thus when OUTP reaches the 95% of its final voltage value, the comparator makes a

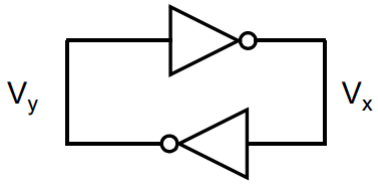


FIGURE 4.10: Simplified model of Comparator in Latch Mode [7]

decision - either OUTP is '1' and OUTN is '0' or, vice versa. For this comparator, latch time constant is very important. The time constant of the latch when the comparator is in latch mode can be calculated by analyzing a simplified back-to-back NOT gate based circuit shown in Fig. 4.10 [7].

If the output voltages V_x and V_y of the inverters are very close at the start of latch mode, they will be in linear range. At that point, each of these inverters can be modeled as voltage controlled current sources driving a RC load (Fig. 4.11) where A_v is a low-frequency gain of each of the inverters [7].

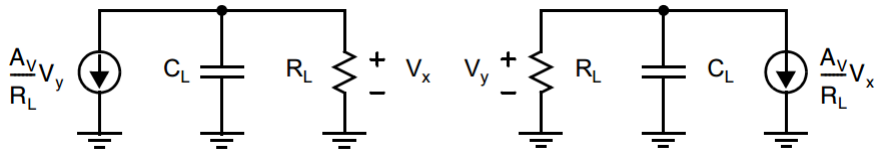


FIGURE 4.11: Linearized model of track-and-latch stage in Latch Mode [7]

For this linearized model, it can be written:

$$\frac{A_V}{R_L}V_y = -C_L(\frac{dV_x}{dt}) - (\frac{V_x}{R_L}) \tag{4.1}$$

$$\frac{A_V}{R_L}V_x = -C_L(\frac{dV_y}{dt}) - (\frac{V_y}{R_L}) \tag{4.2}$$

Time constant, $\tau = R_L C_L$ and by rearranging the above equations, we get:

$$(\frac{\tau}{A_V - 1})(\frac{d\Delta V}{dt}) = \Delta V \tag{4.3}$$

Where, $\Delta V = V_x - V_y$, is the inverters output voltage difference. Equation 4.3 is a first-order differential equation with solution,

$$\Delta V = \Delta V_o e^{\frac{(A_V - 1)t}{\tau}} = \Delta V_o e^{kt} \tag{4.4}$$

In equation 4.4, k is a constant, t represents the settling time (t_{st}) and ΔV_o is the initial voltage difference between the inputs. ΔV can be expressed as ΔV_{logic}, which is the voltage difference between bit=1 and bit=0. Thus settling time is a decreasing function of input voltage difference:

$$t_{st} = \frac{1}{k} ln(\frac{\Delta V_{logic}}{\Delta V_o}) \tag{4.5}$$

If ΔV_o is small, the settling time will be large, and can be even larger than the allowed time for the latch mode. That incident is referred to as *Metastability*. In other words, if

the initial value difference ΔV_o is very small, the differential output voltage does not increase enough to be recognized as the correct logic value [7].

In this dynamic comparator, by keeping the INN at 600mV, the INP value has been increased from 600.001mV to 1100mV. The output OUTP settling time is then plotted against the input voltage difference. Here, it is observed that, after around 2.9ns the curve becomes *saturated*. Thus, even after increasing the common mode input voltage difference beyond 500mV, the settling time does not reduce noticeably.

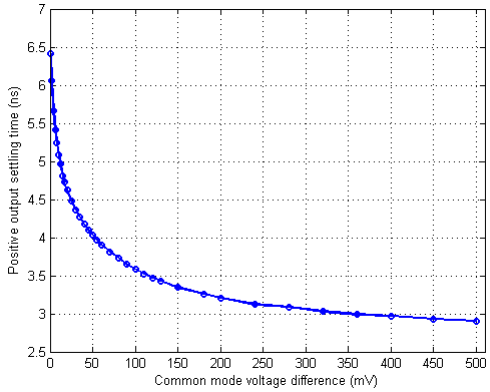


FIGURE 4.12: Output Settling Time with Input Common Mode Voltage Difference

TABLE 4.1: Design parameters for the Latched Comparator

Transistor	**(W/L) Ratio**
T42	870n/1μ
T45	870n/1μ
T44	4.4μ/2μ
T43	4.4μ/2μ
T46	4.4μ/2μ
T47	3μ/1μ
T48	3μ/1μ
T49	3μ/1μ
T50	3μ/1μ
T52	870n/1μ
T51	870n/1μ
T56	870n/1μ
T55	870n/1μ

4.3.3 *XOR Gate and Buffer Circuit*

One XOR gate is used immediately after the dynamic latched comparator. The purpose of this XOR gate is to make sure that OUTP and OUTN signals becomes totally of opposite states. When the comparator makes a comparison decision, then OUTP

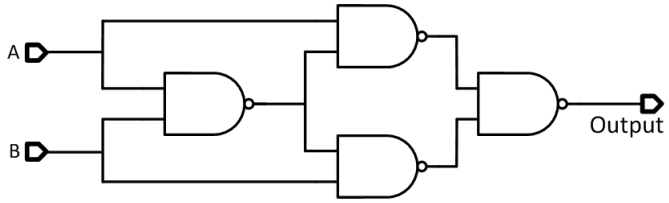


FIGURE 4.13: XOR gate designed with 4 two-input NAND gate

should be '1' (if INP is greater than INN) and OUTN should be 'o' or, OUTP should be 'o' (if INP is smaller than INN) and OUTN should be '1'. As both OUTP and OUTN are analog signals, to make their decision a perfect digital, this XOR gate is used. The XOR gate is designed with 4 two input NAND gates. For designing a NAND gate, two PMOS of size (W/L=480nm/130nm) and two NMOS of size (W/L=480nm/130nm) are used. Fig. 4.14 shows the XOR gate checks whether the dynamic comparator

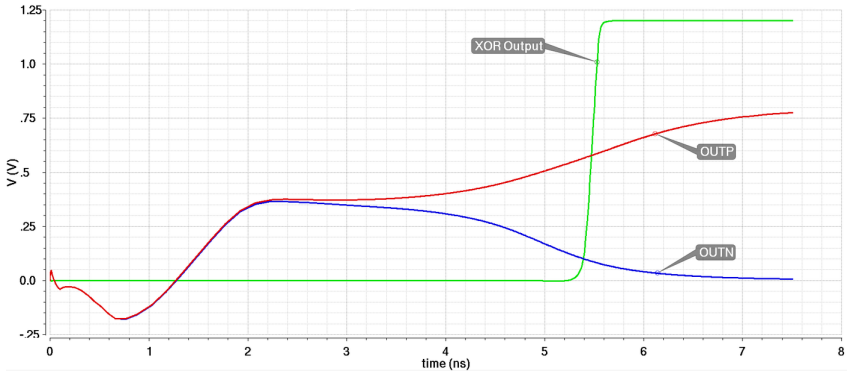


FIGURE 4.14: XOR Gate checks Comparator Output settling

output settles. Although this XOR gate makes sure that the OUTP and OUTN signals become a perfect digital and produce a high output at its own output, the digital signal at the XOR output degrades due to load effect. To restore the signal to its perfect digital shape, one buffer is used immediately after the XOR gate output. The

buffer circuit is designed with two back-to-back NOT gates connected in a series. For the NOT gate, one PMOS transistor of size (W/L=480nm/130nm) and one NMOS transistor of size (W/L=240nm/130nm) are used.

4.3.4 *Delay Line Circuit*

In this soft comparator design, comparator settling time has been utilized to get more than a single bit information at the comparator output. To meet this purpose, a delay line circuit has been used. As mentioned, when the comparator inputs are very close, the settling time is the largest. For example, when INN =600mV and INP=601mV are used, the comparator positive output OUTP settling time is about 6.4ns. Thus for very small common mode input voltage difference, 6.4ns is the time duration the comparator needs to finally make a stable decision. Also, over a 500mV common mode input voltage difference, the settling time becomes almost saturated. Even after increasing the common mode input voltage difference beyond that, the settling time doesn't become significantly smaller.

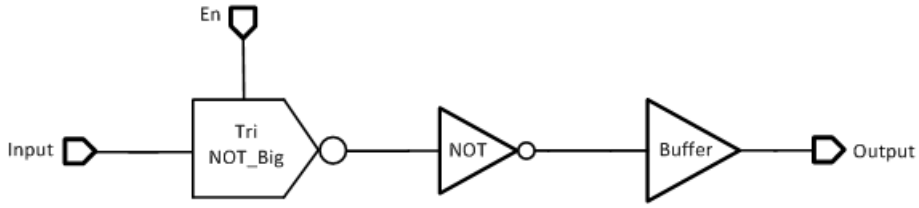


FIGURE 4.15: Big Delay Cell circuit

Thus the total settling time 6.4ns is divided into two parts - from zero to 3ns, when the settling time doesn't get affected by common mode input voltage difference alteration and from 3ns to 6.4ns, when settling time drastically changes with common mode input voltage differences. The first 3ns can be expressed by a *Big Delay Cell* which delays the signal by around 3ns. This *Big Delay Cell* is comprised of a big tristate NOT gate, a NOT gate and a Buffer circuit (Fig. 4.15). The buffer is a simple circuit consisting of two back-to-back NOT gates. The big tristate NOT gate is a special NOT gate with an *Enable* signal (Fig. 4.16). When the *Enable (En)* signal is high, MOSFETs To and T1 will be activated and the circuit will work as a regular NOT gate but with

a bigger signal delay. But when the *Enable (En)* signal is low, MOSFETs To and T1 will be disconnected putting the output at a floating state, which will hold on to its previous value. Thus big tristate NOT gate acts as a *delayed-controlled NOT gate*.

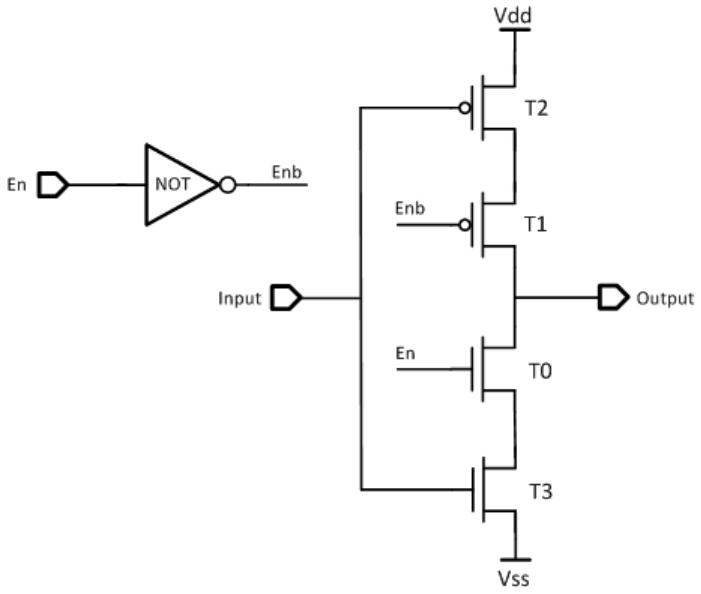


FIGURE 4.16: Big Tristate NOT Gate circuit

TABLE 4.2: Design parameters for the Big Tristate NOT Gate

Transistor	(W/L) Ratio
T2	$2\mu/1.5\mu$
T1	$2\mu/1.5\mu$
To	$1\mu/6\mu$
T3	$1\mu/6\mu$

The second part of the total delay, 3.4ns is divided among 32 smaller delay cells, making each small delay cell's delay around 0.1ns. The 32 delay cells are collectively named as delay line circuit or 32 delay cells (Fig. 4.17).

This circuit is capable of delaying the input signal by around 3.4ns. It consists of four sub-modules - four 8 delay cells and an n-type MOSFET. Its drain and source are connected making it a capacitor built with MOSFET. This MOSFET works as a dummy load for the delay line circuit to improve matching (Fig. 4.18). The total delay line circuit is sub-divided among four 8 delay cells in order to design the layout

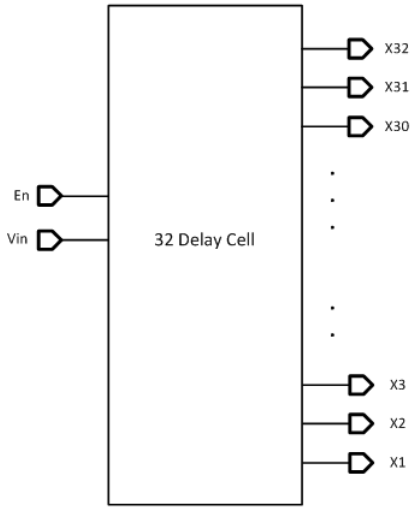


FIGURE 4.17: Delay Line Circuit symbol

easily. The n-type MOSFET (TN0) is used here as a dummy load with size W=1μm and L=500nm.

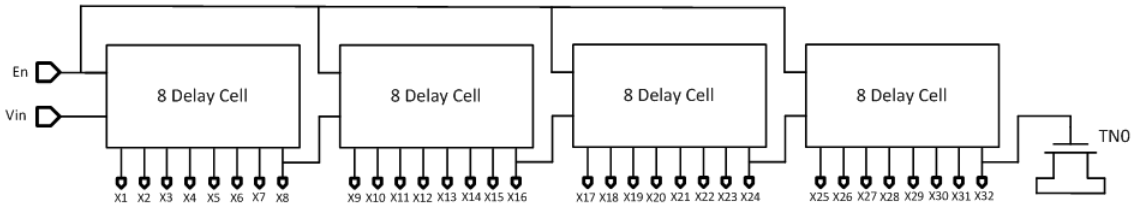


FIGURE 4.18: Delay Line Circuit schematic diagram

Each sub-module has 8 small Delay Cells connected in a series. All the delay cells' *Enable (En)* signals are connected together so that they are active at the same time and also can be deactivated at the same time. The overall 0.85ns signal delay can be achieved with each of these 8 delay cell circuits. Each delay cell has one output, making it an eight-output delay circuit.

Each smaller delay cell is called only *Delay Cell* and is capable of delaying the input digital signal by around 0.1ns. The schematic of this circuit is exactly same as the big delay cell, but with a smaller tristate NOT gate. It is comprised of a tristate NOT gate, a NOT gate and a buffer circuit (Fig. 4.20).

The buffer is a simple circuit consisting of two back-to-back NOT gates. The tristate NOT gate is a NOT gate with an *Enable* signal (Fig. 4.21). But in this case,

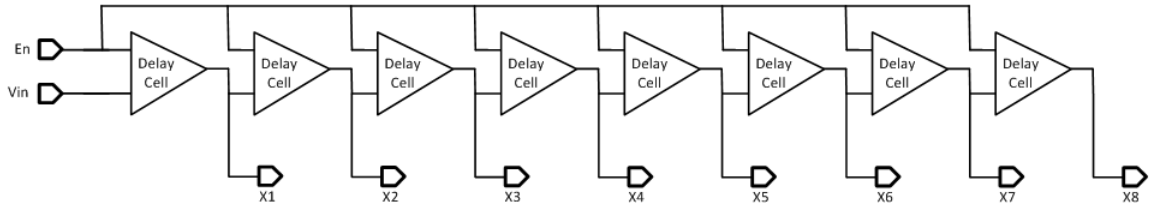


FIGURE 4.19: 8 Delay Cells connected together

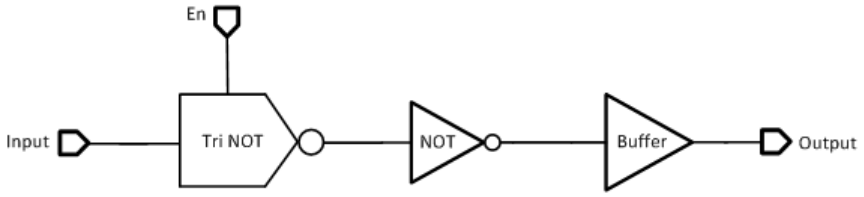


FIGURE 4.20: Delay Cell circuit

the tristate NOT gate is much smaller than the big tristate NOT gate as the later one cannot delay signal as much as the big tristate NOT gate. Thus tristate NOT gate acts as a *delayed-controlled NOT gate* with smaller delay capability.

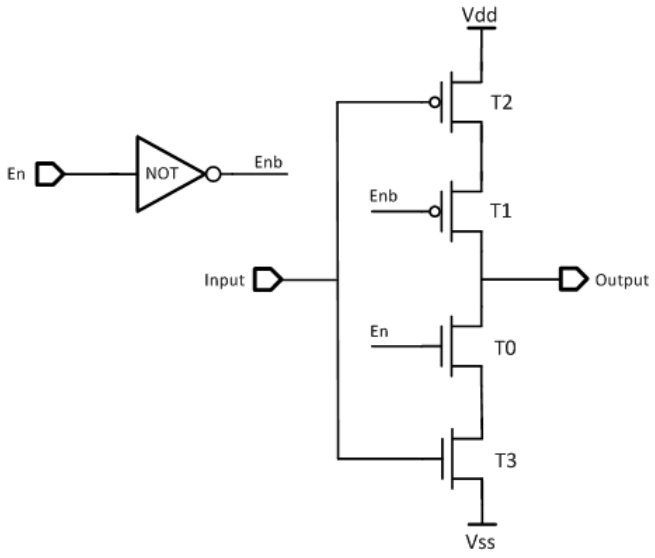


FIGURE 4.21: Tristate NOT Gate circuit

TABLE 4.3: Design parameters for the Tristate NOT Gate

Transistor	(W/L) Ratio
T2	380n/140n
T1	380n/140n
T0	900n/140n
T3	900n/140n

4.3.5 *Memory Circuit*

After the final comparison decision, the latched comparator output becomes *perfectly digital* through the XOR gate and buffer circuit. When the XOR gate becomes high, the propagation of *start comparison* signal through the delay cells stops.

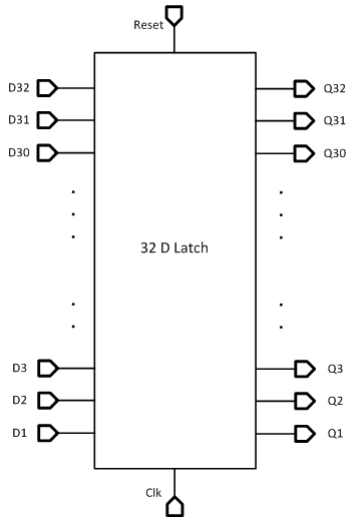


FIGURE 4.22: D-latch based Memory circuit

Each of these 32 delay cells have outputs that represent the different states of the comparison phase. These 32 outputs need to be stored for any instance so that it can be ended in the subsequent stage. For this purpose, 32 D-latch circuits are used in parallel fashion (Fig. 4.19). 32 delay cells' outputs work as 32 D-latches' inputs. All 32 D-latches *Reset* signals are connected and set as *high* in normal operation. All 32 D-latches *CLK* signals are tied together and use Buffer output as the clock signal.

When dynamic comparator is done with the comparison decision, the output of the buffer becomes *high* and at the same moment memory circuit should *stop* taking

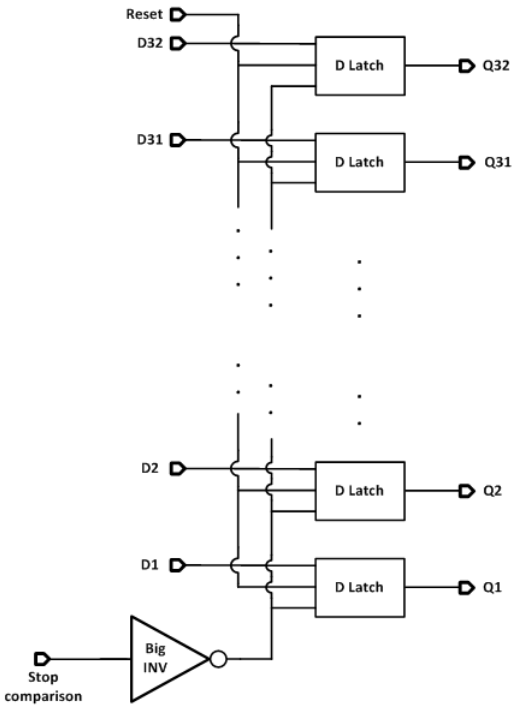


FIGURE 4.23: 32 D-latch connected in parallel

the data at its input and holds onto the last value. Thus the buffer output goes to the memory circuit through a big inverter designed with PMOS size W/L=4μm/130nm and NMOS size W/L=2μm/130nm. This big inverter makes the signal a *clean strong signal*. This inverted buffer output signal which is now a low state signal goes to each of these 32 D-latches *stop comparison* signal (Fig. 4.23).

The D-latch circuit is comprised of a NOT gate, which inverts the incoming clock signal from the big inverter, two transmission gates, one NAND gate and another NOT gate at the end. In this D-latch circuit, when Clock is low, first transmission gate gets disconnected and the output holds on to the last comparison state. But when the Clock is high, the incoming data *D* can pass through the first transmission gate, but the second transmission gate gets disconnected. Thus data goes through the NAND gate and then through the end NOT gate and data *D* can go all the way to output (Fig. 4.24).

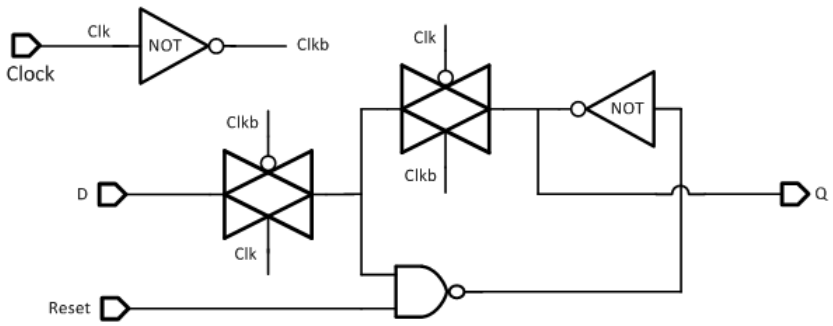


FIGURE 4.24: Schematic of the used D-latch circuit

4.3.6 *Encoder Circuit*

After getting all the 32 memory circuit outputs, these outputs need to be encoded into 5- bits. For this purpose, immediately after the memory circuit, a 32-to-5 encoder circuit is used. It simply takes all the 32 memory circuit outputs and encodes them into 5-bit digital output (Fig. 4.25).

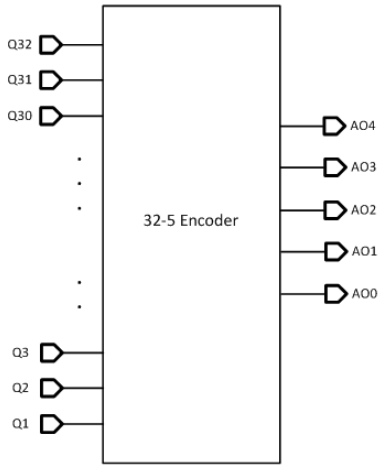


FIGURE 4.25: 32-to-5 Encoder Circuit symbol

The encoder circuit is comprised of 32 XOR gates, five 16-bit OR gates and an n-type dummy MOSFET (To) of size W=240nm and L=130nm, in a diode connected fashion (Fig. 4.26). This MOSFET To is used to prevent X1 output to become a floating node as X1 is not used in the encoder internal connections. Except the 32nd XOR gate, all other 31 XOR gates share one common input with its immediate XOR gate input.

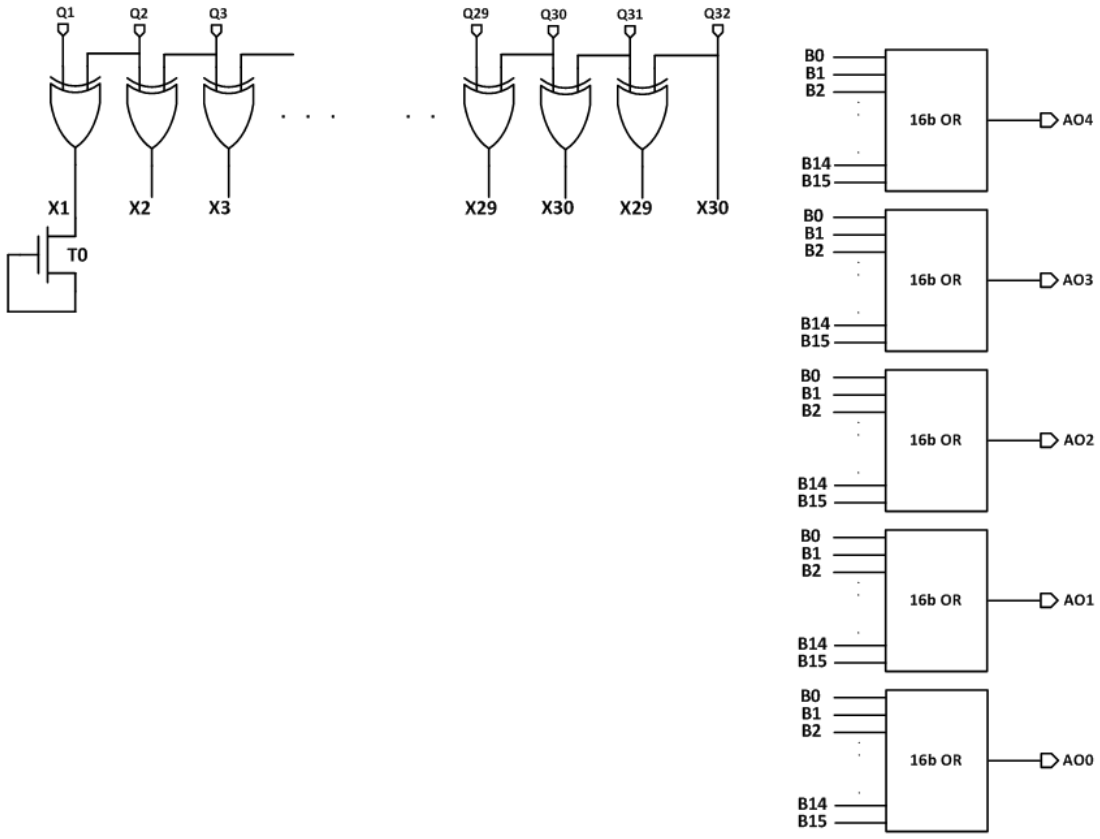


FIGURE 4.26: Schematic of 32-to-5 Encoder circuit

The 16-bit OR gates are connected with the XOR gates with following equations -

$$AO0 = X17 + X18 + X19 + X20 + X21 + X22 + X23 + X24 + X25 + X26 + X27 + X28 + X29 + X30 + X31 + X32 \quad (4.6)$$

$$AO1 = X9 + X10 + X11 + X12 + X13 + X14 + X15 + X16 + X25 + X26 + X27 + X28 + X29 + X30 + X31 + X32 \quad (4.7)$$

$$AO2 = X5 + X6 + X7 + X8 + X13 + X14 + X15 + X16 + X21 + X22 + X23 + X24 + X29 + X30 + X31 + X32 \quad (4.8)$$

$$AO3 = X3 + X4 + X7 + X8 + X11 + X12 + X15 + X16 + X19 + X20 + X23 + X24 + X27 + X28 + X31 + X32 \quad (4.9)$$

$$AO4 = X2 + X4 + X6 + X8 + X10 + X12 + X14 + X16 + X18 + X20 + X22 + X24 + X26 + X28 + X30 + X32 \quad (4.10)$$

Each of these five 16-bit OR gate are designed with four 4-bit NOR gates and one 4-bit NAND gate (Fig. 4.27). All the four 4-bit NOR gates outputs are acting as four inputs of the 4-bit NAND gate.

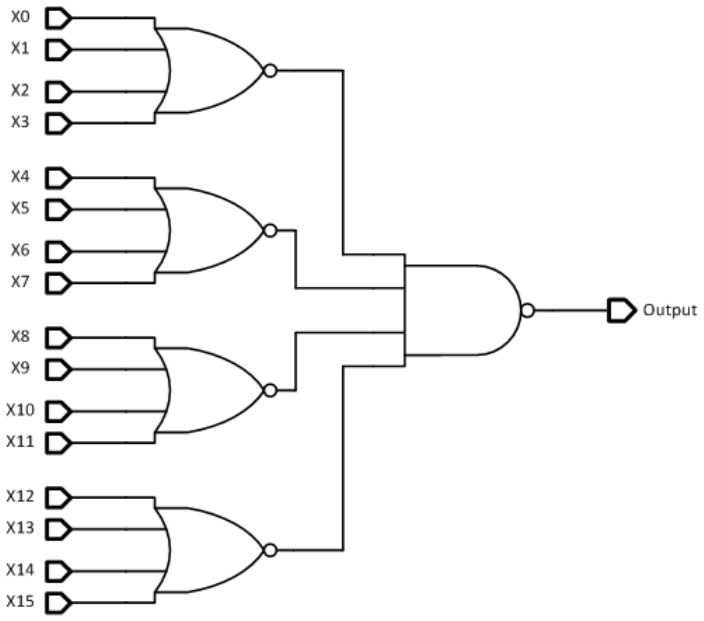


FIGURE 4.27: Schematic of 16-bit OR gate

Each of the 4-bit NOT gates was designed with 4 PMOS (W/L=1.92μ/130n) transistors and 4 NMOS (W/L=240n/130n) transistors. On the other hand, the 4-bit NAND gate was designed with 4 PMOS (W/L=480n/130n) transistors and 4 NMOS (W/L=960n/130n) transistors.

4.4 HOW SOFT COMPARATOR WORKS

The whole purpose of designing the soft comparator is to utilize the dynamic latched comparator's output settling time and extract multiple bits of information. The dynamic comparator works with 800mV while the rest of the soft comparator circuit works with 1.2V supply voltage.

One input of the dynamic comparator INN is held at 600mV which works as the reference voltage. Input analog signal is applied at the other input INP. The dynamic comparator compares INP and INN and produces decision outputs OUTP and OUTN.

If INP is bigger than INN, then OUTP will rise to high and OUTN will fall to zero. If INP is smaller than INN, then OUTN will rise to high and OUTP will fall to zero. Either way after the comparison, both OUTP and OUTN will be in different states.
These two OUTP and OUTN signals are then used as input for the subsequent module XOR gate. As mentioned earlier, this XOR makes sure that OUTP and OUTN signals are completely in different states and produces a high signal at its own output, which indicates the comparison is done. But due to transient behavior the XOR output is not a *clean* digital signal. To restore this signal to a perfect digital output, a buffer circuit is used after the XOR gate. The buffer circuit makes sure that the signal restores to its perfect digital shape.
After the buffer circuit, one big delay cell is used which needs *Enable* high signal to commence working and a 'start comparison' high signal. This 'start comparison' signal comes from the dynamic comparator input 'start comparison' signal. Thus when the dynamic comparator 'start comparison' signal becomes high, it starts the comparison process. At the same time the big delay cell starts *delaying* the clock signal which it takes as input.
After the big delay cell, which delays the clock signal by around 3ns, a delay line circuit is used which delays the output of the big delay cell by roughly 0.1ns per delay cell. This delay line circuit has 32 outputs that are the 32 inputs of the memory circuit which stores these 32 state values. When the buffer circuit output becomes *perfectly* high, that indicates comparison and decision making is done. Thus the buffer output works as the clock signal for the memory circuit. As soon as the buffer output becomes high, the memory circuit stops taking inputs and stores its last state values. These 32 state values represent the settling times. The memory circuit has a *Reset* signal which can clear the memory when necessary and make the memory circuit ready for taking the next comparison input values.
The 32 outputs of the memory circuit then go to the 32-to-5 encoder circuit. The encoder circuit encodes the 32 digital signal into 5-bit digital values and shows them at the 5 outputs - from AO0 to AO4. Thus the soft comparator produces 5-bit digital output corresponding to the magnitude and one sign bit based on OUTP for the polarity, which add up to 6-bits instead of one single bit digital output.

4.5 SOFT COMPARATOR NOISE ANALYSIS

In a flash ADC, to generate a digital output with m bits, we need $2^m - 1$ hard comparators with different thresholds. The difference between two consecutive comparator threshold voltages is one least significant bit (LSB). Each of them produces one bit output. When the input voltage is greater than the threshold, the output is "1" and otherwise the output is "0".

Since the number of comparators grows exponentially with m, using a soft overlapping comparator with multiple output bits is extremely useful. If the input voltage is greater than the threshold, then the first bit is "1" and other bits determine how much is the difference between the input and the threshold voltage. Similarly, for smaller inputs, the first bit is a "0" and other bits indicate the difference.

By smartly choosing the threshold voltages we can reduce the number of comparators while designing ADCs. This section discusses the performance of soft overlapping comparators in the presence of noise. First we analyzed the performance of a single soft comparator. Then we extended the idea to multiple soft comparators.

4.5.1 *Single Soft Comparator*

Fig. 4.28 shows a simple model for a comparator, where an equivalent noise voltage source is added with the ideal input voltage and it causes different measured times and digital outputs. For simplicity, we assume that comparator's offset is removed

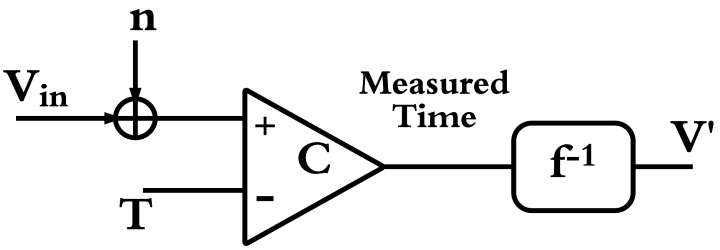


FIGURE 4.28: Single Soft Comparator

during the calibration process. The result of the calibration process is a noise-free curve that depicts the decision making time (t) versus input voltage (V_{in}). A sample

calibration curve is depicted in Fig. 4.29 for a single soft comparator.

The x-axis denotes the voltage difference between the applied input voltage and

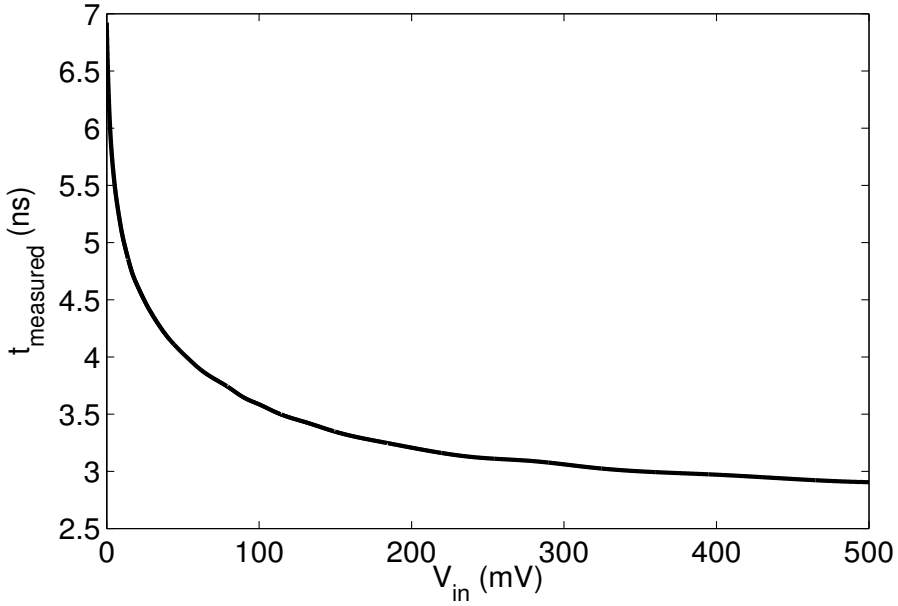


FIGURE 4.29: Decision-making time for different common mode voltage difference in a single soft comparator

threshold voltage and the y-axis denotes the required decision making time for the comparator. In the presence of noise, for a given V_{in} the decision making time $t_{measured}$ is a random process. Let's assume we would like to determine V_{in} by measuring $t_{measured}$ and using the curve in Fig. 4.29. We denote the estimated input voltage by $\hat{V}$ and

$$t_{measured} = f(\hat{V}). \tag{4.11}$$

Thus for comparator C the estimated output can be written as

$$\hat{V} = V_{in} + n, \tag{4.12}$$

where (n) is an Additive White Gaussian Noise (AWGN) with zero mean and variance σ^2. Furthermore, let us assume, there are k points on the V_{in} axis, i.e. V_1, V_2,$\cdots$, V_k, corresponding to "00..01", "00..10", $\cdots$, "111..11" in digital format. For an $(m+1)$-bit soft comparator we have $k = 2^m - 1$ different voltage points on the V_{in} axis that

determine the equivalent digital output. In the presence of noise, using the curve in Fig. 4.29 we can measure the corresponding random variable $\hat{V}$. Then using (4.12), we can calculate the probability that V_{in} is within the interval (V_1, V_2). Similarly, for other intervals the probability can be generated. Finally, the interval with the highest probability specifies the estimated output. Now consider a fixed input voltage V_{in} is applied to an $(m+1)$-bit soft comparator. In general, the probability that V_{in} is within the interval (V_i, V_{i+1}) can be calculated as:

$$\begin{aligned} \Pr\{V_i < V_{in} < V_{i+1}\} &= \Pr\{V_i < \hat{V} - n < V_{i+1}\} \\ &= \Pr\{V_i - \hat{V} < -n < V_{i+1} - \hat{V}\} \\ &= \frac{1}{2}\left[erf\left(\frac{V_{i+1} - \hat{V}}{\sigma\sqrt{2}}\right) - erf\left(\frac{V_i - \hat{V}}{\sigma\sqrt{2}}\right)\right], \end{aligned} \tag{4.13}$$

where, in (4.13) the $\mathrm{erf}(x)$ is the well-known *error function* and σ^2 denotes the noise variance. From (equation 4.13), we understand that the variance of input noise voltage drastically reduces the probability of correct estimation. In other words, the performance of the soft comparator depends on the noise level. We investigate the effect of noise on the performance of a single soft comparator. In a 3-bit soft comparator, two bits show the magnitude and one bit shows the polarity. Thus the calibration curve is divided by 3 different voltage points $V_1 = T$, $V_2 = 2T$ and $V_3 = 3T$, where T denotes interval length. For simulation, we applied a fixed input voltage V_{in} in interval $(0, T)$ under different noise levels. We increased the noise level from 0 up to 100 mV and calculated the probability based on observing $\hat{V}$, V_{in} is correctly detected. We repeated this simulation for different interval length $T \in \{20, 30, 40, 50\}$. Simulation results are presented in Fig. 4.30. As we can see larger intervals have better performance in comparison with smaller intervals. Furthermore, we calculated the probability that V_{in} is wrongly detected in other intervals. We repeated the simulations for two interval lengths $T = 20$ and $T = 40$. The results are presented in Fig. 4.31

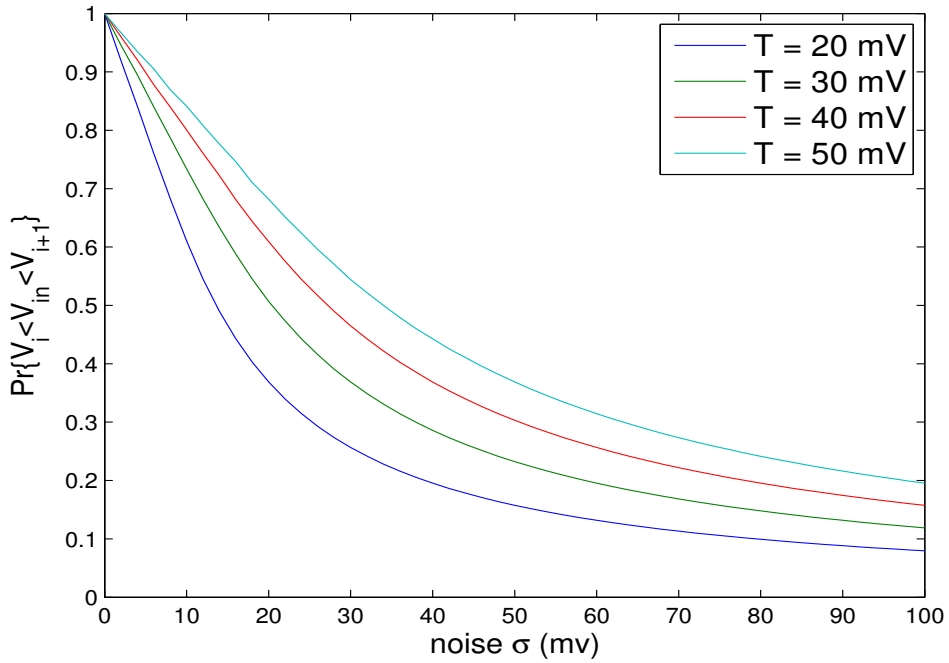


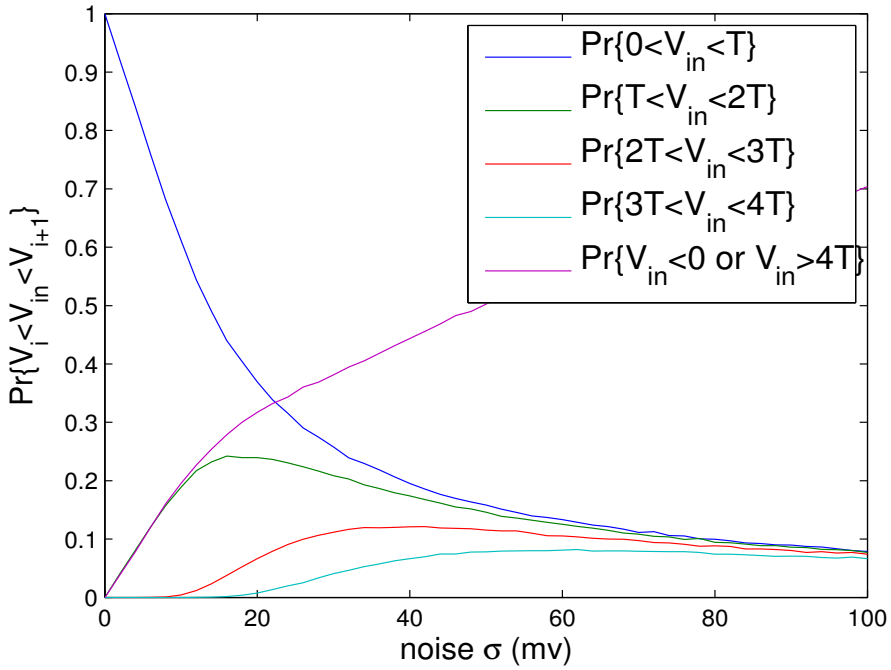
FIGURE 4.30: Probability of correct detection for different interval lengths.

4.5.2 *M Soft Comparators with same threshold*

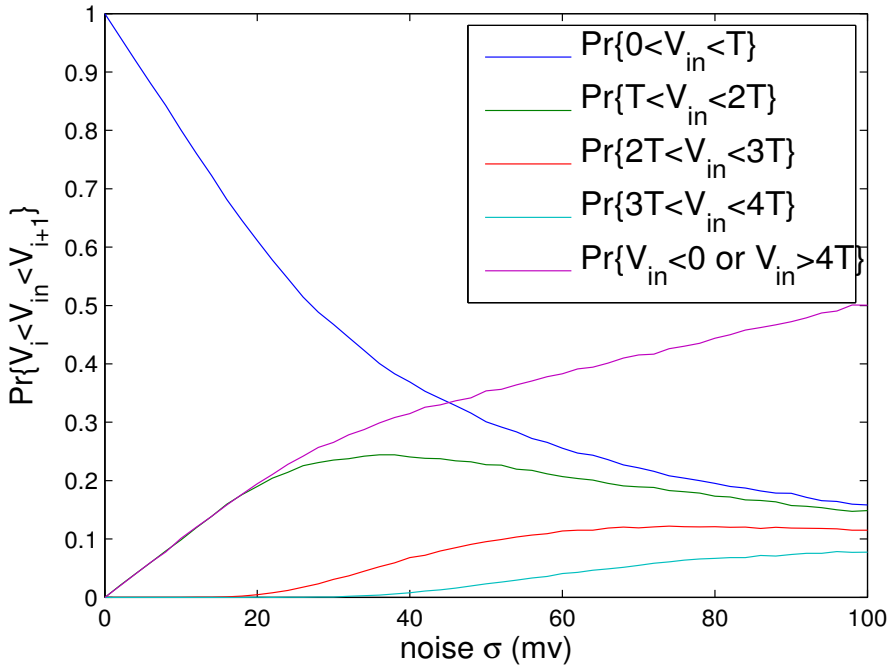
In the last section we saw the effect of noise on the output of a single soft comparator. In this section we analyze the effect of multiple observations on estimation of V_{in}, using M soft comparators. A simple test model is presented in Fig. 4.32. Assuming M independent noise voltages with mean zero and variance σ^2, we can reduce the error probability by increasing the number of observations. Let us denote M different estimations of V_{in} by $\hat{V}_j, j \in \{1, 2, \cdots M\}$. Then, by averaging on all observations, the value of V_{in} can be obtained with no error when $M \to \infty$.

First, we consider the case for two comparators $C1$ and $C2$. Using simulation results, we demonstrated that by increasing the number of observations better estimation for V_{in} can be obtained. When two samples, $\hat{V}_1 = V_{in} + n_1$ and $\hat{V}_2 = V_{in} + n_2$, are observed, the error probability can be reduced in comparison to the single observation. In this case the average observation can be written as

$$\hat{V} = \frac{\hat{V}_1 + \hat{V}_2}{2} = V_{in} + \frac{n_1 + n_2}{2}. \tag{4.14}$$



(A) Interval length $T = 20mV$.



(B) Interval length $T = 40mV$.

FIGURE 4.31: Probability of each interval when fixed V_{in} is applied in interval $[0, T]$

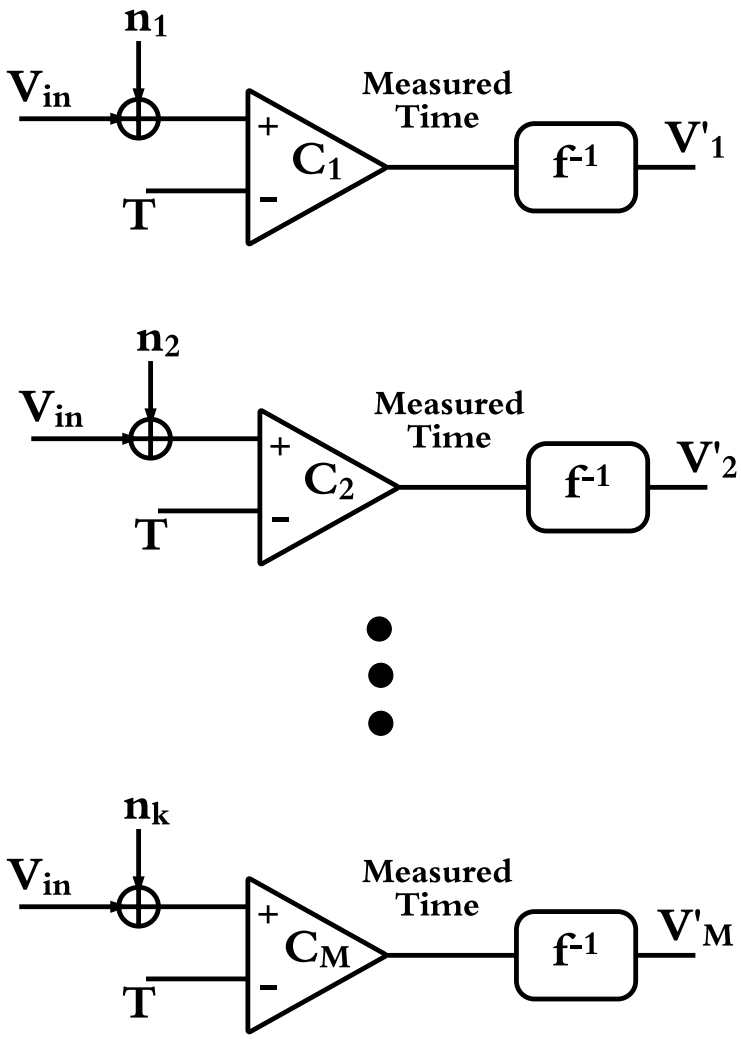


FIGURE 4.32: M Soft Comparators

To see any improvement compared to the single observation, the $\Pr\left\{\left|\frac{n_1+n_2}{2}\right| < |n_1|\right\}$ should be higher than 50 %. We can simplify this probability as

$$\begin{aligned}\Pr\left\{\left|\frac{n_1+n_2}{2}\right| < |n_1|\right\} &= \Pr\left\{-|n_1| < \frac{n_1+n_2}{2} < |n_1|\right\} \\ &= \Pr\left\{-2|n_1| - n_1 < n_2 < 2|n_1| - n_1\right\}\end{aligned}$$

As depicted in Fig. 4.33, assuming $n_1 > 0$, the observation gain can be obtained when $\Pr\left\{-3n_1 < n_2 < n_1\right\} > 0.5$.

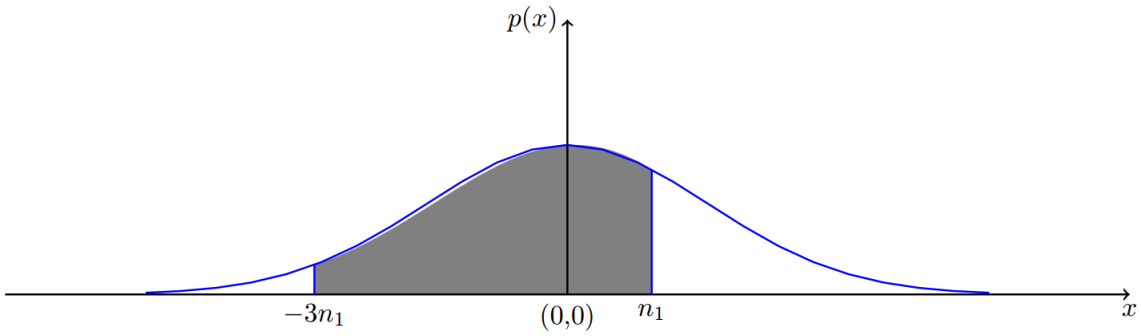


FIGURE 4.33: Two observations with normal distribution.

This probability can be written based on the well-known function erf(x)

$$\Pr\{-3n_1 < n_2 < n_1\} = \frac{1}{2}\left[erf\left(\frac{n_1}{\sigma\sqrt{2}}\right) + erf\left(\frac{3n_1}{\sigma\sqrt{2}}\right)\right] \geq 0.5 \tag{4.15}$$

Solving equation (4.15), we obtain a valid range $0 < n_1 < 0.360$, which can occur with probability equal to $\frac{1}{2}erf\left(\frac{0.360}{\sigma\sqrt{2}}\right) = 0.14$. Thus by increasing the number of observations from 1 to 2 we have 14 % more chance for better estimation.

Obviously, we can make better estimations by increasing the number of observations and averaging them. In order to do that, we repeated similar simulations for a group of M comparators with the same threshold. We assumed M different independent noise with variance σ^2 for each comparator. Fig. 4.32 depicts a simple test setup for M soft comparators with the same threshold voltage.

It's clear that, by scaling down a random variable by M, its variance is divided by M^2. However, by adding M independent normal random variables, the variance will be multiplied by M, so the overall variance will be divided by M [116]. Mathematically explained, we might consider a weighted sum of independent variables $x_i, i \in \{1, 2, \cdots M\}$ with normal distribution (μ_i, σ_i^2) and coefficient c_i

$$y = \sum_{i=1}^{M} c_i x_i. \tag{4.16}$$

Then, the variable y has a normal distribution with mean μ_y and variance σ_y^2 where :

$$\mu_y = \sum_{i=1}^{M} c_i \mu_i, \tag{4.17}$$

$$\sigma_y^2 = \sum_{i=1}^{M} c_i^2 \sigma_i^2. \tag{4.18}$$

For the test setup presented in Fig. 4.32, all noise distributions have equal variance and all the coefficients are the same and equal to $1/M$. Thus, the overall observation has a normal distribution with mean 0 and variance $\sigma_y^2 = \frac{\sigma^2}{M}$. Averaging multiple outputs is a straight forward way to find a more stable output. Two other useful ways also exist. The first way is based on majority rule. In this method, all of the outputs of comparators are counted and the more probable output is the output with the maximum counter index.

The second way and also the ideal one to find the most probable output is based on multiplication. The idea behind this method is based on variable node operation for non-binary LDPC codes [117]. We know that for $(m+1)$-bit soft comparators we have 2^m different intervals and each of these intervals represent one element in $\alpha \in GF(2^m)$. Again consider the test setup presented in Fig.4.32. Assume that $P_i, i \in \{1, 2, \cdots M\}$ is the probability vector of each comparator C_i. This probability vector has $q = 2^m$ elements related to the probability of each symbol in $GF(2^m)$, i.e,

$$P_i = [p_i(\alpha)], \quad \alpha \in GF(2^m). \tag{4.19}$$

Furthermore, let us denote by $P^* = [p^*(\alpha)], \quad \alpha \in GF(2^m)$, the final estimated probability vector which can be found as

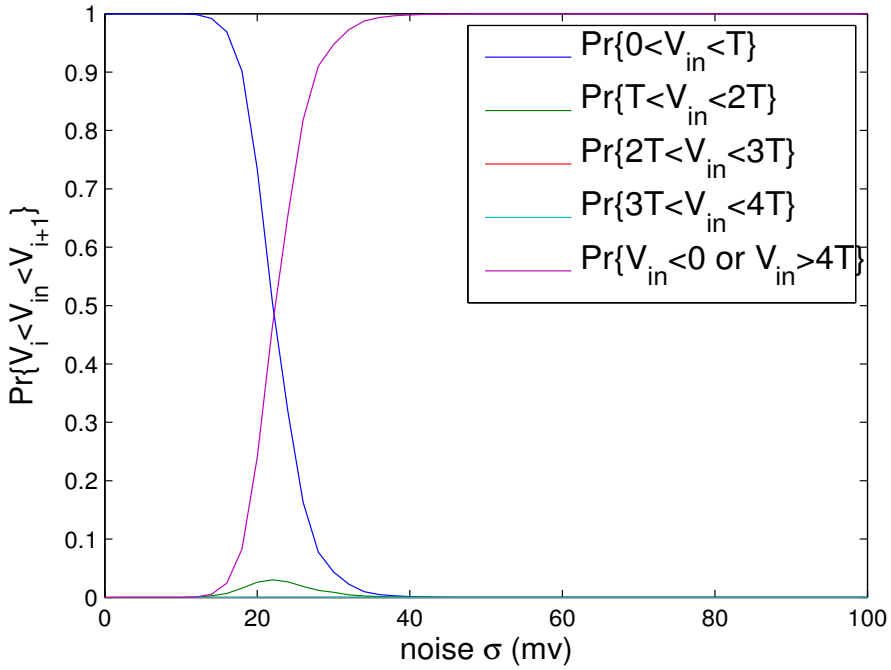
$$p^*(\alpha) = \mu \prod_{i=1}^{M} p_i(\alpha), \quad \alpha \in GF(2^m), \tag{4.20}$$

where parameter μ is a normalized factor in such a way that $\sum_{\alpha \in GF(2^m)} p^*(\alpha) = 1$. Finally, the estimation of applied input voltage is equal to the corresponding element

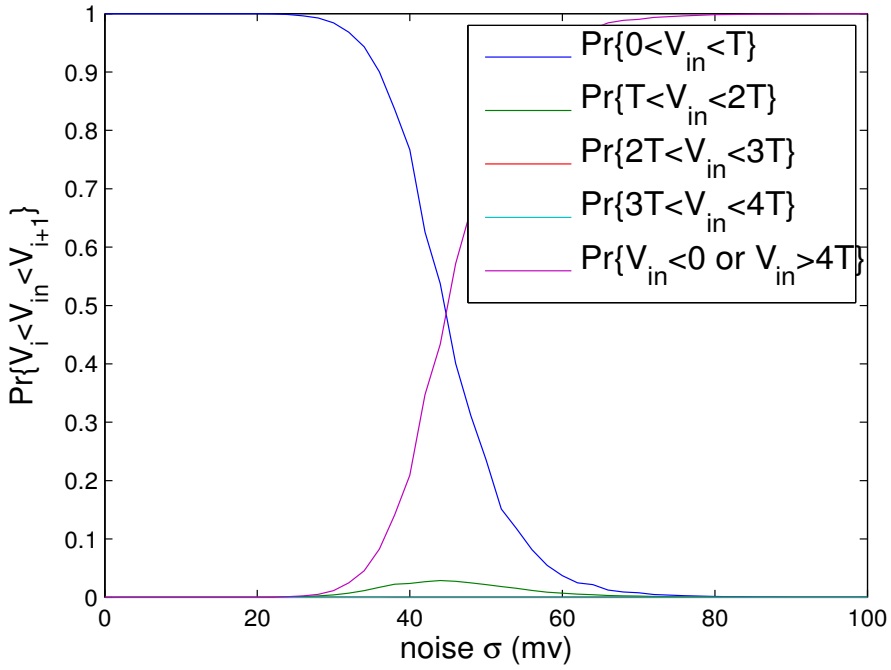
in P^* which has maximum probability value or

$$\hat{V} = \max[p^*(\alpha) \mid \alpha \in GF(2^m)]. \tag{4.21}$$

The simulation results for 8 observations for multiplication methods are presented in Fig. 4.34a and Fig. 4.34b, respectively for interval length $T = 20$ and $T = 40$.



(A) Interval length $T = 20mV$.



(B) Interval length $T = 40mV$.

FIGURE 4.34: Effect of multiple observations for multiplication method. A fixed V_{in} is applied in interval $[0, T]$

CHAPTER 5

Circuit Layout and Evaluation

For implementing this soft comparator, IBM 130nm CMOS technology was chosen. The total available area was limited by 4mm x 4mm. Out of this available area, 2mm x 2mm area was utilized for this chip, which was sufficient for this design purpose. The overall chip layout was designed step by step - from comparator to encoder.

5.1 CIRCUIT LAYOUT PLAN

The final chip layout contains four soft comparators, which are connected in an overlapping fashion to give it an ADC structure along with a separate dynamic comparator. The internal soft comparator sub-module layout configuration plan is shown in Fig. 5.1.

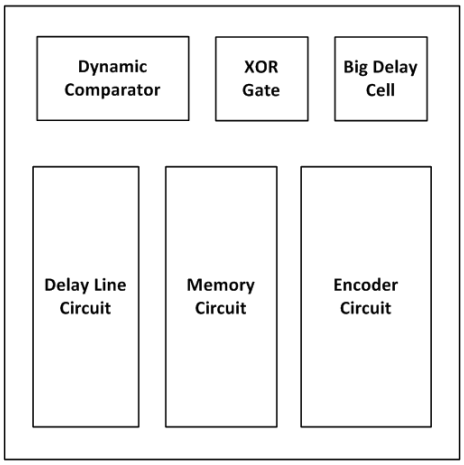


FIGURE 5.1: Soft Comparator Layout configuration plan

5.2 SOFT COMPARATOR LAYOUT

The soft comparator layout was constructed by attaching different sub-modules, like a comparator, a delay line circuit, a memory circuit, and an encoder circuit, according to the schematic design. For overall layout design, 7 layers of metals were used.

5.2.1 *Dynamic Comparator*

Fig. 5.2 shows the layout of the Dynamic Latched Comparator. The design rule checking (DRC) was ran every time to make sure there was no error.

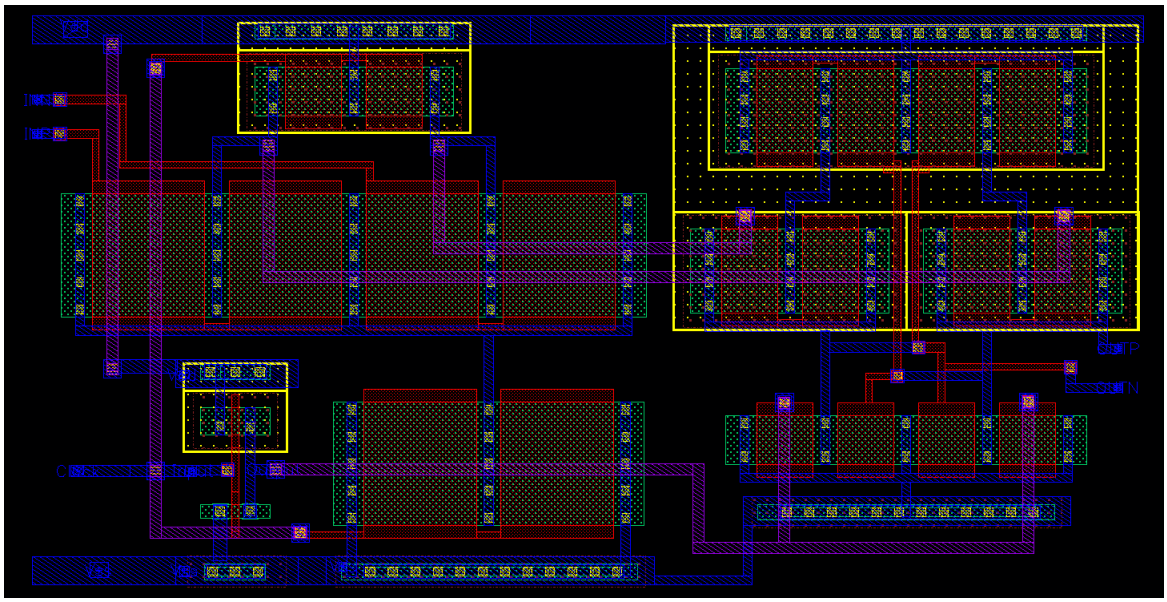


FIGURE 5.2: Dynamic Comparator Layout

5.2.2 *XOR Gate and Buffer Circuit*

According to the schematic design, after the comparator cell, there is one XOR gate and a Buffer circuit. Here, the XOR gate is designed by connecting four 2 input NAND gates (Fig. 5.3). There was not any other specific design challenges except keeping the DRC clean. After the XOR gate, there is a Buffer circuit.

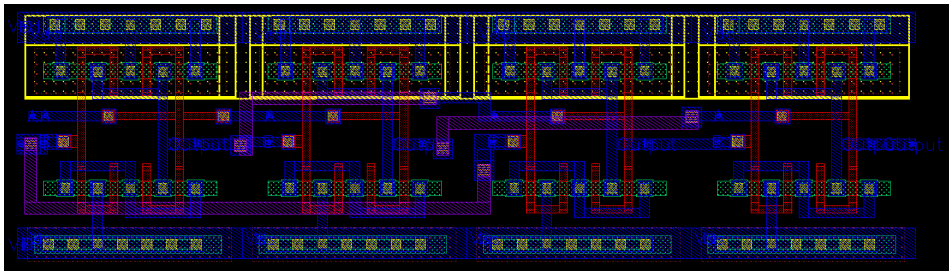


FIGURE 5.3: XOR Gate Layout

This Buffer circuit is simply designed by connecting two NOT gates in a series (Fig. 5.4).

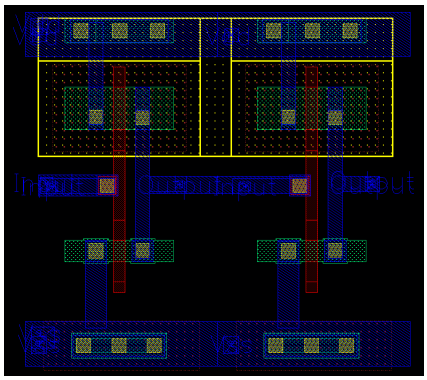


FIGURE 5.4: Buffer Circuit Layout

5.2.3 *Big Delay Cell and Delay Line Circuit*

Immediately after the Buffer circuit, one Big Delay Cell is introduced in a series. The Big Delay Cell is comprised of a Big Tristate NOT gate, one NOT gate, and one Buffer circuit connected serially (Fig. 5.5). The Big Tristate NOT gate occupied a lot of space in the layout platform and there was not any other specific design challenges except following the design rules.

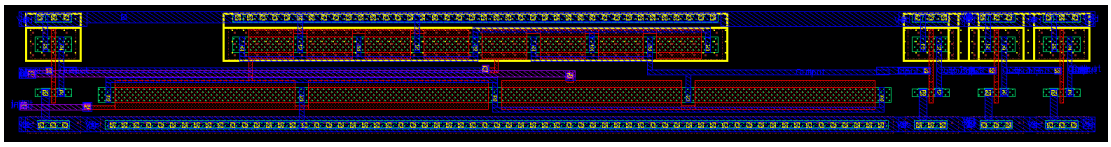


FIGURE 5.5: Big Delay Cell Layout

Followed by the Big Delay Cell, a Delay Line Circuit is introduced. A Delay Line Circuit is designed by connecting 32 Delay Cells in a series, where their *Enable* signal nodes are tied together (Fig. 5.6).

The first Delay Cell's output works as the input of next Delay Cell, which is connected in a series and in this way the rest of the Delay Cells are connected. At the end of the Delay Cell Line, one dummy n-type MOSFET, whose source and drain are tied together, is connected. This MOSFET works as a dummy load. Designing this Delay

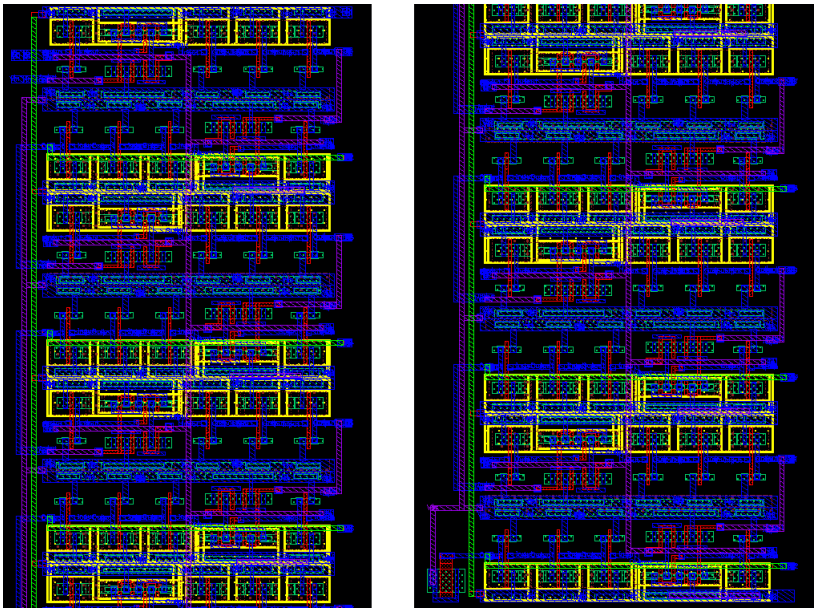


FIGURE 5.6: Delay Line Circuit (Top and Bottom portions are shown)

Line Circuit asked for more metal layers as only metal 1 could not provide all the wiring requirement without touching each other. Thus metal 2 and metal 3 layers are introduced here to make efficient wiring connection.

5.2.4 *Memory Circuit*

The memory circuit consists of 32 D-Latches. Each of these D-Latches is designed by connecting two Transmission gates, two NOT gates, and one two-input NAND gate (Fig. 5.7).

The Memory Circuit has 32 D-Latches connected in parallel, with their clock signals

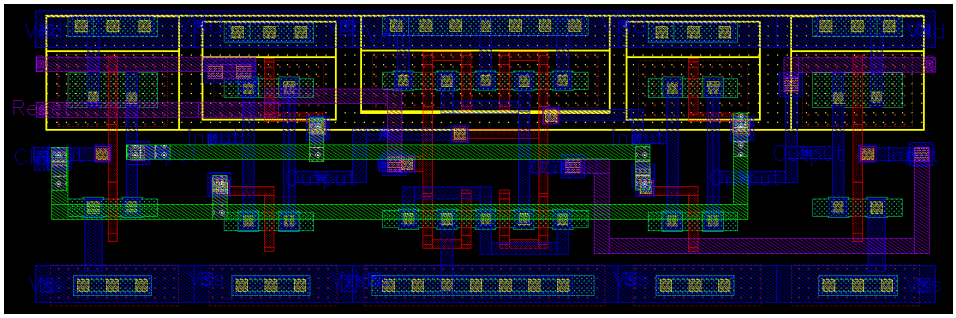


FIGURE 5.7: D-Latch Circuit Layout

tied together which comes through a Big Inverter (Fig. 5.8).

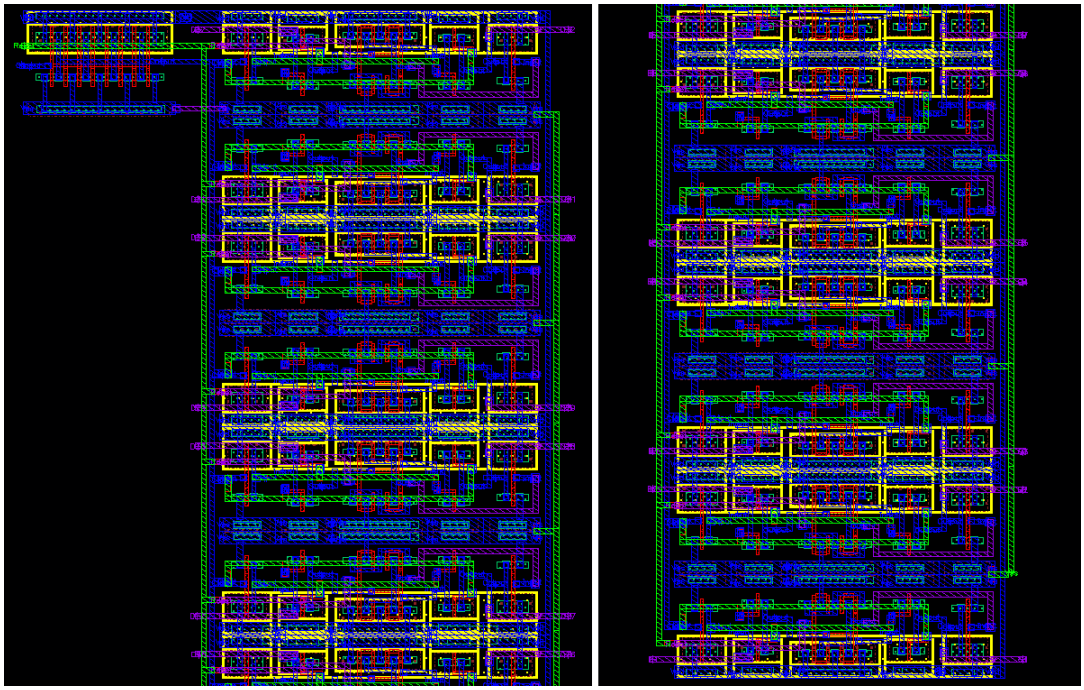


FIGURE 5.8: Memory Circuit Layout (Top and Bottom portions are shown)

5.2.5 *Encoder Circuit*

Layout designing for the 32-to-5 Encoder Circuit was the most challenging task. It consists of five 16-bit OR gates, 32 XOR gates, and an n-type MOSFET added in a diode-connected fashion. (Fig. 5.9). Out of 32 XOR gates, 31 XOR gates' output were connected to 5 16-bit OR gate in different combinations, which asked for intelligent wiring connections. This Encoder layout also took the most amount of layout spaces.

Each of the five 16-bit OR gates is designed by connecting four 4-bit NOR gates and one 4-bit NAND gate. All four outputs from the four 4-bit NOR gates act as the four inputs of the 4-bit NAND gate (Fig. 5.9).

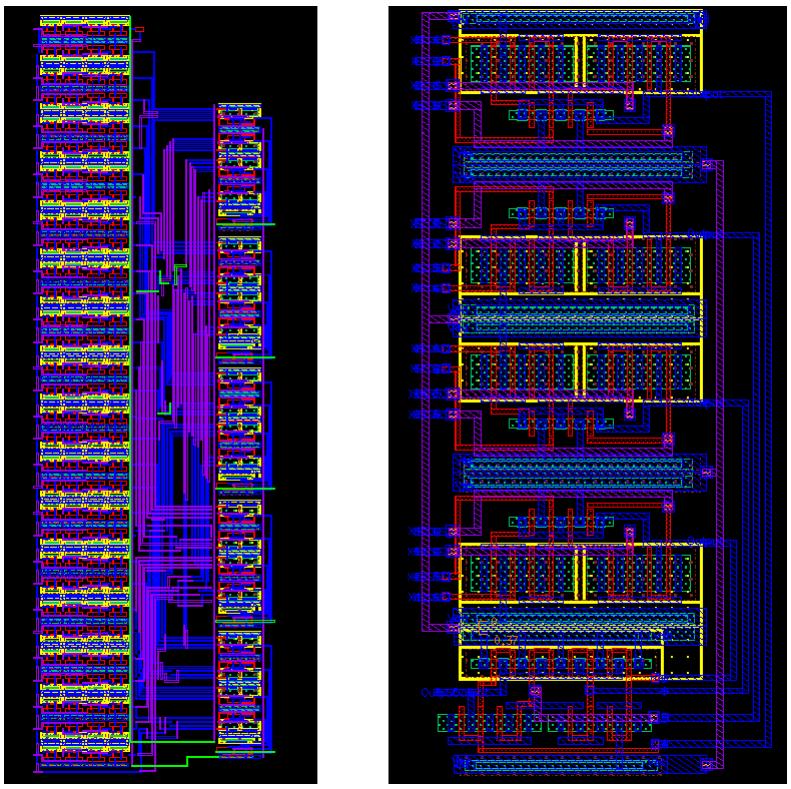


FIGURE 5.9: 32-to-5 Encoder Layout and 16-bit OR Gate Layout

5.2.6 *Soft Comparator*

All the sub-modules layouts are connected according to the schematic design to build the soft comparator layout. The comparator, XOR gate, and the Big Delay Cell are put on the top side. The Delay Line Circuit, Memory Circuit, or the 32 D-Latches in parallel, and the 32-to-5 Encoder Circuit are located at the bottom of the soft comparator layout (Fig. 5.10). All the internal wiring followed the schematic wiring. DRC checking and Layout Versus Schematic (LVS) checking were pretty challenging, but were found to be error free.

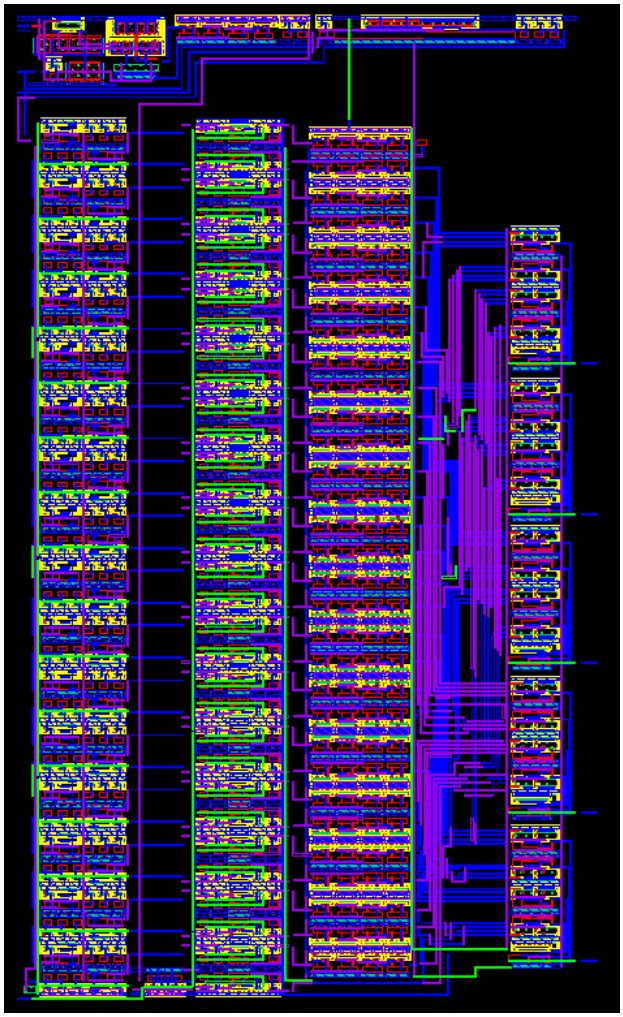


FIGURE 5.10: Soft Comparator Layout

5.3 METAL FILLING AND CAPACITORS

Soft Comparator layout is copied four times and put at the center of the layout window along with a Dynamic Comparator layout. These are then connected in a fashion so that testing can be done easily. All the wirings are done using metal layers from metal 1 to metal 6. As the total chip area is 2mm by 2mm and even after placing four Soft Comparators and one Dynamic Comparator, there were still large amount of blank spaces available. In order to keep the metal density uniformly throughout the chip, metal filling was required. For metal filling, different sizes of rectangular metal shapes were placed throughout the blank areas and connected to the ground (Fig. 5.11).

For electro static discharge (ESD) protection, twenty dual metal-insulator-metal

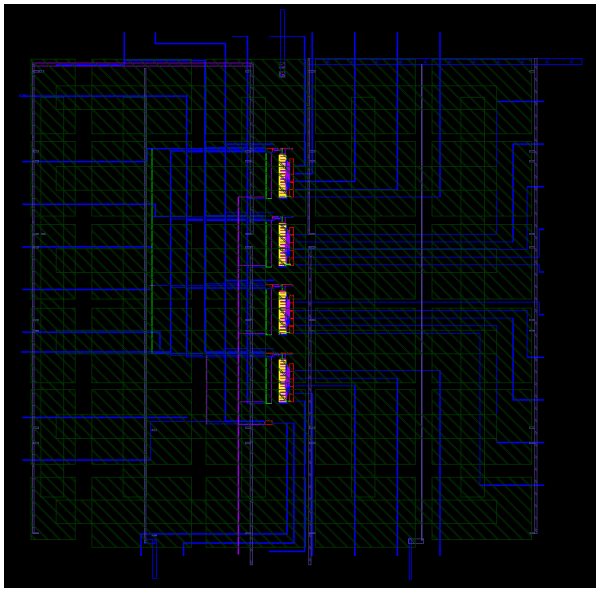


FIGURE 5.11: Metal filling in the chip area

capacitors (dualmimcap) were used (Fig. 5.12). They also worked as Vdd, Vcc, and GND bypass capacitors.

TABLE 5.1: Dualmimcap Capacitor values

Capacitor	**Values**	**No of Capacitor**
C1	255.1129p F	6
C2	279.8893p F	3
C3	341.8302p F	3
C4	317.0538p F	3
C5	238.2299p F	2
C6	261.3662p F	1
C7	319.2071p F	1
C8	296.0708p F	1

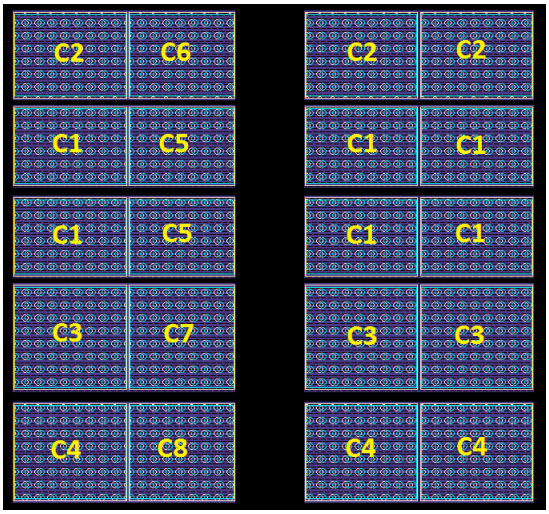


FIGURE 5.12: Dualmimcap Capacitors used in final chip layout

5.4 PAD FRAME CREATION

Pad frame is the interface between the main circuit and the outer world. Physical pads are the points where bond wiring is done during the chip packaging process. Each of the pads has its own output power and ground rail.

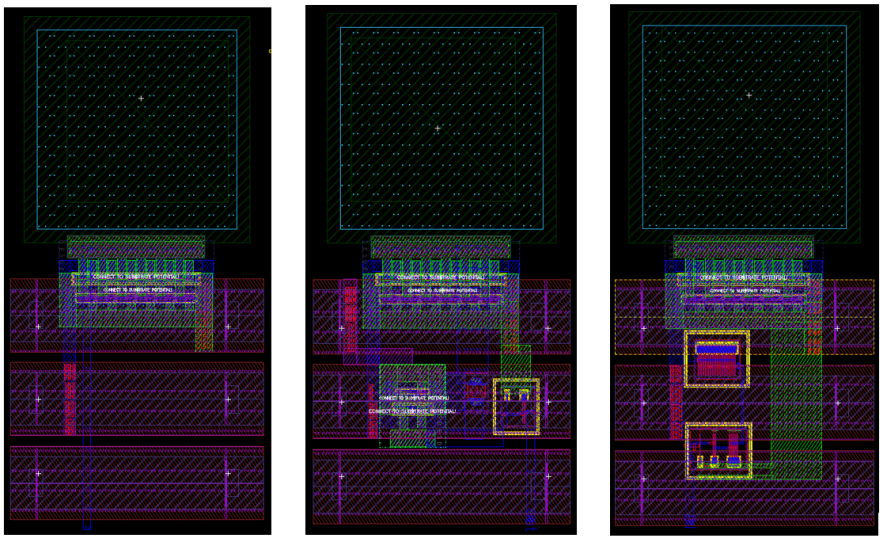


FIGURE 5.13: Analog Pad, Digital Input Pad, and Digital Output Pad

They also have a ESD protection circuit. For this Soft Comparator and the Dynamic Comparator circuit connections, digital input and output pads, analog pads, Vdd pads, Vcc pads, and GND pads were used. After connecting all the pads together, it creates the pad frame.

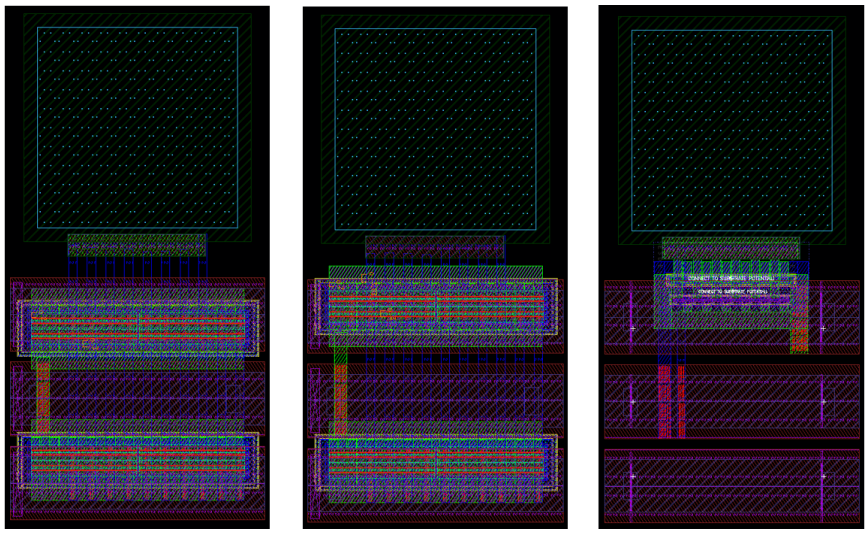


FIGURE 5.14: Vdd Pad, Vcc Pad, and GND Pad

The Analog pad, Digital input pad, and Digital output pad are shown in Fig. 5.13. The Analog pad doesn't need any receiving or level shifting circuitry. It only contains ESD protection circuitry. This is used both as an analog input and output pad. Digital pads have similar shapes, but different internal components. The power supply pads - Vdd and Vcc look similar, but the ground pad GND looks different than the power supply pads (Fig. 5.14).

Before the pad frame was created, a pin configuration was planned. There are 36 pins in this chip circuitry. Thus 36 pads were needed for wire bonding. The final pin configuration corresponds to the pin output numbers (Fig. 5.15).

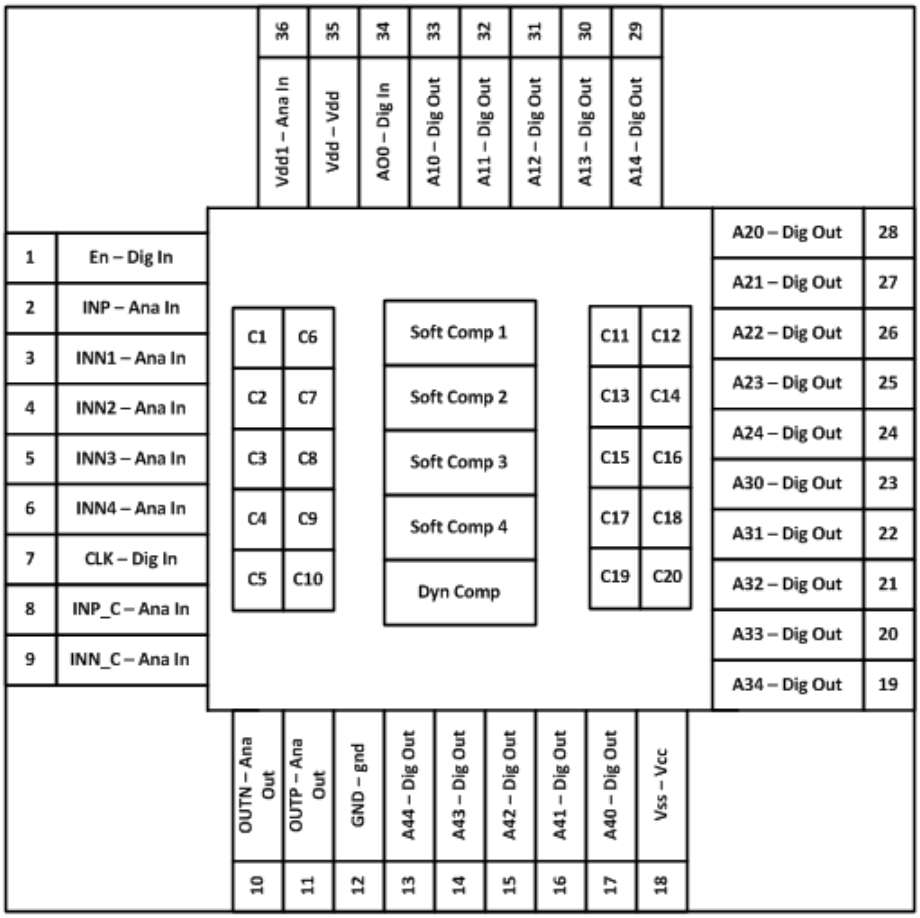


FIGURE 5.15: Pad Frame Pin Configuration

5.5 FINAL CHIP LAYOUT

After filling the blank spaces with metal, adding the capacitors, creating the pads and pad frame and connecting them with the internal circuitry, final chip layout was almost done. One image bevel was used around the final chip layout which showed the physical border of the chip. It was also situated within the chip layout area, which is 2mm by 2mm. The final chip layout is shown in Fig. 5.16.

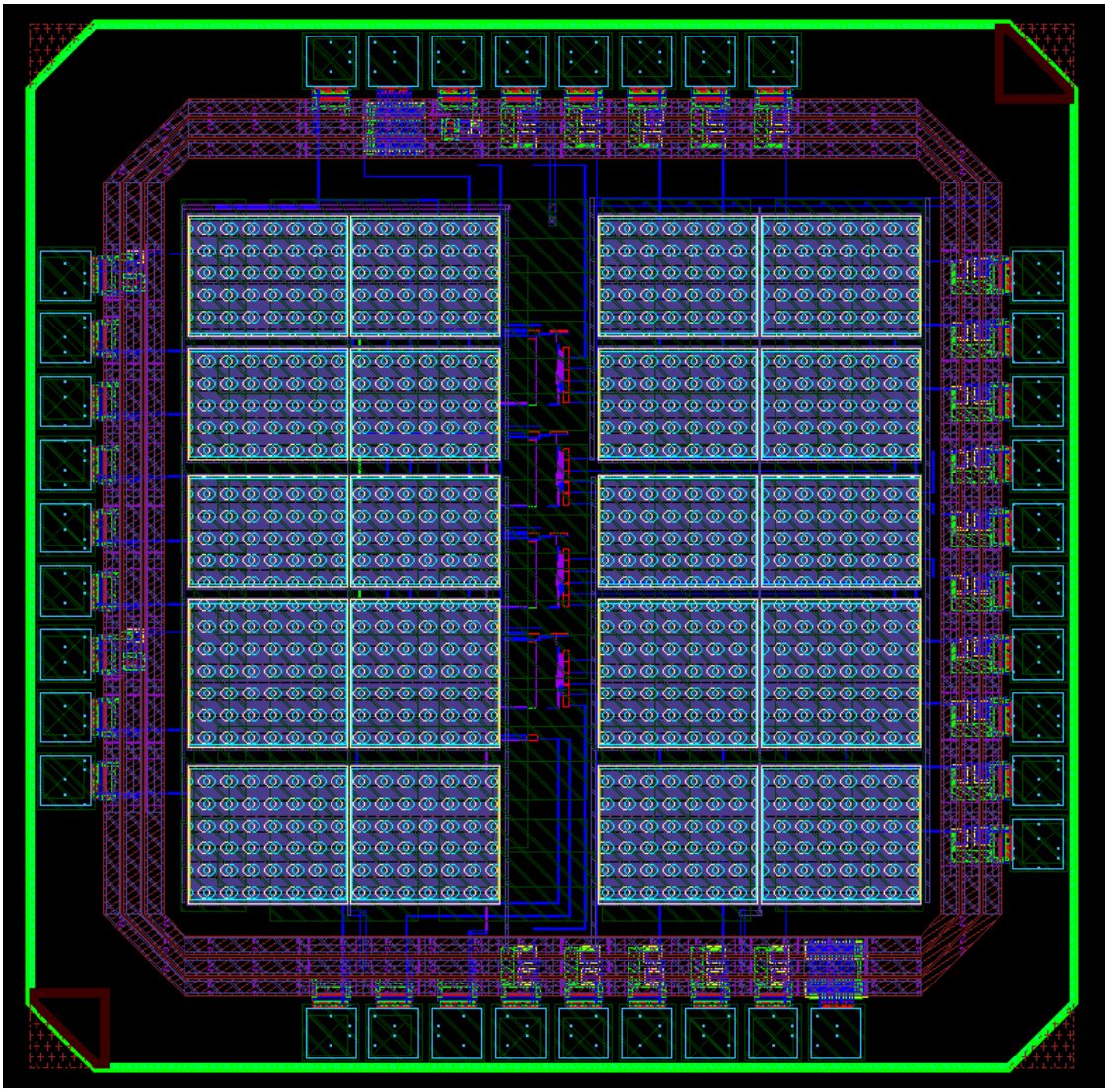


Figure 5.16: Final Chip Layout

5.6 CHIP EVALUATION

The overlapping Soft Comparator chip is designed with IBM 130nm CMOS technology. It was designed in room temperature, which is 27°C. It uses the supply voltage of 800mV for the Dynamic Comparator (which is tunable). The rest of the circuit supply voltage is 1.2V. Clock frequency is 25 MHz and the output is a 6-bit digital data (5-bit for magnitude and 1-bit for sign). The chip is simulated over temperature range from 0°C to 80°C. Corner Simulation is also done to test the chip performances in the worst cases.

In this design, the dynamic latched comparator uses 800mV supply voltage (V_{dd1}), which is tunable. This supply voltage (V_{dd1}) can be used for adjusting the accuracy in a calibration mode. Also, in the overall chip design, one single dynamic comparator is put together with 4 Soft Comparators. The positive output of that comparator (OUTP) can indicate whether the input is bigger or smaller than the reference signal. This is referred as *Sign Bit*. Thus the *Sign Bit* can verify the general functionality of the Soft Comparator.

5.6.1 *Performance test with Temperature variation*

The design has been simulated for a wide range of temperatures, starting from 0°C to 80°C with every 5°C difference. For INN = 600mV, INP = 625.6mV, the simulation ran for 12ns. Here, at a temperature of 27°C, for inputs INN = 600mV and INP = 625.6mV, the Soft Comparator Sign Bit produces '1' and the 5-bit binary output stream is '01000'. The decimal equivalent of that value is '8'.

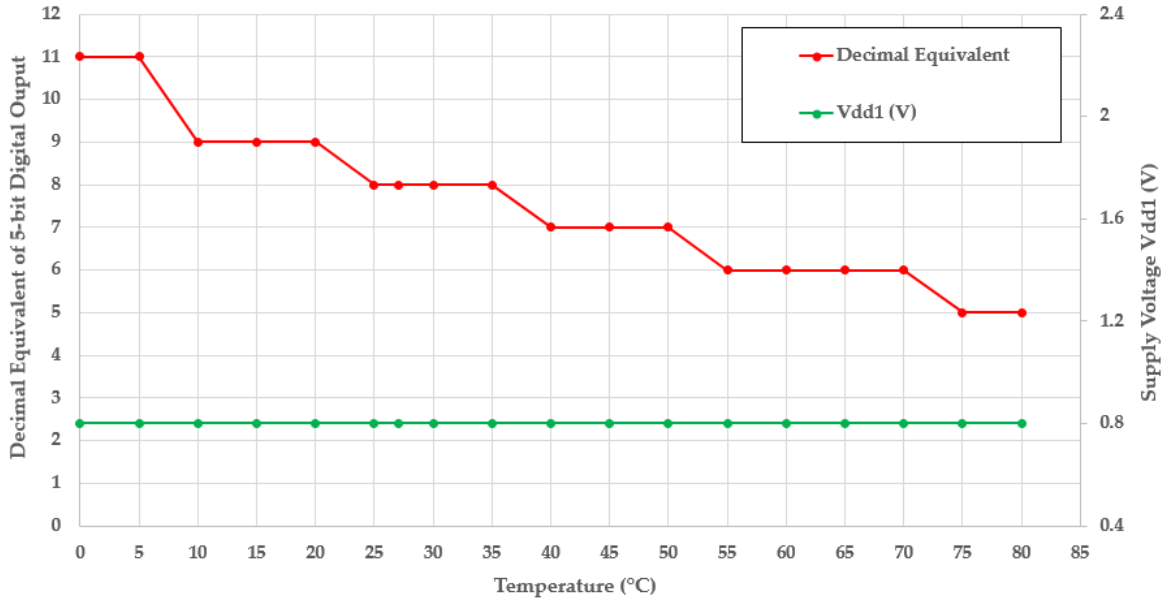


FIGURE 5.17: Decimal Equivalent of Digital Output change with Temperature

But with temperature higher than the room temperature, the binary values start to decrease. On the other hand, for temperatures lower than the room temperature, the output binary values start to increase. Which means delaying in the delay cells

decreases as temperature increases. The LSB value changes with temperature very rapidly, but the MSB value keeps it value almost constant over all temperature ranges. In the temperature ranges from 10°C to 50°C, the Soft Comparator binary value changes only '1' LSB bit.

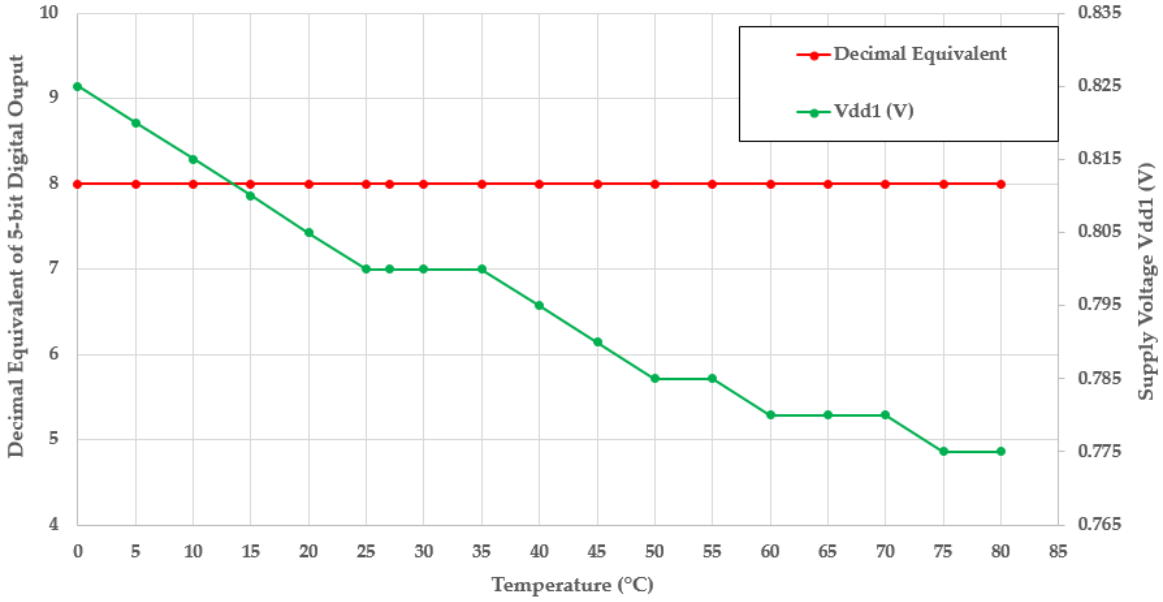


FIGURE 5.18: Decimal Equivalent of Digital Output after V_{dd1} Calibration

By calibrating V_{dd1}, we can tune the digital output, so that for all the temperature from 0°C to 80°C, the output remain the same (Fig. 5.18).

5.6.2 *Corner Simulation*

The Soft Comparator chip is designed for *typical* behavior of both n-type and p-type MOSFETs, which is nom-nom (tt) option, supply Vdd of 1.2V and for room temperature of 27°C. The 'Corners' can be defined in various ways. The one used for this Soft Comparator, is shown in Table 5.3

The Soft Comparator is simulated to test the Corners. The simulation model is changed from 'tt' to 'ss', 'fs', 'sf' and, finally to 'ff'. For model, 'tt', p-type MOSFETs act as 'nom' and n-type MOSFETs also act as 'nom'. Under the conditions: temperature = 27°C, V_{dd} = 1.2V, INN = 600mV, and INP = 625.6mV, the Soft Comparator binary output bit stream was '01000' for this model.

TABLE 5.2: Corner Definition used in Corner Simulation

Corners (x) & Variables (y)	**slowslow (ss)**	**fastslow (fs)**	**typtyp (tt)**	**slowfast (sf)**	**fastfast (ff)**
PMOS	slow	fast	nom	slow	fast
NMOS	slow	slow	nom	fast	fast

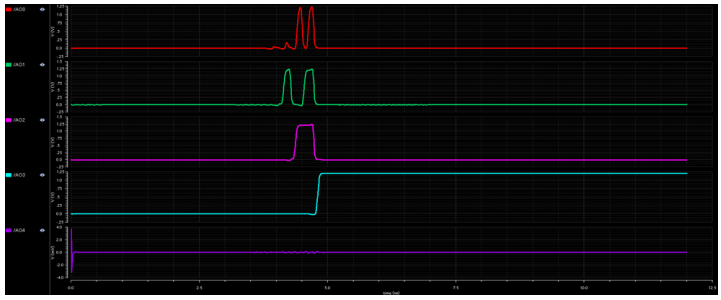


FIGURE 5.19: Soft Comparator Output for typtyp (tt) Corners

For model, 'fs', p-type MOSFETs act as 'fast' and n-type MOSFETs act as 'slow'. Inputs were same: INN = 600mV and INP = 625.6mV. The Soft Comparator binary output bit stream for this model was '11111', which is way far from the original output '01000'.

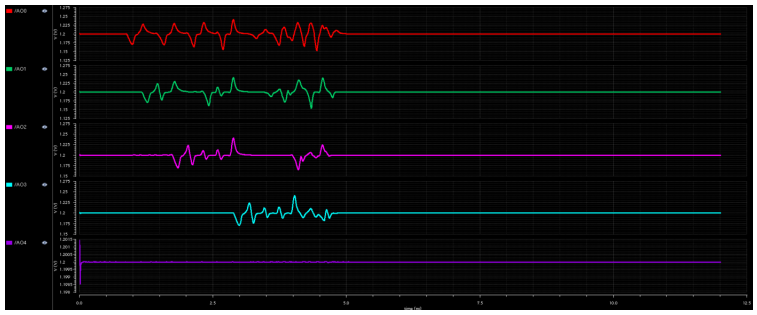


FIGURE 5.20: Soft Comparator Output for fastslow (fs) Corners

For model, 'sf', p-type MOSFETs act as 'slow' and n-type MOSFETs act as 'fast'. Inputs were same: INN = 600mV and INP = 625.6mV. The Soft Comparator binary output bit stream for this model was '01001', which is only '1' LSB greater than the original output '01000'.

For model, 'ss', p-type MOSFETs act as 'slow' and n-type MOSFETs also act as 'slow'. Inputs were same: INN = 600mV and INP = 625.6mV. The Soft Comparator

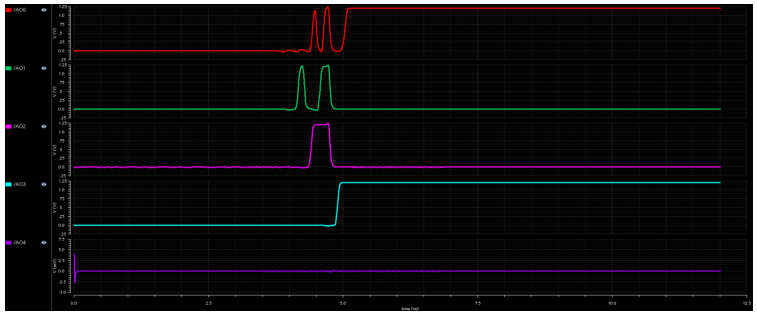


FIGURE 5.21: Soft Comparator Output for slowfast (sf) Corners

binary output bit stream for this model was '00111', which is only '3' bits smaller than the original output '01011'.

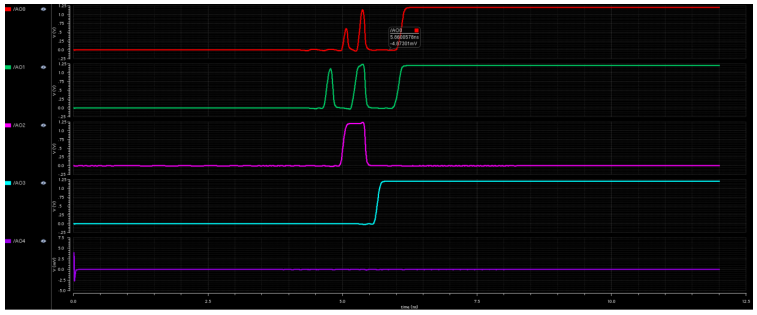


FIGURE 5.22: Soft Comparator Output for slowslow (ss) Corners

For model, 'ff', p-type MOSFETs act as 'fast' and n-type MOSFETs also act as 'fast'. Inputs were same: INN = 600mV and INP = 625.6mV. The Soft Comparator binary output bit stream for this model was '11111', which is way far from the original output '01000'.

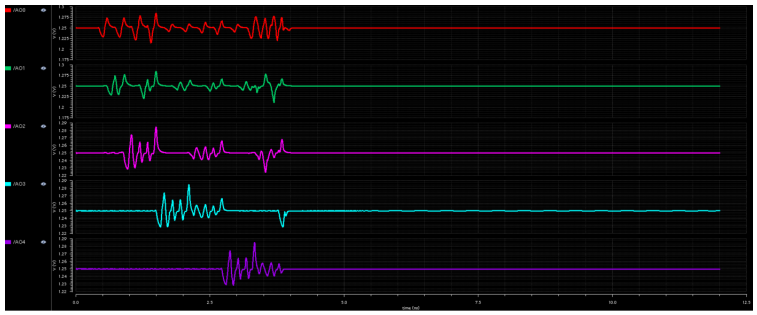


FIGURE 5.23: Soft Comparator Output for fastfast (ff) Corners

Thus, it's been observed that the Soft Comparator performs fairly well in models 'tt' and 'sf'. It starts to change its value significantly in the 'ss' model. But the Soft Comparator could not perform close the 'tt' model, when it worked under the 'fs' and 'ff' models. Thus, the chip needs calibration and V_{dd1} can be used to calibrate the chip

TABLE 5.3: Corner Simulation Summary (without calibration)

Corners	V_{dd1} **(V)**	**5-bit Digital Output**	**Decimal Equivalent**
typtyp (tt)	0.8	01000	8
fastslow (fs)	0.8	11111	31
slowfast (sf)	0.8	01001	9
slowslow (ss)	0.8	01011	11
fastfast (ff)	0.8	11111	31

to work in the 'fs', 'ss', and 'ff' models. Adding to that, signal processing modules can also be used in calibration. After the calibration, the performances of model 'ss' and 'sf' have been improved and matched the outcome with 'tt' model.

TABLE 5.4: Corner Simulation Summary (after calibration)

Corners	V_{dd1} **(V)**	**5-bit Digital Output**	**Decimal Equivalent**
typtyp (tt)	0.8	01000	8
fastslow (fs)	-	11111	31
slowfast (sf)	0.81	01000	8
slowslow (ss)	0.825	01000	8
fastfast (ff)	-	11111	31

5.6.3 *Offset Calculation: Monte Carlo Simulation*

In order to calculate the input referred offset voltage of the Soft Comparator, Monte Carlo Simulation was needed. A large number of sample points and a longer simulation time can give more accurate offset measurement. In this case, only 30 sample points were used and 2.4μs was used as the simulation time. The sampling method was chosen as *Random*. *Process* and *Mismatch* methods were taken into consideration. A common mode voltage of 600mV was used at both the inputs: INN and INP.
A slowly rising *Ramp* voltage was applied at the INP input on top of the common

mode voltage of 600mV. The output of the Monte Carlo Simulation was observed and the longest transition time was located where the OUTP signal went through transition. It was found at the 29^{th} sample point and at 960ns. The offset was calculated by multiplying the longest transition time with the slope of the *Ramp* signal.

$$Offset = (\frac{40mV}{2.4\mu s}) * 960ns = 16mV \tag{5.1}$$

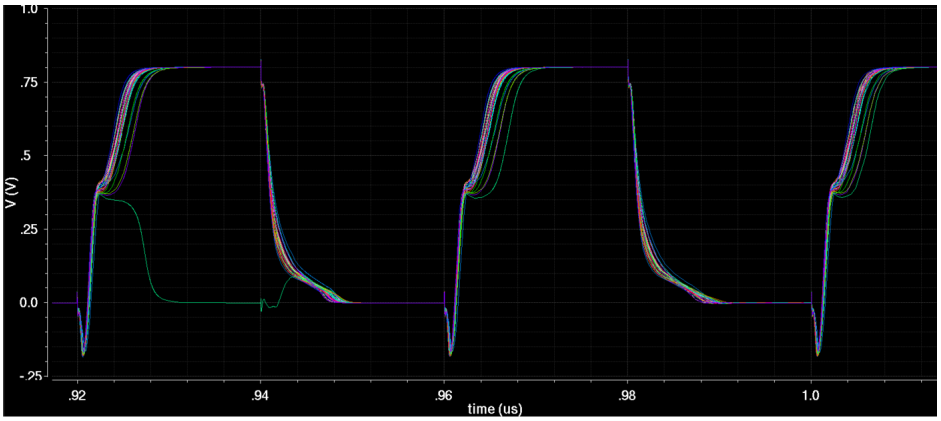


FIGURE 5.24: Monte Carlo Simulation Output of the Soft Comparator

Fig. 5.24 is showing the Monte Carlo Simulation output of the Soft Comparator (time frame between 920ns and 1.2μs are shown).The output is for 30 sample points and a simulation time of 2.4μs. Fig. 5.25 is showing the longest transition incidents

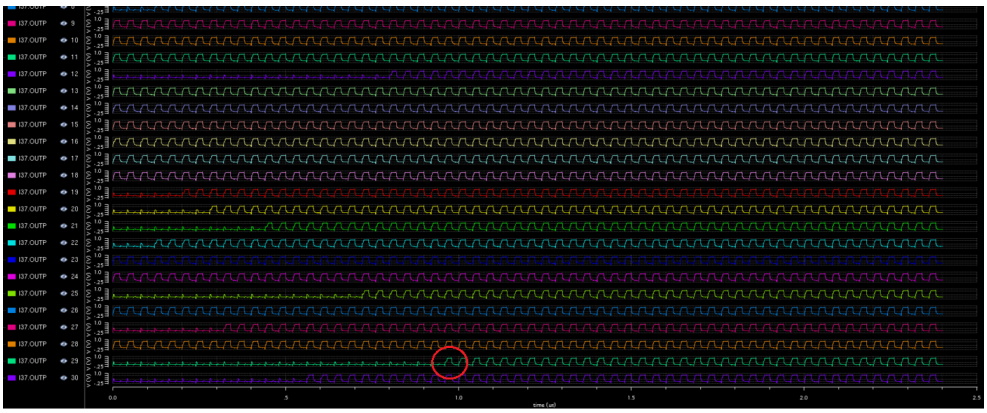


FIGURE 5.25: Longest Transition at the 29^{th} sample point in the simulation

in the Monte Carlo Simulation. The longest transition happened at the 29^{th} sample point and it happened at 960ns.

TABLE 5.5: Monte Carlo Simulation Summary

Method	Process and Mismatch
Sampling Method	Random
Number of Points	30
Ramp Voltage	40mV
Simulation Time	2.4μs
Transition Sample	29^{th}
Transition Time	920ns
Offset	16mV

5.6.4 *Performance Summary*

The performance of the Soft Comparator chip is summarized in Table 5.5.

TABLE 5.6: Performance Summary of the Soft Comparator

Architecture	Soft Comparator
Technology	IBM 130nm CMOS
Resolution	6-bit (1 Sign Bit and 5-bit Digital Output)
Frequency	25 MHz
Supply V_{dd}	1.2V
Supply V_{dd1}	800mV (Tunable)
Power	26μ W

CHAPTER 6

Conclusion

Flash ADC, which is the fastest ADC around, cannot have high resolution due to power issue, meta-stability, lack of high number of accurate comparators, noise, and offset issues. Designing and fabricating a large number of similar and precise a comparator is very challenging. In this work, a different approach of designing a comparator is proposed where the comparator settling time is utilized to extract multiple bits of digital output instead of only one. This is referred to as a Soft Comparator. While output bits have different reliabilities, using a number of Soft Comparators together, it is possible to achieve high accuracy. Noise analysis of the Soft Comparator is done which showed that using multiple overlapping Soft Comparators, correct input detection is possible which is the pre-condition of getting reliable multiple bits output. As high resolution Flash ADCs need large number of precise traditional comparators, using the proposed Soft Comparator design, it is possible to design high resolution Flash ADCs with much fewer comparators. This reduces the power consumption drastically, alleviates meta-stability and offset error issues. Also, it can speed up the overall data conversion process.

6.1 FUTURE WORK

The fundamental concept behind a Soft Comparator is to utilize the dynamic comparator settling time to extract multiple bits of digital output instead of only one. This work used 32 small Delay Cells connected in series, each of which was capable of delaying the input signal by around 0.1ns. This Delay Cell was designed with one Tristate NOT gate, one NOT gate, and one Buffer circuit. These 32 Delay Cells together was named a 'Delay Line Circuit'. Thus, in this process, the Delay Line Circuit was comprised of 96 logic gates, which increases the overall power consumption.
In a future work, instead of these 32 individual delay cells, different lengths of metal wire can be used to create different delay times. For example, one short wire can

be connected at the output of Big Delay Cell, which will introduce a small amount of delay, a little longer wire can be connected at the output of the Big Delay Cell to get a little more amount of delay. This way, different lengths of wire are capable of delaying the same signal by different amounts of time. Thus, without 96 logic gates, power consumption could be much smaller and the overall process will be faster.
Another approach is to use a long wire and connect it to the Big Delay Cell's output. Then tapping it at different distances of the wire can give different amounts of delay. In this case, the process will be even faster, which is suitable for ultra-high speed data converter applications. Both of these alternating design approaches can be performed easily by removing the delay line circuit and replacing it with wiring delay systems.
As the measured settling time with input voltage difference is non-linear, one Decision Making Module (DMM) can be designed. Using Digital Signal Processing techniques inside the DMM, multiple bits reliable output can be generated.
In a future digitally assisted soft comparator design, the delay in the comparator can be modified by controlling its supply voltage V_{dd1} in a feedback loop to improve the accuracy of the comparator under different scenarios.

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