Capacitor Bank Unbalance Protection Enhancements

A Dissertation

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by

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Authorization to Submit Dissertation

This dissertation of Satish Samineni, submitted for the degree of Doctor of Philosophy with a major in Electrical Engineering and titled "Capacitor Bank Unbalance Protection Enhancements," has been reviewed in final form. Permission, as indicated by the signatures and dates given below, is now granted to submit final copies to the College of Graduate Studies for approval.

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Abstract

Shunt capacitor banks (SCBs) are critical power system assets that play a crucial part in providing reactive power support, improving voltage profile, increasing system capacity, and reducing system losses. SCBs are widely installed in the system as they are relatively inexpensive compared with transmission or generation system upgrades. SCBs consists of a number of single phase capacitor units connected in series and parallel to meet the desired voltage and VAr ratings.

Continuous overvoltage stress results in capacitor unit failures. If faulty units are not detected and replaced quickly they can cause additional overvoltage stress on the remaining healthy units eventually resulting in a cascading failure. Unbalance protection provides the primary protection against unit failures in capacitor banks by detecting unbalances within the bank. Unbalance protection asserts an alarm if the unbalance magnitude is small, but trips the bank if the unbalance is high enough to potentially cause a cascading failure. Using the unbalance phase angle provides an economical way to quickly locate the faulty units and minimize bank outage time.

All unbalance protection schemes have an inherent problem detecting canceling or balanced failures; i.e., units or elements fail in multiple phases or sections in the bank that cancel or reduce the net unbalance. If the canceling failure is symmetric, then the measured unbalance will be zero. If the canceling failure is asymmetric, then the measured degree of unbalance will be decreased compared to failures in one section of the bank. Both symmetric and asymmetric canceling failures results in reduced sensitivity of unbalance protection and affects the reliability of capacitor bank protection.

This thesis proposes an algorithm that can detect the symmetric and asymmetric canceling failures, thereby improving the reliability of the capacitor bank unbalance protection. The research investigates using a combination of the change of unbalance magnitude and unbalance angle before and after a disturbance in SCBs as a canceling failure detection approach. The proposed algorithm is tested and validated using time domain computer simulation with an electromagnetic transients program. The proposed

algorithm is economical and practical as it uses unbalance magnitude and phase angle which are available as part of unbalance protection.

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Dedication

To my wife, Haritha for her unconditional love and relentless support, and my son, Akshaj for his love, and encouragement.

To my parents, Bhaskar Rao and Rama Devi for their endless love and sacrifice in my upbringing.

To my brother, Mahesh for inspiration and sacrifice, and my sister, Madhu for support.

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Definitions

Shunt Capacitor Bank (SCB) – Series, parallel, or series and parallel configured capacitor elements making up capacitor units that in turn are connected in series, parallel or series, and parallel to make a capacitor bank and all supporting accessories.

Capacitor Element – Two electrode plates separated by a dielectric.

Capacitor Unit – A collection of capacitor elements in a case with terminals to be connected to the power circuit.

MVA - Megavolt-amperes. Units for complex power, the product of the total current and voltage in an electrical circuit.

MVAr - Mega volt-amperes reactive, the component of complex power that is reactive.

kVAr - Kilo volt-amperes reactive, the component of complex power that is reactive.

Capacitor Inrush Current – Transient current when a capacitor bank is switched on or connection made to a voltage source.

Discharge Device – A device that is switched to remove residual voltages from the bank after disconnecting the bank from the power system it was connected to.

Externally Fused Capacitor – A device constructed of one or more series groups of parallel-connected capacitor units where each capacitor unit is protected with a fuse external to the unit.

Fused Capacitor – A capacitor having fuses mounted on its terminals, inside a terminal enclosure, or inside the capacitor case, to disconnect a failed capacitor element, unit, or group.

Fuseless Capacitor – A capacitor bank with no fuse connected in its internal or external connections.

Internally Fused Capacitor (Unit) – A capacitor unit that is internally fused.

Parallel Connected Capacitor – A capacitor unit where the individual elements are connected in parallel. A capacitor unit that has a single string between capacitor terminals is referred to as a parallel-connected unit.

Series Connected Capacitor – A capacitor unit that the individual elements are connected in series. A capacitor unit that is made up of a single connection of elements between capacitor terminals is referred to as a series-connected unit.

String of Capacitors – Series connected capacitor units connected between line terminals.

RTDS – Real Time Digital Simulator

Chapter 1 Introduction

Shunt capacitor banks are essential in electrical power systems. They play a crucial part in providing reactive power support [1][2]. They provide voltage support and an improved system voltage profile at key points within the grid. In addition, they provide increased system capacity through the reduction of losses, and they provide a significant reduction and postponement of investments in transmission and generation capacity by relieving requirements to transmit reactive power over long distances. Because capacitor banks are relatively inexpensive, are quick to install, and can be deployed nearly anywhere on the grid, they are an ideal choice for reactive power support when compared with transmission or generation system upgrades.

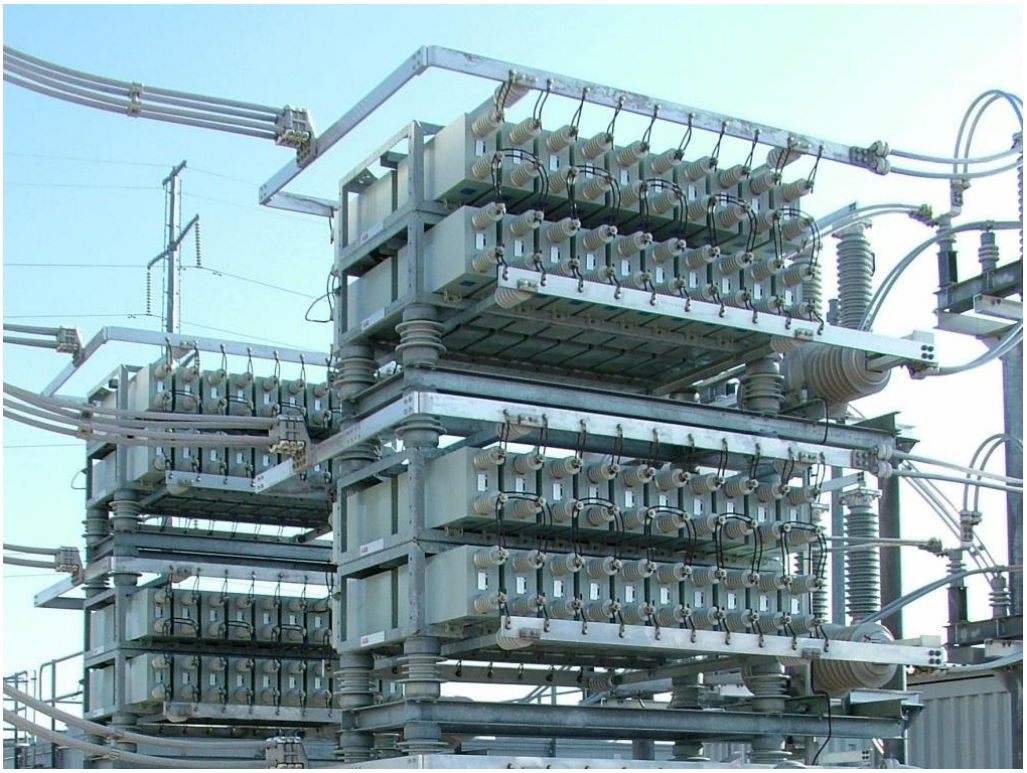


Figure 1-1. Typical Shunt Capacitor Bank

Because of their importance to system operation, the protection of capacitor banks is crucial. Figure 1-1 shows a typical shunt capacitor bank. Developing a protection scheme

for SCBs requires good understanding of their design and failure mechanisms. SCBs can be configured as single-WYE, double-WYE, or H-bridge and can be grounded or ungrounded. SCBs consist of a number of capacitor units connected in series and parallel to meet the voltage and VAr rating of the bank. Each unit consists of a number of capacitor elements connected in series and parallel. Capacitor units most often fail due to continuous overvoltage stress. Fusing provides the first line of protection against failure of capacitor units. SCBs can be externally fused, internally fused or fuseless. With the advent of new dielectrics, the industry trend is more towards fuseless banks. Unbalance protection provides the primary protection against unit or element failures and prevents cascading failure of remaining healthy units. Unbalance protection needs to be sensitive and secure.

Unbalance protection asserts an alarm if the unbalance magnitude is small, but trips the bank if the unbalance is high enough to potentially cause a cascading failure. Using the unbalance phase angle provides an economical way to quickly locate the faulty units and minimize the bank outage time [2].

All unbalance protection schemes have an inherent problem detecting canceling or balanced failures; i.e., units or elements fail in multiple phases or sections in the bank that cancel or reduce the measured net unbalance. If the canceling failure is symmetric, then the measured unbalance will be zero. If the canceling failure is asymmetric, then the measured degree of unbalance will be decreased compared to failures in a single section of the bank. Both symmetric and asymmetric canceling failures result in reduced sensitivity of unbalance protection and affect the reliability of capacitor bank protection. There is very little published in the literature on the topic of canceling failures in shunt capacitor banks.

This thesis proposes an algorithm that can detect symmetric and asymmetric canceling failures and thereby improving the reliability of the capacitor bank unbalance protection. The research investigates using a combination of the change of unbalance magnitude and unbalance angle before and after disturbances in SCBs as a canceling failure detection approach. The proposed algorithm is tested and validated using time domain computer simulation with an electromagnetic transients program. The proposed algorithm is

economical and practical as it uses the unbalance magnitude and phase angle which are available as part of unbalance protection.

1.1 Research Objectives

The goal of this research is to develop an algorithm that can detect symmetric or asymmetric canceling failures and thereby improve the reliability of the capacitor unbalance protection.

The main objectives of this research are as follows:

- Demonstrate the benefit of shunt capacitor banks in power systems, explain bank configurations and failure mechanisms.
- Demonstrate how a SCB is protected and the current state of the art for SCB protection techniques.
- Demonstrate the importance of detecting canceling failures and how they affect the reliability of unbalance protection.
- Develop an algorithm that can detect canceling failures and thereby improve the reliability of capacitor bank unbalance protection. The algorithm should be economical and practical to apply by using measurements already available as part of capacitor bank protection.

The following publications from the author are related to the work in this dissertation.

- "Principles of Shunt Capacitor Bank Application and Protection" [2], will be presented in Chapter 2.
- "Minimizing Capacitor Bank Outage Time Through Fault Location" [6], will be presented in Chapter 3.

1.2 Thesis Outline

Chapter 2 gives a brief brief overview of capacitor bank configurations, terminology and failure mechanisms providing background material needed to understandthis research.

Chapter 3 presents shunt capacitor bank protection methods which are the basis for the proposed canceling failure detection approach.

Chapter 4 presents a literature review on the currently available solutions and point out gaps and opportunities that triggered this research.

Chapter 5 introduces the proposed solutions. The chapter presents the theoretical background of the symmetric and asymmetric canceling fault detection solutions with mathematical derivations.

Chapter 6 will demonstrate the simulation setup and present cases in detail to discuss the relationship between the mathematical assumptions and the simulation results.

Chapter 7 presents the summary of the research, draws conclusions from the research, and suggests future work building from this research.

Chapter 2 Capacitor Bank Configuration and Failure Mechanism

Chapter 2 gives a brief overview of capacitor bank configurations, terminology and failure mechanisms to provide background material needed to understand this research.

2.1 Capacitor Bank Configuration

A shunt capacitor bank, as shown in Figure 2-1, consists of a number of single-phase capacitor units connected in parallel to form a series group. A number of series groups are connected in series to achieve the desired voltage and VAr rating.

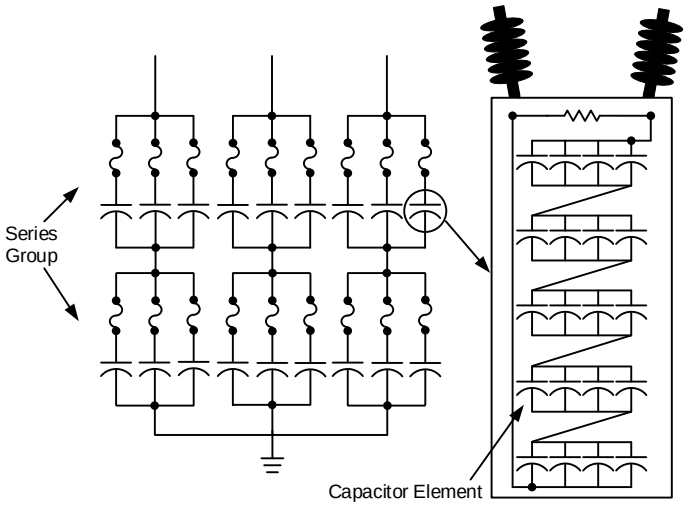


Figure 2-1. Capacitor Bank Configuration

Similarly, each capacitor unit consists of individual capacitor elements connected in series and parallel combinations to meet the desired voltage and VAr rating of the unit.

2.1.1 Capacitor Unit Construction

Capacitor elements are made out of thin sheets of aluminum foil (electrode) rolled together with a polypropylene film (dielectric) as shown in Figure 2-2.

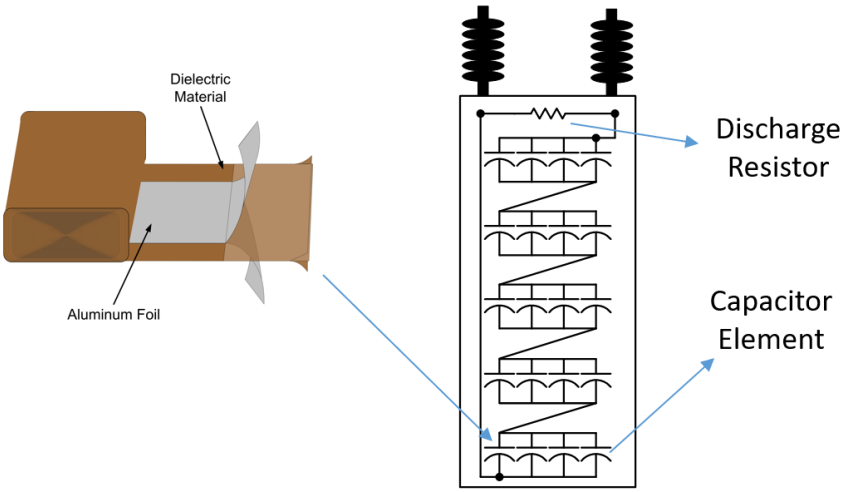


Figure 2-2. Capacitor Unit Construction

The rolled assembly is placed in a stainless steel tank and filled with dielectric liquid to cover the voids in the dielectric material. The electrodes are terminated through bushings with a discharge resistor. When the capacitor unit is disconnected from the source, the discharge resistor is designed in such a way that the residual voltage across the terminals will fall to 50V or less within 5 minutes [3].

2.1.2 Capacitor Unit Configuration

The capacitor units can be fused, or fuseless. Figure 2-1, shows a capacitor bank with externally fused capacitor units. Externally fused capacitor units are fuseless capacitor units with individual fuses connected externally. Internally fused capacitor units have individual fuses for each element inside the capacitor unit. A fuseless capacitor unit doesn't have any fuse.

2.1.3 Capacitor Unit Specifications

IEEE Standard 18 [3] specifies the standard ratings of the capacitor units used for shunt capacitor banks. Capacitor units should not exceed the following ratings when operated continously:

- 110% of rated root-mean-square (RMS) terminal voltage
- 120% of rated peak voltage including harmonics

- 135% of rated RMS current
- 135% of rated kVAr

2.1.4 Externally Fused Banks

Units in an externally fused bank have a few elements in parallel but many elements in series. When an element fails (shorts), the entire row of elements shorts out (Figure. 2-3a). With only a few elements in parallel, the capacitance lost when an element fails is small, and with many elements in series, the increase in voltage across the healthy series units when a unit fails is also small. Units can be designed for a relatively high voltage because the external fuse can interrupt cascade due to a high-voltage fault.

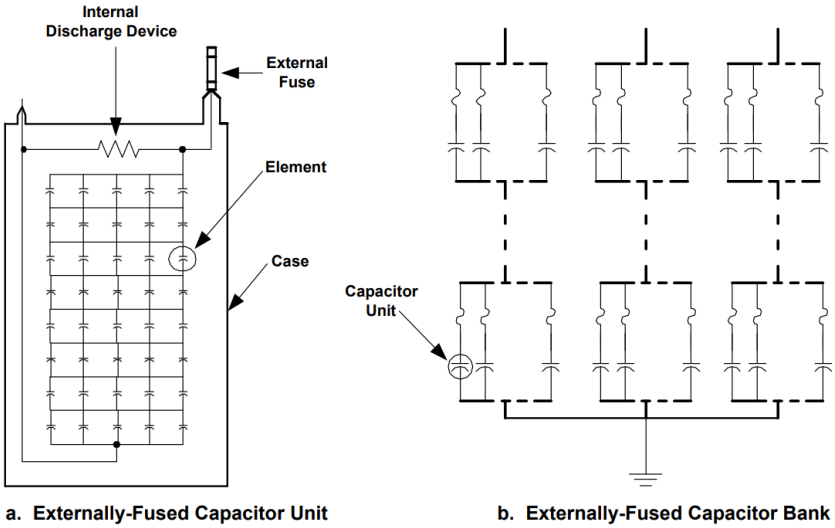


Figure 2-3. Externally Fused Bank [4]

2.1.5 Internally Fused Banks

Internally fused units are manufactured with many elements in parallel. When an element fails (shorts), the fuse of the faulty elements blows, disconnecting the faulty element from the other parallel elements (Figure. 2-4a).

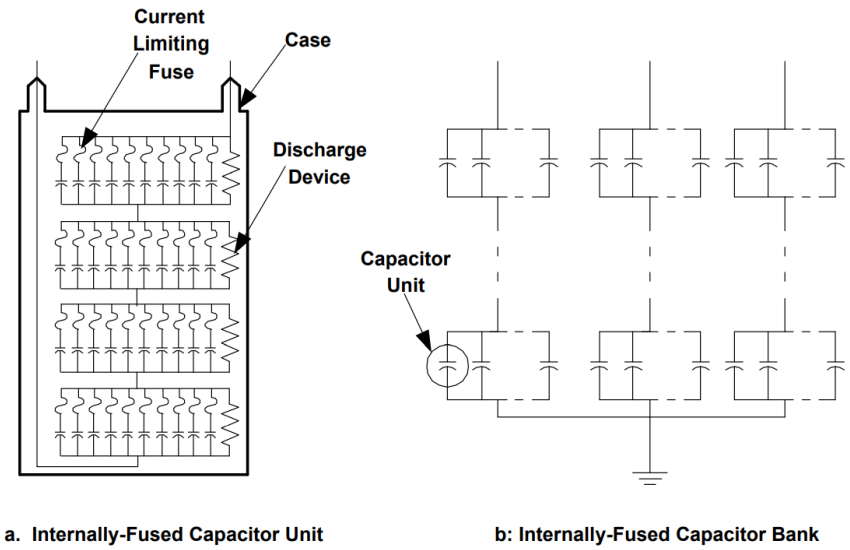


Figure 2-4. Internally Fused Bank [4]

With many elements in parallel, lost capacitance due to a failed element is small and the increase in voltage across the healthy parallel units is also small. Because of the large number of parallel elements in this unit, many elements can fail before unbalance tripping is necessary to remove the bank from service.

2.1.6 Fuseless Banks

Based on modern-day high-quality dielectrics, fuseless units are similar in construction to externally fused units (few elements in parallel, but many elements in series). When an element fails (shorts), the entire row of elements shorts out (Figure 2-5a). However, unlike the fused installations, there are now no fuses to blow, and the effect of a failed element on the bank is permanent. Because there are no fuses in this bank, the bank can be visualized in terms of elements rather than units.

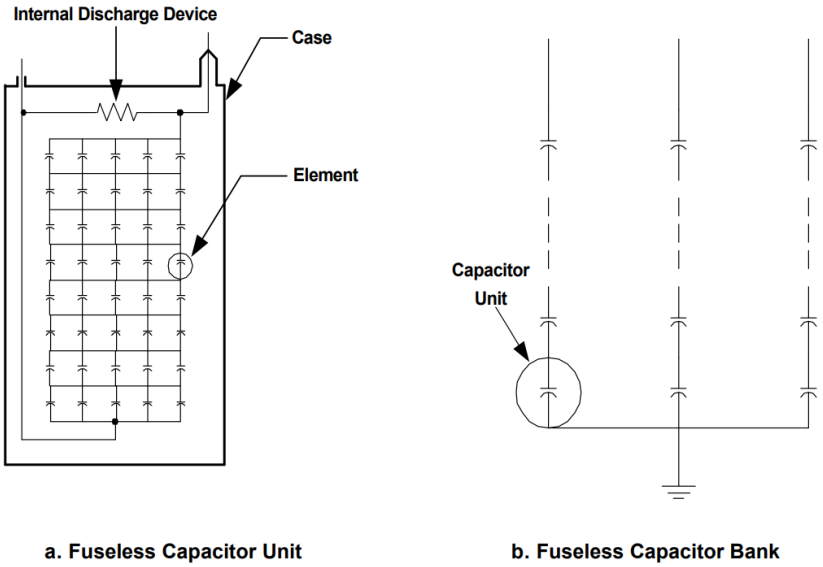


Figure 2-5. Fuseless Bank [4]

2.1.1 Capacitor Bank Connections

Figure 2-6 shows the most common WYE-connected capacitor bank connections [5]. Most transmission-level capacitor banks are WYE connected, either grounded or ungrounded.

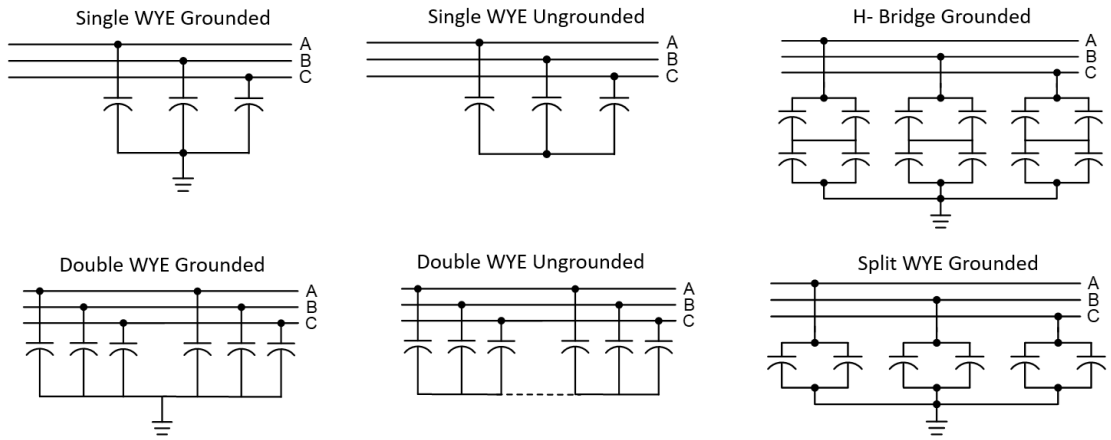


Figure 2-6. Capacitor Bank Connections

Characteristics of a grounded bank are as follows:

- Provides a low impedance to ground for lightning surge currents
- Provides a degree of protection from surge voltages
- Reduces recovery voltages for switching equipment (approximately twice normal peak voltage)
- Provides a low impedance to ground for triplen and other harmonic currents

Characteristics of an ungrounded bank are as follows:

- Does not provide a path for zero-sequence currents, triplen, and other harmonic currents
- Does not provide a path for capacitor discharge currents during system ground faults
- Requires the neutral to be insulated to full line-to-ground voltage

Many factors affect the selection of bank connection such as capacitor unit rating, size of the bank, type of fusing, and protection reliability.

Large capacitor banks with many capacitor units connected in parallel are configured as H-bridge banks. An H-bridge bank has each phase split into four sections with equal capacitance. Each section consists of a number of capacitor units connected in strings if fuseless or in series groups if fused. If the capacitances are equal in all the four sections then there is no current through the bridge. If the capacitance changes in any of the four sections then current flows through the bridge. As long as the bridge is balanced. this configuration is immune to system unbalance, meaning no current flows through the bridge for system changes such as external faults, voltage changes, and unbalance in other phases. So this configuration can make protection sensitive and secure.

2.2 Failure Mechanisms

Although many factors influence the design of a capacitor bank, developments in the dielectric play a major role in determining the character of element failures within a unit [2].

Earlier capacitor units used kraft paper with a PCB impregnant as dielectric. Although the kraft paper was highly refined, there were still many non-uniformities in the paper [4]. To avoid weak spots in the dielectric, capacitor units had several layers of paper inserted between the foil layers. When dielectric material of this type failed, the foil layers did not weld together to form a solid connection. Instead, the cellulose continued to arc, resulting in charring of the paper that generated gas inside the sealed capacitor unit. In many cases, this gas buildup caused the unit to rupture, resulting in damage beyond the failure of a single element.

Present-day dielectrics are manufactured with as few as two to three layers of impregnated polypropylene film (as opposed to many layers of kraft paper). Because the film layers are thin, failures now cause the foils to weld together, thus forming a solid connection between the foils without arcing or charring, effectively shorting the cell.

To understand the failure mechanism in a fused or fuseless bank, an example arrangement is shown in Figure 2-7. This arrangement shows four series groups of 10 identical capacitors in parallel, with a constant applied voltage of 12 V. Each capacitor represents either one series group of elements in an internally fused unit or a complete unit in an externally fused bank.

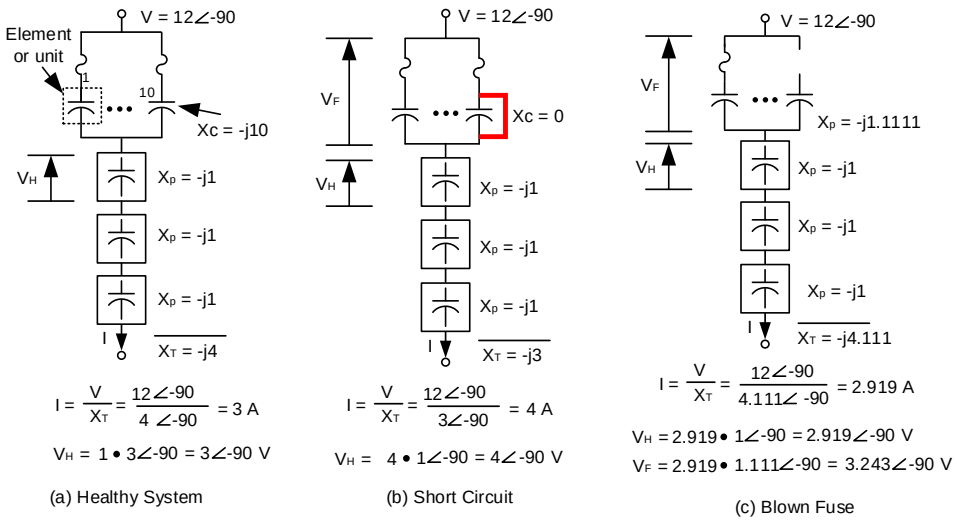


Figure 2-7. Three Stages of Fuse Blowing [6]

The labels in Figure 2-7 are as follows.

Xc = The reactance of each element/unit (10 Ω)

Xp = Reactance of a parallel group of elements/units

XT = Total reactance of the circuit

VF = Voltage across the faulted parallel group of elements/units

VH = Voltage across the healthy parallel group of elements/units

In Figure 2-7(a), the system is healthy and the voltage across each of the four series groups is 3 V. Figure 2-7(b) depicts the circuit just after a short circuit occurs, but before the fuse blows (if it is a fused application). Figure 2-7(b) shows the final state in a fuseless bank. In this state, the following circuit conditions prevail:

- All the elements/units in parallel with the faulted element/unit are shorted out
- The total reactance decreases
- The total capacitance increases
- The total current increases
- The voltage across the healthy series elements/units increases
- The increased voltage is evenly distributed among the healthy series elements/units

Figure 2-7(c) depicts the circuit after the fuse blows. At this point, the following circuit conditions prevail:

- The reactance of the faulted parallel group increases
- The voltage across all the elements/units in the faulted parallel group increases
- The total reactance increases
- The total capacitance decreases
- The total current decreases
- The voltage across the healthy elements/units decreases
- The decreased voltage is evenly distributed among the healthy elements/units

When a capacitor element fails in a fused unit, there is an increase in current through the fuse of the failed element. This current consists of two components:

- Increase in fundamental frequency current resulting from the decrease in reactance
- Increase in transient current, resulting from the discharge current from the healthy parallel elements

Both components must be considered when selecting a fuse size: the fuse on the healthy elements must not blow when discharging into an adjacent faulted capacitor but must quickly and effectively remove a failed element/unit.

2.3 Summary

This chapter gave a brief overview of capacitor bank configurations, terminology and failure mechanisms, which provides the background material needed to understand this research. The chapter also covered the capacitor unit construction, capacitor unit specifications, fusing methods, and common capacitor bank connections.

Chapter 3 Capacitor Bank Unbalance Protection and Fault Location

This chapter presents current practices for capacitor bank unbalance protection and fault location methods that can be applied to various capacitor bank configurations. This chapter provides the basis for understanding the canceling failure issue discussed in Chapter 4 and the solution proposed to address it in Chapter 5.

3.1 Capacitor Bank Unbalance Protection

Unbalance protection methods provide primary protection against unit failures in capacitor banks. These methods detect unbalances within the bank due to element or unit failures.

Unbalance protection asserts an alarm signal if the unbalance is small but trips the bank if the unbalance is high enough to cause a cascading failure.

There are four commonly used unbalance protection methods [5][6][7]:

- Phase voltage unbalance.
- Neutral voltage unbalance.
- Phase current unbalance.
- Neutral current unbalance.

The choice of protection method depends on various factors such as bank configuration, availability and location of instrument transformers, desired sensitivity, and desired security. The unbalance protection methods use one or more of the measured quantities such as bus voltages, bank currents, neutral voltage, and neutral current to calculate the unbalance quantity.

The unbalance quantity is a phasor, and its magnitude directly measures the unbalance within the bank due to element or unit failures. The magnitude of the unbalance quantity directly indicates the number of failed elements or units. Unbalance protection is

generally set to ALARM when the voltage across healthy elements or units is more than 105% of rated after a set time delay and TRIP when the voltage across healthy elements or units is more than 110% after short time delay.

The unbalance protection will be sensitive and secure for detecting faulty conditions if the unbalance protection first compensates for inherent unbalance within the bank. The inherent unbalance can be from the manufacturing tolerances in the individual bank capacitor units, and temperature changes.

Unbalance protective relays are often provided with either a manual command or an auto option to reset the inherent unbalance. In addition, a bank with a limited number of element or unit failures that result in an acceptable overvoltage can be left in operation for some time awaiting scheduled or emergency maintenance. This can cause an unbalance alarm that needs to be reset by the protective relay so that subsequent failures are detected with maximum sensitivity.

The phase angle of the unbalance quantity when referenced properly can provide fault location [8][9][10]. The reference can be a phase voltage (bus), phase current (bank), positive-sequence bus voltage, and positive-sequence bank current. If the bank is protected with the phase voltage or phase current unbalance protection method, then use phase voltage (bus) or phase current (bank) as the reference quantity. If the bank is protected with the neutral voltage or neutral current unbalance protection method, then use positive-sequence bus voltage or positive-sequence bank current as the reference quantity. The fault location is supervised by unbalance protection operation (ALARM or TRIP assertion). The fault location helps in identifying the phase and section of the bank that has the faulty element or unit. The fault location information can be included as part of the event report and can be used by the utility crew to perform planned maintenance.

For sensitivity, the fault location technique is supervised with an alarm or trip condition from unbalance protection. For security, a ±15-degree blinder is applied to exclude unbalances not resulting from capacitor failures, such as instrument transformer errors. The fault location technique is embedded as part of the unbalance protection, and hence, it is an economical solution.

The fault location technique is not affected by the inherent unbalance as long as the unbalance protection compensates for it. Unbalance protective relays are often provided with a manual command to reset the inherent unbalance.. A bank with element or unit failures that cause acceptable overvoltage can be left in operation for some time awaiting scheduled or emergency maintenance. This can cause an unbalance alarm that needs to be reset by the protective relay so that subsequent failures are detected with maximum sensitivity. The fault location information needs to be saved before resetting the unbalance alarm. When a second failure happens, which results in an alarm or trip, the fault location technique is accurate for the second failure despite the preexisting failure. When the bank is taken out of service, personnel must search for two failures using the original and subsequent fault location information.

3.2 Phase Voltage Unbalance Protection

3.2.1 Single-Wye Grounded Bank With Tapped Potential Transformer

Phase voltage unbalance or phase voltage differential protection is applied to a WYE-connected capacitor bank with a potential transformer (PT) at the tap point, as shown in Figure 3-1. The tap point can be at the midpoint of the bank or at a low voltage capacitor just above the neutral point of the WYE connection.

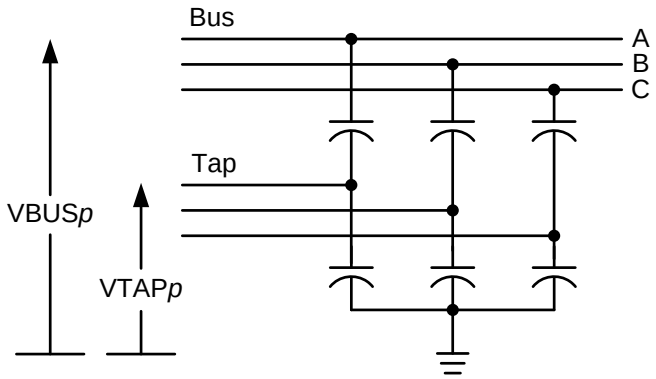


Figure 3-1. Banks Using Tapped PT-Based Phase Voltage Unbalance Protection

The protection uses the tapped voltage and bus voltage measurements to calculate the unbalance quantity as shown in (3.1).

$$DVp = VBUSp - Kp \bullet VTAPp \qquad (3.1)$$

where:

VBUS*p* is the Phase *p* bus voltage phasor.

VTAP*p* is the Phase *p* tap voltage phasor.

K*p* is the Phase *p* phasor setting based on relay measurements that reset inherent unbalance.

p is A, B, or C.

The unbalance quantity is per-phase and so is the unbalance protection. The phase (A, B, or C) of the bank with the faulty unit or element is the phase for which the protection has operated (based on unbalance quantity magnitude). Comparing the phase angle of the unbalance quantity with the phase angle of the bus voltage allows the fault location to be further narrowed down by identifying the section (top or bottom from the tapped point) of the phase.

Figure 3-2 shows the fault location technique for banks using voltage inputs from the tap point to provide per-phase voltage unbalance protection. The phase angle of the unbalance quantity is referenced to the phase angle of the respective bus voltage, and the referenced phase unbalance angle, DV*p*A, is then checked to determine if it is in Sector 1 (0° ± 15°) or Sector 2 (180° ± 15°).

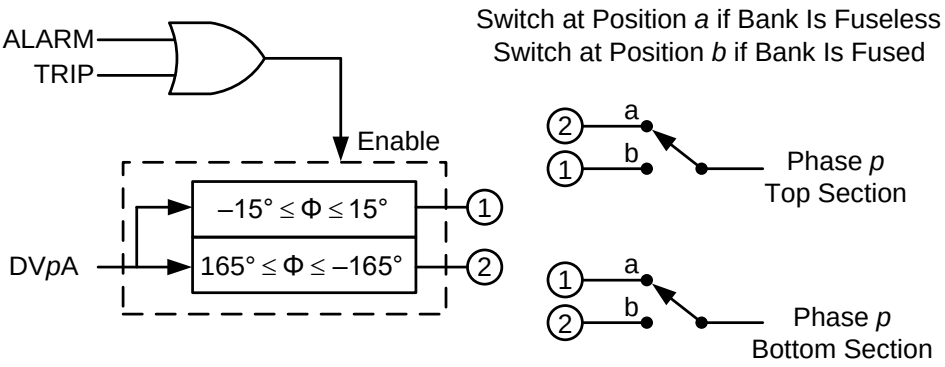


Figure 3-2. Fault Location for Banks Using Phase Voltage Unbalance

For a fused bank, if DV*p*A is in Sector 1, then the faulty unit or element is in Phase *p* and the top section from the tap point. If DV*p*A is in Sector 2, then the faulty unit or element is in Phase *p* and the bottom section from the tap point. If the bank is fuseless, then the

section identification is opposite (i.e., if DV*p*A is in Sector 1, then the fault is in the bottom section, and if DV*p*A is in Sector 2, then the fault is in the top section).

This economical fault location technique reduces the investigation time by 83.3 percent (one out of six possible fault locations) for a WYE-connected grounded or ungrounded bank that uses phase voltage unbalance protection. Maximum gains in the search time are possible if the tap is at the midpoint. The worst-case reduction approaches 66 percent (only a faulted phase) if the tap is very close to the neutral point of the bank.

3.3 Neutral Voltage Unbalance Protection

3.3.1 Single-or Double-Wye Bank With Neutral-to-Ground Potential Transformer

Neutral voltage unbalance protection is applied to a WYE connected capacitor bank with a neutral to ground PT, as shown in Figure 3-3. The bank can be single or double WYE.

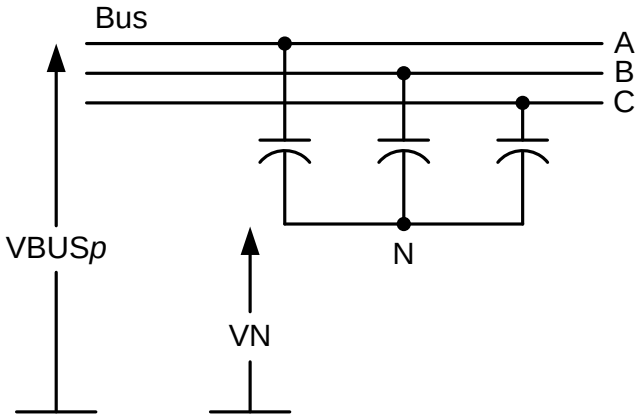


Figure 3-3. Ungrounded Banks Using Neutral Voltage Unbalance Protection

The unbalance protection uses the neutral voltage and bus voltage measurements to calculate the unbalance quantity as shown in (3.2).

$$DVG = VBUSA + VBUSB + VBUSC - 3 \bullet VN - \big(K1 \bullet (VBUSB - VN) + K2 \bullet (VBUSC - VN)\big) \quad (3.2)$$

where:

VBUS*p* is the Phase *p* bus voltage phasor.

VN is the neutral voltage phasor.

K1 and K2 are the scale factor settings based on the relay measurements that reset inherent unbalance.

The unbalance quantity is not per-phase, so the phase that has the faulty unit or element cannot be determined based on the unbalance protection operation. However, by comparing the phase angle of the unbalance quantity with the phase angle of the positive-sequence bus voltage, we can identify the phase that has the faulty unit or element.

Figure 3.4 shows the fault location technique for ungrounded banks using neutral voltage unbalance protection. The phase angle of the unbalance quantity is referenced to the phase angle of the positive-sequence bus voltage. The referenced phase unbalance angle, DVGA, is then checked to determine if it is in Sector 1 (0° ± 15°), Sector 2 (180° ± 15°), Sector 3 (–120° ± 15°), Sector 4 (60° ± 15°), Sector 5 (120° ± 15°), or Sector 6 (–60° ± 15°). For a fuseless bank, if DVGA is in Sector 1, then the faulty unit or element is in Phase A. If DVGA is in Sector 3, then the faulty unit or element is in Phase B. If DVGA is in Sector 5, then the faulty unit or element is in Phase C.

For a fused bank, if DVGA is in Sector 2, then the faulty unit or element is in Phase A. If DVGA is in Sector 4, then the faulty unit or element is in Phase B. If DVGA is in Sector 6, then the faulty unit or element is in Phase C.

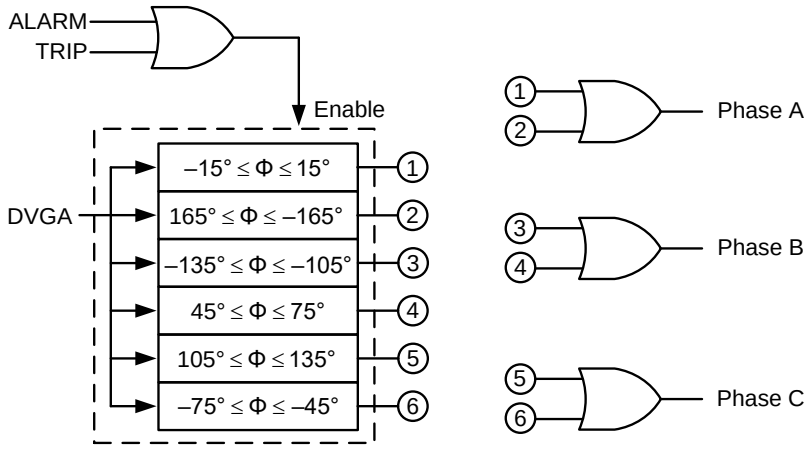


Figure 3-4. Fault Location for Single-Wye Banks Using Neutral Voltage Unbalance Protection

This economical fault location technique reduces investigation time by 66.6 percent (one out of three possible faulted phases) for a single-WYE ungrounded bank that uses neutral voltage unbalance protection.

This fault location technique can be applied to a double-WYE ungrounded bank with a common neutral and a single neutral PT for neutral unbalance protection. In this case, however, the fault location technique cannot identify the section of the bank that has the fault. It can still identify the phase of the bank, resulting in a 66.6 percent (two out of six possible fault locations) reduction in investigation time.

3.3.2 Double-Wye Bank With Potential Transformer between Neutrals

Neutral voltage unbalance protection is applied to a double-WYE ungrounded capacitor bank with a PT between the neutrals, as shown in Figure 3-5.

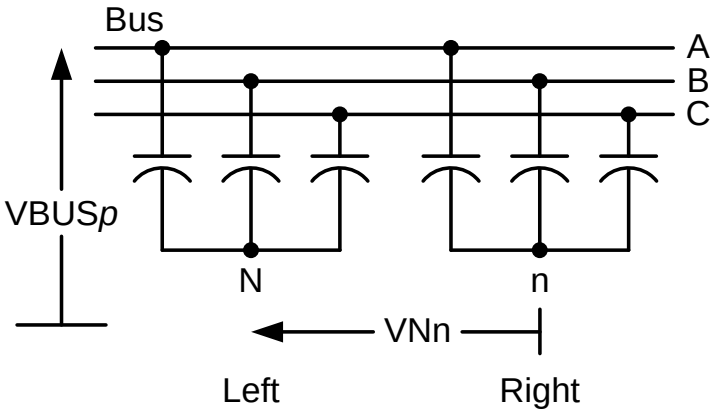


Figure 3-5. Ungrounded Banks with a Neutral PT Using Neutral Voltage Unbalance Protection

The unbalance protection uses the neutral voltage and bus voltage measurements to calculate the unbalance quantity as shown in (3.3).

$$DVG = VNn - K \bullet V1BUS \qquad (3.3)$$

where:

VN*n* is the neutral voltage phasor.

V1BUS is positive sequence bus voltage based on measured bus voltages VBUS*p*.

K is the phasor setting based on relay measurements that resets inherent unbalance.

Figure 3-6 shows the fault location technique for double-WYE ungrounded banks with a PT between the neutrals and using neutral voltage unbalance protection. The phase angle of the unbalance quantity is referenced to the phase angle of the positive-sequence bus voltage, and the referenced phase unbalance angle, DVGA, is then checked to determine if it is in Sector 1 (0° ± 15°), Sector 2 (180° ± 15°), Sector 3 (–120° ± 15°), Sector 4 (60° ± 15°), Sector 5 (120° ± 15°), or Sector 6 (–60° ± 15°).

For a fuseless bank, if DVGA is in Sector 1, then the faulty unit or element is in Phase A and the left section of the bank. If DVGA is in Sector 2, then the faulty unit or element is in Phase A and the right section of the bank. Similar logic applies to Phase B and Phase C.

For a fused bank, if DVGA is in Sector 2, then the faulty unit or element is in Phase A and the left section of the bank. If DVGA is in Sector 1, then the faulty unit or element is in Phase A and the right section of the bank. Similar logic applies to Phase B and Phase C.

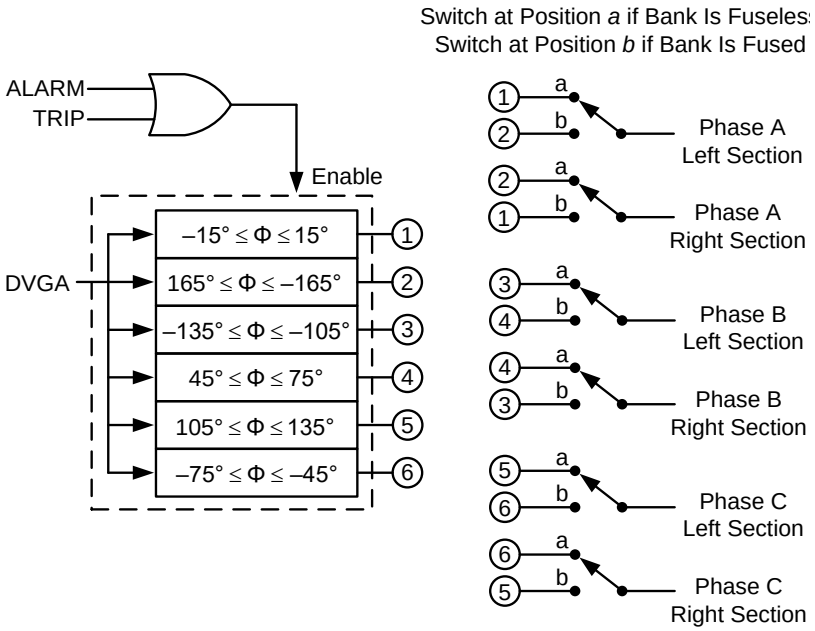


Figure 3-6. Fault Location for Double-Wye Banks Using Neutral Voltage Unbalance Protection

This economical fault location technique reduces investigation time by 83.3 percent (one out of six possible fault locations) for a double-WYE ungrounded bank with a PT between the neutrals that uses neutral voltage unbalance protection.

3.4 Phase Current Unbalance Protection

3.4.1 H-Bridge Bank With Current Transformer (CT) in Each Phase

Phase current unbalance protection is applied to an H-bridge-connected capacitor bank, as shown in Figure 3-7.

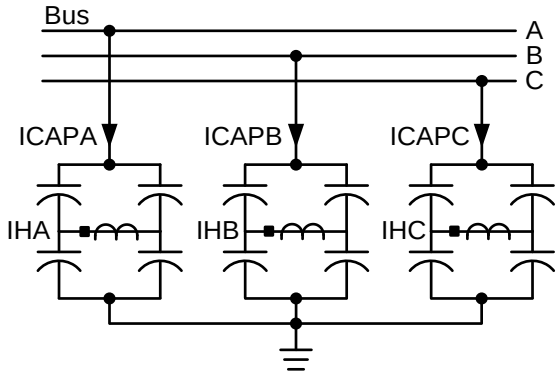


Figure 3-7. H-Bridge Bank Using Phase Current Unbalance Protection

The protection uses balance or bridge current and bank current measurements to calculate the unbalance quantity as shown in (3.4).

$$60p = IHp - Kp \bullet ICAPp \qquad (3.4)$$

where:

ICAP*p* is the Phase *p* bank current phasor.

IH*p* is the Phase *p* bridge current phasor.

K*p* is the Phase *p* phasor setting based on the relay measurements that resets inherent unbalance.

The unbalance quantity is per-phase and so is the unbalance protection. The phase of the bank with the faulty unit or element is the phase for which the protection has operated (based on unbalance quantity magnitude). By comparing the phase angle of the unbalance quantity with the phase angle of the bank current, we can further narrow down the fault location by identifying the section.

Figure 3-8 shows the fault location technique for H-bridge banks with phase current unbalance protection. The phase angle of the unbalance quantity is referenced to the phase angle of the respective bank current, and the referenced phase unbalance angle, 60*p*A, is then checked to determine if it is in Sector 1 (0° ± 15°) or Sector 2 (180° ± 15°).

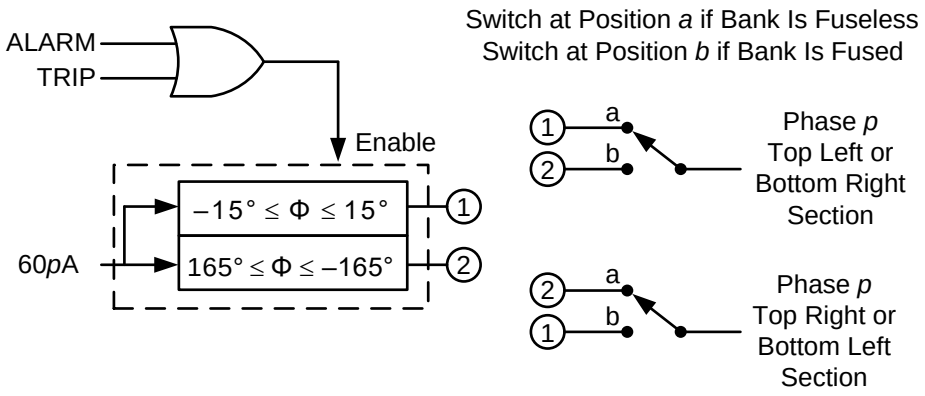


Figure 3-8. Fault Location for H-Bridge Banks Using Phase Current Unbalance

For a fuseless bank, if 60*p*A is in Sector 1, then the faulty unit or element is in Phase *p* and either the top left or bottom right section. If 60*p*A is in Sector 2, then the faulty unit or element is in Phase *p* and either the top right or bottom left section. If the bank is fused, then the section identification is the opposite.

This economical fault location technique reduces the investigation time by 83.33 percent (2 out of 12 possible fault locations) for an H-bridge-connected grounded or ungrounded bank that uses phase current unbalance protection.

3.4.2 H-Bridge Bank With Current Transformer (CT) in Each Phase and PT at Tap at Bridge Point

Modern protective relays can be configured to provide multiple unbalance protection schemes that are operative at the same time. This improves the reliability of the capacitor bank protection. If the H-bridge bank is provided with a PT at the tap point along with the bridge CTs, then both phase voltage and phase current unbalance protection can be applied at the same time. This scheme provides protection reliability.

Figure 3-9 shows the fault location technique for banks using tapped voltage-based phase voltage unbalance and bridge CT-based phase current unbalance protection. Recall that the phase current unbalance-based fault location can identify if the fault is in either the top left or bottom right sections and the top right or bottom left sections. Also, the phase voltage unbalance protection based on the voltage from the tap point can identify if the fault is in the top or bottom sections. Combining information from these two fault location techniques, we can identify any of the 12 fault locations in an H-bridge bank.

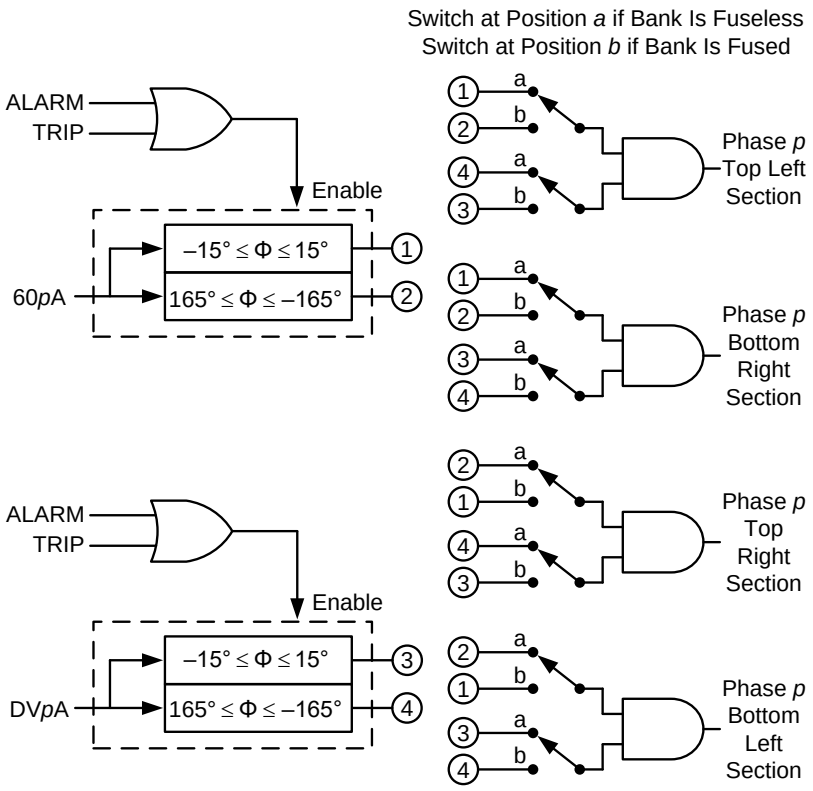


Figure 3-9. Fault Location for H-Bridge Banks Using Phase Current and Phase Voltage Unbalance

This fault location technique reduces investigation time by 91.6 percent (1 out of 12 possible fault locations) for an H-bridge-connected grounded or ungrounded bank that uses phase current and phase voltage unbalance protection.

3.4.3 Double-Wye Bank With CT Measuring Each Phase Unbalance

Phase current unbalance protection is applied to a WYE connected capacitor bank with a CT measuring the phase current unbalance, as shown in Figure 3-10. The unbalance protection is same as for the H-bridge bank.

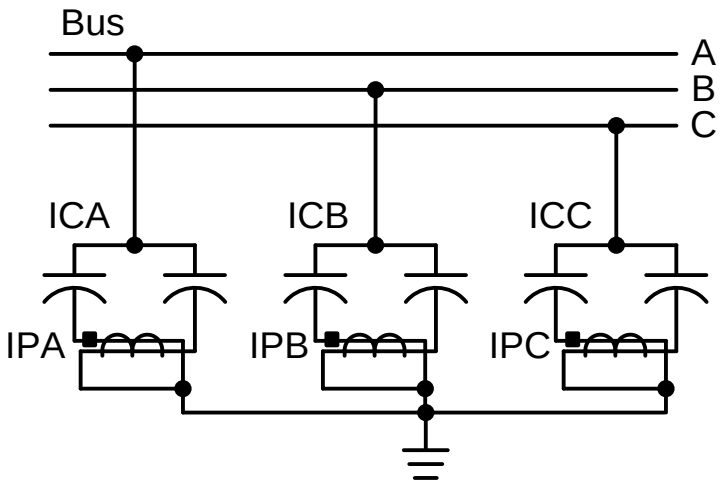


Figure 3-10. Double-Wye Bank Using Phase Current Unbalance Protection

The unbalance protection and fault location technique are the same as for the H-bridge bank, but there are no top or bottom sections. Figure 3-11 shows the fault location technique for this configuration.

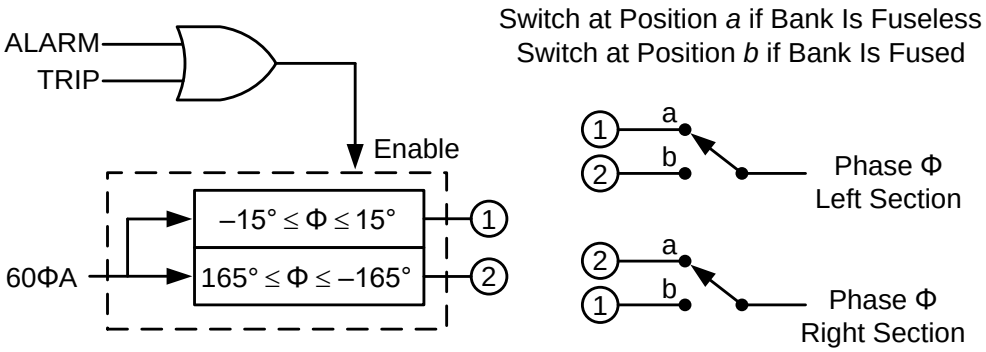


Figure 3-11. Fault Location for Double-Wye Banks Using Phase Current Unbalance

This fault location technique reduces investigation time by 83.3 percent (one out of six possible fault locations) for double-WYE-connected grounded or ungrounded banks that use phase current unbalance protection.

3.5 Neutral Current Unbalance Protection

3.5.1 Double-Wye Bank With Current Transformer (CT) in the Neutral

Neutral current unbalance protection is applied to a double-WYE-connected ungrounded capacitor bank with a CT in the common neutral, as shown in Figure 3-12.

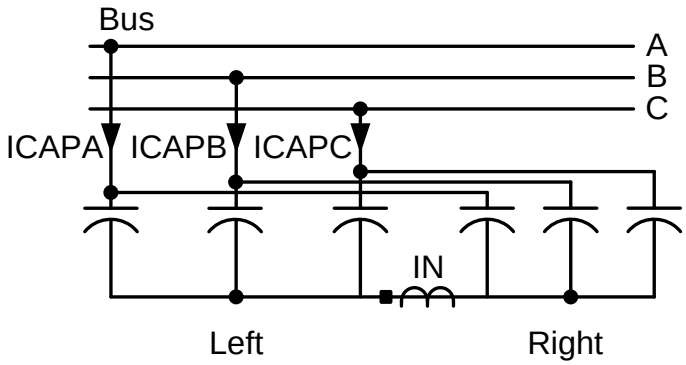


Figure 3-12. Double-Wye Bank Using Neutral Current Unbalance Protection

The unbalance protection uses neutral current and bank current measurements to calculate the unbalance quantity as shown in (3.5).

$$60N = IN - (K1 \bullet ICAPB + K2 \bullet ICAPC) \qquad (3.5)$$

where:

ICAP*p* is the Phase *p* bank current phasor.

IN is the neutral current phasor.

K1 and K2 are the scale factor settings based on the relay measurements that resets inherent unbalance.

Figure 3-13 shows the fault location technique for double-WYE ungrounded banks with a CT in the common neutral and using neutral current unbalance protection. The phase angle of the unbalance quantity is referenced to the phase angle of the positive-sequence bank current (derived from ICAP*p*), and the referenced phase unbalance angle, 60NA, is then checked to determine if it is in Sector 1 (0° ± 15°), Sector 2 (180° ± 15°), Sector 3 (–120° ± 15°), Sector 4 (60° ± 15°), Sector 5 (120° ± 15°), or Sector 6 (–60° ± 15°). For sensitivity, the fault location technique is supervised with an alarm or trip condition from

the unbalance protection. For security, a ±15-degree blinder is applied for unbalances not resulting from capacitor failures.

For a fuseless bank, if 60NA is in Sector 1, then the faulty unit or element is in Phase A in the left section of the bank. If 60NA is in Sector 2, then the faulty unit or element is in Phase A in the right section of the bank. Similar logic applies for Phase B and Phase C.

For a fused bank, if 60NA is in Sector 2, then the faulty unit or element is in Phase A in the left section of the bank. If 60NA is in Sector 1, then the faulty unit or element is in Phase A in the right section of the bank. Similar logic applies for Phase B and Phase C.

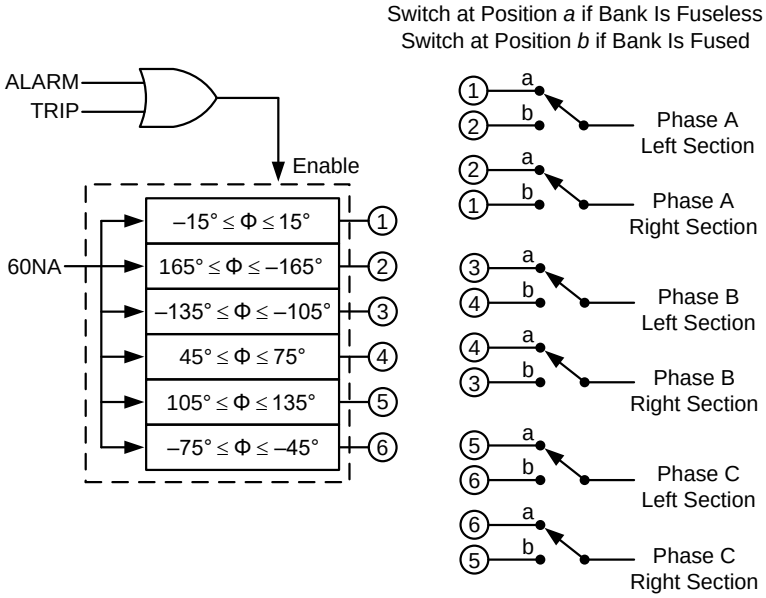


Figure 3-13. Fault Location for Double-Wye Banks Using Neutral Current Unbalance Protection

This economical fault location technique reduces investigation time by 83.3 percent (one out of six possible fault locations) for a double-WYE-connected ungrounded bank that uses neutral current unbalance protection.

3.6 Summary

This chapter presented four common capacitor bank unbalance protection methods and fault location techniques that can be applied to various capacitor bank

configurations. This chapter provides the basis for understanding the proposed canceling failure detection.

Chapter 4 Canceling Failure Issue and Literature Survey

All unbalance protection schemes have an inherent problem detecting canceling failures. This chapter provides an understanding of the canceling failure issue in unbalance protection schemes and presents a literature survey on the state of research in this area.

4.1 Canceling Failure Issue

The unbalance protection schemes discussed in Chapter 3 respond to unbalance within the bank. When multiple units fail in different sections of the bank, it is possible for the measured unbalance to be reduced or canceled out entirely when there are simultaneous failed units in different parts of the bank.

Figure 4-1 shows a fuseless H-bridge bank that uses phase current unbalance protection for detecting faulty units in the bank. If same number of units or elements fail in the left top and left bottom section of Phase A, then the change of reactance in the left top and left bottom section will be same as will the voltage drop, resulting in canceling out the effect of the failed units on the measured unbalance current. From equation (3.4), the phase current unbalance will be zero and the Phase A current unbalance protection will not be able to detect the faulty units in this case. This type of failure is called symmetric canceling failure.

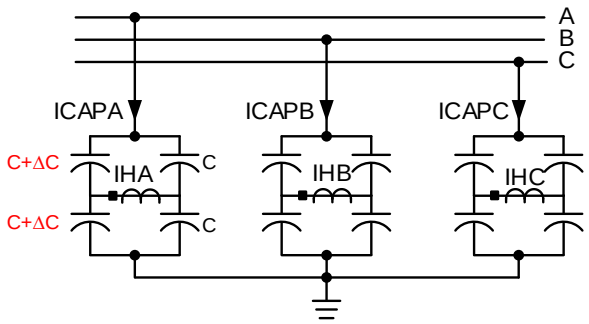


Figure 4-1. Canceling Failure in H-Bridge Banks Using Phase Current Unbalance Protection

If the number of elements or units failed in the left top and left bottom section of Phase A in Figure 4-1 are not same, then the measured unbalance current will be reduced. This type of failure is called an asymmetric canceling failure.

Both symmetric and asymmetric canceling failures result in reduced sensitivity of unbalance protection and affect the reliability of capacitor bank protection.

The same canceling failures can happen when we have element or unit failures in left top and left right, right top and right bottom, left bottom and right bottom.

Figure 4-2 shows a Single-Wye grounded fuseless bank with a tapped PT that uses phase voltage unbalance protection. Symmetric and asymmetric canceling failures can happen if units or elements fail in the top and bottom section of Phase A. The change of reactance in the left top and left bottom section will be same and as is the voltage ratio, resulting in canceling out the measured unbalance voltage. From equation (3.1), the phase current unbalance will be zero and Phase A voltage unbalance protection will not be able to detect the faulty units in this case.

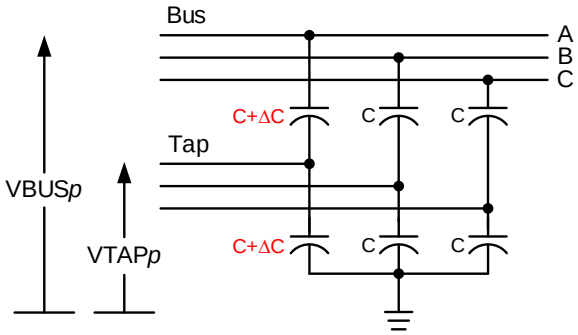


Figure 4-2. Canceling Failure in Single-Wye Grounded Banks With Tapped PT

Figure 4-3 shows a Double-Wye grounded fuseless bank with a neutral CT that uses neutral current unbalance protection. Symmetric and asymmetric canceling failures can happen if units or elements fail in the left and right section of Phase A. The change of reactance in the left and right section will be same, and as a result there will be no voltage drop, resulting in canceling out the measured unbalance current. From equation (3.5), the neutral current unbalance will be zero and neutral current unbalance protection will not be able to detect the faulty units in this case even though the bank is unbalanced.

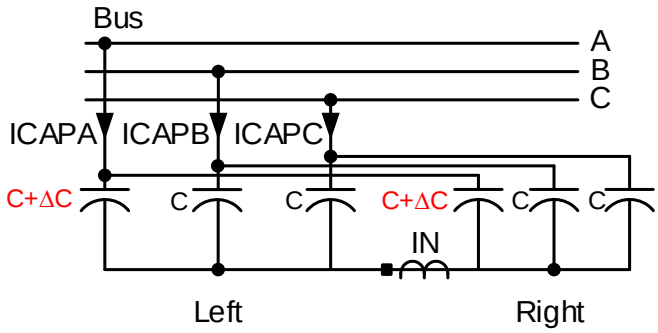


Figure 4-3. Canceling Failure in Double-Wye Ungrounded Bank with Neutral CT

Symmetric and asymmetric canceling failures result in reduced sensitivity of unbalance protection and affect the reliability of capacitor bank protection.

4.2 Literature Survey

The author did an extensive literature survey using IEEExplore and various relay vendor manuals and found that there is very little published in the literature on the topic of canceling failures in shunt capacitor banks.

The IEEE Guide for Protection of Shunt Capacitor Banks discusses the canceling failure problems and generally suggests applying multiple unbalance protection methods to address this issue [6]. For example, the Double-Wye ungrounded bank shown in Figure 4-3 uses a neutral CT for neutral current unbalance protection. By adding neutral PT to the bank, we can apply neutral voltage unbalance protection. This improves reliability of protection as they use different principles and as an added benefit it can detect canceling failures. The suggestion might not be economical nor practical based on the bank configuration and utility practices.

The authors of [11] proposed a new method called intra-phase string current unbalance protection. A CT is installed to measure each string current in the bank. Traditional phase current unbalance protection is applied between each string current for a phase in a loop. The method reduces the possibility of canceling failure as we are increasing the number of unbalance protection elements. But the solution might become complex and difficult to maintain depending on the bank size.

4.3 Summary

This chapter explained the symmetric and asymmetric canceling failure issues and how they affect the sensitivity and reliability of unbalance protection schemes. This chapter also presented the few references related to this research area.

Chapter 5 Canceling Failure Detection: Proposed Solution

This chapter presents the mathematical analysis of canceling failures and introduces the proposed solution to enhance capacitor bank unbalance protection by detecting symmetric and asymmetric canceling failures.

The research investigates using a combination of the change of unbalance magnitude and unbalance angle before and after a disturbance in a single-WYE grounded H-bridge bank as a canceling failure detection approach. It provides a mathematical analysis of the proposed solution for single-WYE grounded fuseless banks connected as H-bridges, which can be easily extended to other bank configurations.

5.1 Canceling Failure Analysis

Figure 5-1 shows a per-phase representation of a single-WYE grounded fuseless capacitor bank connected as an H-bridge.

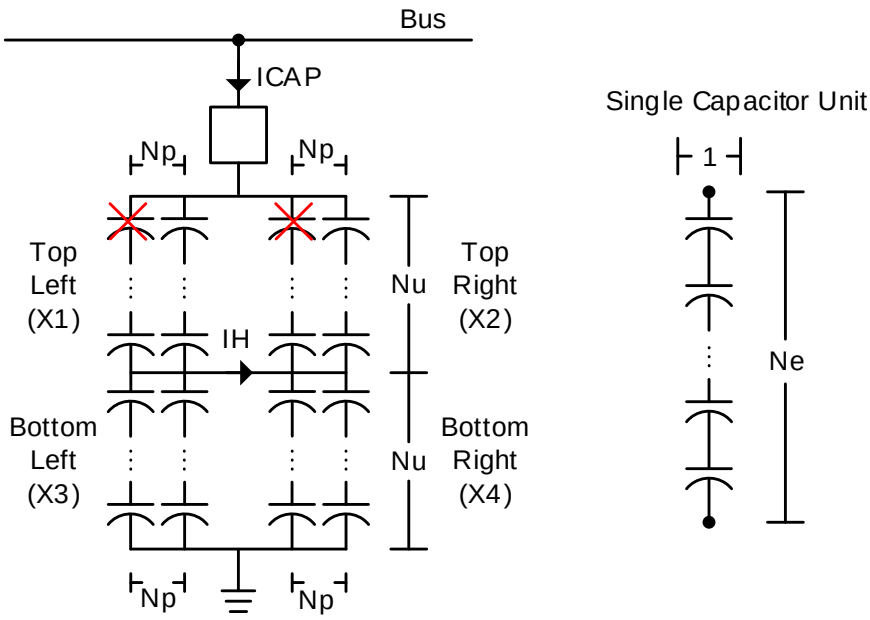


Figure 5-1. Balanced Failure in Single-WYE Grounded Banks Connected in a H-Bridge

The following definitions are used for the canceling failure analysis of a single-WYE grounded fuseless bank shown in Figure 5-1:

Ne is number of elements in a unit

Nu is number of units in a string in a section

Np is number of parallel strings in a section

Ns is number of elements in a string

Ce is capacitance of element

IH is the bridge current

ICAP is the phase current of the bank

V is the phase voltage of the bus

X1, X2, X3, X4 are reactances of each section of the bank

C1, C2, C3, C4 are capacitances of each section of the bank

Total number of elements in a string:

$$Ns = Nu \cdot Ne \tag{5.1}$$

Total capacitance in a section:

$$C = \frac{Ce}{Ns} Np \tag{5.2}$$

Total capacitance in a string:

$$dC = \frac{Ce}{Ns} \tag{5.3}$$

Total number of strings in a section:

$$p = \frac{C}{dC} = Np \tag{5.4}$$

Total capacitance of a section with *x* number of shorted elements:

$$Cf(x) = \frac{Ce}{Ns-x} + \frac{Ce}{Ns}(Np - 1) \tag{5.5}$$

$$Cf(x) = \frac{Ce}{Ns}(Np) + Ce\left(\frac{1}{Ns-x} - \frac{1}{Ns}\right) \tag{5.6}$$

$$Cf(x) = \frac{Ce}{Ns}(Np) + \frac{Ce}{Ns}\left(\frac{x}{(Ns-x)}\right) \tag{5.7}$$

$$f(x) = \frac{x}{(Ns-x)} \tag{5.8}$$

$$Cf(x) = C + f(x) \cdot dC \tag{5.9}$$

Equations (5.10) to (5.20) show bridge current derivation in terms of section capacitances.

$$IH = \frac{ICAP}{2}\left[\frac{X2-X1}{X1+X2} + \frac{X3-X4}{X3+X4}\right] \tag{5.10}$$

$$IH = \frac{ICAP}{2}\left[\frac{X2(X3+X4)-X1(X3+X4)+X3(X1+X2)-X4(X1+X2)}{(X1+X2)(X3+X4)}\right] \tag{5.11}$$

$$IH = \frac{ICAP}{2}\left[\frac{X2\cdot X3+X2\cdot X4-X1\cdot X3-X1\cdot X4+X3\cdot X1+X3\cdot X2-X4\cdot X1-X4\cdot X2}{(X1+X2)(X3+X4)}\right] \tag{5.12}$$

$$IH = \frac{ICAP}{2}\left[\frac{X2\cdot X3-X1\cdot X4+X3\cdot X2-X4\cdot X1}{(X1+X2)(X3+X4)}\right] \tag{5.13}$$

$$IH = ICAP\left[\frac{X2\cdot X3-X1\cdot X4}{(X1+X2)(X3+X4)}\right] \tag{5.14}$$

$$ICAP = \frac{V}{\left(\frac{X1\cdot X2}{X1+X2}\right)+\left(\frac{X3\cdot X4}{X3+X4}\right)} \tag{5.15}$$

$$IH = \left[\frac{V}{\left(\frac{X1\cdot X2}{X1+X2}\right)+\left(\frac{X3\cdot X4}{X3+X4}\right)}\right]\left[\frac{X2\cdot X3-X1\cdot X4}{(X1+X2)(X3+X4)}\right] \tag{5.16}$$

$$IH = \left[\frac{V((X1+X2)(X3+X4))}{X1\cdot X2(X3+X4)+X3\cdot X4(X1+X2)}\right]\left[\frac{X2\cdot X3-X1\cdot X4}{(X1+X2)(X3+X4)}\right] \tag{5.17}$$

$$IH = \left[\frac{V}{\frac{X1\cdot X2(X3+X4)+X3\cdot X4(X1+X2)}{X1\cdot X2\cdot X3\cdot X4}}\right]\left[\frac{X2\cdot X3-X1\cdot X4}{X1\cdot X2\cdot X3\cdot X4}\right] \tag{5.18}$$

$$IH = \left[\frac{V}{\frac{1}{X1}+\frac{1}{X2}+\frac{1}{X3}+\frac{1}{X4}}\right]\left[\frac{1}{X1\cdot X4}-\frac{1}{X2\cdot X3}\right] \tag{5.19}$$

$$IH = j\omega V\left[\frac{C1\cdot C4-C2\cdot C3}{C1+C2+C3+C4}\right] \tag{5.20}$$

Bridge Current with no Fault

Starting with a balanced bank, C1=C2=C3=C4=C and substituting in (5.20), we see that the H-bridge current is zero.

$$IH = j\omega V\left[\frac{C^2-C^2}{4C}\right] = 0 \tag{5.21}$$

Bridge Current with Fault in One Section

Faulty elements in left top section (*m*):

C1(m)=C+f(*m*)·dC

C2=C3=C4=C

$$IH(m) = j\omega V\left[\frac{C\cdot(C+f(m)\cdot dC)-C^2}{3C+f(m)\cdot dC}\right] = j\omega V\left[\frac{C\cdot f(m)\cdot dC}{3C+f(m)\cdot dC}\right] \tag{5.22}$$

$$IH(m) = j\omega CV\left[\frac{f(m)}{3p+f(m)}\right] \tag{5.23}$$

Equation (5.23) shows that the bridge current magnitude increases as the number of shorted or faulted elements increases, but the phase angle stays the same since *f(m)* and 3*p* are scalars. Unbalance protection uses the bridge current and compensates for any system changes or inherent unbalance as discussed in Section 3.4.1.

Faulty elements in right top section (*m*):

C2= C+f(*m*)·dC

C1=C3=C4=C

$$IH(m) = j\omega V\left[\frac{C^2-(C+f(m)\cdot dC)\cdot C}{3C+f(m)\cdot dC}\right] = j\omega V\left[\frac{-C\cdot f(m)\cdot dC}{3C+f(m)\cdot dC}\right] \tag{5.24}$$

$$IH(m) = j\omega CV\left[\frac{-f(m)}{3p+f(m)}\right] \tag{5.25}$$

Equation (5.25) shows that the bridge current magnitude increase as the number of faulted elements increase but the phase angle stays the same. Note that magnitude increase is same as in (5.23) but phase angle is 180° out of phase.

Faulty element in left bottom section (m):

C3=C+ f(m)·dC

C1=C2=C4=C

$$IH(m) = j\omega V\left[\frac{C^2-(C+f(m)\cdot dC)\cdot C}{3C+f(m)\cdot dC}\right] = j\omega V\left[\frac{-C\cdot f(m)\cdot dC}{3C+f(m)\cdot dC}\right] \quad (5.26)$$

$$IH(m) = j\omega CV\left[\frac{-f(m)}{3p+f(m)}\right] \quad (5.27)$$

Equation (5.27) shows that the bridge current response for left bottom section is same as in right bottom section.

Faulty element in right bottom section (m):

C4= C+f(m)·dC

C1=C2=C3=C

$$IH(m) = j\omega V\left[\frac{C\cdot(C+f(m)\cdot dC)-C^2}{3C+f(m)\cdot dC}\right] = j\omega V\left[\frac{C\cdot f(m)\cdot dC}{3C+f(m)\cdot dC}\right] \quad (5.28)$$

$$IH(m) = j\omega CV\left[\frac{f(m)}{3p+f(m)}\right] \quad (5.29)$$

Equation (5.29) shows that the bridge current response for right bottom section is same as in left top section.

Bridge Current with Fault in Two Sections

Faulty element in left top (m) and right top (n) sections:

C1= C+f(m)·dC

C2= C+f(n)·dC

C3=C4=C

$$IH(m,n) = j\omega V\left[\frac{(C+f(m)\cdot dC)\cdot C-(C+f(n)\cdot dC)\cdot C}{(2C+(f(m)+f(n))\cdot dC)}\right] \quad (5.30)$$

$$IH(m,n) = j\omega CV\left[\frac{f(m)-f(n)}{2p+(f(m)+f(n))}\right] \quad (5.31)$$

Equation (5.31) shows that for a symmetric failure i.e., same number faulted elements in left top and right top section, the bridge current magnitude is zeroed out, resulting in a symmetric cancel failure. For an asymmetric failure the number of faulted elements, *f(m)* and *f(n)*, are not the same, the bridge current magnitude decreases, but does not go to zero. Note that the phase angle changes if number of faulted elements in right top section is larger than the number of faulted elements in left top section.

Faulty element in left top (*m*) and left bottom (*n*) section:

C1= C+f(*m*)·dC

C3= C+f(*n*)·dC

C2=C4=C

$$IH(m,n) = j\omega V\left[\frac{(C+f(m)\cdot dC)\cdot C-C\cdot(C+f(n)\cdot dC)}{(2C+(f(m)+f(n))\cdot dC)}\right] \quad (5.32)$$

$$IH(m,n) = j\omega CV\left[\frac{f(m)-f(n)}{2p+(f(m)+f(n))}\right] \quad (5.33)$$

Equation (5.33) is same as (5.31) so the response for symmetric and asymmetric failures will be the same as discussed above.

Faulty element in left top (*m*) and right bottom (*n*) section:

C1= C+f(*m*)·dC

C4= C+f(*n*)·dC

C2=C3=C

$$IH(m,n) = j\omega V\left[\frac{(C+f(m)\cdot dC)(C+f(n)\cdot dC)-C^2}{(2C+(f(m)+f(n))\cdot dC)}\right] \quad (5.34)$$

$$IH(m,n) = j\omega V\left[\frac{(C\cdot(C+f(n)\cdot dC)+f(m)\cdot dC\cdot(C+f(n)\cdot dC))-C^2}{(2C+(f(m)+f(n))\cdot dC)}\right] \quad (5.35)$$

$$IH(m,n) = j\omega V\left[\frac{((C^2+f(n)\cdot C\cdot dC)+(f(m)\cdot C\cdot dC+f(m)\cdot f(n)\cdot dC^2))-C^2}{(2C+(f(m)+f(n))\cdot dC)}\right] \quad (5.36)$$

$$IH(m,n) = j\omega V\left[\frac{f(m)\cdot f(n)\cdot dC^2+(f(m)+f(n))\cdot C\cdot dC}{(2C+(f(m)+f(n))\cdot dC)}\right] \quad (5.37)$$

$$IH(m,n) = j\omega CV\left[\frac{\frac{f(m)\cdot f(n)}{p}+(f(m)+f(n))}{(2p+(f(m)+f(n)))}\right] \quad (5.38)$$

Equation (5.38) shows that for symmetric and asymmetric failures in the left top and right bottom section, the bridge current magnitude increases, so this is not a canceling failure.

Faulty element in right top (m) and left bottom (n) section:

C2=C+ f(m)·dC

C3=C+ f(n)·dC

C1=C2=C

$$IH(m,n) = j\omega CV\left[\frac{-(f(m)f(n)p+(f(m)+f(n)))}{(2p+(f(m)+f(n)))}\right] \quad (5.39)$$

Equation (5.39) shows that for symmetric and asymmetric failures in the right top and left bottom section, the bridge current magnitude increases, but the phase angle is 180° out of phase with the earlier result.

Phase current unbalance protection is used to protect against element or unit failures for single-WYE grounded H-bridge bank with a CT measuring the bridge current. Equation (3.4) uses the bridge current and compensates for the inherent unbalance within the bank. Failures in different parts of the bank are extremely unlikely to occur at precisely the same time. Therefore by monitoring the unbalance phasor magnitude and the unbalance phasor angle before and after a disturbance using an algorithm similar to the one used to cancel inherent unbalance we can detect canceling failures.

For a symmetric canceling failure in left top section followed by a fault in right top section, the unbalance magnitude decreases to zero and the unbalance angle changes from 0° to having no reference for determining an angle as magnitude is zeroed.

For a symmetric cancelling failure in right top section followed by a fault in left top section, the unbalance magnitude decreases to zero and the unbalance angle changes from 180° to no reference as magnitude is zeroed.

For an asymmetric canceling failure in left top section (*m*) followed by a fault in right top section (*n*) with *m* less than *n*, the unbalance magnitude increases and the unbalance angle changes from 0° to 180°.

For an asymmetric canceling failure in right top section (*n*) followed by a fault in left top section (*m*) with *m* less than *n*, the unbalance magnitude decreases, and the unbalance angle stays at 180°.

For an asymmetric canceling failure in left top section (*m*) followed by a fault in right top section (*n*) with *m* more than *n*, the unbalance magnitude decreases, and the unbalance angle stays at 0°.

For an asymmetric canceling failure in right top section (*n*) followed by a fault in left top section (*m*) with *m* less than *n*, the unbalance magnitude increases, and the unbalance angle changes from 180° to 0°.

We can see that for symmetric canceling failures in left top section followed by failures in the right top section, just checking the decrease in unbalance magnitude is sufficient, but for asymmetric canceling failures it is not, as there are cases where unbalance magnitude increases. We can use the change in unbalance phase angle for these cases.

Symmetric and asymmetric canceling failures in left top section followed by left bottom section will be same as left top section followed by right top section.

For symmetric and asymmetric canceling failures in left top section followed by right bottom section or vice versa, the unbalance magnitude increases, and the unbalance angle remains unchanged at 0°.

For symmetric and asymmetric canceling failures in left top section followed by right bottom section or vice versa, the unbalance magnitude increases, and the unbalance angle remains unchanged at 180°.

5.2 Canceling Failure Detection Logic

Figure 5-2 shows unbalance disturbance detector logic. The top part of the logic subtracts the present unbalance phasor value from its *n* samples old, buffered value and the magnitude of that is compared to a pickup value (PU1). The output is a pulse (60KIX1DDR) that is asserted whenever a disturbance happens. The rising edge of 60KIX1DDR latches asserting 60KIX1DD and resetting the latch *n* samples after 60KIX1DDR deasserts. 60KIX1DH is the rising edge and 60KIX1DL is the falling edge of 60KIX1DD.

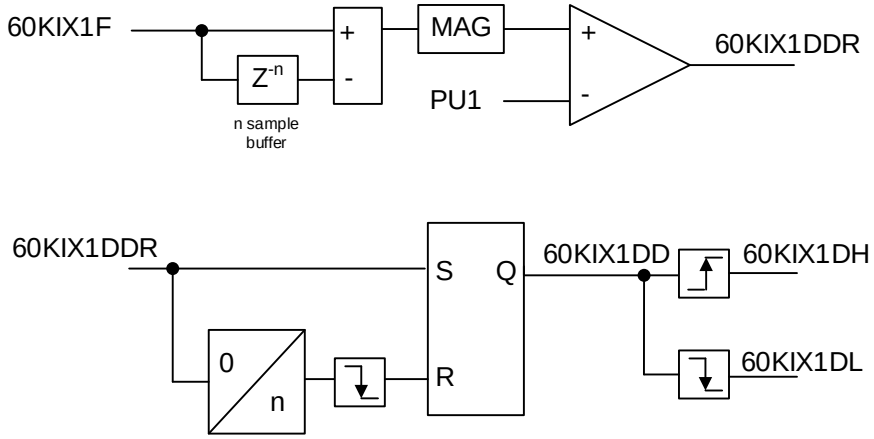


Figure 5-2. Unbalance Disturbance Detector Logic

The number of samples for the buffer should be based on the phasor estimation settling delay (and fuse blowing time if the bank is fused). For this research, the buffer is fixed at 16 which is two power system cycles. The PU1 value needs to be chosen at one half of the unbalance magnitude seen for one element failure. Note that if the failure happens within the buffer time, the logic won't be able to detect the disturbance.

Figure 5-3 shows the canceling failure unbalance magnitude logic. The *n* samples old, buffered unbalance current magnitude and present unbalance current magnitude are captured on the rising and falling edges of the unbalance disturbance detector.

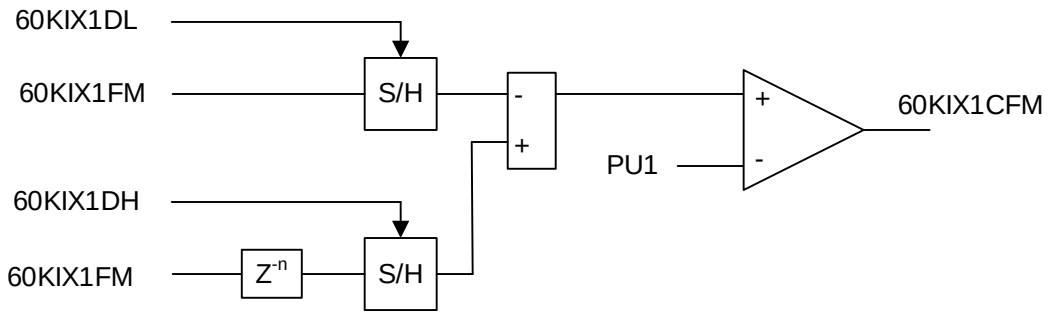


Figure 5-3. Canceling Failure Unbalance Magnitude Logic

The falling edge captured unbalance magnitude is subtracted from the rising edge captured unbalance magnitude and it is checked to see if it is above PU1 value. If that occurs, then a canceling failure is detected. Basically the logic is checking for a decrease in unbalance current magnitude.

Figure 5-4 shows the canceling failure unbalance angle logic. The unbalance phase angles captured at the falling and rising edge are checked to see if there is a 180° change in the fault location angle before and after the disturbance. For security, a ±15-degree blinder is applied to exclude unbalances not resulting from capacitor failures, such as instrument transformer errors. If a change is detected, then there is an asymmetric canceling failure with increased unbalance magnitude and 60KIX1CFA asserts. Since unbalance angle is 180°off for fused banks as discussed in Chapter 3, the proposed logic can be applied to fused bank too.

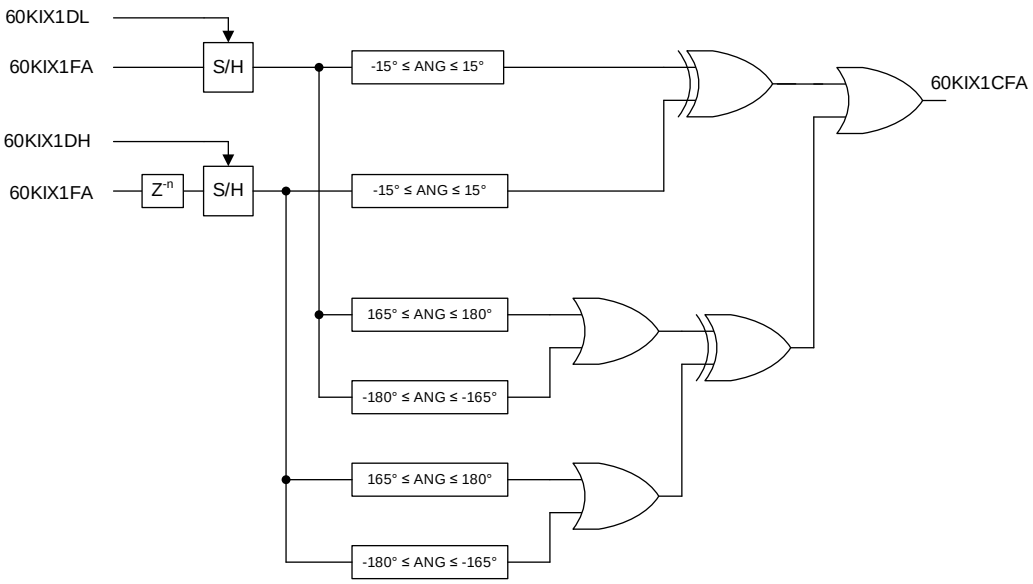


Figure 5-4. Canceling Failure Unbalance Angle Logic

Figure 5-5 shows the canceling failure unbalance detection logic. Once the canceling failure is detected through either magnitude or angle changes, it is latched and 60KIX1CF asserts. This information can be used by the protection engineer to either trip the bank immediately for rebalancing or do a scheduled maintenance by issuing a KSET command. The latch is reset when the KSET is issued.

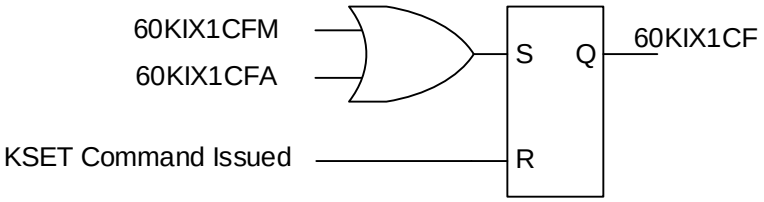


Figure 5-5. Canceling Failure Detector

The proposed algorithm is economical and practical as it uses the unbalance magnitude and phase angle which are already available as part of unbalance protection. The algorithm doesn't need additional measurement devices but require additional computation.

5.3 Sensitivity

The sensitivity of the proposed canceling failure detector depends on the sensitivity of the existing unbalance protection. Usually the bank is designed such a way that the unbalance protection can detect a single element failure. The higher the element or unit rating, the better the sensitivity. Also increasing the number of units or elements decreases the sensitivity.

5.4 Summary

This chapter presented a mathematical analysis of symmetric and asymmetric canceling failures and introduced the proposed solution that enhances the capacitor bank unbalance protection by detecting symmetric and asymmetric canceling failures. Conventional unbalance protection will not be able to detect these failures even when the bank is unbalanced, resulting in continuous overvoltage on healthy elements which can lead to a cascading failure. The proposed method resolves this problem.

Chapter 6 Simulation Results

6.1 Simulation setup

To demonstrate the performance of canceling failure detection, the power system shown in Figure 6.1 was modeled using a RTDS. The power system model consists of a 345 kV source S1, a 100 km transmission line L1, a 345 kV/115 kV step down transformer T1, a shunt capacitor bank C1 connected to bus B2 through a circuit breaker CB1 and a load LD1 connected to bus B3.

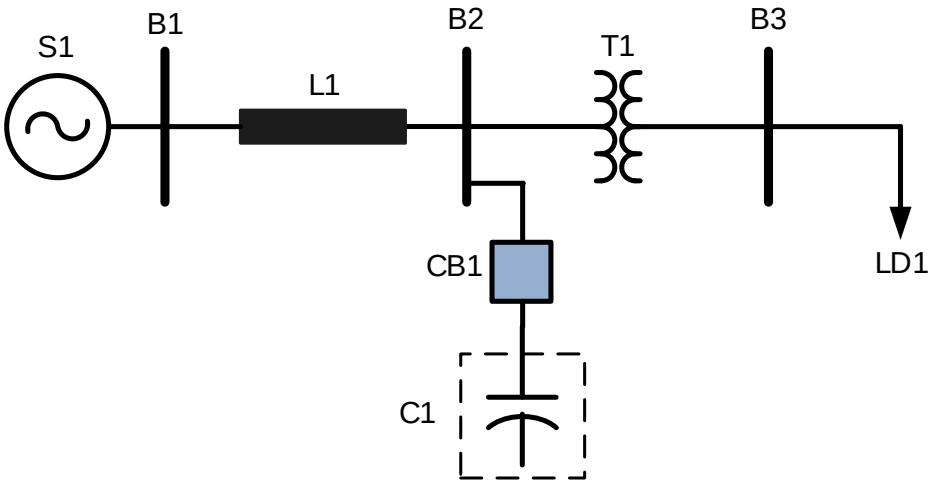


Figure 6-1. Power System Modeled in RTDS to Test Canceling Failure Detection Scheme

Figure 6-2 shows a per-phase representation of a 345 kV, 130.9 MVAr single-WYE grounded capacitor bank connected as an H-bridge. Not shown in the figure is a 0.1 H series reactor connected in series to the capacitor bank for inrush and outrush transient current suppression.

The bank is fuseless and consists of 264 capacitor units. Each phase of the bank has eight parallel strings with 11 units connected in series, for a total of 88 units per-phase. Each capacitor unit consists of a single string of six elements in series. The capacitor unit is rated at 9.96 kV and 600 kVAr.

The simulated bank can be configured to have a standing unbalance to account for manufacturing tolerances or temperature variance.

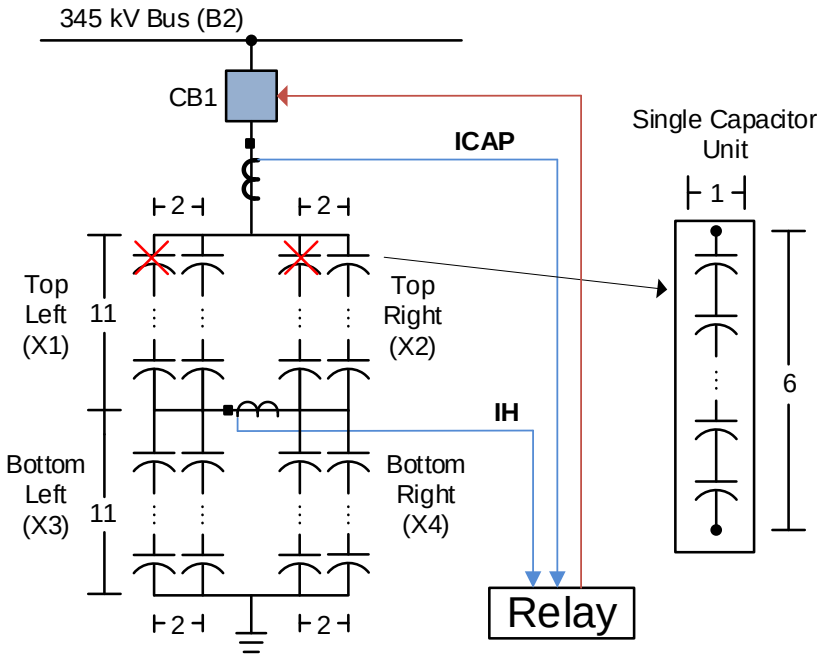


Figure 6-2. Single-WYE Grounded Capacitor Bank Connected as an H-bridge

A current transformer (CT) model with 1000/5 CT ratio measures the bank phase currents (ICAP*p*) and a CT model with 25/5 CT ratio measures the bridge phase currents (IH*p*).

From the measured bank and bridge phase currents, a digital relay model provides conventional phase current unbalance protection (60P) for the capacitor bank. The relay trips breaker CB1 if the phase current unbalance protection magnitude exceeds a threshold that represents 110% of the capacitor unit rating. During runtime, the phase unbalance protection can compensate for inherent unbalance within the bank using a push button.

Internal faults are simulated by shorting one or five or six elements in a unit. Fault initiation control logic can simulate internal faults in any phase or any of four sections of each phase of the bank.

The proposed canceling failure detection logic is modeled in the simulation. The logic is per-phase since the applied unbalance protection method is per-phase and uses phase current unbalance magnitude and phase angle from the per-phase unbalance protection logic.

The performance of the model is evaluated for the following fault scenarios:

- Internal faults in the same phase and same section of the H-bridge bank
- Internal faults, both symmetric and asymmetric in the same phase but different sections of the H-bridge bank

6.2 Capacitor bank energization

The capacitor bank is energized by manually closing circuit breaker CB1 with a 10% inherent unbalance in Phase A top left section of the bank. Figure 6-3 shows a simulation capture for this case. Graph 1 from the top shows bank phase currents (ICAPA, ICAPB and ICAPC) measured by the phase CT model in Amperes secondary. Graph 2 shows bridge currents (IHA, IHB and IHC) measured by the bridge CT model in Amperes secondary. Graph 3 shows Phase A current unbalance protection magnitude from the digital relay model in Amperes secondary. Graph 4 shows Phase A current unbalance angle in degrees referenced to Phase A bank current from the digital relay model.

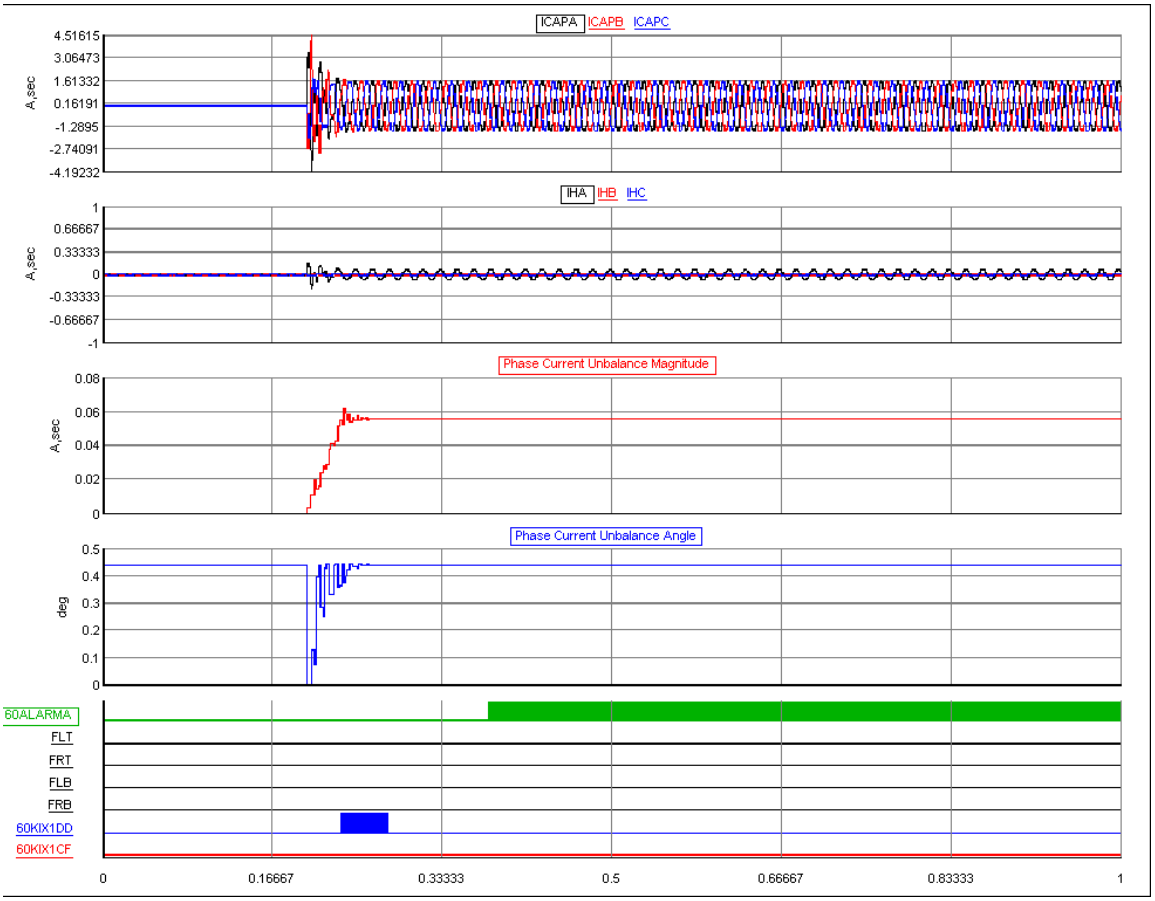


Figure 6-3 Capacitor Bank Energization

Graph 5 shows digital outputs from Phase A capacitor unbalance protection (60ALARMA), fault control (FLT, FRT, FLB, FRB) and Phase A canceling failure detection logic (60KIX1DD, 60KIX1CF) from the digital relay model. 60ALARMA asserts 10 cycles after Phase A current unbalance protection magnitude exceeds 0.02 Amperes secondary. FLT is asserted when an internal fault is simulated in the left top section of the bank. Similarly FRT for right top section, FLB for left bottom section, and FRB for right bottom section. 60KIX1DD is asserted when the disturbance is detected in Phase A. 60KIX1CF is asserted when a canceling failure is detected in Phase A.

Figure 6-3 shows that the bank is energized at 0.2 s. Since the bank is energized with 10% inherent unbalance on Phase A, we can see there is a standing phase current unbalance magnitude 0.055 Amperes secondary and 60ALARMA asserted. Also phase current unbalance angle is close to zero degrees confirming that the unbalance is in Phase A top left or bottom right section. 60KIX1DD asserted as there is a change in

Phase A current unbalance magnitude due to the prescence of inherent unbalance in the bank. We can see 60KIX1CF is secure and did not assert as this is not a canceling failure.

6.3 Compensating inherent unbalance to improve security and sensitivity

The capacitor bank is energized with 10% inherent unbalance in Phase A top left section of the bank. To improve the security and sensitivity of phase current unbalance protection this inherent unbalance needs to be compensated by the relay. Unbalance protective relays are often provided with a manual command or a push button on the front panel or an auto option to reset the inherent unbalance. Figure 6-4 shows that the inherent unbalance is compensated by pressing a push button at 0.2 s. We can see that the standing phase current unbalance magnitude 0.055 Amperes secondary is zeroed out and 60ALARMA is deasserted. Since unbalance magnitude is zeroed out at 0.2 s, current unbalance angle has no reference and it oscillates. 60KIX1DD asserted as there is a change in phase current unbalance magnitude. We can see 60KIX1CF is secure and did not assert as this is not a canceling failure.

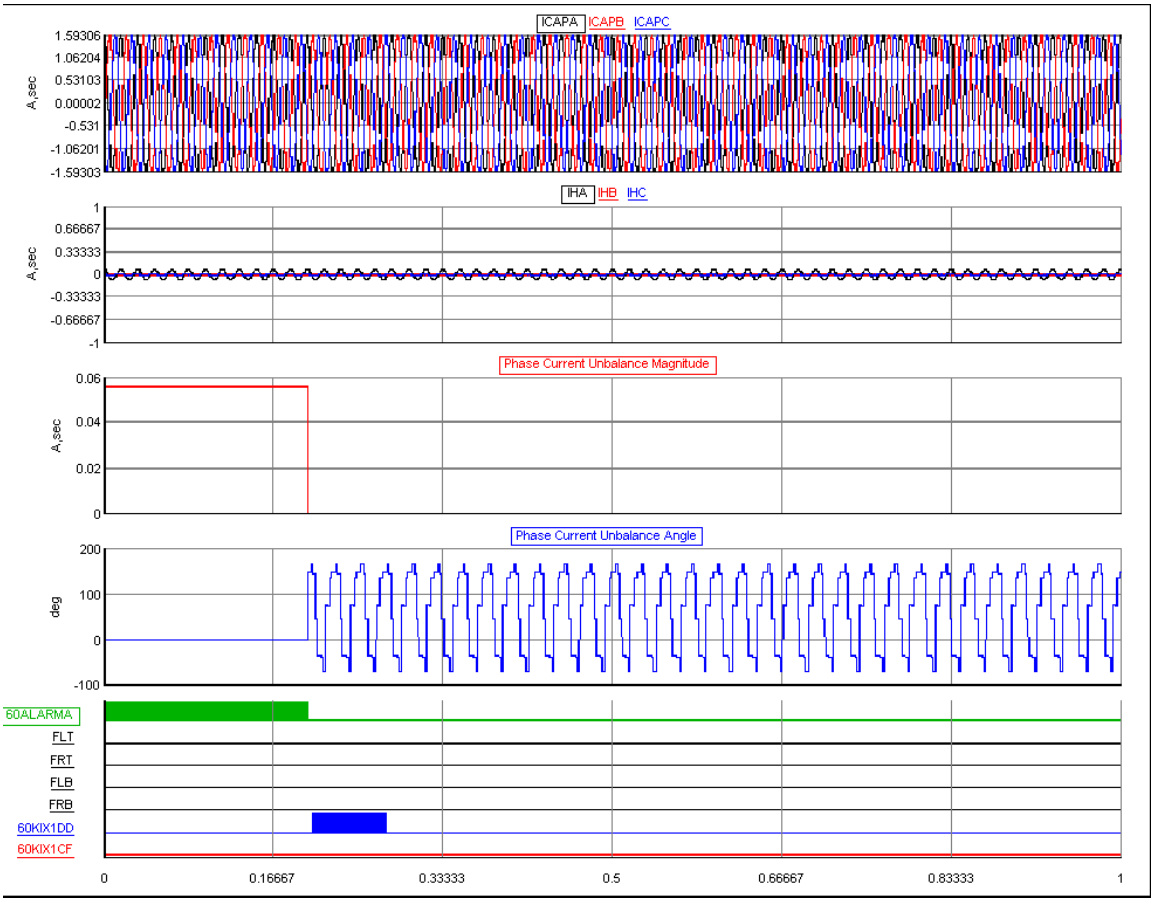


Figure 6-4 Compensating Inherent Unbalance to Improve Phase Current Unbalance Protection Security and Sensitivity

6.4 Internal fault in the same phase and same section of the H-bridge bank

6.4.1 Internal fault - left top section (one element) of the H-bridge bank

After compensating the inherent unbalance, an internal fault is simulated by shorting one element in a unit in Phase A and the left top section of the healthy bank. Figure 6-5 shows that FLT is asserted at 0.2 s indicating fault is initiated in left top section of the bank. The fault results in an unbalance current magnitude of 0.084 Amperes secondary and an unbalance current angle close to 0 degrees. Graph 5 in Figure 6-5 shows that the unbalance protection alarm (60ALARMA) asserted after 10 cycles as the unbalance current magnitude is more than 0.02 Amperes secondary for more than 10 cycles.

60KIX1DD asserted as there is a change in phase current unbalance magnitude. We can see 60KIX1CF is secure and did not assert as this is not a canceling failure.

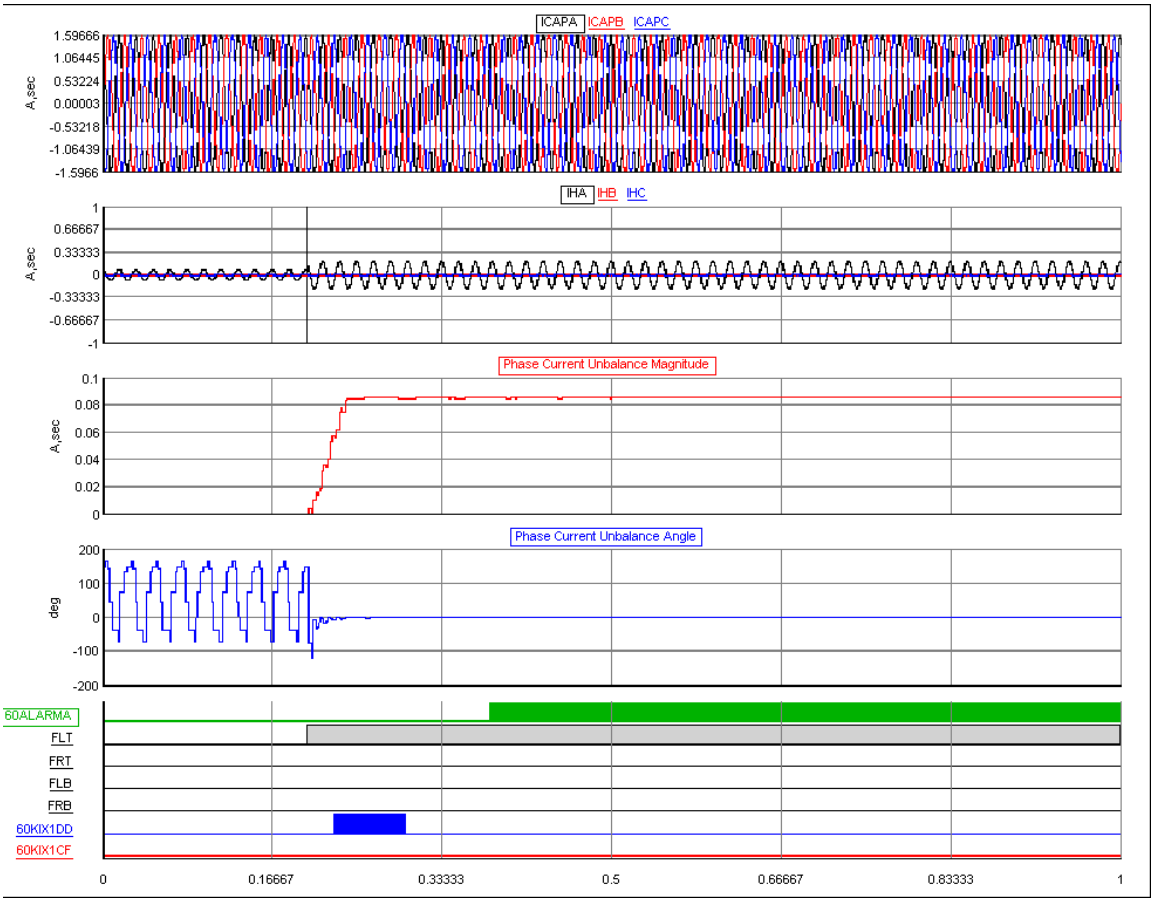


Figure 6-5. Internal Fault in the Left Top Section of the H-Bridge Bank

6.4.2 Internal fault - right top section (one element) of the H-bridge bank

An internal fault is simulated by shorting one element in a unit in Phase A and the right top section of the healthy bank. Figure 6-6 shows that FRT is asserted at 0.2 s indicating fault is initiated in right top section of the bank. The fault results in an unbalance current magnitude of 0.084 Amperes secondary and an unbalance current angle close to 180 degrees. 60ALARMA asserted after 10 cycles as the unbalance current magnitude is more than 0.02 Amperes secondary for 10 cycles. 60KIX1DD

asserted as there is a change in phase current unbalance magnitude. We can see 60KIX1CF is secure and did not assert as this is not a canceling failure.

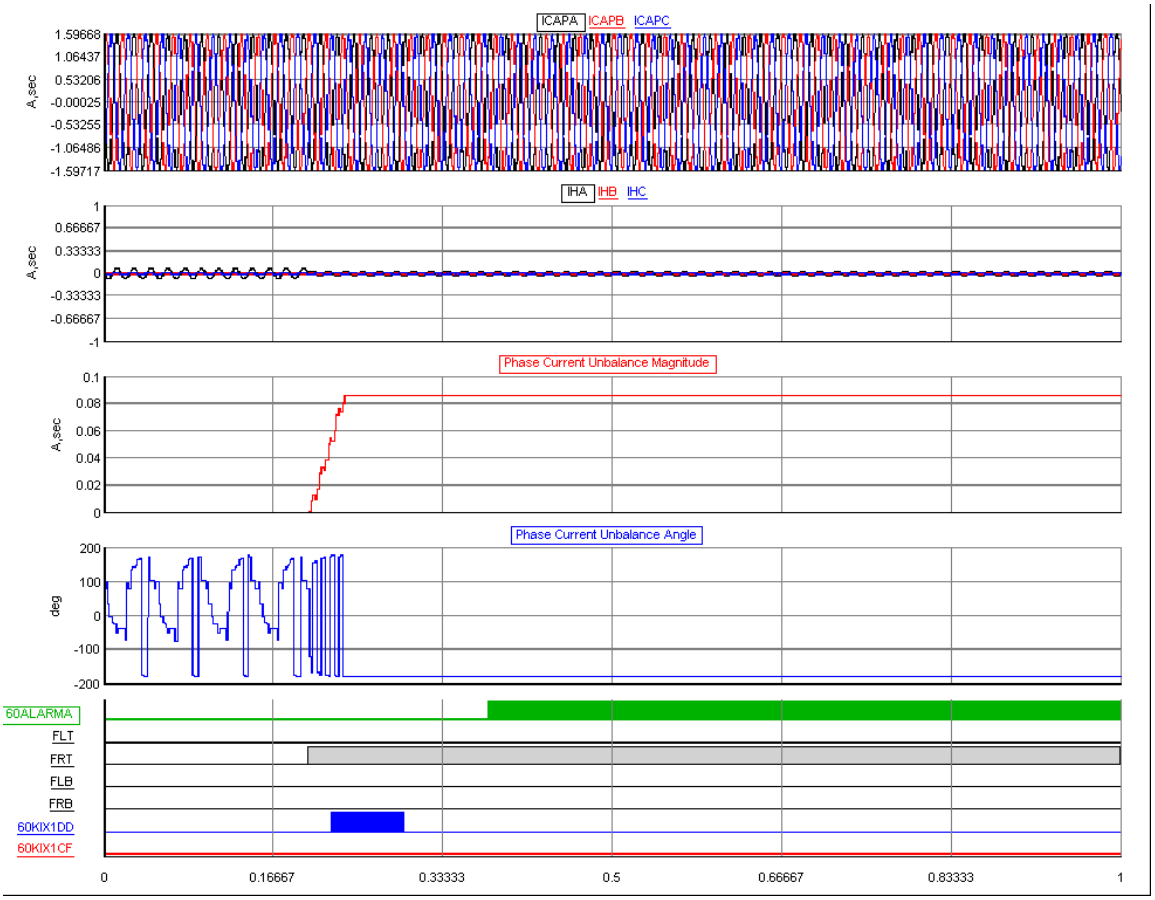


Figure 6-6. Internal Fault in the Right Top Section of the H-Bridge Bank

6.4.3 Internal fault - left bottom section (one element) of the H-bridge bank

An internal fault is simulated by shorting one element in a unit in Phase A and the left bottom section of the healthy bank. Figure 6-7 shows that FLB is asserted at 0.2 s indicating fault is initiated in left bottom section of the bank. The fault results in an unbalance current magnitude of 0.084 Amperes secondary and an unbalance current angle close to 180 degrees. 60ALARMA asserted after 10 cycles as the unbalance current magnitude is more than 0.02 Amperes secondary for 10 cycles. 60KIX1DD

asserted as there is a change in phase current unbalance magnitude. We can see 60KIX1CF is secure and did not assert as this is not a canceling failure.

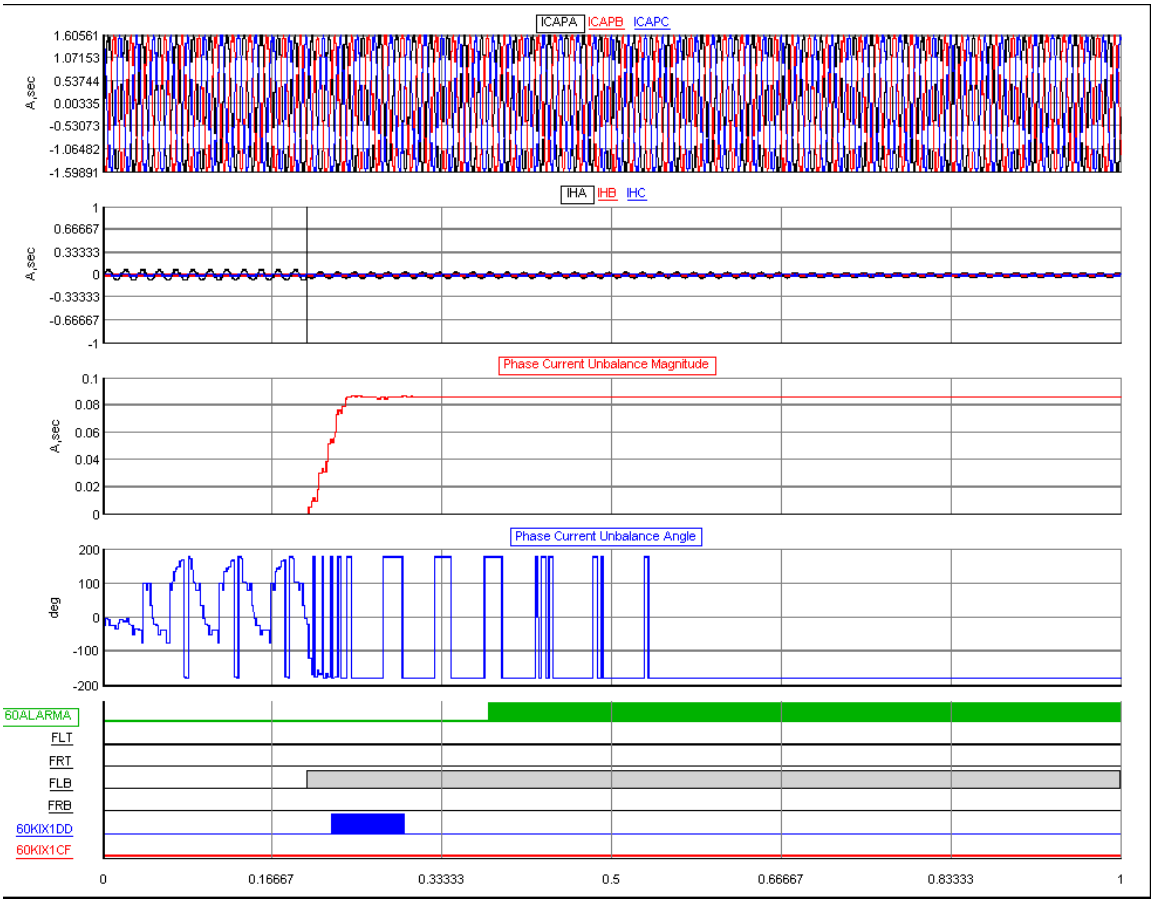


Figure 6-7. Internal Fault in the Left Bottom Section of the H-Bridge Bank

6.4.4 Internal fault - right bottom section (one element) of the H-bridge bank

An internal fault is simulated by shorting one element in a unit in Phase A and the right bottom section of the healthy bank. Figure 6-8 shows that FRB is asserted at 0.2 s indicating fault is initiated in right bottom section of the bank. The fault results in an unbalance current magnitude of 0.084 Amperes secondary and an unbalance current angle close to 0 degrees. 60ALARMA asserted after 10 cycles as the unbalance current magnitude is more than 0.02 Amperes secondary for 10 cycles. 60KIX1DD asserted as

there is a change in phase current unbalance magnitude. We can see 60KIX1CF is secure and did not assert as this is not a canceling failure.

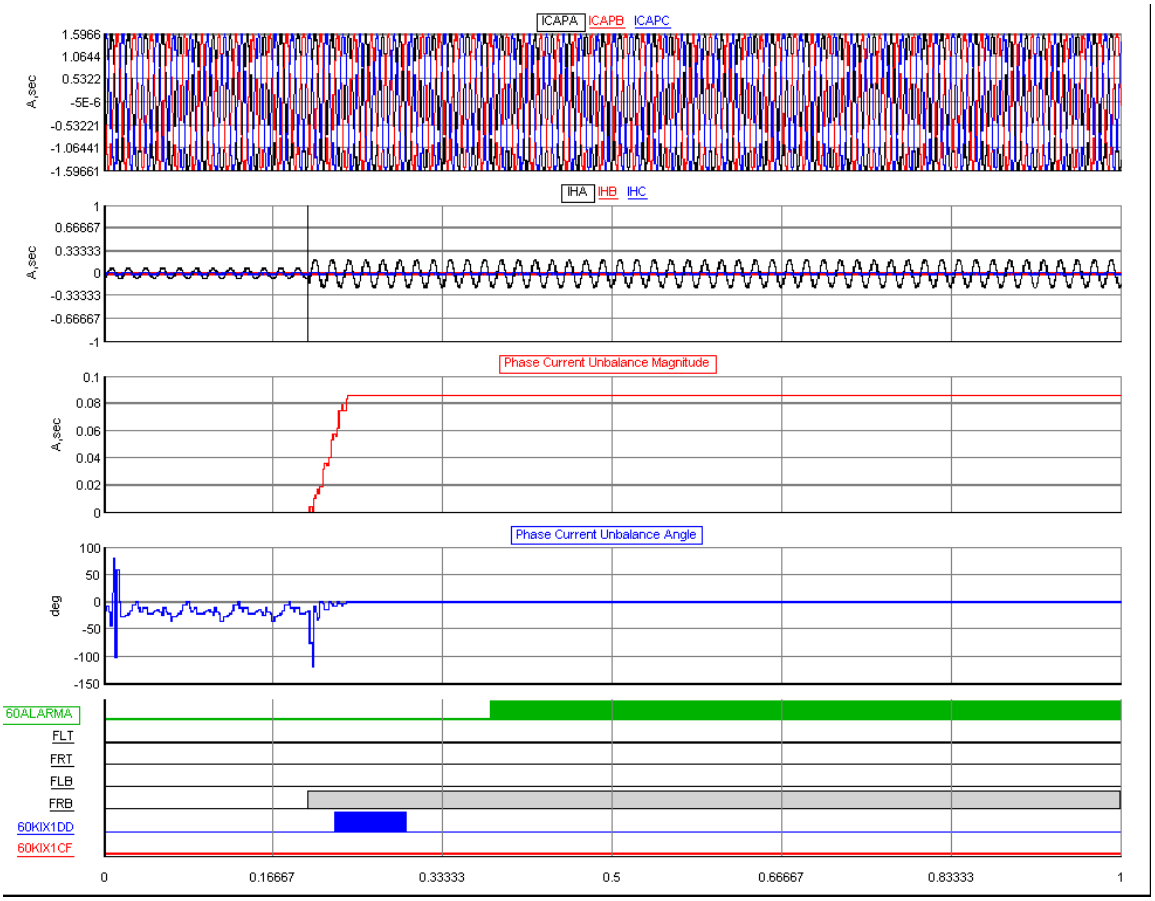


Figure 6-8. Internal Fault in the Right Bottom Section of the H-Bridge Bank

6.4.5 Internal fault - left top section (one element) followed by another in the left top section (four elements) of the H-bridge bank

An internal fault is simulated by shorting one element in a unit in Phase A and the left top section of the healthy bank followed by shorting five more elements in the same unit. Figure 6-9 shows that FLT is asserted at 0.2 s indicating fault is initiated in left top section of the bank. The fault results in an unbalance current magnitude of 0.084 Amperes secondary and an unbalance current angle close to 0 degrees. Then 0.5 s later four more elements are shorted in the same unit which results in an increase in unbalance current magnitude to 0.44 Amperes secondary and unbalance current angle still close to 0 degrees. 60ALARMA asserted after 10 cycles of the first internal fault and stays

asserted for the second fault as the unbalance current magnitude is more than 0.02 Amperes secondary. 60KIX1DD asserted and deasserted twice as there is a change in phase current unbalance magnitude for both the first and second faults. Canceling failure detection logic evaluates on the falling edge of the second 60KIX1DD assertion. Since the unbalance current magnitude increased with no change in unbalance current angle, this is not a canceling failure and we can see 60KIX1CF is secure and did not assert.

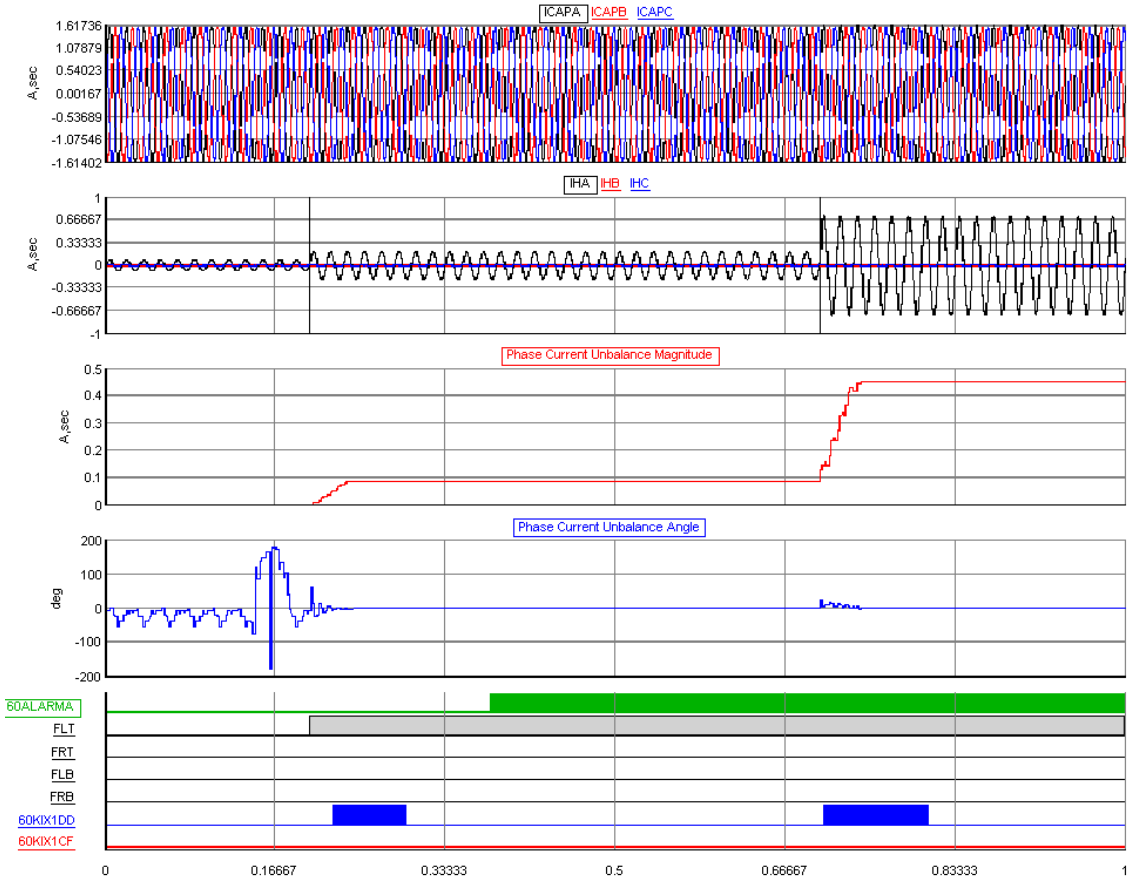


Figure 6-9. Internal Fault in the Left Top section (One Element) Followed by Another in the Left Top section (Five Elements) of the H-Bridge Bank

6.5 Internal faults in the same phase but different sections of the H-bridge bank

6.5.1 Symmetric internal fault - left top section (one element) followed by right top section (one element) of the H-bridge bank

An internal fault is simulated by shorting one element in a unit in the left top section at 0.2 s and after 0.5 s a symmetric internal fault is simulated by shorting one element in a unit in the right top section. Figure 6-10 shows Phase A current unbalance magnitude of 0.084 Amperes secondary for the first fault followed by zeroing out of the unbalance magnitude due to the canceling effect of the second fault. The Phase A current unbalance angle is 0 degrees for the first fault but since magnitude is zeroed out for second fault, the current unbalance angle has no reference and it oscillates as it did prior to the first fault. 60ALARMA asserted after 10 cycles of the first internal fault but deasserted after the second fault occurred as the unbalance current magnitude is zeroed out. 60KIX1DD asserted and deasserted twice as there is a change in phase current unbalance magnitude for the first and second faults. Since the unbalance current magnitude decreased on the falling edge of the second 60KIX1DD assertion, this is a canceling failure and we can see 60KIX1CF asserted correctly.

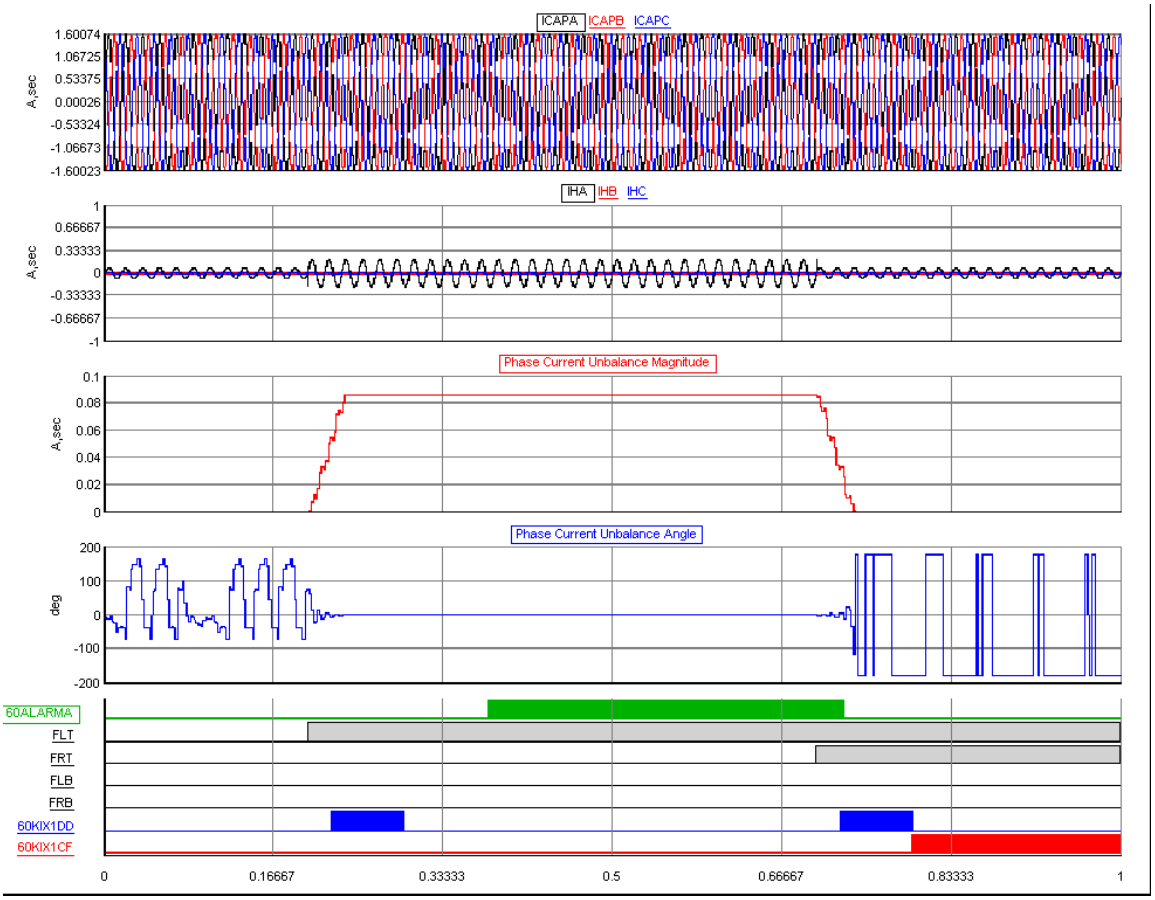


Figure 6-10. Symmetric Internal Fault in the Left Top Section (One Element) Followed by Another in the Right Top Section (One Element) of the H-Bridge Bank

6.5.2 Symmetric internal fault - right top section (one element) followed by left top section (one element) of the H-bridge bank

An internal fault is simulated by shorting one element in a unit in the right top section at 0.2 s and after 0.5 s a symmetric internal fault is simulated by shorting one element in a unit in the left top section. Figure 6-11 shows Phase A current unbalance magnitude of 0.084 Amperes secondary due to the first fault followed by zeroing out the current unbalance after the second fault occured. Phase A current unbalance angle is 180 degrees for the first fault but since magnitude is zeroed out for second fault, the current unbalance angle has no reference and it oscillates. 60ALARMA asserted after 10 cycles

of the first internal fault but deasserted following the second fault as the unbalance current magnitude is zeroed out. 60KIX1DD asserted and deasserted twice as there is a change in phase current unbalance magnitude for the first and second faults. Since the unbalance current magnitude decreased on the falling edge of the second 60KIX1DD assertion, this is a canceling failure and we can see 60KIX1CF asserted correctly.

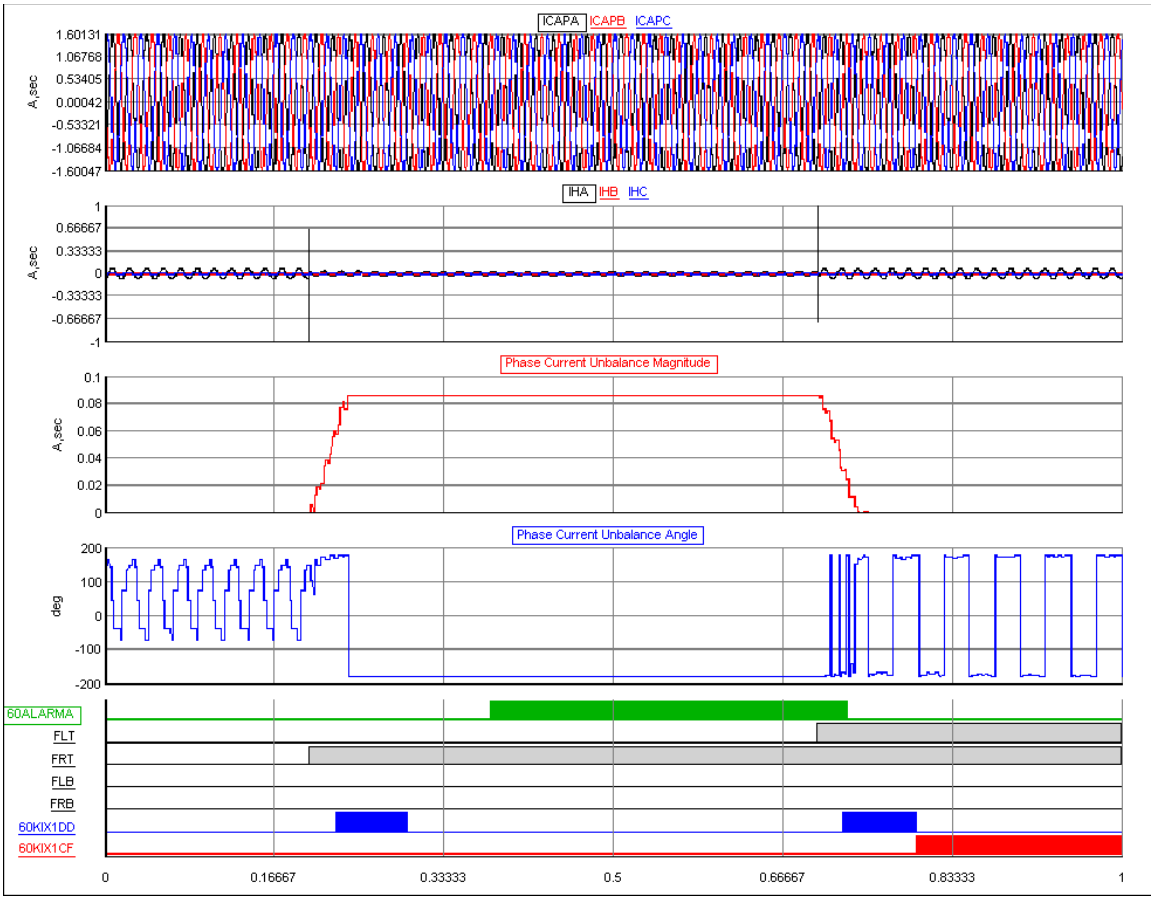


Figure 6-11. Symmetric Internal Fault in the Right Top Section (One Element) Followed by Another in the Left Top Section (One Element) of the H-Bridge Bank

6.5.3 Asymmetric internal fault - left top section (one element) followed by right top section (five elements) of the H-bridge bank

An internal fault is simulated by shorting one element in a unit in the left top section at 0.2 s and after 0.5 s an asymmetric internal fault is simulated by shorting five

elements in a unit in the right top section. Figure 6-12 shows Phase A current unbalance magnitude of 0.084 Amperes secondary for the first fault and increases to 0.37 Amperes secondary after the second fault. The Phase A current unbalance angle is 0 degrees for the first fault and changes to 180 degrees due to the second fault. 60ALARMA asserted after 10 cycles of the first internal fault and stays asserted for the second fault as the unbalance current magnitude is greater than 0.02 Amperes secondary. 60KIX1DD asserted and deasserted twice as there is a change in phase current unbalance magnitude for the first and second faults. Since the unbalance current magnitude increased on the falling edge of the second 60KIX1DD assertion and the unbalance current angle changes from 0 to 180 degrees, this is a canceling failure and we can see 60KIX1CF asserted correctly.

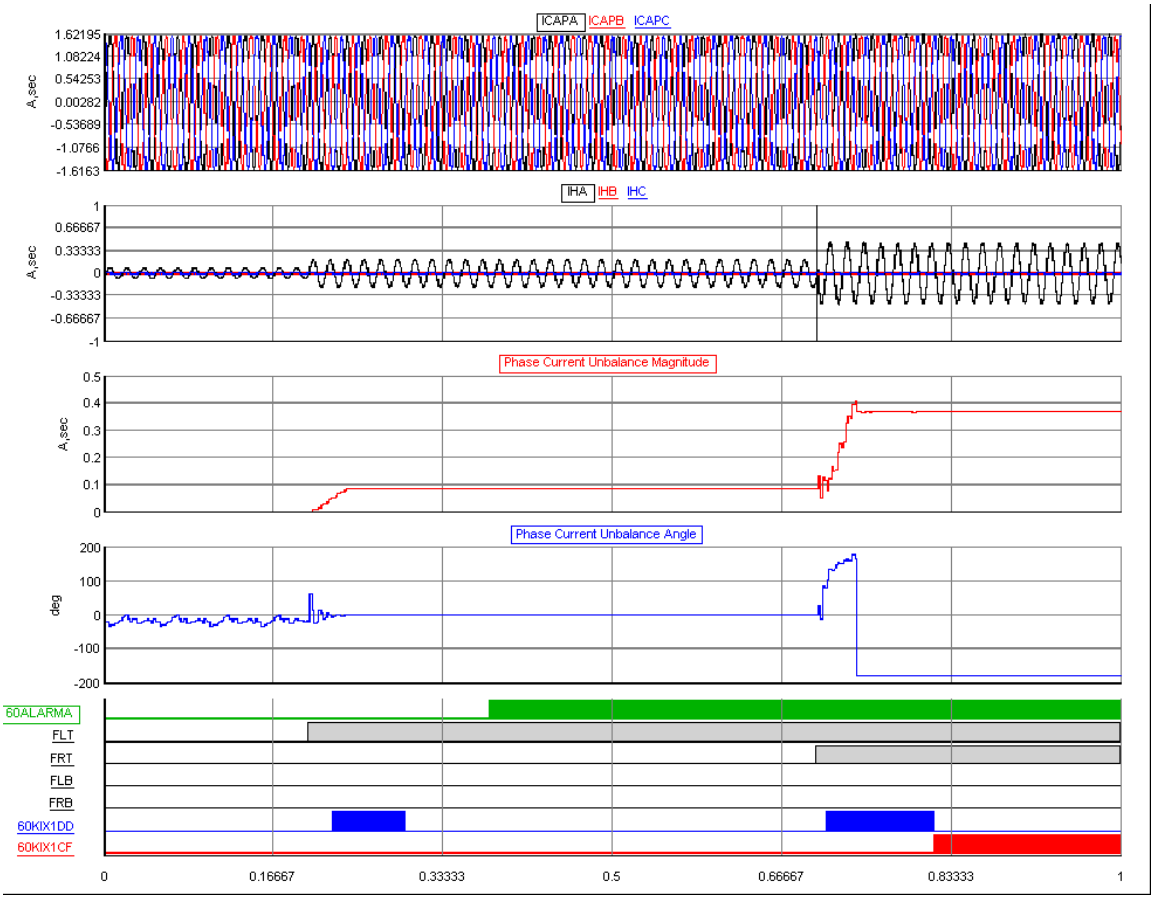


Figure 6-12. Asymmetric Internal Fault in the Left Top Section (One Element) Followed by Another in the Right Top section (Five Elements) of the H-Bridge Bank

6.5.4 Asymmetric internal fault - right top section (five elements) followed by left top section (one element) of the H-bridge bank

An internal fault is simulated by shorting five elements in a unit in the right top section at 0.2 s and after 0.5 s an asymmetric internal fault is simulated by shorting one element in a unit in the left top section. Figure 6-13 shows Phase A current unbalance magnitude of 0.45 Amperes secondary for the first fault and decreases to 0.37 Amperes secondary for the second fault. Phase A current unbalance angle is 180 degrees for the first fault and stays same for the second fault. 60ALARMA asserted after 10 cycles of the first internal fault and stays asserted for the second fault as the unbalance current magnitude is

greater than 0.02 Amperes secondary. 60KIX1DD asserted and deasserted twice as there is a change in phase current unbalance magnitude for the first and second faults. Since the unbalance current magnitude decreased on the falling edge of the second 60KIX1DD assertion and the unbalance current angle doesn't change, this is a canceling failure and we can see 60KIX1CF asserted correctly.

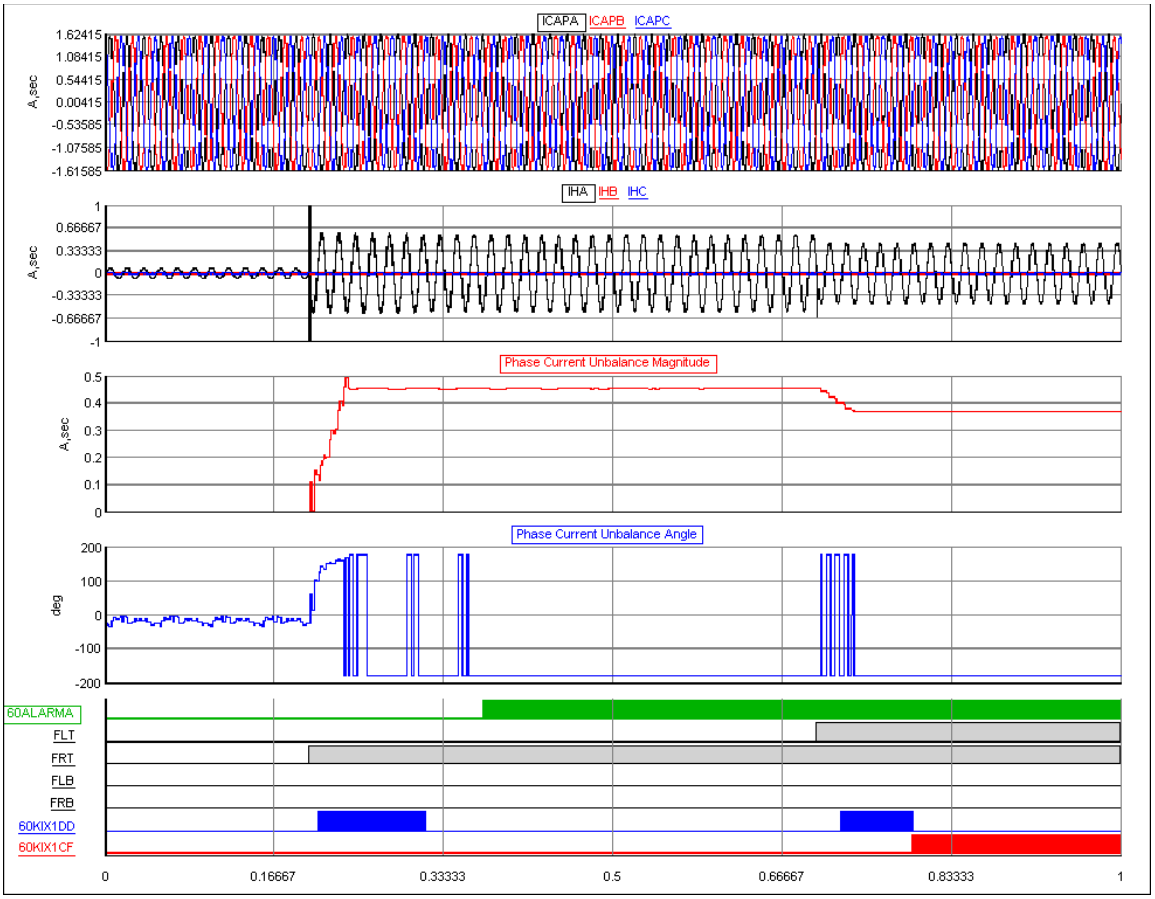


Figure 6-13. Asymmetric Internal Fault in the Right Top Section (Five Elements) Followed by Another in the Left Top Section (One Element) of the H-Bridge Bank

6.5.5 Asymmetric internal fault - left top section (five elements) followed by right top section (one element) of the H-bridge bank

An internal fault is simulated by shorting five elements in a unit in the left top section at 0.2 s and after 0.5 s an asymmetric internal fault is simulated by shorting one

element in a unit in the right top section. Figure 6-14 shows Phase A current unbalance magnitude of 0.45 Amperes secondary for the first fault and decreases to 0.37 Amperes secondary due to the second fault. Phase A current unbalance angle is 0 degrees for the first fault and stays same for the second fault. 60ALARMA asserted after 10 cycles of the first internal fault and stays asserted for the second fault as the unbalance current magnitude is greater than 0.02 Amperes secondary. 60KIX1DD asserted and deasserted twice as there is a change in phase current unbalance magnitude for the first and second faults. Since the unbalance current magnitude decreased on the falling edge of the second 60KIX1DD assertion and the unbalance current angle doesn't change, this is a canceling failure and we can see 60KIX1CF asserted correctly.

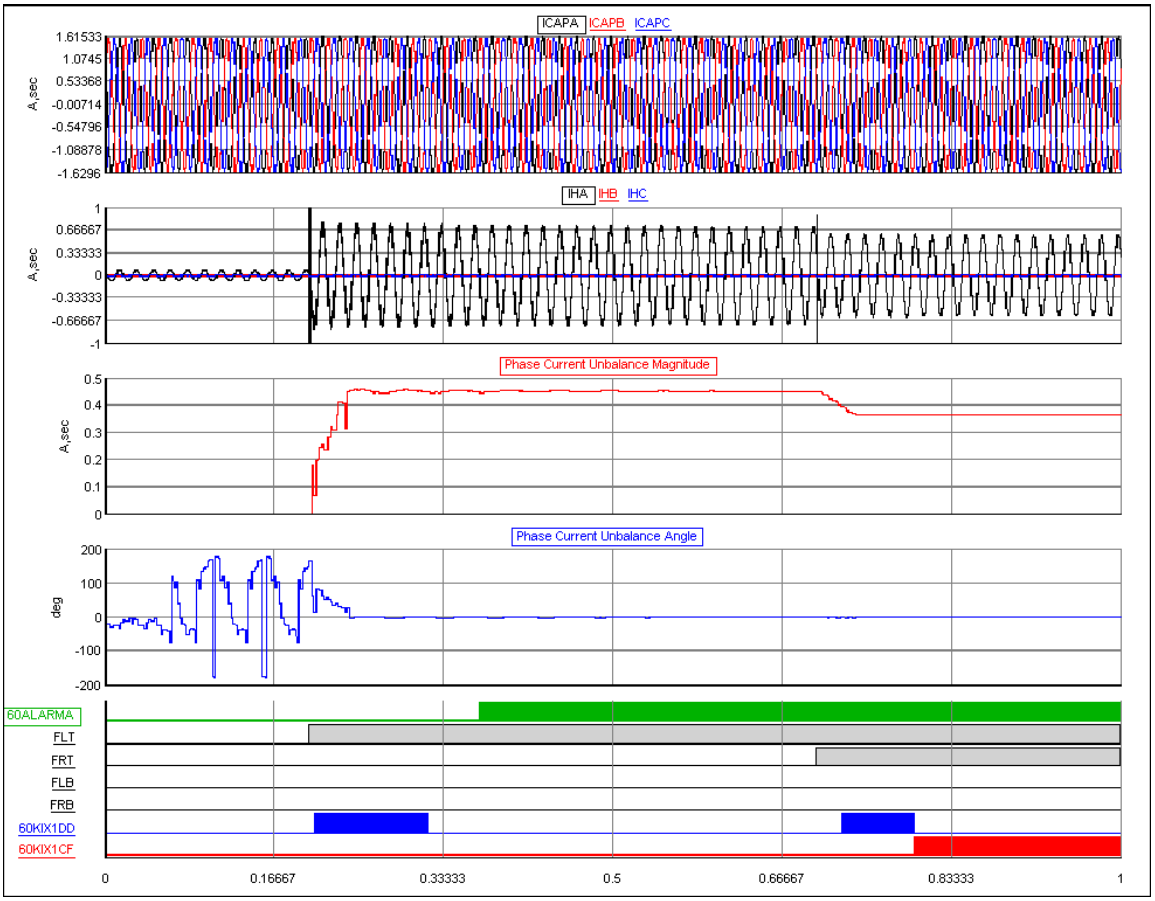


Figure 6-14. Asymmetric Internal Fault in the Left Top Section (Five Elements) Followed by Another in the Right Top Section (One Element) of the H-Bridge Bank

6.5.6 Asymmetric internal fault - right top section (one element) followed by left top section (five elements) of the H-bridge bank

An internal fault is simulated by shorting one element in a unit in the right top section and after 0.5 s an asymmetric internal fault is simulated by shorting five elements in a unit in the left top section. Figure 6-15 shows Phase A current unbalance magnitude of 0.084 Amperes secondary for the first fault and increases to 0.37 Amperes secondary for the second fault. Phase A current unbalance angle is 180 degrees for the first fault and changes to 0 degrees due to the second fault. 60ALARMA asserted after 10 cycles of the first internal fault and stays asserted for the second fault as the unbalance current

magnitude is greater than 0.02 Amperes secondary. 60KIX1DD asserted and deasserted twice as there is a change in phase current unbalance magnitude for the first and second faults. Since the unbalance current magnitude increased on the falling edge of the second 60KIX1DD assertion and the unbalance current angle changed, this is a canceling failure and we can see 60KIX1CF asserted correctly.

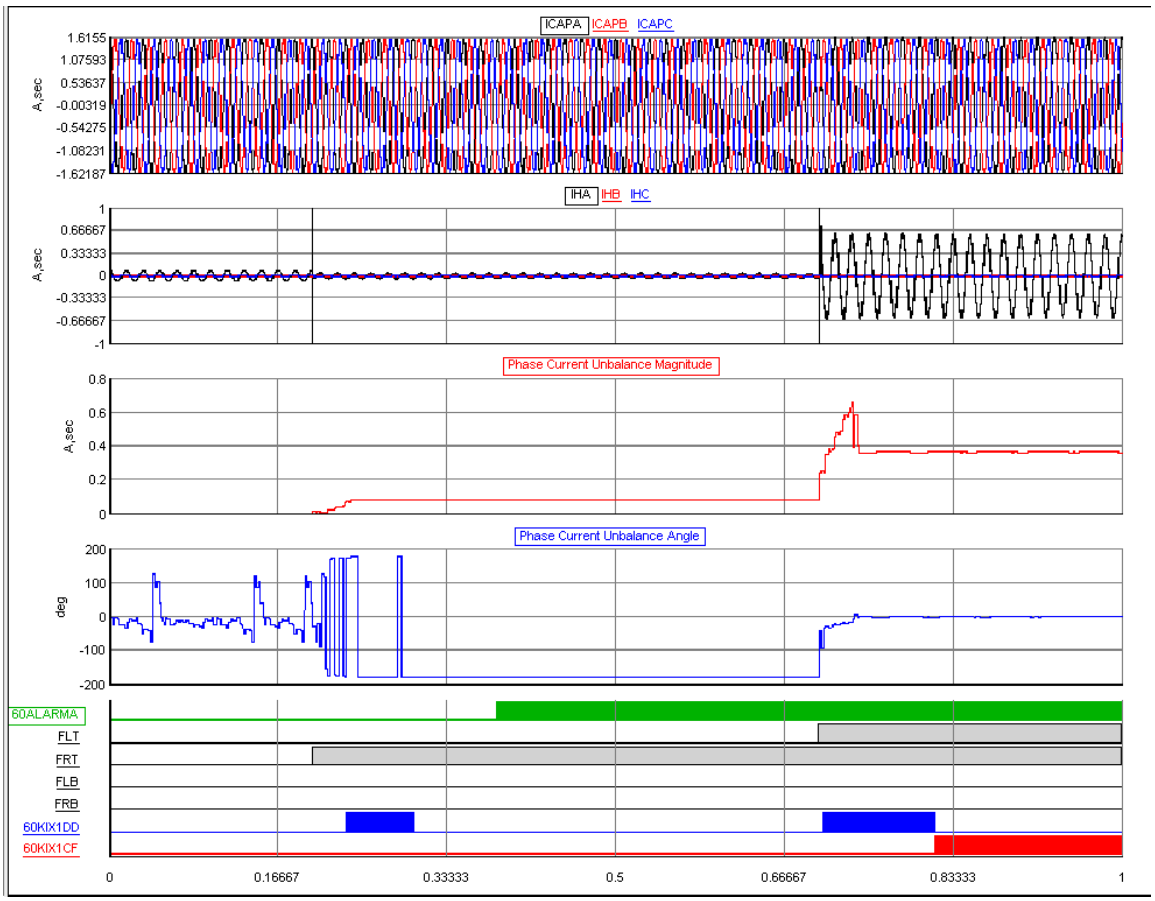


Figure 6-15. Asymmetric Internal Fault in the Right Top Section (One Element) Followed by Another in the Left Top Section (Five Elements) of the H-Bridge Bank

6.5.7 Symmetric internal fault - left top section (one element) followed by left bottom section (one element) of the H-bridge bank

An internal fault is simulated by shorting one element in a unit in the left top section and after 0.5 s a symmetric internal fault is simulated by shorting one element in a unit in

the left bottom section. Figure 6-16 shows Phase A current unbalance magnitude of 0.084 Amperes secondary for the first fault decreases to 0 Amperes secondary for the second fault. Phase A current unbalance angle is 0 degrees for the first fault but since magnitude is zeroed out by the second fault, the current unbalance angle has no reference. 60ALARMA asserted after 10 cycles of the first internal fault but deasserted for the second fault as the unbalance current magnitude is zeroed out. 60KIX1DD asserted and deasserted twice as there is a change in phase current unbalance magnitude for the first and second faults. Since the unbalance current magnitude decreased on the falling edge of the second 60KIX1DD assertion, this is a canceling failure and we can see 60KIX1CF asserted correctly.

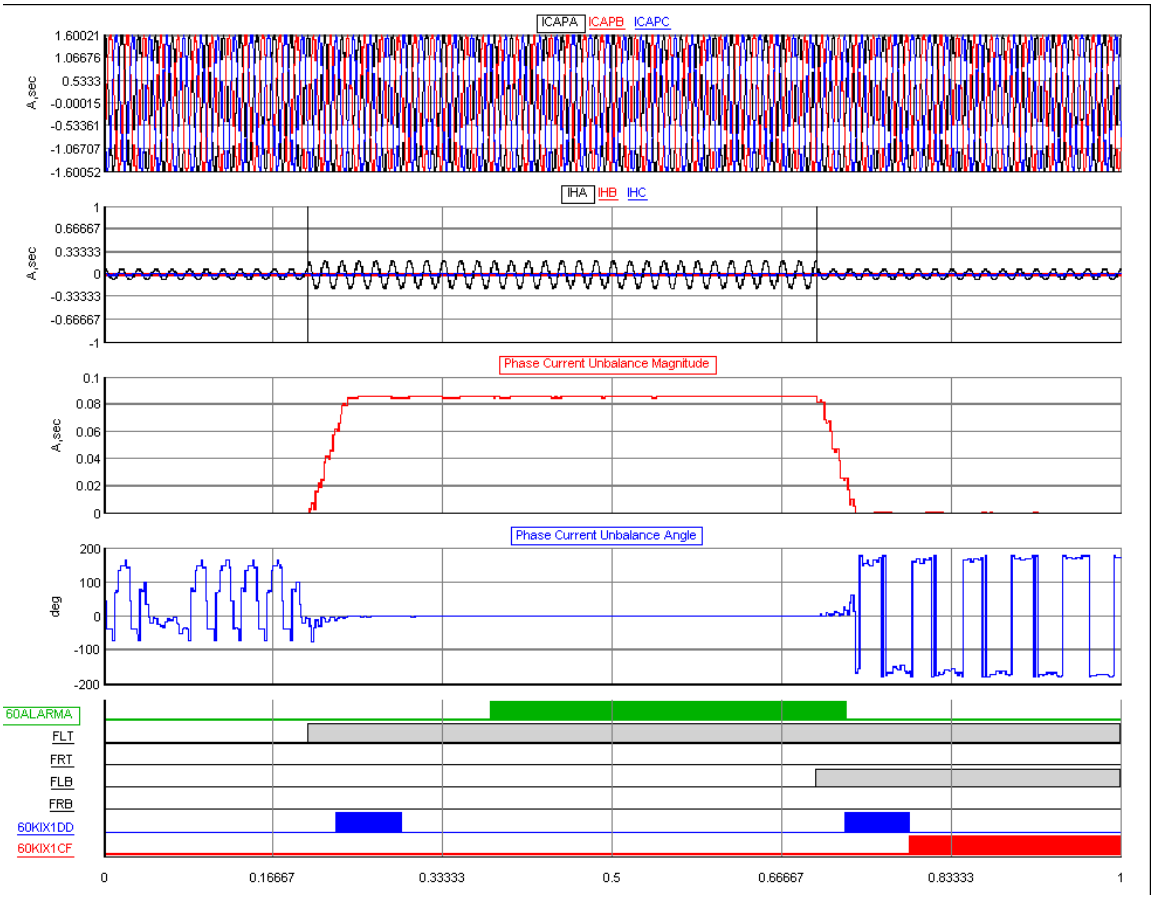


Figure 6-16. Symmetric Internal Fault in the Left Top Section (One Element) Followed by Another in the Left Bottom Section (One Element) of the H-Bridge Bank

6.5.8 Asymmetric internal fault - left top section (one element) followed by left bottom section (five elements) of the H-bridge bank

An internal fault is simulated by shorting one element in a unit in the left top section and after 0.5 s an asymmetric internal fault is simulated by shorting five elements in a unit in the left bottom section. Figure 6-17 shows Phase A current unbalance magnitude of 0.084 Amperes secondary for the first fault and increases to 0.37 Amperes secondary for the second fault. Phase A current unbalance angle is 0 degrees for the first fault and changes to 180 degrees for the second fault. 60ALARMA asserted after 10 cycles of the first internal fault and stays asserted for the second fault as the unbalance current

magnitude is greater than 0.02 Amperes secondary. 60KIX1DD asserted and deasserted twice as there is a change in phase current unbalance magnitude for the first and second faults. Since the unbalance current magnitude increased on the falling edge of the second 60KIX1DD assertion and the unbalance current angle changes from 0 to 180 degrees, this is a canceling failure and we can see 60KIX1CF asserted correctly.

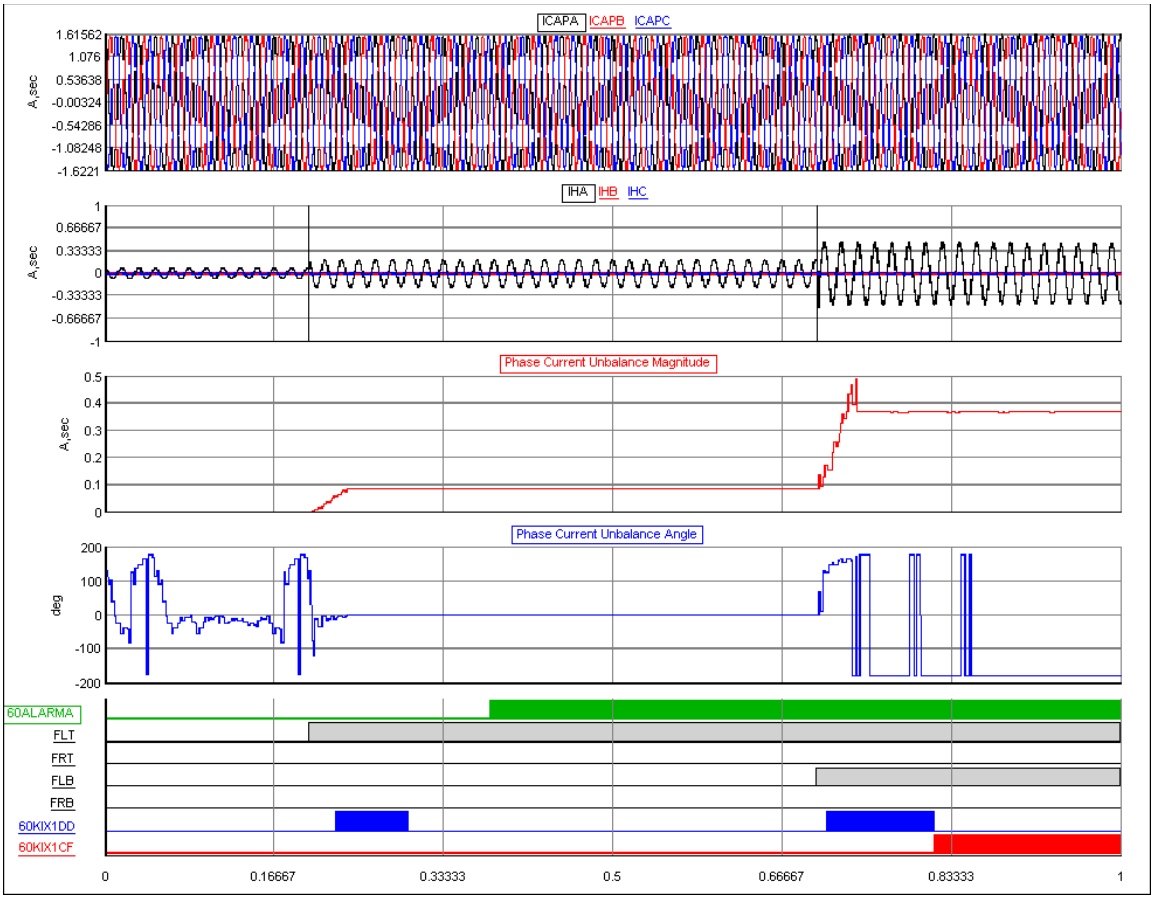


Figure 6-17. Asymmetric Internal Fault in the Left Top Section (One Element) Followed by Another in the Left Bottom Section (Five Elements) of the H-Bridge Bank

6.5.9 Symmetric internal fault - left top section (one element) followed by right bottom section (one element) of the H-bridge bank

An internal fault is simulated by shorting one element in a unit in the left top section and after 0.5 s a symmetric internal fault is simulated by shorting one element in a unit in

the right bottom section. Figure 6-18 shows a Phase A current unbalance magnitude of 0.084 Amperes secondary for the first fault which increases to 0.16 Amperes secondary for the second fault. Phase A current unbalance angle is 0 degrees for the first fault and stays the same for second fault. 60ALARMA asserted after 10 cycles of the first internal fault and stays asserted for the second fault as the unbalance current magnitude is greater than 0.02 Amperes secondary. 60KIX1DD asserted and deasserted twice as there is a change in phase current unbalance magnitude for the first and second faults. Since the unbalance current magnitude increased with no change in unbalance current angle, this is not a canceling failure and we can see 60KIX1CF is stable and did not assert.

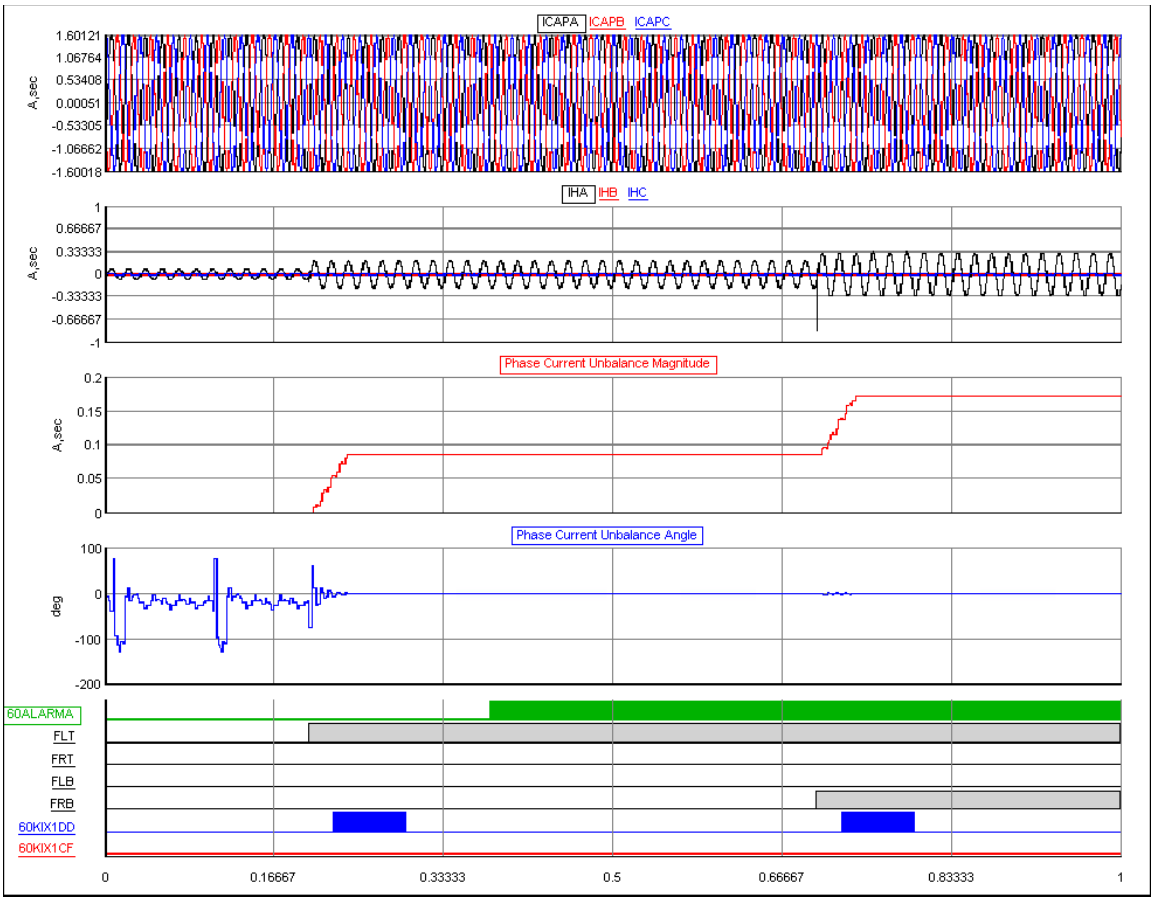


Figure 6-18. Symmetric Internal Fault in the Left Top Section (One Element) Followed by Another in the Right Bottom Section (One Element) of the H-Bridge Bank

6.5.10 Asymmetric internal fault - left top section (one element) followed by right bottom section (five elements) of the H-bridge bank

An internal fault is simulated by shorting one element in a unit in the left top section and after 0.5 s an asymmetric internal fault is simulated by shorting five elements in a unit in the right bottom section. Figure 6-19 shows a Phase A current unbalance magnitude of 0.084 Amperes secondary for the first fault which increases to 0.54 Amperes secondary for the second fault. Phase A current unbalance angle is 0 degrees for the first fault and stays the same for second fault. 60ALARMA asserted after 10 cycles of the first internal fault and stays asserted for the second fault as the unbalance current magnitude is greater than 0.02 Amperes secondary. 60KIX1DD asserted and deasserted twice as there is a change in phase current unbalance magnitude for the first and second faults. Since the unbalance current magnitude increased with no change in unbalance current angle, this is not a canceling failure and we can see 60KIX1CF is stable and did not assert.

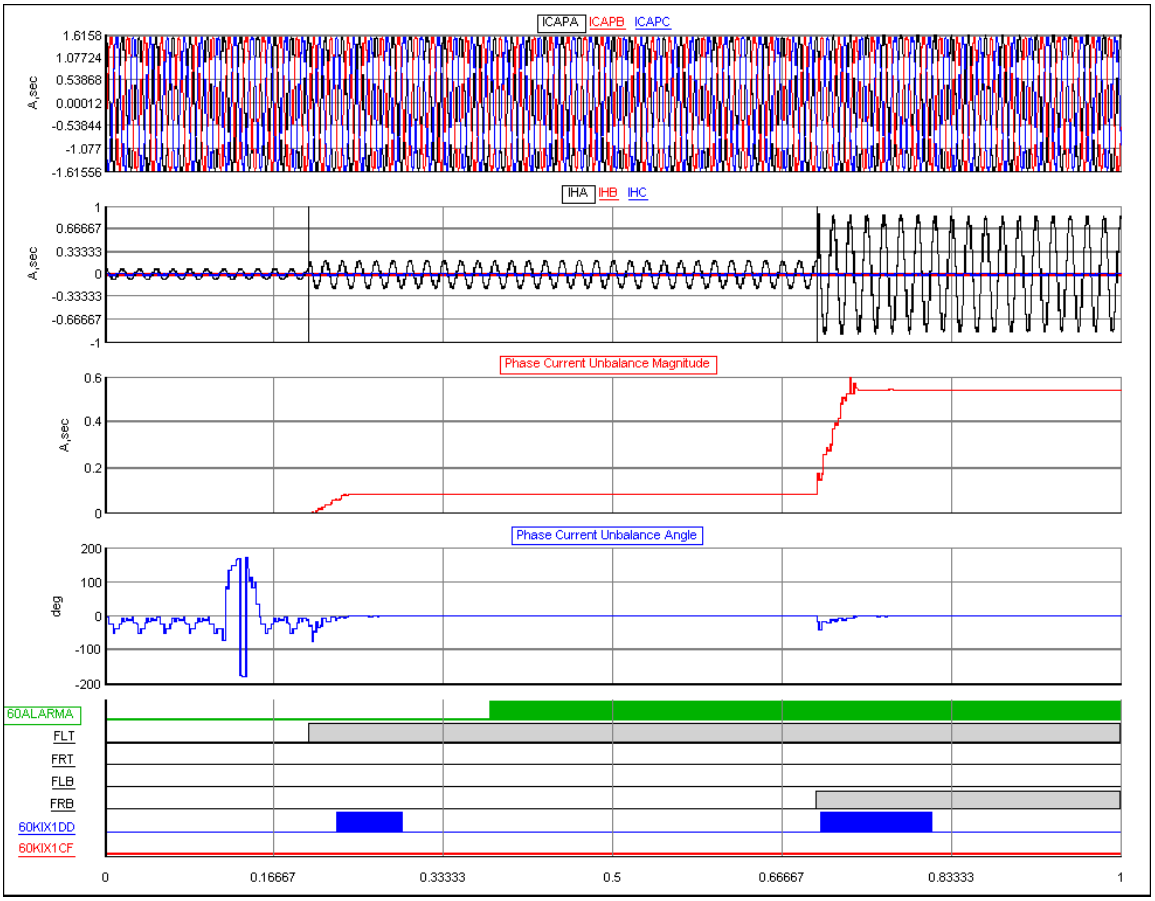


Figure 6-19. Asymmetric Internal Fault in the Left Top Section (One Element) Followed by Another in the Right Bottom Section (Five Elements) of the H-Bridge Bank

6.5.11 Symmetric internal fault - right top section (one element) followed by left bottom section (one element) of the H-bridge bank

An internal fault is simulated by shorting one element in a unit in the right top section and after 0.5 s a symmetric internal fault is simulated by shorting one element in a unit in the left bottom section. Figure 6-20 shows a Phase A current unbalance magnitude of 0.084 Amperes secondary for the first fault which increases to 0.16 Amperes secondary for the second fault. Phase A current unbalance angle is 180 degrees for the first fault and stays the same for second fault. 60ALARMA asserted after 10 cycles of the first internal fault and stays asserted for the second fault as the unbalance current magnitude is greater

than 0.02 Amperes secondary. 60KIX1DD asserted and deasserted twice as there is a change in phase current unbalance magnitude for the first and second faults. Since the unbalance current magnitude increased with no change in unbalance current angle, this is not a canceling failure and we can see 60KIX1CF is stable and did not assert.

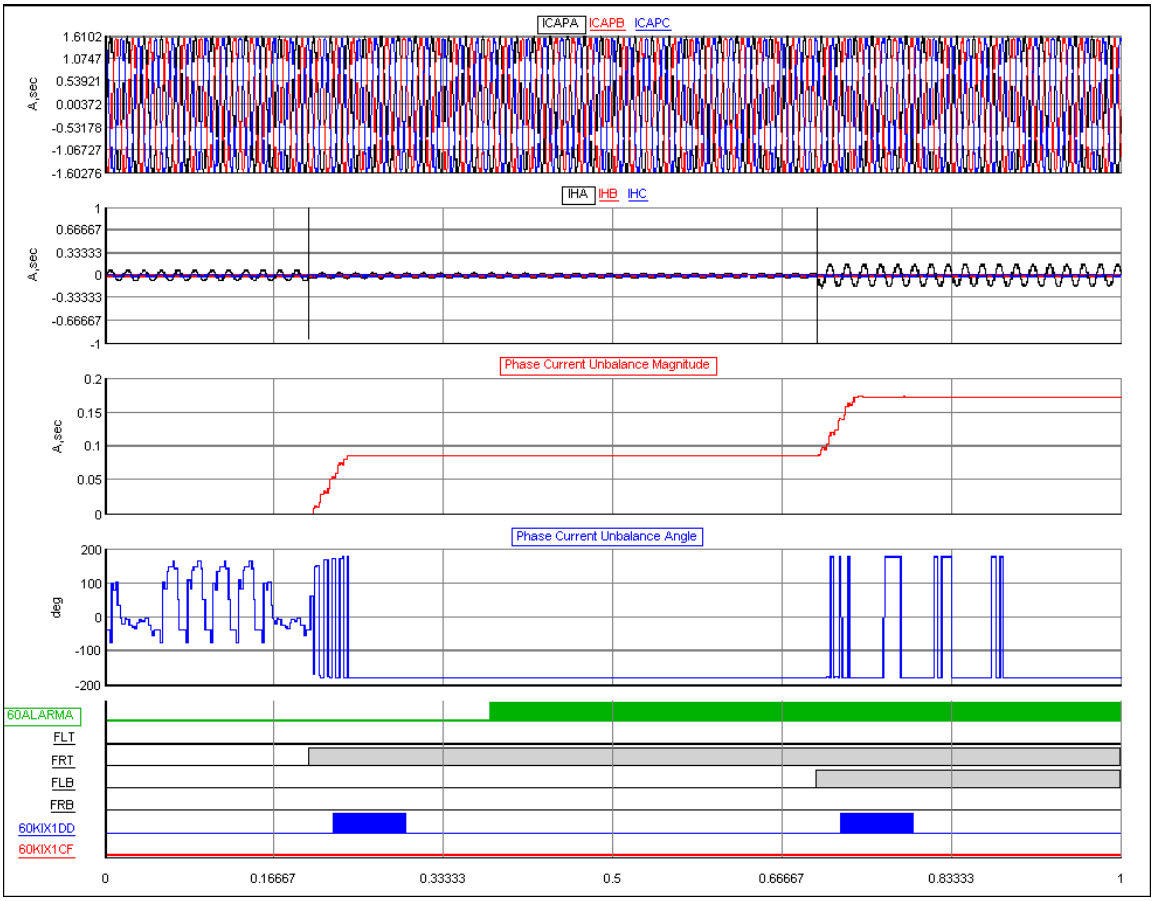


Figure 6-6-20. Symmetric Internal Fault in the Right Top Section (One Element) Followed by Another in the Left Bottom Section (One Element) of the H-Bridge Bank

6.5.12 Asymmetric internal fault - right top section (one element) followed by left bottom section (five elements) of the H-bridge bank

An internal fault is simulated by shorting one element in a unit in the right top section and after 0.5 s an asymmetric internal fault is simulated by shorting five elements in a unit in the left bottom section. Figure 6-21 shows a Phase A current unbalance

magnitude of 0.084 Amperes secondary for the first fault which increases to 0.54 Amperes secondary for the second fault. Phase A current unbalance angle is 180 degrees for the first fault and stays the same for second fault. 60ALARMA asserted after 10 cycles of the first internal fault and stays asserted for the second fault as the unbalance current magnitude is greater than 0.02 Amperes secondary. 60KIX1DD asserted and deasserted twice as there is a change in phase current unbalance magnitude for the first and second faults. Since the unbalance current magnitude increased with no change in unbalance current angle, this is not a canceling failure and we can see 60KIX1CF is stable and did not assert.

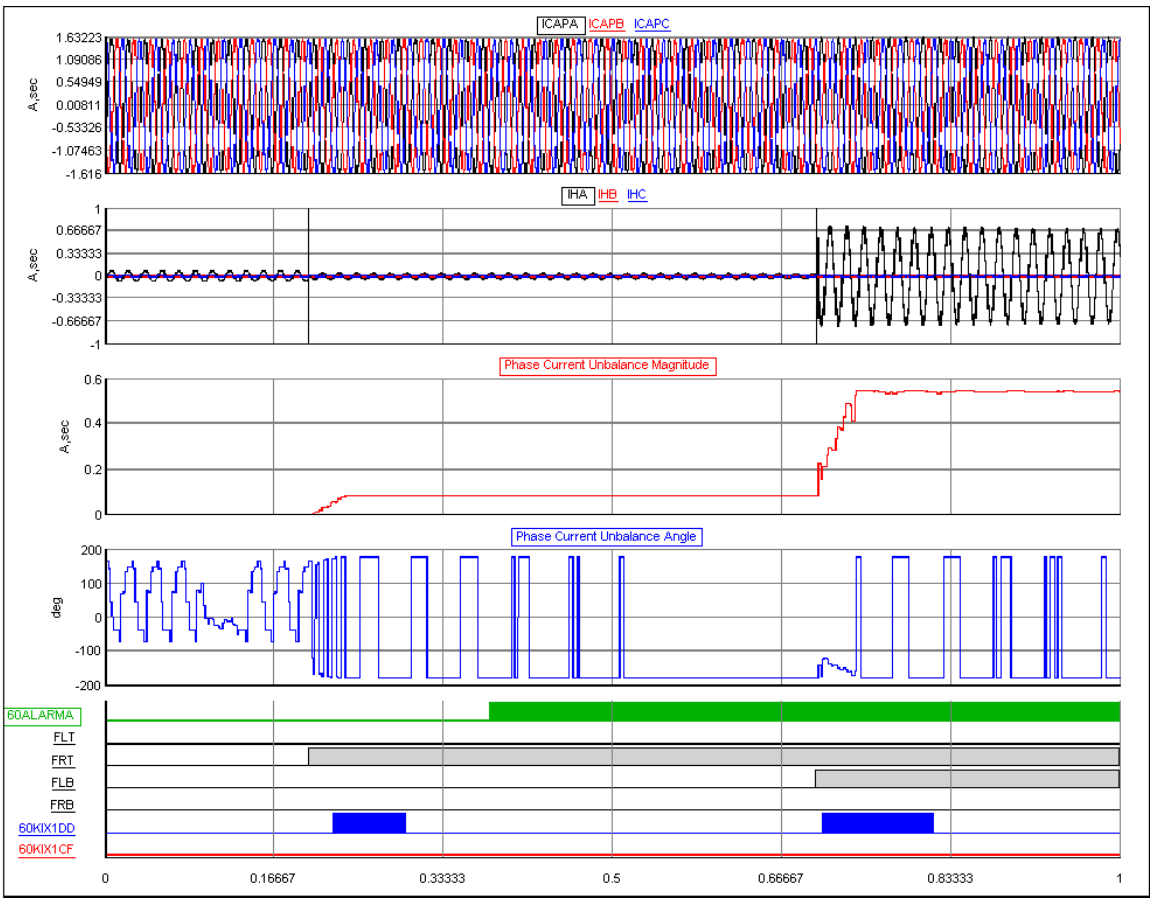


Figure 6-21. Asymmetric Internal Fault in the Left Top Section (One Element) Followed by Another in the Right Bottom Section (Five Elements) of the H-Bridge Bank

6.6 Summary

This chapter presented simulation setup and evaluated the performance of the proposed canceling failure detection logic for various fault scenarios. The simulation results confirmed that the proposed canceling failure detection logic reliably detects the canceling failure for both symmetric and asymmetric faults in multiple sections of the H-bridge bank and does not generate false detections for faults that are not canceling faults.

Chapter 7 Summary, Conclusions, and Future Work

This chapter summarizes the research, draws conclusions from the research, and provides possible future research directions in the area of capacitor bank unbalance protection enhancements related to canceling failure detection.

7.1 Summary

Chapter 1 introduced the topic, presented the research objectives of this thesis as well as the research outline.

Chapter 2 introduced capacitor bank background, common connections, configurations, fusing and failure mechanisms.

Chapter 3 presented four common capacitor bank unbalance protection methods and fault location techniques that can be applied to various capacitor bank configurations. This chapter provides the basis for the proposed canceling failure detection.

Chapter 4 explained the symmetric and asymmetric canceling failure issues and how they affect the sensitivity and reliability of unbalance protection schemes. This chapter also presented the few references related to this research area.

Chapter 5 showed mathematical analysis of symmetric and asymmetric canceling failures and introduced the proposed solution that enhances the capacitor bank unbalance protection by detecting symmetric and asymmetric canceling failures.

Chapter 6 presented simulation setup and evaluated the performance of the proposed canceling failure detection logic for various fault scenarios. The simulation results confirmed that the proposed canceling failure detection logic reliably detects the canceling failure for both symmetric and asymmetric faults in multiple sections of the H-bridge bank and does not generate false detections for faults that are not canceling faults.

7.2 Conclusions

The main objective of this thesis was to develop an algorithm that can detect the symmetric and asymmetric canceling failures, thereby improving the reliability of the capacitor bank unbalance protection. Canceling failures will result in nulling out or reducing the unbalance magnitude. Unbalance protection will not be able to detect these failures even when the bank is unbalanced, resulting in continuous overvoltage on healthy elements which can lead to a cascading failure.

To address this, a solution is provided in Chapter 5. The algorithm checks both the change in unbalance magnitude and change in unbalance phase angle before and after a disturbance.

The solution verified in this research is economical and practical as it uses the unbalance magnitude and phase angle which are already available as part of unbalance protection. The algorithm doesn't need additional measurement devices.

The solution was tested and validated using time domain computer simulation with an electromagnetic transients program. The simulation results presented in Chapter 6, demonstrate that the proposed solution solves the problem.

The solution developed by this research is one more tool the power system industry could use to make electric power both economical and reliable.

7.3 Future Work

The proposed solution can easily be extended to single-WYE grounded banks with tapped PTs that use per-phase voltage unbalance protection. Note that that the unbalance quantity input to the canceling failure detection logic will be phase voltage unbalance.

The proposed solution can be applied to double-WYE or split-WYE banks with CTs that use per-phase current unbalance protection, as they are similar to H-bridge banks but with only two sections.

The proposed solution can easily be extended to double-WYE ungrounded banks with neutral CTs that use neutral current unbalance protection. The canceling failure unbalance angle logic in (5-4) needs to account for more fault sectors.

The proposed disturbance detector can be made more secure by setting it to respond only to element or unit failures within the bank. This could be done using the fault signature due to element failure.

The proposed solution should be tested and verified on a real system. The solution could first be implemented in a programmable device and fed measurements from instrument transformers in a laboratory capacitor bank. Staged failures could be created to test the algorithm. Following the laboratory testing, the algorithm could be tested in a utility scale environment.

Since canceling failure result in reduced sensitivity of unbalance protection, using the proposed canceling failure, unbalance protection can be made adaptable by biasing the unbalance magnitude with the amount of unbalance that got cancelled due to canceling failure.

Bibliography

[1] R. Natarajan, *Power System Capacitors*. CRC Press, Boca Raton, FL, 2005.

[2] S. Samineni, C. Labuschagne, and J. Pope, "Principles of Shunt Capacitor Bank Application and Protection," *Proceedings of the 36th Annual Western Protective Relay Conference, Spokane, WA, October 2009*.

[3] IEEE Standard 18-2012, *IEEE Standard for Shunt Power Capacitors*.

[4] M. Dhillon, D. Tziouvaras, "Protection of Fuseless Capacitor Banks Using Digital Relays," *Proceedings of the 26th Annual Western Protective Relay Conference, Spokane, WA, October 1999.*

[5] IEEE Standard 1036-2010, *IEEE Guide for the Protection of Shunt Capacitor Banks*.

[6] IEEE Standard C37.99-2012, IEEE Guide for Application of Shunt Capacitor Banks.

[7] B. Kasztenny, J. Schaefer, and E. Clark, "Fundamentals of Adaptive Protection of Large Capacitor Banks," *Proceedings of the 60th Annual Georgia Tech Protective Relaying Conference, Atlanta, GA, May 2006.*

[8] J. Schaefer, S. Samineni, C. Labuschagne, S. Chase, and D. Hawaz, "Minimizing Capacitor Bank Outage Time Through Fault Location," in *Protective Relay Engineers, 2014 67th Annual Conference for, March 2014, pp. 72–83.*

[9] S. Samineni and C. A. Labuschagne, *Apparatus and Method for Identifying a Faulted Phase in A Shunt Capacitor Bank*. US Patent 8 575 941, November 2013.

[10] S. Samineni, C. Labuschagne, J. Pope, and B. Kasztenny, "Fault Location in Shunt Capacitor Banks," in *Developments in Power System Protection (DPSP 2010). Managing the Change, 10th IET International Conference on, March 2010, pp. 1–5.*

[11] E. Price and R. Wolsey, "String Current Unbalance Protection and Faulted String Identification for Grounded-Wye Fuseless Capacitor Banks," *in 65th Annual Georgia Tech Protective Relaying Conference, May 2011.*

Appendix A

Chapter 2 presents the material from a conference paper which was co-authored by the same author of this research. Chapter 2 provides the background material for shunt capacitor bank configuration and fault mechanism which forms the basis for the canceling failure detection research. To reuse [2], IEEE's copyright permission was requested and the permission in Figure A-1- is granted.

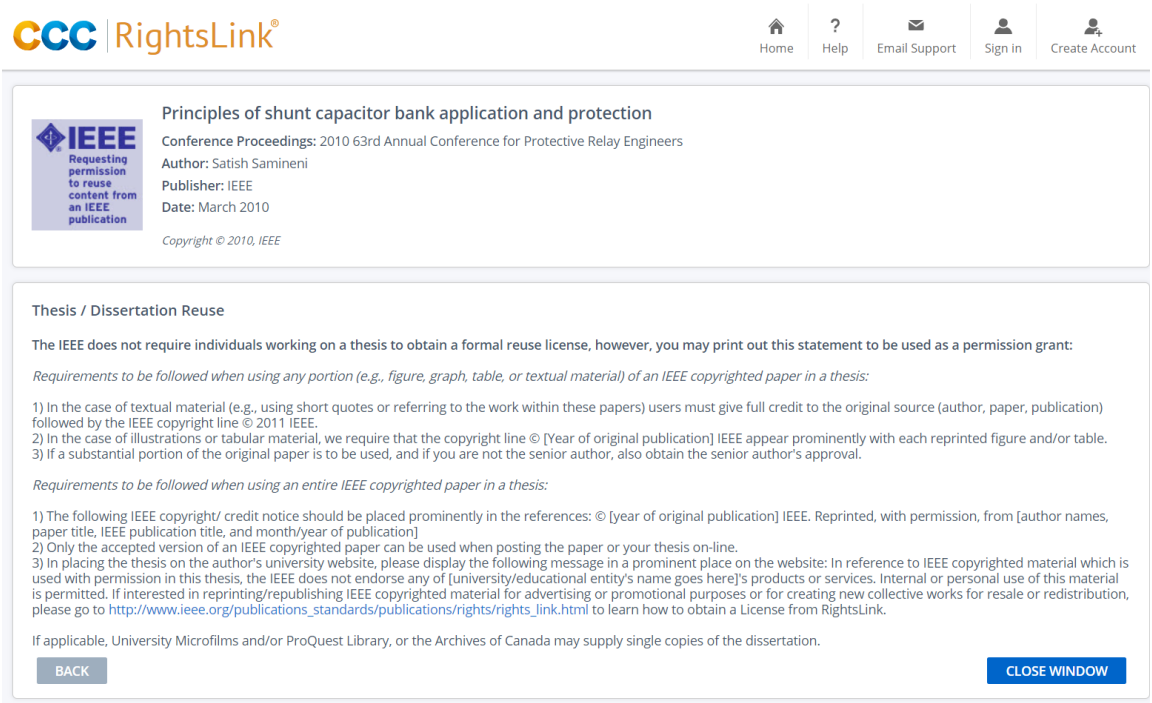
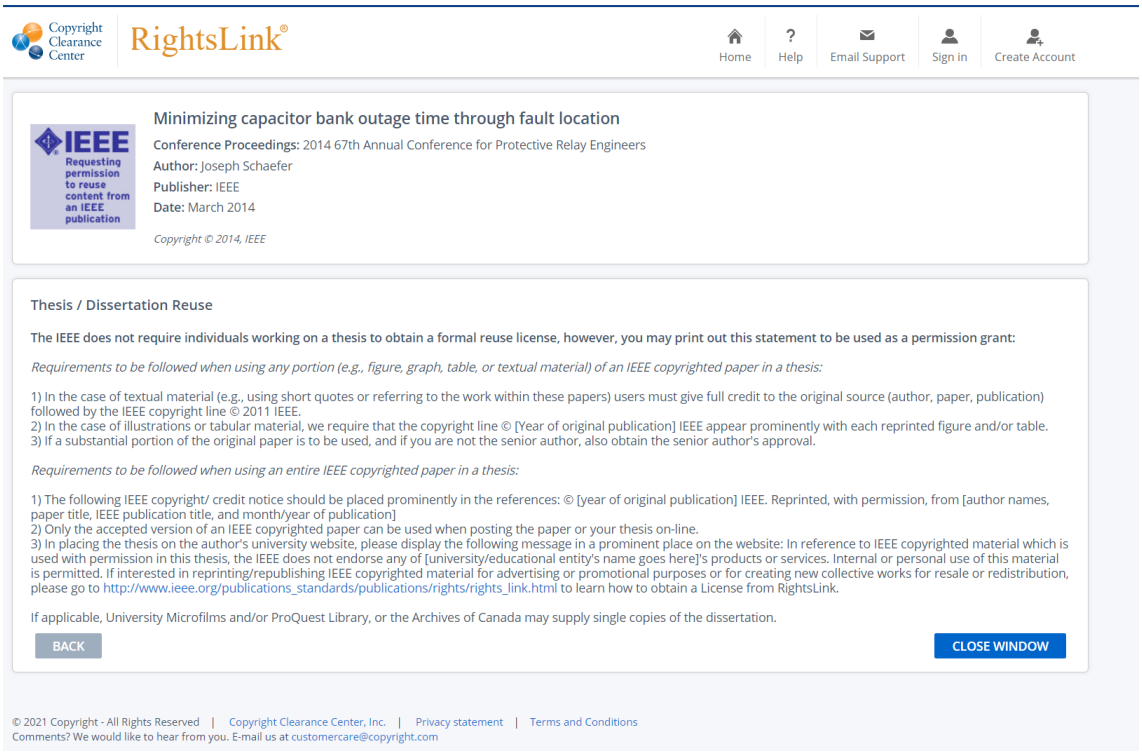


Figure A-0-1. IEEE Copywrite Permission to Reuse [2]

Chapter 3 presents the material from a conference paper which was co-authored by the same author of this research. Chapter 3 provides the background material for unbalance protection methods and fault location which forms the basis for the canceling failure detection research. To reuse [6], IEEE's copyright permission was requested and the permission in Figure A-2- is granted.



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