An Adaptive Phase Quantization Noise Cancellation Architecture for ΔΣ Fractional-N Frequency Synthesizers

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Authorization To Submit Dissertation

This dissertation of Jonathon C. Stiff submitted for the degree of Doctor of Philosophy with a major in Electrical Engineering and titled "**An Adaptive Phase Quantization Noise Cancellation Architecture for ΔΣ Fractional-N Frequency Synthesizers**," has been reviewed in final form. Permission, as indicated by the signatures and dates given below, is now granted to submit final copies to the College of Graduate Studies for approval.

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Abstract

A fractional-N PLL phase quantization cancellation architecture using adaptive digital delay word scaling is presented and demonstrated. A digital sign-error adaptive filter utilizing the 1-bit quantized PLL phase error and the feedback divider delta-sigma modulator accumulated error generates the optimal control word scaling for a phase cancelling digital delay. A comprehensive analytic phase noise model is derived and compared to time-domain simulation and measurement. The proposed fractional-N synthesizer, with a 2.4 GHz center frequency VCO is fabricated on a PCB with commercially available integrated circuits as a proof of concept. The synthesizer output frequency range is 144-156 MHz with 2 ppm resolution for a 20 MHz crystal oscillator reference. The adaptive phase cancellation is measured to reduce phase noise by as much as 25 dB.

Acknowledgements

I would like to thank my wife Kama and children Klarissa and Kameron for their support while completing my research and degree. I would also like to thank several of my former co-workers for their technical support on PCB design as well as being a sounding board for some of my research ideas.

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Chapter 1. Introduction

Fractional-N phase locked loop (PLL) frequency synthesizers are a common solution for generating precision frequency signals based on a high quality, lower frequency source (ex. a crystal oscillator). By utilizing a delta-sigma modulated feedback divider, fractional-N PLLs (Fig. 1.1.1) can achieve the fine frequency resolution, calculated in (1.1.1), of an integer-N synthesizer without reducing the phase-frequency detector (PFD) frequency and the associated PLL closed loop bandwidth in order to maintain loop stability.

$$F_{OUT} = F_{REF}\left(N_{INT} + N_{FRAC}\right) \tag{1.1.1}$$

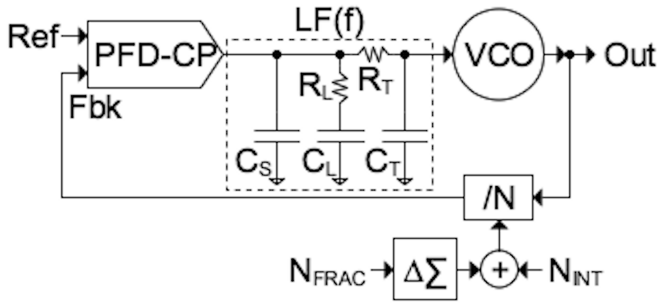

Fig. 1.1.1 Conventional fractional-N frequency synthesizer.

The higher PLL closed loop bandwidth allows for greater voltage controlled oscillator (VCO) phase noise attenuation and, generally, much lower in-band phase noise. The trade-off faced when utilizing a fractional-N synthesizer is the resultant phase quantization noise generated by the modulated feedback divider, contributing to the overall PLL output phase noise. By utilizing a delta-sigma modulator, the phase quantization noise is high-pass shaped and then significantly attenuated by

the PLL low-pass response. However, dependence on the PLL attenuation once again places a limitation on the PLL closed loop bandwidth, typically $1/50^{th}$-$1/100^{th}$ of the reference frequency, F_{REF}. Increasing the VCO frequency and/or reference frequency can mitigate the problem by decreasing modulation step size and, therefore, quantization noise magnitude, or by shifting the noise to higher frequency for greater attenuation, respectively. However, practical circuit and component limitations restrict the extent of noise reduction using either of these techniques. Therefore, phase quantization cancellation, rather than loop attenuation, is the only practical means of substantially reducing the phase quantization contribution to PLL output phase noise while maintaining high bandwidth.

General phase quantization noise cancellation architectures utilize a digital-to-analog converter (DAC) cancellation element placed between the feedback divider output and loop filter to cancel the modulated feedback divider phase quantization noise. The cancellation magnitude is the accumulated feedback divider delta-sigma output error, ierr(n), in units of VCO period, t_{VCO}. This value is re-quantized (often with another delta-sigma modulator) to the DAC element array word length. The DAC must self-scale in order to translate the digital word to the correct analog units for phase cancellation. As every DAC array exhibits element mismatch, some form of dynamic element matching (DEM), such as data weighted averaging (DWA), is necessary to high pass shape the mismatch noise which would otherwise manifest as broad band white noise. The mismatch noise would limit the quantization noise cancellation and add significant low frequency PLL output phase noise ([1], [2]).

In [3] and [4] the phase quantization error cancellation is made at the PLL loop filter using a charge DAC (Fig. 1.1.2). The DAC output scaling for correctly translating ierr(n) to charge for error cancellation is $I_{CP} \times t_{VCO}$, where I_{CP} is the PLL charge pump magnitude. This necessitates a fairly complex charge DAC, especially as it must directly utilize the high frequency VCO output (or a fixed divided version) for correct charge scaling.

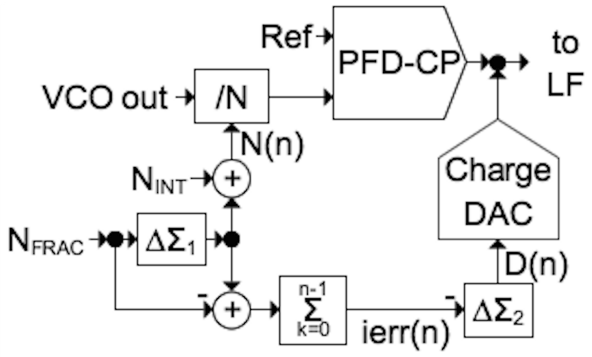

Fig. 1.1.2 General phase quantization noise cancellation architecture using a charge DAC.

In [5], [6], [7] and [8] a direct phase error cancellation is made with a delay DAC placed between the feedback divider output and PFD input (Fig. 1.1.3). An analog delay locked loop (DLL) sets the DAC unit element delay (either directly or using replica elements) proportional to t_{VCO}. As with the charge DAC solution, this is another non-trivial analog design, though with the advantage of only requiring t_{VCO} for DAC scaling. Another advantage is that the phase DAC technique reduces the effect of PFD and charge pump (PFD/CP) nonlinearity by delivering smaller instantaneous phase errors to the PFD input.

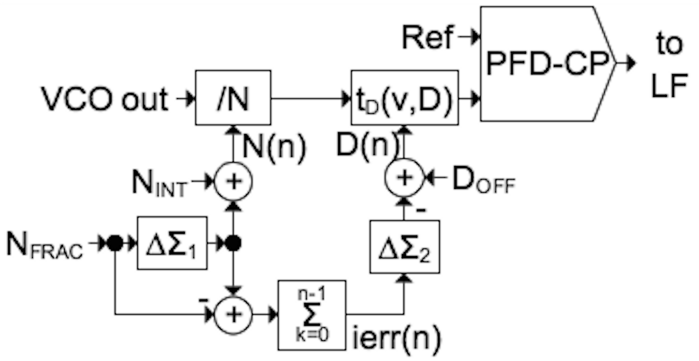

Fig. 1.1.3 General phase quantization noise cancellation architecture using a phase DAC.

While previous phase quantization noise cancellation architectures have been demonstrated, the increase in overall analog circuit complexity, principally tied to scaling the cancellation DAC to ierr(n), is undesirable as it is difficult to add to existing designs and export to new integrated circuit (IC) technologies. In addition, the previous techniques only provide passive phase cancellation as the cancellation magnitude is based on relative scaling rather than on direct phase error measurement, inherently making for a less robust design.

Adaptive phase quantization cancellation solves this issue by making the cancellation scaling dependent on in-circuit error measurement. Adaptive cancellation has been employed in previous fractional-N implementations. In [10], a least mean square (LMS) adaptive algorithm was utilized to determine the input phase error time-to-digital converter (TDC) delay scaling for digital phase cancellation in an all-digital fractional-N PLL. In [9], a charge DAC phase cancellation design was demonstrated using a partially analog sign-sign LMS adaptive loop for charge scaling. However, though [10] and [9] are adaptive, they

still require the design of additional complex analog blocks. The phase quantization cancellation architecture presented in this dissertation utilizes an adaptive algorithm to digitally scale a fixed unit digital delay control word based on ierr(n) using direct phase error measurement. Unlike previous phase cancellation architectures, the presented design is entirely implemented in the digital domain, with the exception of the digital delay.

Chapter 2 presents the system architecture including a detailed description of the adaptive algorithm. Chapter 3 details the fractional-N PLL phase noise modeling using the adaptive phase quantization cancellation architecture. The circuit implementation and experimental measurements are reviewed in Chapter 4 and Chapter 5, respectively. Chapter 6 concludes with a summary of the adaptive phase quantization cancellation fractional-N PLL architecture design results, the estimated output phase using DWA digital delay and comments on future implementations.

Chapter 2. System Architecture

2.1 Introduction

The proposed adaptive phase quantization noise cancellation architecture is presented in Fig. 2.1.1. It is similar to the general phase cancellation architecture in Fig. 1.1.3 with the addition of the adaptive filter blocks scaling ierr(n) in order to produce a cancellation word, D(n), for the fixed unit digital delay. These blocks and the adaptive filter algorithm are detailed in the following subsections.

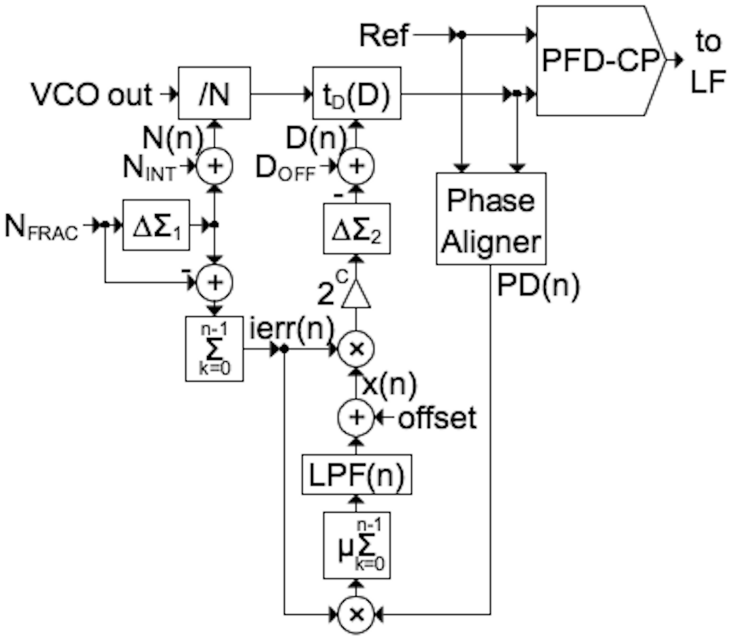

Fig. 2.1.1 Proposed adaptive phase quantization noise cancellation architecture.

2.2 Phase Cancellation Error

In PLL phase lock, the phase cancellation error is the difference between the modulated feedback divider accumulated phase quantization noise and the phase

canceling digital delay. As both are products of ierr(n), the error between them determines how ierr(n) is transformed into phase in the feedback divider and delay paths. The feedback divider accumulated phase quantization noise is scaled by the VCO period, t_{VCO}. The digital delay cancellation is scaled by the unit delay value t_{UNIT}, fixed prescaler 2^C and the adaptive multiplier x(n). The phase cancellation error can be written as the general adaptive filter error function in (2.2.1) by defining the feedback divider modulation phase conversion as the system function *h(n)* and the digital delay conversion as the estimated system function $\hat{h}(n)$.

$$e(n) = ierr(n)\left(h(n) - \hat{h}(n)\right), \text{ where } h(n) = t_{VCO} \text{ and } \hat{h}(n) = x(n)2^C t_{UNIT} \tag{2.2.1}$$

2.3 Sign-Error Adaptive Filter

From [16] and [18], the sign-error steepest descent gradient algorithm, with the general update solution in (2.3.2), has several features that make it desirable for this application. By using a cost function based on the mean absolute error (rather than the mean square error), the phase error analog-to-digital conversion is simplified to a sign operation, as calculated in (2.3.3) where E is the statistical expectation operation. The phase error sign output also simplifies one loop multiplication (with ierr(n)) to a selectable two's complement operation. The phase error sign operation can be implemented with a simple 1-bit phase detector.

$$\hat{h}(n) = -2^C t_{UNIT} \mu \sum_{j=0}^{n} \frac{\delta C(j)}{\delta \hat{h}(j)}, \text{ where } C(j) = E\left(\left|e(j)\right|\right) \tag{2.3.2}$$

$$\frac{\partial C(j)}{\partial \hat{h}(j)} = E\left(\frac{\partial\left(\left|e(j)\right|\right)}{\partial e(j)} \frac{\partial e(j)}{\partial \hat{h}(j)} \right) = -E\left(\text{sgn}(e(j))ierr(j)\right) \tag{2.3.3}$$

The initial adaptive multiplier x(n) update solution (2.3.4) is found by substituting (2.3.3) into (2.3.2) and solving for x(n).

$$x(n) = \sum_{j=0}^{n} E\left(\text{sgn}(e(j))ierr(j)\right) \tag{2.3.4}$$

One consequence of a 1-bit phase detector is the requirement for a zero mean e(n). Static phase offset can lead to erroneous sign-error output, disrupting the adaptive update. While the PLL already inherently minimizes the PFD phase error, unless the 1-bit phase detector is physically located at the PFD, it will exhibit a different static phase offset. A phase aligner decouples the 1-bit phase detector static phase offset error correction from the PLL, which can also allow faster phase correction and greater immunity to input phase modulation (ex. phase shift keying modulation). The digital phase aligner is composed of a digital delay line, with unit delay t_{PA}, and loop filter, f_{PA}. The digital phase aligner phase error correction is represented by $e_{PA}(n)$ in (2.3.5).

$$x(n) = \mu \sum_{j=0}^{n} E\left(\text{sgn}(e(j) - e_{PA}(j))ierr(j)\right) \tag{2.3.5}$$

A digital low pass filter, LPF(n), provides an estimate of the expectation in (2.3.5). The low-pass filter also provides high frequency quantization noise attenuation from x(n) truncation prior to multiplication with ierr(n), which is desirable

for multiplier size reduction. The resulting x(n) adaptive update solution is shown in (2.3.6).

$$x(n) \approx \mu \left(\sum_{j=0}^{n} \mathrm{sgn}(e(j) - e_{PA}(j)) ierr(j) \right) * LPF(n) \tag{2.3.6}$$

The complete sign-error adaptive update solution in Fig. 2.3.2 can be implemented with a digital phase aligner, a digital accumulator, a digital low pass filter, a selectable two's complement block (for ±1 multiplication), a digital multiplier and bit shift operations for convergence constant μ and multiplier scalar 2^C. Not shown in Fig. 2.3.2 are the sub-block clock delays necessary for completing each operation. These delays do not impede the adaptive update loop as long as the additional phase doesn't cause loop instability and two signal time alignments are maintained. First, the feedback divider phase modulation and cancellation digital delay must be generated by the same ierr(n) for correct cancellation. Lastly, that same ierr(n) must multiply the resulting measured phase error for a correct adaptive update. The collective adaptive update loop delay is modeled as a P clock cycle delay block.

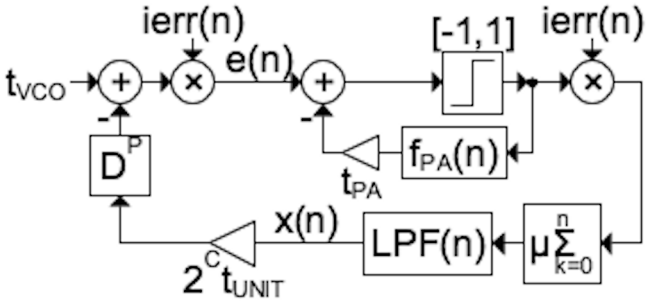

Fig. 2.3.2 Sign-error adaptive update algorithm.

2.4 Adaptive Filter Update Loop Stability

An adaptive update loop function is necessary in order to establish stability. First, the 1-bit phase detector must be approximated as a linear block. In [16] and [18], a 1-bit detector is modeled with the scalar transfer function (2.4.7) whose magnitude is determined by e(n) variance.

$$g_{PA} = \sqrt{\frac{2}{\pi\sigma_e^2}}, \text{ where } \sigma_e^2 = E\left[e^2(n)\right] \tag{2.4.7}$$

Using this result, the z-domain phase aligner transfer function can be calculated as (2.4.8). The equivalent sign-error adaptive update algorithm is shown in Fig. 2.4.2.

$$H_{PA}(z) = \frac{g_{PA}}{1 + t_{PA} g_{PA} F_{PA}(z)}, \text{where} F_{PA}(z) = Z\left[f_{PA}(n)\right] \tag{2.4.8}$$

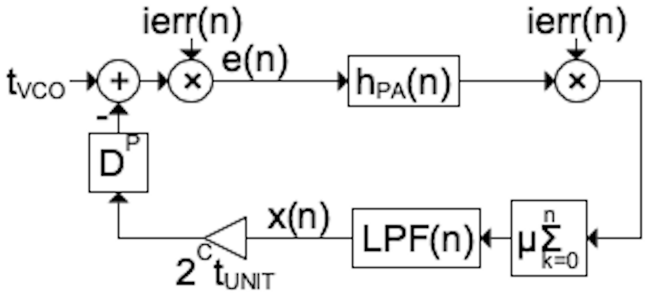

Fig. 2.4.2 Sign-error adaptive algorithm with the equivalent digital phase aligner transfer function.

Lastly, as the adaptive filter update contains two nonlinear multiplication operations of the zero mean random variable ierr(n), an explicit linear response function does not exist. However, an expected loop response can be found by

applying the expectation operation to the loop difference equation ([18], [19]). The expectation operation transforms the multiplications and phase aligner to an equivalent expected transfer function $f_{iPA}(n)$, shown in (2.4.9), which is the product of $h_{PA}(n)$ and the ierr(n) autocorrelation, $R_{ierr}(n)$. The z-transform of (2.4.9), $F_{iPA}(z)$ in (2.4.10), is the convolution of $H_{PA}(z)$ and the ierr(n) noise power spectral density, $S_{ierr}(z)$. Application of (2.4.9) simplifies the sign-error adaptive update algorithm, as shown in Fig. 2.4.3.

$$f_{iPA}(n) = E\Big[\, ierr(n)\big(ierr(n) * h_{PA}(n)\big)\Big] = R_{ierr}(n) h_{PA}(n) \tag{2.4.9}$$

$$F_{iPA}(z) = Z\big(f_{iPA}(n)\big) = S_{ierr}(z) * H_{PA}(z) \tag{2.4.10}$$

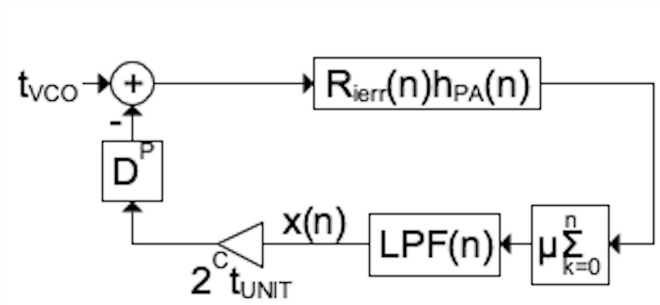

Fig. 2.4.3 Sign-error adaptive algorithm with the expected digital phase aligner/ierr(n) multiplications transfer function block.

With the remaining adaptive filter update loop blocks unchanged by the expectation operation, the expected z-domain loop response is (2.4.11).

$$X(z) = \frac{\mu g_{PA} t_{VCO} LPF(z)\left(\dfrac{z^{-P}}{1 - z^{-1}}\right)\big(S_{ierr}(z) * H_{PA}(z)\big)}{1 + \mu g_{PA} 2^{C} t_{UNIT} LPF(z)\left(\dfrac{z^{-P}}{1 - z^{-1}}\right)\big(S_{ierr}(z) * H_{PA}(z)\big)} \tag{2.4.11}$$

While the poles in (2.4.11) can be determined numerically, an approximate loop response equation can be obtained by making a couple of practical assumptions. First, as both $S_{ierr}(f)$ and $H_{PA}(f)$ are high pass shaped, $S_{ierr}(f)*H_{PA}(f)\approx SF$ (a constant) for a wide band at low frequency. Lastly, if α is chosen much less than 1, the adaptive filter update loop response function can be approximated as (2.4.12).

$$X(z)\approx\frac{\beta z^{-P}\prod_{k=0}^{M}(1-z_{LPF,k}z^{-1})}{\left(1-(1-\alpha)z^{-1}\right)\left(1-\alpha\lambda z^{-P+1}\right)\prod_{k=0}^{N}\left(1-p_{LPF,k}z^{-1}\right)}, \tag{2.4.12}$$

where: $P\geq 2, \alpha=\mu g_{PA}2^{C}t_{UNIT}SF, \beta=\mu g_{PA}t_{VCO}SF, \lambda\equiv$ LPF(z) unity gain scalar

Assuming a relatively high frequency low-pass filter, a single dominant pole governs the adaptive filter update loop. Loop stability is achieved by selecting μ within the bounds set in (2.4.13).

$$0<\mu<<\frac{1}{g_{PA}2^{C}t_{UNIT}SF} \tag{2.4.13}$$

Chapter 3. Phase Noise Modeling

3.1 Introduction

A comprehensive analytic phase noise model for the adaptive phase cancellation architecture is necessary for generating confident estimates that not only help to validate the design with comparisons of the model results to measurements but also serve as a means of informing block designs for subsequent implementations.

3.2 PLL Phase Noise Model

The fractional-N PLL output phase noise can be estimated using the frequency domain, linear time-invariant (LTI) model in Fig. 3.2.1. Table 3.2.1 details the PLL model parameters, transfer functions and noise power spectral densities. The model estimates the total output phase noise as the sum of individual, uncorrelated PLL noise contributors multiplied by their respective noise transfer functions. Noise functions are obtained by calculation and/or simulation of the originating sub-blocks.

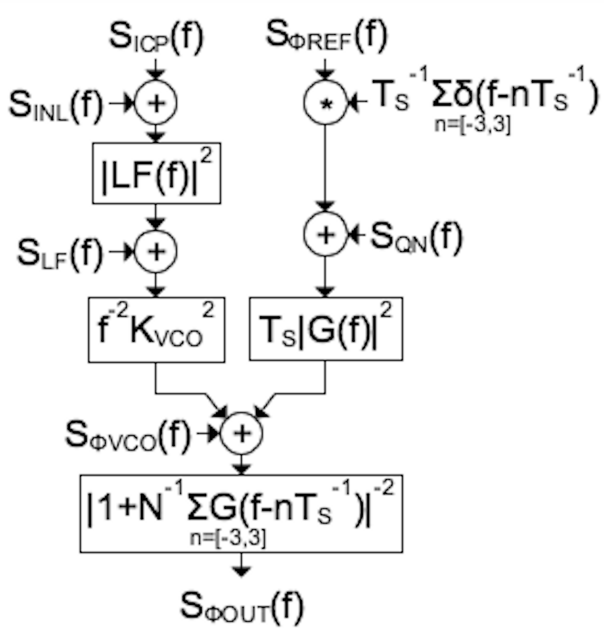

Fig. 3.2.1 Fractional-N PLL LTI phase noise model.

Table 3.2.1 Fractional-N PLL phase noise modeling parameters and noise power spectral densities (PSD).

Parameter	Description	Units
I_{CP}	Charge pump current magnitude.	A
K_{VCO}	VCO frequency vs. input voltage gain.	Hz/V
N	PLL feedback divider value.	#
T_S	PLL reference/PFD sampling period.	s
T_P	PLL PFD mean absolute time error.	s
LF(f)	PLL loop filter transfer function.	V/A
G(f)	PLL forward loop transfer function.	1
$S_{INL}(f)$	Charge pump non-linearity noise PSD.	A^2/Hz
$S_{QN}(f)$	Fractional-N based noise PSD.	rad^2/Hz
$S_{ICP}(f)$	Charge pump current noise PSD.	A^2/Hz
$S_{LF}(f)$	Loop filter voltage noise PSD.	V^2/Hz
$S_{\Phi REF}(f)$	PLL reference signal phase noise PSD.	rad^2/Hz
$S_{\Phi VCO}(f)$	VCO phase noise PSD.	rad^2/Hz
$S_{\Phi OUT}(f)$	PLL output phase noise PSD.	rad^2/Hz

PFD phase error sampling is modeled by convolving the reference and feedback signals by a limited summation of delta functions (at the reference frequency harmonics). The PLL forward loop transfer function (3.2.1) is composed of the PFD/charge pump, loop filter and VCO transfer functions. A sinc pulse function utilizing the mean absolute phase error, T_P, is utilized to approximate the conversion of the sampled phase error into a phase error pulse, which cannot be directly captured in an LTI model.

$$G(f)=\left(\frac{I_{CP}}{2\pi}\text{sinc}(\pi f T_P)\right)LF(f)\left(\frac{K_{VCO}}{if}\right) \tag{3.2.1}$$

The PFD/charge pump phase-to-charge non-linearity noise, $S_{INL}(f)$, is calculated in (3.2.2), where pr(qout) is the probability of a particular feedback divider delta-sigma modulator output qout and $Q_{CP\text{-}ERR}(t)$ is the PFD/charge pump output charge error for an input time difference t. Phase quantization cancellation does not remove this noise but reduces it by mostly cancelling out the large PFD phase error steps from the feedback divider modulation.

$$S_{INL}(f)=\frac{1}{T_S^2}\sum_{qout=Min}^{Max} pr(qout)Q^2_{CP-ERR}(qout\times t_{VCO}) \tag{3.2.2}$$

$S_{QN}(f)$ represents the fractional-N generating blocks contribution to the total PLL phase noise. In the standard fractional-N PLL architecture, $S_{QN}(f)$ is the accumulated feedback divider delta-sigma modulated quantization phase noise (Fig. 3.2.3.A). In the phase quantization cancellation fractional-N PLL architecture, $S_{QN}(f)$

is phase noise generated by the accumulated noise sources in the adaptive filter update loop and digital delay block (Fig. 3.2.2.B).

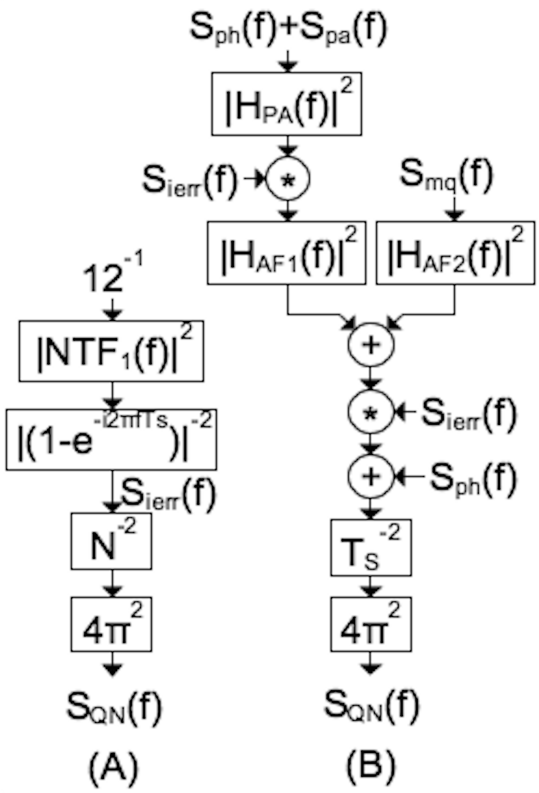

Fig. 3.2.2 Fractional-N PLL phase quantization noise model for the conventional (A) and the presented phase quantization cancellation architectures (B).

As with the adaptive update loop response equation, noise transfer equation derivations are made challenging by the ierr(n) multiplications. Noise transfer calculation is simplified by creating the equivalent block diagram in Fig. 3.2.3 where the input noise sources and output path ierr(n) multiplications are pulled out of the adaptive update loop.

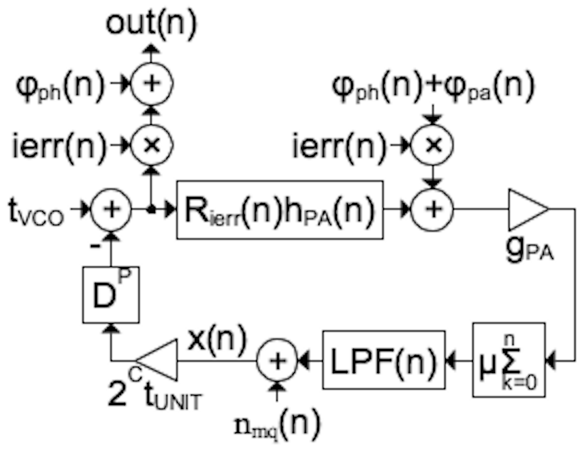

Fig. 3.2.3 Equivalent adaptive update loop for noise transfer function calculation.

Expected adaptive update loop transfer functions can be applied to the noise transfer equations while preserving the non-linear effects of the ierr(n) multiplications. The two adaptive update loop noise transfer functions are given in (3.2.3) and (3.2.4).

$$\left|H_{AF1}(z)\right|^2 = \left| \frac{\mu g_{PA} 2^C t_{UNIT} LPF(z)\left(\frac{z^{-P}}{1-z^{-1}}\right)}{1+\mu g_{PA} 2^C t_{UNIT} LPF(z)\left(\frac{z^{-P}}{1-z^{-1}}\right) F_{iPA}(z)} \right|^2 \tag{3.2.3}$$

$$\left|H_{AF2}(z)\right|^2 = \left| \frac{2^C t_{UNIT}}{1+\mu g_{PA} 2^C t_{UNIT} LPF(z)\left(\frac{z^{-P}}{1-z^{-1}}\right) F_{iPA}(z)} \right|^2 \tag{3.2.4}$$

$S_{ph}(f)$, shown in (3.2.5), models the noise contributors at the digital delay output. This includes the digital delay time quantization noise high-pass shaped by an error feedback delta-sigma modulator. Also included is the digital delay non-linearity error noise $S_{TCC}(f)$, modeled as a white noise source in (3.2.6), where pr(D)

is the probability of control word D with associated digital delay $t_D(D)$. For a DWA digital delay, the non-linearity noise is approximately the same magnitude but with 1st order high-pass noise shaping, as shown in (3.2.7).

$$S_{ph}(f) = S_{TCC}(f) + \frac{t_{UNIT}^2}{12}\left|NTF_2(f)\right|^2 \tag{3.2.5}$$

$$S_{TCC}^{'}(f) = \sum_{D=0}^{Max} pr(D)\left[t_{UNIT}\left(D - D_{OFF}\right) - t_D(D) + t_D(D_{OFF})\right]^2 \tag{3.2.6}$$

$$S_{TCC}(f) = \begin{Bmatrix} S_{TCC}^{'}(f): & \text{for binary decode,} \\ S_{TCC}^{'}(f)\left|1 - e^{-i2\pi T_S f}\right|^2: & \text{for DWA decode} \end{Bmatrix} \tag{3.2.7}$$

$S_{pa}(f)$, detailed in (3.2.8), includes the phase aligner 1-bit phase detector input referred quantization error, the phase aligner feedback delay quantization error and the PLL reference and feedback phase noise.

$$S_{pa}(f) = \frac{1}{g_{PA}^2}\frac{\left(2\right)^2}{12} + \frac{t_{PA}^2}{12} + \frac{T_S^2}{4\pi^2}\left(S_{\phi REF}(f) + S_{\phi FBK}(f)\right) \tag{3.2.8}$$

$S_{qn}(f)$ estimates using the analytic model and time-domain (Verilog and Simulink) simulation (for the adaptive phase quantization cancellation implementation described in the following section) are plotted in Fig. 3.2.4 for standard fractional-N mode, adaptive phase quantization cancellation without digital delay non-linearity noise, and with and without DWA non-linearity noise. In this instance, the analytic model provides a good estimate of the time-domain simulation

results, showing the dominance of the digital delay non-linearity noise (with and without DWA) followed by the digital delay time quantization noise.

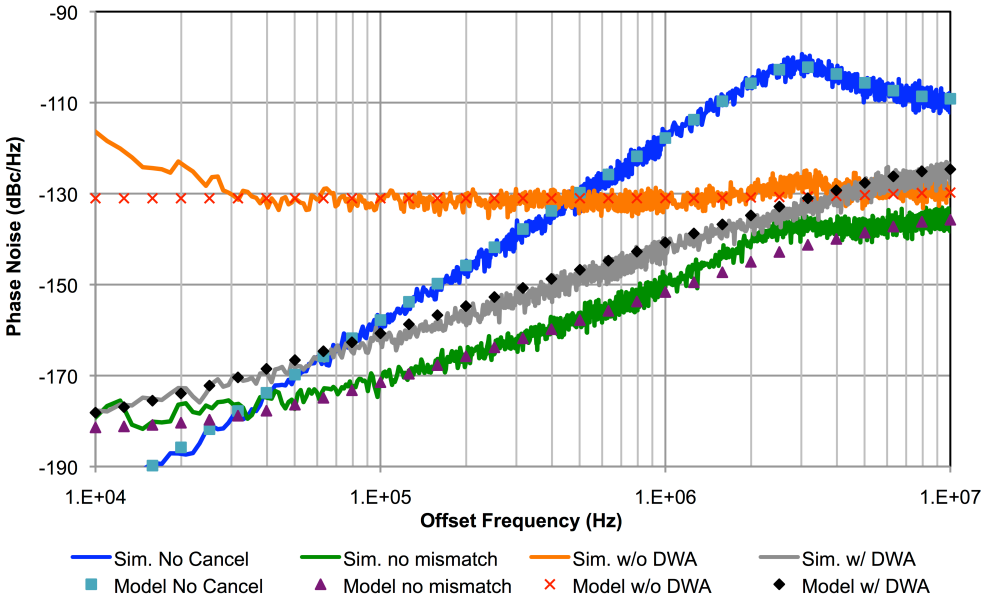

Fig. 3.2.4 Modeled and simulated fractional-N PLL phase quantization noise with no cancellation, cancellation with and without delay mismatch and cancellation with DWA delay mismatch.

Additional testing shows less correspondence between modeled and simulated results when phase aligner based noise contributors dominate $S_{QN}(f)$, though this is expected as the majority of model approximations are made in this block. The analytic model is also incapable of estimating spurious tone generation, which can only be examined using time-domain simulation. As further supporting evidence of the analytic noise model, the adaptive multiplier x(n) noise power spectral density estimate also compares closely to the time-domain simulation (Fig. 3.2.5).

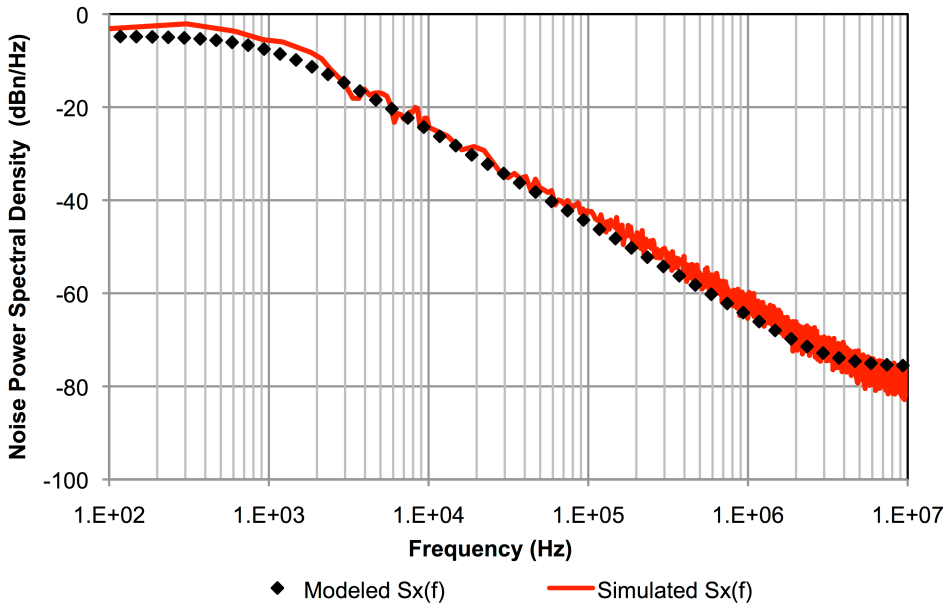

Fig. 3.2.5 Modeled and simulated adaptive multiplier x(n) noise.

Several design observations can be made from the analytic phase quantization cancellation phase noise model. First, it is necessary to have a zero mean ierr(n) as any DC component will mix adaptive multiplier x(n) noise to low frequency. Therefore, the feedback divider delta-sigma modulator is required to generate zero mean ierr(n). Next, multiplier x(n) and output code word D(n) quantization can be significant noise contributors. Their total noise contribution can be mitigated with the low-pass filter design and use of an error feedback delta-sigma modulator for quantization noise shaping, respectively. Digital delay non-linearity noise can also be a dominate noise contributor making it essential for implementations seeking the minimum attainable phase noise to employ dynamic element matching digital delay. Lastly, both the model and time-domain simulation results indicate that the adaptive filter update loop itself is not a significant noise

source and can be left perpetually active, rather than just for initial calibration, without degrading the PLL output phase noise.

Chapter 4. Implementation

4.1 Introduction

While the phase quantization cancellation architecture is targeted primarily for IC fractional-N PLL application, a printed circuit board (PCB) implementation, shown in Fig. 4.1.1 and Fig. 4.1.2, was fabricated with commercially available ICs for experimentation and proof of concept. Of the previously mentioned phase quantization cancellation techniques, only this one can be readily implemented on a PCB. As no dynamic element matching digital delay ICs were commercially available, a standard binary decoded digital delay was used. The resulting unshaped digital delay non-linearity noise does not allow the minimum attainable output phase noise to be measured. However, this implementation is sufficient to prove the adaptive phase quantization noise cancellation architecture operation.

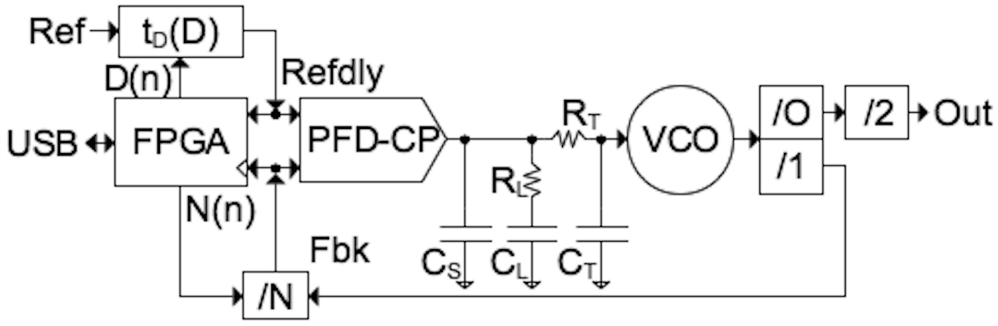

Fig. 4.1.1 Implemented fractional-N PLL with adaptive quantization noise cancellation.

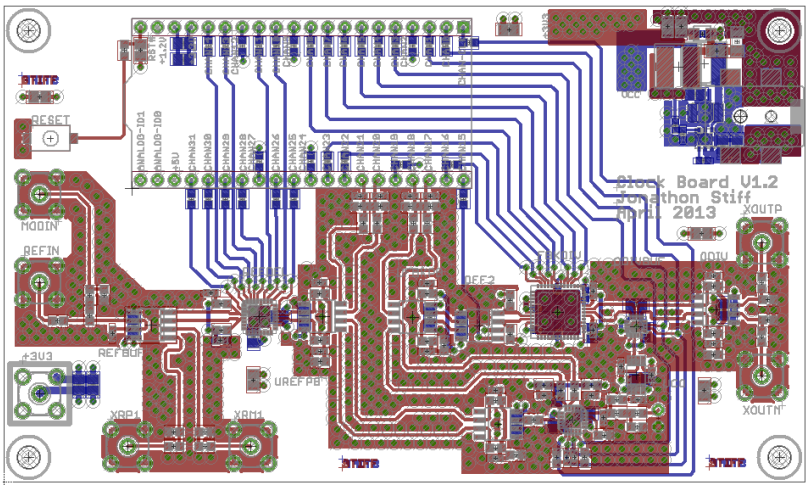

Fig. 4.1.2 Implemented fractional-N PLL PCB diagram.

4.2 PLL

The PLL is entirely composed of commercial ICs including the PFD and charge pump, passive loop filter, feedback divider, output dividers, signal buffers and a 2.4 GHz center frequency LC-VCO (Table 4.2.1). A 20 MHz crystal oscillator generates the PLL reference signal. The 1.6 MHz PLL closed loop bandwidth (N_{INT}=124) was verified by measurement (Fig. 5.4.2).

Table 4.2.1 Implemented fractional-N PLL parameters.

Parameter	Description	Value(s)	Units
K_{VCO}	VCO frequency vs. voltage gain.	110	MHz/V
F_{VCO}	VCO frequency.	2.3-2.5	GHz
F_{REF}	Reference frequency.	20	MHz
I_{CP}	Charge pump current magnitude.	4.6	mA
C_L	Loop filter capacitor.	2.2	nF
C_S, C_T	Loop filter capacitors.	22	pF
R_L	Loop filter resistor.	1.69	kΩ
R_T	Loop filter resistor.	50	Ω
N	Feedback divider value.	115-125	#
O	Output divider values.	2, 4, 8, 16	#
CLBW	PLL closed loop bandwidth (N_{INT}=124).	1.6	MHz
CLPK	PLL closed loop peaking.	0.4	dB

4.3 Digital Delay

A 10 ps resolution, 10-bit digital skew adjustment IC is utilized for the phase cancellation digital delay block (Table 4.3.2). The digital delay was placed in the reference signal path, rather than the feedback path, in order to avoid PLL stability degradation. This modification requires only a sign change in the digital delay correction word D(n) path.

Table 4.3.2 Digital delay IC parameters.

Parameter	Description	Value(s)	Units
$t_{D\text{-}RANGE}$	Nominal digital delay range	10240	ps
t_{UNIT}	Nominal digital unit delay	10	ps

4.4 FPGA

The phase aligner, digital logic and signal processing blocks are implemented with a Xilinx Spartan 3A FPGA ([20]). A USB interface provides digital logic block configuration and monitoring for experimental measurements.

A. *Feedback Divider Delta-Sigma Modulator*

The 3rd order, 19-bit input, 3-bit output feedback divider delta-sigma modulator design (Fig. 4.4.1) utilizes a single feedback, input feed forward architecture ([17]) in order to fulfill the zero mean ierr(n) requirement and provide an all-pass transfer function, as described in (4.4.1), (4.4.2), (4.4.3) where $a_{DS0\text{-}2}$ are constants. The modulator has a ±0.5 input range with less than 2 ppm (parts per million) resolution. By generating ierr(n) within the modulator loop, an additional external accumulator is saved in the design. Dither is generated with a linear feedback shift register based design ([14],[15]) for spurious tone reduction.

$$L(z) = a_{DS0} z^{-1} + a_{DS1} \frac{z^{-2}}{\left(1 - z^{-1}\right)^1} + a_{DS2} \frac{z^{-3}}{\left(1 - z^{-1}\right)^2} \tag{4.4.1}$$

$$NTF_1(z) = \frac{z^{-1}(1 - z^{-1})}{1 + z^{-1}\left(L(z) - 1\right)} \tag{4.4.2}$$

$$out(z) = in(z) z^{-1} + Q(z) NTF_1(z) \tag{4.4.3}$$

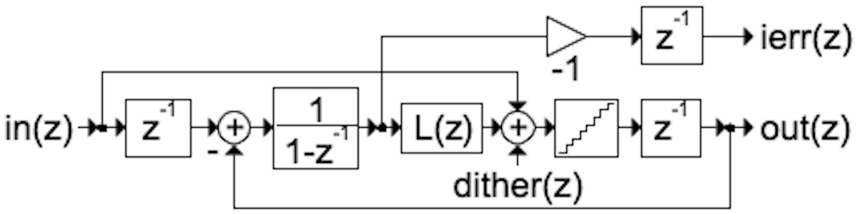

Fig. 4.4.1 Feedback divider delta-sigma modulator.

B. *Digital Phase Aligner*

The 2nd order digital phase aligner (Fig. 4.4.2) is implemented with the digital loop filter in (4.4.4), where $a_{PA0\text{-}1}$ are constants. The digital delay line is composed of a 64-element FPGA arithmetic carry chain path with a unit delay t_{PA}=69-90 ps. The delay line phases are sampled by a fixed delayed feedback signal with the loop filter selecting the phase detector output. A logic block following the delay register guarantees monotonic delay. The atypical phase aligner design is a result of limited FPGA resources, but proves adequate for this implementation.

$$F_{PA}(z)=\frac{a_{PA0}z^{-1}}{\left(1-z^{-1}\right)^{1}}+\frac{a_{PA1}z^{-1}}{\left(1-z^{-1}\right)^{2}} \tag{4.4.4}$$

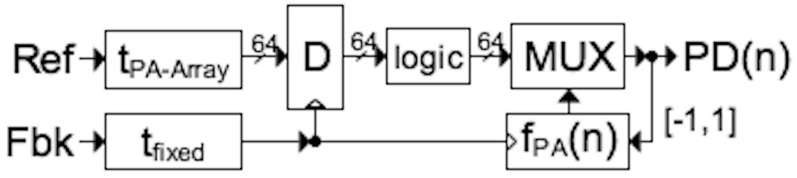

Fig. 4.4.2 Digital phase aligner.

C. *Adaptive Filter Blocks*

LPF(n) is implemented with a 2nd order digital Butterworth low-pass filter where the multiplier x(n) is quantized from 24 to 9 signed bits. Prior to multiplication

with ierr(n), x(n) is limited to ±0.5 and offset by the ideal expected value of 1.25. The 24x10 bit multiplication is implemented with two internal 16x16 bit FPGA multipliers. The resulting product is truncated to 10-bits using a 1st order error feedback delta-sigma modulator with noise transfer function in (4.4.5) and offset (nominally) to ½ the maximum digital delay value.

$$NTF_2(z) = 1 - z^{-1} \tag{4.4.5}$$

Chapter 5. Measurements

5.1 Introduction

Measurements of the implemented adaptive phase quantization cancellation fractional-N PLL are designed to verify the operation and test the performance of the new architecture. This includes comparing the measured results to those estimated in the analytic frequency domain and time-domain (Verilog, Simulink) models. The measurements presented include the output frequency, PFD/charge pump linearity, PLL closed loop transfer function, output phase noise and adaptive multiplier x(n).

5.2 Output Frequency

The implemented fractional-N PLL output frequency (and frequency error) was measured over several N_{FRAC} values in standard fractional-N mode (Fig. 5.2.1) in order to verify correct fractional frequency operation. The measurements were repeated in adaptive phase quantization cancellation mode (Fig. 5.2.2) in order to confirm the new architecture has no impact on output frequency. Both sets of measurements show the correct output frequencies in both fractional-N PLL modes.

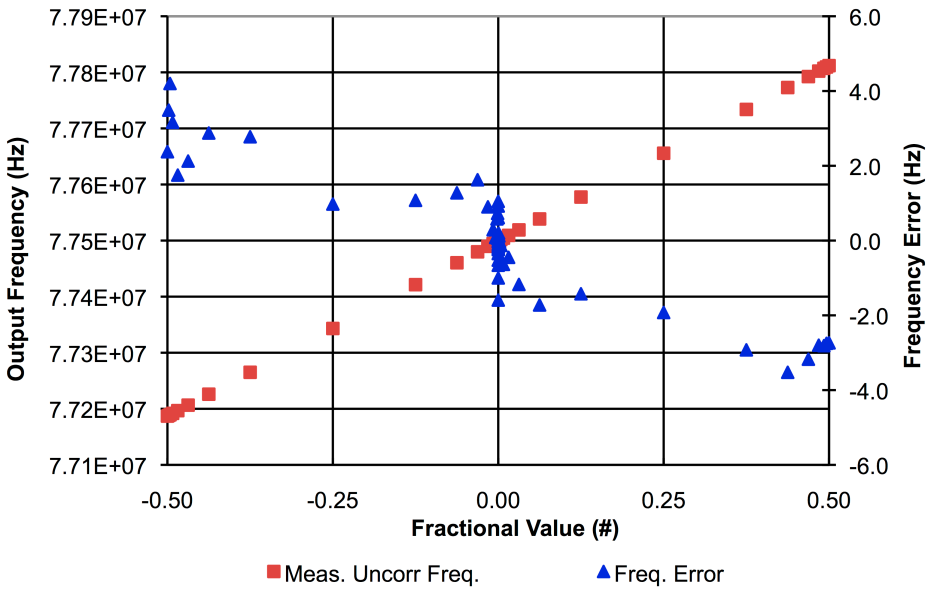

Fig. 5.2.1 Measured implemented fractional-N PLL output frequency and frequency error vs. N_{FRAC} in standard fractional-N mode.

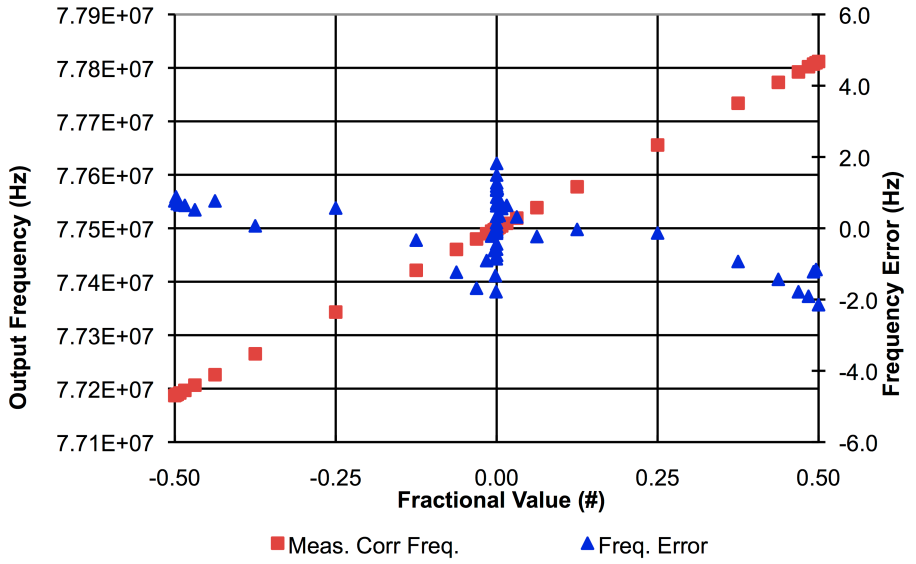

Fig. 5.2.2 Measured implemented fractional-N PLL output frequency vs. N_{FRAC} in adaptive phase quantization cancellation mode.

5.3 PFD/Charge Pump Linearity

The implemented fractional-N PLL PFD/charge pump average output current vs. input phase error (Fig. 5.3.1) was measured by injecting current into the PLL loop filter and observing the resulting PLL generated PFD phase shift necessary to overcome the injected charge and remain phase locked. Measurements taken between ±800 ps in Fig. 5.3.2 reveal a noticeable non-linearity near 0 ps phase error. The measured PFD/charge pump average output current vs. input phase error curve was added to the time-domain simulation model in order to make more accurate output phase noise predictions. The measured non-linearity is also consistent with the magnitude of implemented fractional-N PLL PFD/charge pump non-linearity noise observed in output phase noise measurements.

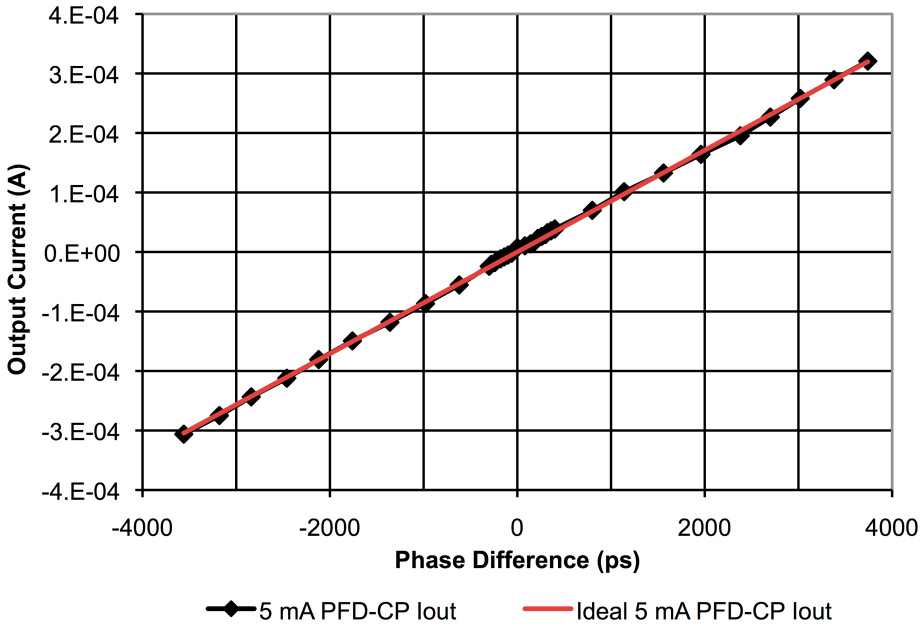

Fig. 5.3.1 Implemented fractional-N PLL measured PFD-charge pump average output current vs. input phase error (±3500 ps).

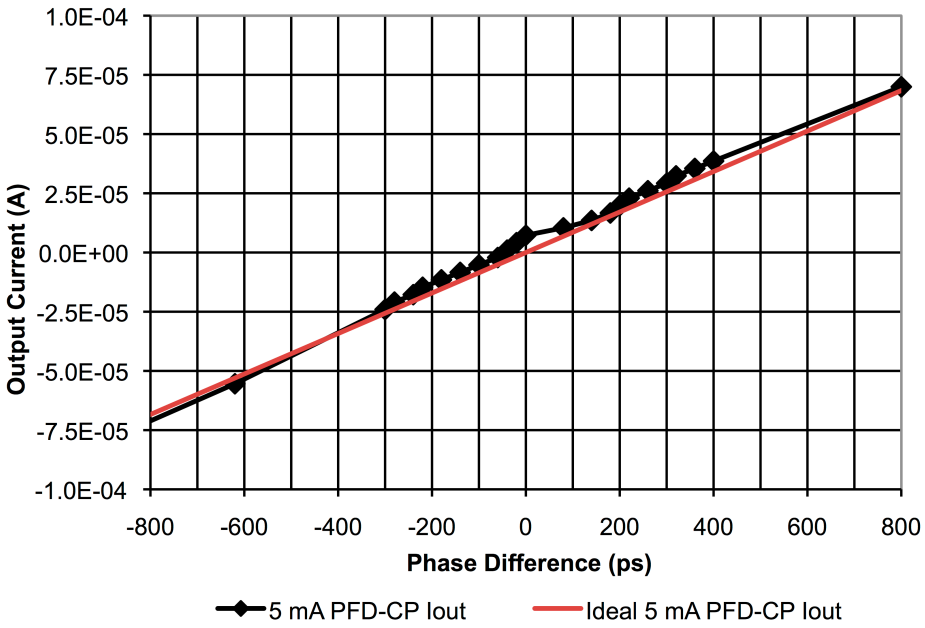

Fig. 5.3.2 Implemented fractional-N PLL measured PFD-charge pump average output current vs. input phase error (±800 ps).

5.4 PLL Closed Loop Transfer Function

The implemented fractional-N PLL closed loop transfer function was measured by modulating the PLL reference signal with a varying frequency, small signal sinusoid and observing the resulting output tone at the same frequency with a spectrum analyzer (Fig. 5.4.1). The relative output tone magnitude vs. frequency traces the PLL closed loop transfer function. The measured closed loop transfer function in Fig. 5.4.2 closely matches the modeled function.

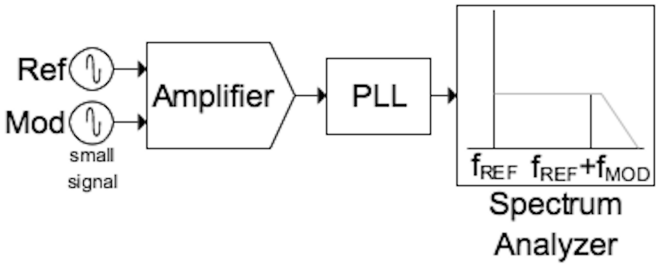

Fig. 5.4.1 PLL closed loop transfer function measurement setup.

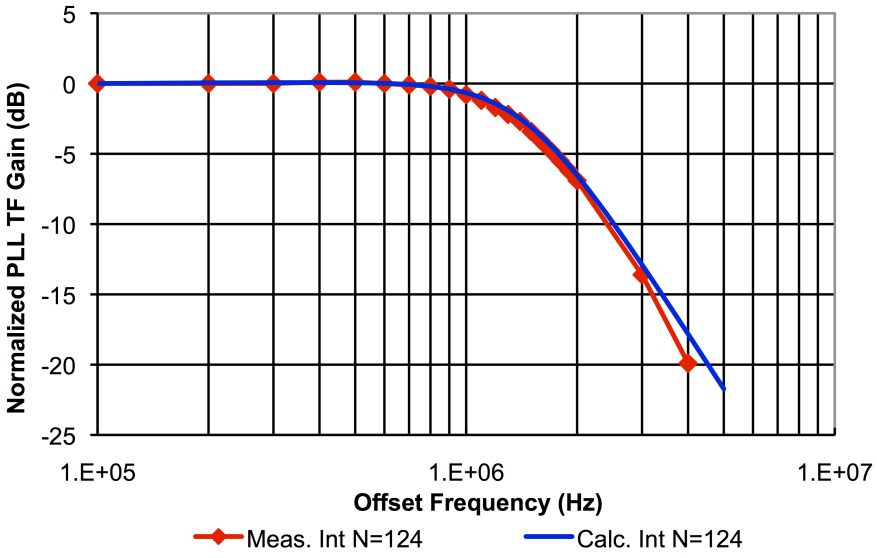

Fig. 5.4.2 Measured and calculated implemented PLL closed loop transfer function.

5.5 Output Phase Noise

Output phase noise is the primary measurement for demonstrating the operation of the adaptive phase quantization cancellation architecture. Measured and modeled output phase noise for the implemented PLL is shown in Fig. 5.5.1 for integer-N, standard fractional-N and fractional-N with adaptive phase quantization cancellation modes of the implemented device at 155 MHz. Comparison of the phase quantization cancellation and the standard fractional-N mode phase noise plots demonstrates up to a 25 dB noise reduction. Spurious tones at 50 kHz, 3 MHz

and 5 MHz (including harmonics) originate from the PCB power supply and FPGA module.

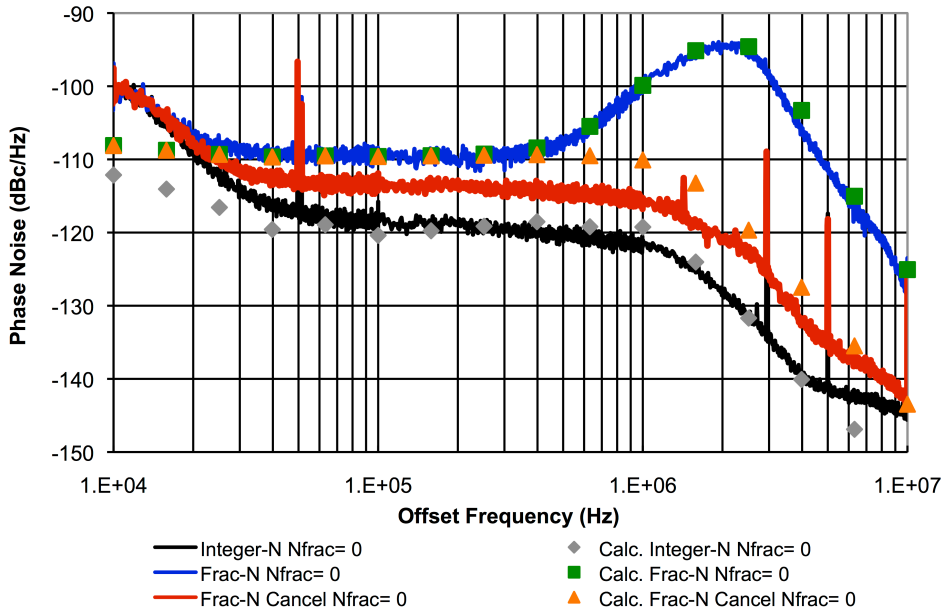

Fig. 5.5.1 Measured and modeled PLL phase noise for integer-N and fractional with and without adaptive phase quantization cancellation (N_{INT}=124, F_{OUT}=155.00 MHz) modes (using HP11729B phase noise system).

Phase quantization cancellation mode output phase noise measurements for several N_{FRAC} values are shown in Fig. 5.5.2. Spurious tones are generated for different N_{FRAC} values and are mainly attributable to the non-linear digital delay. In-band PLL phase noise also varies with N_{FRAC} where, from the analytic phase noise model and time-domain simulation, the digital delay non-linearity noise is predicted as the dominant source. This prediction is supported from (3.2.6) where variation in N_{FRAC} changes the digital delay correction word D(n) frequency and, therefore, the digital delay non-linearity noise. Similar measured in-band phase noise variation with D_{OFFSET}, which only has the effect of changing the digital delay correction word frequency but not the actual delay correction, further supports this hypothesis.

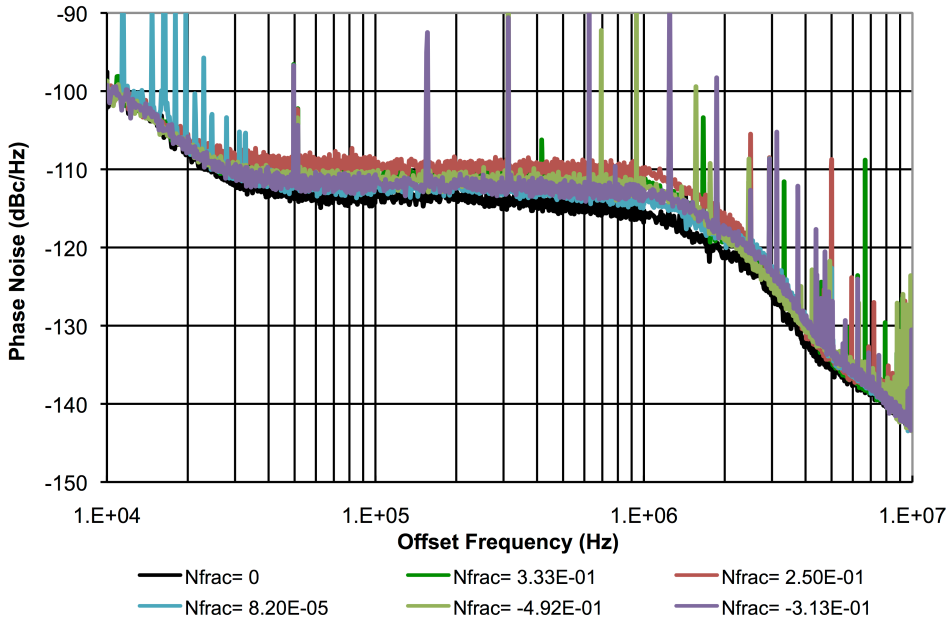

Fig. 5.5.2 Measured adaptive phase quantization cancellation phase noise for several N_{FRAC} values (N_{INT}=124, F_{OUT}=154.39-155.42 MHz) (using HP11729B phase noise system).

5.6 Adaptive Filter Update Loop

While the previous measurements demonstrate the phase noise reduction achieved with the adaptive phase cancellation architecture, they do not prove a correctly operating adaptive update loop as even a very non-optimal adaptive multiplier x(n) solution can decrease output phase noise. One method for directly testing the adaptive design is to measure the average x(n), over VCO frequency, F_{VCO}, for several N_{FRAC} values. The ideal optimal x(n) in (5.6.1) scales inversely with F_{VCO} and the average digital unit delay, t_{UNIT}. Therefore, if the adaptive phase quantization cancellation is operating correctly, x(n) will follow (5.6.1) with some expected variation due to control word D(n) dependent digital delay non-linearity.

$$x_{IDEAL} = \left(32 t_{UNIT} F_{VCO}\right)^{-1} \tag{5.6.1}$$

Average x(n) measurements, taken over 400 non-consecutive samples, vs. F_{VCO} are shown in Fig. 5.6.2. The measurements for N_{FRAC}=0 (taken immediately after PLL reset) represent a special case with a smaller D(n) set, reducing average t_{UNIT} variation from digital delay non-linearity. Measurements of x(n) vs. F_{VCO} in this mode correspond closely to (5.6.1) for t_{UNIT}=10 ps. For other N_{FRAC} values with a larger D(n) set, the plots are less linear with an average t_{UNIT}=9.1-9.4 ps but still follow the expected linear curve. All data indicate the adaptive update loop achieving an x(n) solution that is consistent with prediction.

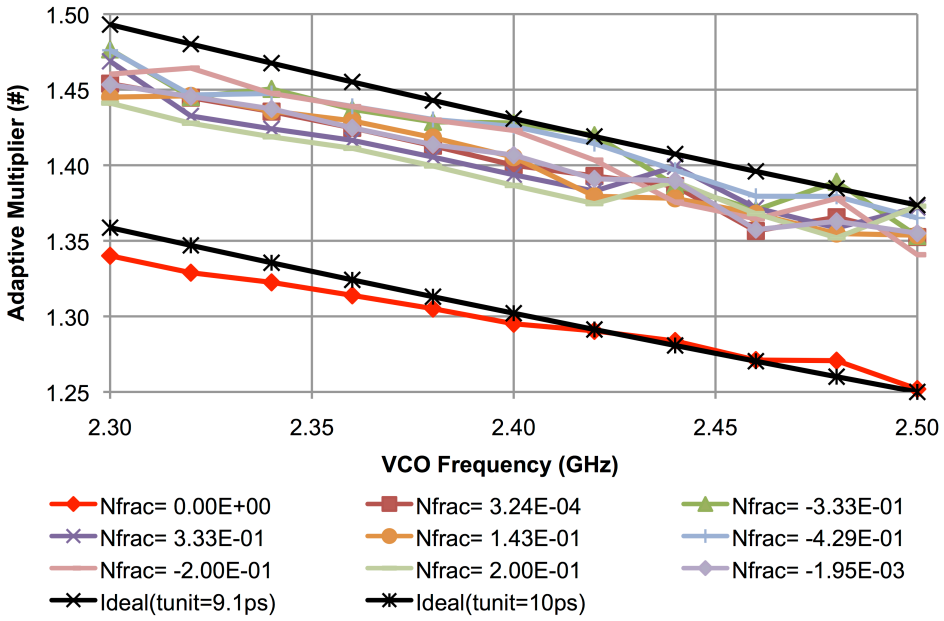

Fig. 5.6.2 Measured adaptive multiplier vs. VCO frequency for multiple N_{FRAC} values (where ideal represents calculated linear delay).

Chapter 6. Conclusions

6.1 Introduction

The presented dissertation conclusions include an adaptive phase quantization cancellation fractional-N PLL architecture design summary, the expected output phase noise using DWA digital delay and comments about future implementations for this architecture.

6.2 Design Summary

The presented adaptive phase quantization cancellation fractional-N PLL architecture was shown, by model results and measurements of the implemented architecture, to substantially and predictably reduce fractional-N feedback divider modulator quantization error. A detailed analytic frequency-domain phase noise model was developed and shown to closely correlate to time-domain simulation and measurement results. Finally, the architecture was shown to be simpler to implement than previous phase quantization cancellation solutions. This is highlighted by the presented architecture being implemented on a PCB without custom components, which was not possible for the prior architectures.

6.3 Output Phase Noise with DWA Digital Delay

Due to the good correlation between modeled, simulated and measured phase noise for the implemented adaptive phase quantization cancellation fractional-N PLL, a reasonable phase noise estimate when using a 1^{st} order high-pass noise

shaping DWA digital delay (described in (3.2.7)) can be made with confidence. Fig. 6.3.1 presents the estimated phase noise using DWA digital delay along with the modeled integer-N, fractional-N and adaptive phase quantization cancellation fractional-N with binary decoded digital delay phase noise. The estimated phase noise achieves the desired result of integer-N mode performance at PLL in-band frequencies while still being substantially less than the standard fractional-N mode at high frequency. Not shown are the possible DWA induced spurious tones, which are inherent in its 1st order noise shaping ([11], [12]). DWA dither algorithms, demonstrated in [7], can be utilized to reduce the spurious tones.

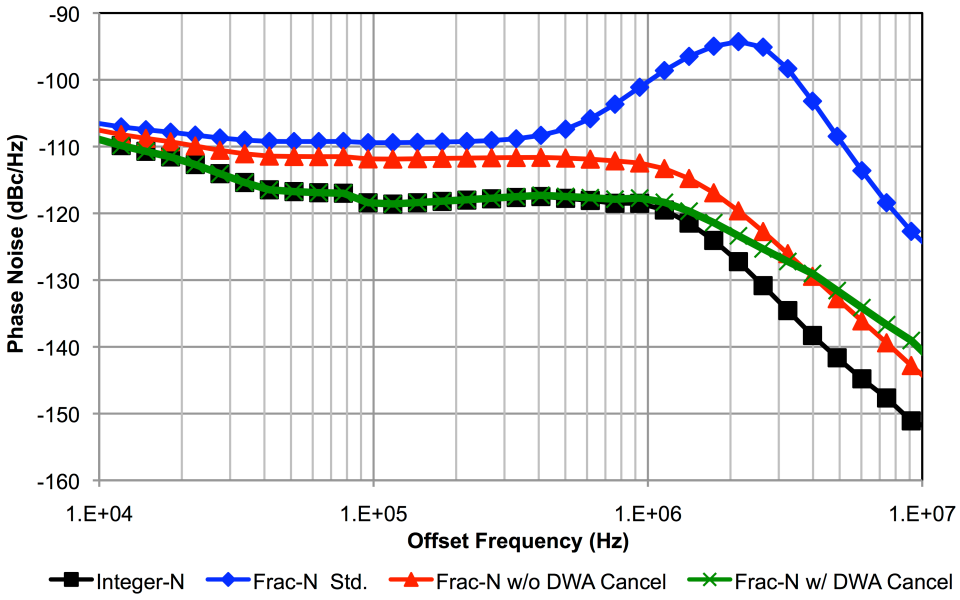

Fig. 6.3.1 Implemented fractional-N PLL modeled and simulated output phase noise for integer-N, fractional-N, fractional-N with adaptive phase cancellation with and without DWA digital delay (155 MHz output).

6.4 Future Implementations

While the presented adaptive phase quantization cancellation fractional-N architecture implementation was designed as a proof of concept with an eye to experimentation and easier observation, subsequent IC implementations should exploit its simplicity of design with a focus on minimizing block sizes based on particular application requirements. For example, the feedback modulator can be reduced to as low as 2^{nd} order and, in some implementations, an adaptive update loop low-pass filter may be determined unnecessary to meet output phase noise specifications. As a majority of the design is implemented in relatively low frequency (10-100 MHz) logic blocks, it is also exceedingly portable as an HDL synthesizable block to be applied to any desired technology. Alternatively, the design can be implemented as software on one or more embedded processors.

Glossary

ADC	Analog-to-digital converter.
D(n)	Digital delay control word (at discrete time n).
DAC	Digital-to-analog converter.
DEM	Dynamic element matching.
DWA	Data weighted averaging.
e(n)	Phase locked loop (PLL) reference and feedback phase difference or error (at discrete time n).
$e_{PA}(n)$	Digital phase aligner corrected phase locked loop (PLL) reference and feedback phase difference or error (at discrete time n).
$f_{PA}(n)$	Digital phase aligner loop filter impulse response function.
$F_{PA}(z)$	Digital phase aligner loop filter z-domain, $Z(f_{PA}(n))$, transfer function.
G(f)	Phase locked loop (PLL) forward path frequency-domain transfer function.
g_{PA}	Digital phase aligner 1-bit quantizer approximate gain.
$h_{PA}(n)$	Digital phase aligner impulse response function.

$H_{PA}(z)$	Digital phase aligner z-domain, $Z(h_{PA}(n))$, transfer function.
I_{CP}	Phase locked loop (PLL) charge pump current magnitude (in Amperes).
Ierr(n)	Phase locked loop (PLL) feedback divider delta-sigma modulator accumulated output error (at discrete time n).
K_{VCO}	Voltage controlled oscillator (VCO) output frequency vs. input voltage gain (in Hz/V).
LF(f)	Phase locked loop (PLL) loop filter frequency-domain transfer function.
LMS	Least mean square.
LPF(n)	Low-pass filter impulse response function.
LTI	Linear time-invariant.
N(n)	Phase locked loop (PLL) feedback divider value (at discrete time n).
NTF(z)	Noise transfer function (in the z-domain).
PD(n)	Digital phase aligner 1-bit phase detector output (at discrete time n).
PFD	Phase locked loop (PLL) phase-frequency detector.

PFD/CP	Phase locked loop (PLL) phase-frequency detector and charge pump.
PLL	Phase locked loop.
ppm	Parts-per-million.
PSD	Power spectral density.
$\mathbf{t_{VCO}}$	Voltage controlled oscillator (VCO) period (in seconds).
$\mathbf{t_{UNIT}}$	Digital delay resolution (in seconds).
VCO	Voltage controlled oscillator.
$\mathbf{R_{ierr}(n)}$	Phase locked loop (PLL) feedback divider delta-sigma modulator accumulated output error, ierr(n), autocorrelation function.
$\mathbf{S_{ierr}(z)}$	Phase locked loop (PLL) feedback divider delta-sigma modulator accumulated output error, ierr(n), noise power spectral density function (in the z-domain).
$\mathbf{S_{INL}(f)}$	Phase locked loop (PLL) charge pump non-linearity noise power spectral density (PSD) function.
$\mathbf{S_{ICP}(f)}$	Charge pump current noise power spectral density (PSD) function.
$\mathbf{S_{LF}(f)}$	Loop filter voltage noise power spectral density (PSD) function.

$S_{ph}(f)$	Cumulative digital delay noise power spectral density (PSD) function.
$S_{QN}(f)$	Phase locked loop (PLL) fractional-N generation (in standard and phase cancellation models) based noise power spectral density (PSD) function.
$S_{TCC}(f)$	Digital delay non-linearity noise power spectral density (PSD) function.
$S_{\Phi REF}(f)$	Phase locked loop (PLL) reference signal phase noise power spectral density (PSD) function.
$S_{\Phi OUT}(f)$	Phase locked loop (PLL) output phase noise power spectral density (PSD) function.
$S_{\Phi VCO}(f)$	Phase locked loop (PLL) voltage controlled oscillator (VCO) phase noise power spectral density (PSD) function.
$t_D(D)$	Digital delay value for a given control word D (in seconds).
T_P	Phase locked loop (PLL) phase-frequency detector (PFD) mean absolute time error.
t_{PA}	Digital phase aligner delay resolution (in seconds).
T_S	Sample period.
$x(n)$	Adaptive filter multiplier (at discrete time n).

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