Silicon Photonics: Overview, Building Block Modeling, Chip Design and its Driving Integrated Circuits Co-Design

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Rui Wang

Major Professor: Herbert L. Hess, Ph.D.

Committee Members: Feng Li, Ph.D.; Yacine Chakhchoukh, Ph.D.;

Kumar Gautam, Ph.D.

Department Administrator: Joseph D. Law, Ph.D.

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Authorization to Submit Dissertation

This dissertation of Rui Wang, submitted for the degree of Doctor of Philosophy with a major in Electrical Engineering and titled "Silicon Photonics: Overview, Building Block Modeling, Chip Design and its Driving Integrated Circuits Co-Design," has been reviewed in final form. Permission, as indicated by the signatures and dates given below, is now granted to submit final copies to the College of Graduate Studies for approval.

Major Professor:	Herbert L. Hess — Digitally signed by Herbert L. Hess DN: cn=Herbert L. Hess, o=University of Idaho, ou=Dept of ECE, email=hhess@uidaho.edu, c=US Date: 2020.06.22 11:53:57 -07'00'	Date:	22 June 2020
	Herbert L. Hess, Ph.D.		
Committee Members:	Feng Li — Digitally signed by Feng Li Date: 2020.06.23 15:26:22 -07'00'	Date:	6/23/2020
	Feng Li, Ph.D.		
	Yacine Chakhchoukh — Digitally signed by Yacine Chakhchoukh Date: 2020.06.23 15:51:15 -07'00'	Date:	6/23/2020
	Yacine Chakhchoukh, Ph.D.		
	Gautam Kumar — Digitally signed by Gautam Kumar Date: 2020.06.24 13:41:51 -07'00'	Date:	6/24/2020
	Kumar Gautam, Ph.D.		
Department Administrator:	Joseph D. Law — Digitally signed by Joseph D. Law Date: 2020.06.25 11:32:02 -07'00'	Date:	6/25/2020
	Joseph D. Law, Ph.D.		

Abstract

This dissertation presents a complete design flow for realizing my proposed silicon-based photonics circuits, which are able to generate multi-level optical signal outputs. The design flow only depends on the tools that are accessible to traditional integrated circuits designers and overcomes the need to produce specific design tools for photonic circuit design. The proposed photonics circuits use the heterogenerous integration method where the optical circuits are fabricated using IMEC-ePIXfab SiPhotonics ISIPP50G technology and the electrical circuits are simulated using the PDK of TSMC 65nm technology.

Compact Verilog-AMS modelings for optical blocks are developed, which include the models for continuous-wave lasers, couplers, photodiodes, electro-absorption modulators and waveguides/phase-shifters. All of the parameters used in the models above are derived from either the testing results of the standard microring modulator or the corresponding optical devices provided by IMEC ISIPP50G technology.

A coupling-based microring modulator, which is based on IMEC ISIPP50G technology, has been proposed and its design is realized using Verilog-A model in Cadence Virtuoso. The final simulation results show that the proposed coupling-based microring modulator is able to realize extinction ratio as large as 46dB when both the coupling coefficient tuning and resonant wavelength shifting are enabled.

A photonic chip with the block size of $2500\mu m$ and $2500\mu m$ was fabricated using IMEC ISIPP50G technology and a PCB board for testing has been designed. Testing plan has been proposed and prospective testing results have been discussed.

A three-segment microring modulator—a proposed electro-optical modulator—has been proposed and is implemented in a scheme where equispaced optical PAM-4 output can be generated. The proposed scheme includes both coarse and precise tuning, which can be further categorized into lower “1” tuning and higher “0” tuning. A transmitter structure emanated from the proposed scheme is realized using TSMC 65nm LP technology and its

simulation results derived from the extracted layout show 25-Gb/s optical PAM-4 output with the extinction ratio of 9dB and the PAM-4 energy efficiency of 0.5pJ/bit. The adaptability of the scheme can be justified by the following two results: a high percentage of level separation mismatch ratio (R_{LM}) can be achieved when $\pm 10\%$ phase-shifter length variation inside the three-segment microring is present; a total number of 4800 possible PAM-4 levels can be achieved.

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Although my stay at University of Idaho is close to four years, my journey of getting my PhD degree starts from University of Rochester seven years ago. Seven year is such a long time and I have indeed learnt a lot both on how to do research and how to interact with other people in life. There were so many obstacles that I have overcome throughout these years and there is no way that I can come this far without the supports that I have received from during this time.

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Dedication

To my Mom

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List of Abbreviations

AMS	...	Analog/Mixed-Signal
AS	...	Aggregation Switch
ASP	...	Application Service Provider
AWG	...	Arrayed-Waveguide Grating
BERT	...	Bit-Error-Rate-Tester
BOX	...	Buried Oxide
CML	...	Current-Mode Logic
CMOS	...	Complementary Metal-Oxide Semiconductor
CR	...	Core Router
DCVLS	...	Differential Cascade Voltage Swing Logic
DRC	...	Design Rule Check
DRIE	...	Deep Reactive-Ion Etching
DSM	...	Deep-Submicron
DWDM	...	Dense Wavelength-Division Multiplexing
EA	...	Electro-Absorption
EAM	...	Electro-Absorption Modulator
EMI	...	Electromagnetic Interference
ER	...	Extinction Ratio
FDE	...	Finite Difference Eigenmode
FK	...	Franz-Keldysh
FSR	...	Free-Spectrum Range
FWHM	...	Full Width at Half Maximum
GCI	...	Global Cloud Index
GSiP	...	Generic Silicon Photonics
HaaS	...	Hardware as a Service

HNLFs ... Highly Nonlinear Fibers

IaaS ... Infrastructure as a Service

ICT ... Information and Communication Technology

IL ... Insertion Loss

IoT ... Internet of Things

IPSO ... Internet Protocol for Smart Objects

LOCOS ... Local Oxidation of Silicon

LSI ... Large-Scale Integration

MMF ... Multi-Mode Fiber

MMI ... Multi-Mode Interferometer

MPW ... Multi-Project Wafer

MRM ... Microring Modulator

MSI ... Median-Scale Integration

MZI ... Mach-Zehnder Interferometer

MZM ... Mach-Zehnder Modulators

NFC ... Near Field Communications

NRZ ... Non-Return-to-Zero

OCS ... Optical Circuit Switching

ONoCs ... Optical Networks-on-Chip

OPS ... Optical Packet Switching

PaaS ... Platform as a Service

PAM ... Pulse-Amplitude Modulation

PDJ ... Pattern-Dependent Jitter

PDN ... Pull-Down Network

PL ... PhotoLuminescence

PLUT	...	Programmable Logic Under Test
PMC	...	Perfect Magnetic Conductor
PML	...	Perfectly Matched Layer
POI	...	Passive Optical Interconnect
PPLN	...	Poled Lithium Niobate
QCSE	...	Quantum Confined Stark Effect
QW	...	Quantum-Well
RAMZI	...	Ring-Sssisted Mach-Zehnder Interferometer
RFID	...	Radio-Frequency IDentification
RPCVD	...	Remote Plasma-enhanced Chemical Vapor Deposition
SaaS	...	Software as a Service
SDL	...	Schematic Driven Layout
SiP	...	System-in-Package
SOAs	...	Semiconductor Optical Amplifiers
SoC	...	System-on-a-Chip
SOI	...	Silicon-on-Insulator
SSI	...	Small-Scale Integration
ToR	...	Top-of-the-Rack
TWMZM	...	Traveling-Wave Mach-Zehnder Modulator
UBC	...	University of British Columbia
ULSI	...	Ultra-Large-Scale Integration
VLSI	...	Very-Large-Scale Integration
WAN	...	Wide-Area Network
WSAN	...	Wireless Sensor and Actuator Networks
XaaS	...	Everything as a Service

Chapter 1: Introduction

1.1 Motivation

Nowadays, we are living in a world where the consumption of information is exploding on an unprecedented level and this trend is growing everyday without any sign of ever slowing down. With the advent of the Internet of Things(IoT) and cloud computing, we might even enter a new era where the information consumed by the masses will grow to a point where none of the state-of-the-art technologies can provide a possible solution.

Data center interconnect technology is at the forefront of this new era. Most of the information consumed by the masses will be either stored or processed by data centers and the speed of the data center interconnect will decide how much information this data center can handle. Although currently only upper layers of the data centers are using optical devices while the other parts use electrical devices, the electrical circuits have difficulty catching up with the current demands from the IoTs and cloud computing due to the bandwidth bottleneck of electrical I/Os. Optical I/Os usually have much higher bandwidth but are very bulky. With the maturity of the state-of-the-art IC technology, optical I/Os can be implemented using silicon-based photonics technology, which is realized using the similar facilities as that of silicon-based IC technology and can reduce the overall size of the optical I/Os.

Just like IC design, the final goal of the silicon-based photonics technology is to realize either a monolithic photonics chip, which contains both optical and electrical components or a photonics chip, which only contains optical components and is driven by an electrical chip. Unlike state-of-the-art IC design, however, there is no consensus on how to realize photonics chips as well as their driving ICs. Therefore, in my thesis, I will discuss the whole process on how to realize photonics chips from using Verilog-A modeling for optical blocks, fabricating photonics chip layout based on those optical blocks to designing their peripheral circuits.

1.2 Contributions

My dissertation puts an emphasis on the modeling and layout generation of photonics chips; design and layout implementation of a transmitter that is able to realize optical PAM-4. Specifically, the dissertation has addressed the following research topics:

- How to develop generic Verilog-A models for optical devices such as continuous-wave laser, coupler, photodiode, electro-absorption modulator, mirocring modulator, waveguide/phase-shifter, which can be used for co-simulations with electrical circuits in Cadence Virtuoso.

- How to develop a self-contained Verilog-A modeling library that is based on IMEC-ePIXfab SiPhotonics ISIPP50G technology. The resulting library should be able to generate the same results in Cadence Virtuoso as in other photonics tools such Lumerical Interconnect.

- Based on the aforementioned Verilog-A models, propose a new microring modulator, coupling-based microring modulator, which is able to improve upon state-of-the-art microring modulators in terms of extinction ratio.

- How to setup layout tool such as Klayout that can modify the layouts of individual optical component and Pyxis that is able to create global routing to connnect individual optical component through waveguides. Also, Pyxis should also be modified to create photonics chip layout based on IMEC-ePIXfab SiPhotonics ISIPP50G technology.

- How to create testing structures for the optical components on my photonics chip layout. Also, I will show the prospective testing results of the optical components using my simulation tools.

- Propose a new microring modulator, three-segment microring modulator. Proposed a scheme that is able to achieve high-speed optical PAM-4 signals with high linearity

based on this proposed modulator. Also, this scheme is able to provide much higher tuning flexibility than other state-of-the-art designs.

- Propose a transistor-level 65nm transmitter design that is based on the aforementioned scheme. The transmitter structure includes the components such as CML 4-to-1 selector, CML D-type Flip-flop, CML-to-CMOS converter, etc. and its design is verified using post-layout co-simulations in Cadence Virtuoso.

1.3 Dissertation Organization

The remaining chapters of the dissertation are organized as follows. Chapter 2 discusses two cutting edge technologies, internet of things(IoTs) and cloud computing, which are gaining popularity over the years and are pushing the data rate of the data center interconnect towards 400G. Also, pulse-amplitude modulation(PAM)-4 has been examined as another technology which is able to further increase data rate without relying on more advanced technologies. Chapter 3 demonstrates one of the solutions, silicon photonics, to satisfy the push for increasing the data rate of the data center interconnect over 400G. The background and overview of the silicon photonics are presented and specifically, the IMEC-ePIXfab SiPhotonics ISIPP50G technology has been discussed in detail, which includes basic optical devices as well as electro-optics modulators. Chapter 4 discusses the development of the Verilog-A model for photonics devices and the parameters used in those models are based on IMEC-ePIXfab SiPhotonics ISIPP50G technology. With the assistance of the behavior model, a coupling-based microring modulator is proposed, which is able to further increase the extinction ratio to as high as 46dB when both phase-shifters inside the microring and the adjustable coupler are enabled. Chapter 5 presents the process of generating the layout of my proposed silicon photonics chip, which includes the layout generation of both individual optical device and the global routing, which provides optical domain connections between optical devices. Also, the floorplan of my proposed photonics chip is described and testing

structures for the fabricated chip as well as the prospective testing results have been presented in this chapter. Chapter 6 first proposes a three-segment microring modulator and later, its simulation results based on Verilog-A model are presented. Based on the proposed three-segment microring modulator, a new scheme, which is able to achieve the level separation mismatch ratio as high as 97%, is demonstrated. The scheme is justified by performing transient simulations at the data rate of 12.5GS/s and making sure the eye-diagram can produce high percentage of level separation mismatch ratio. The adaptability of the scheme is also presented in this chapter by simulating two variations of the three-segment microring modulator and making sure the percentage of the level separation mismatch in both cases is high. To further verify the validity of the scheme, chapter 7 has proposed a transmitter structure that is able to be implemented in the transistor level. This proposed transmitter structure, based on its extraction simulation results using the PDK of TSMC 65nm technology, can achieve a data rate of 25Gb/s, an extinction ratio of 9dB, and a PAM-4 energy efficiency of 0.5pJ/bit under the driver supply of 2.4V. There are 4800 possible PAM-4 optical levels that can be realized by the proposed scheme, which further verifies the adaptability of my proposed scheme.

Chapter 2: Data Center Interconnect: the road to 400G and Beyond

2.1 Internet of Things

Back in the spring of 1999, Kevin Ashton coined the name "Internet of things"(IoT) while he prepared for a PowerPoint presentation at Procter and Gamble. Almost 20 years later, according to the Hype Cycle report for emerging technologies in 2018 as shown in Fig. 2.1 [1], expectations for the development of IoT are still high above other trending technologies such as 5G, quantum computing etc. However, IoT is not an unprecedented technology since automated teller machines(ATMs), which can be considered as some of the first IoT objects, went online as far back as 1974 [2]. On the other hand, IoT has become more and more advanced over time: from smart fridges which can text you as soon as you are out of milk, to smart homes which can help you to control the heat remotely and finally to smart cities which can control the traffic light according to the road situation [3]. Unsurprisingly, as time goes on, there will be more and more everyday objects connected to the Internet and it is reported that by 2008, there were already more objects than people connected to the Internet. Some experts forecast that by 2020, the number of Internet-connected things might even exceed 50 billion.

Let's first look at the two words from IoT: the Internet and the "things". We are all familiar with the concept of the Internet since we are using it almost every day. As for the definition of the "things", it is exactly as universal as it sounds: naturally, all of the electronic devices, gadgets and equipment that are technologically advanced and used widely in our daily life are included in the "things". What makes IoT intriguing and revolutionary is that any object or person or even animal can be considered as "things" and the only reason that they are not implemented in IoT at the moment is the limitation of the progression of technology and our own imaginations [4].

Although the definitions for both internet and things are mostly agreed upon, there

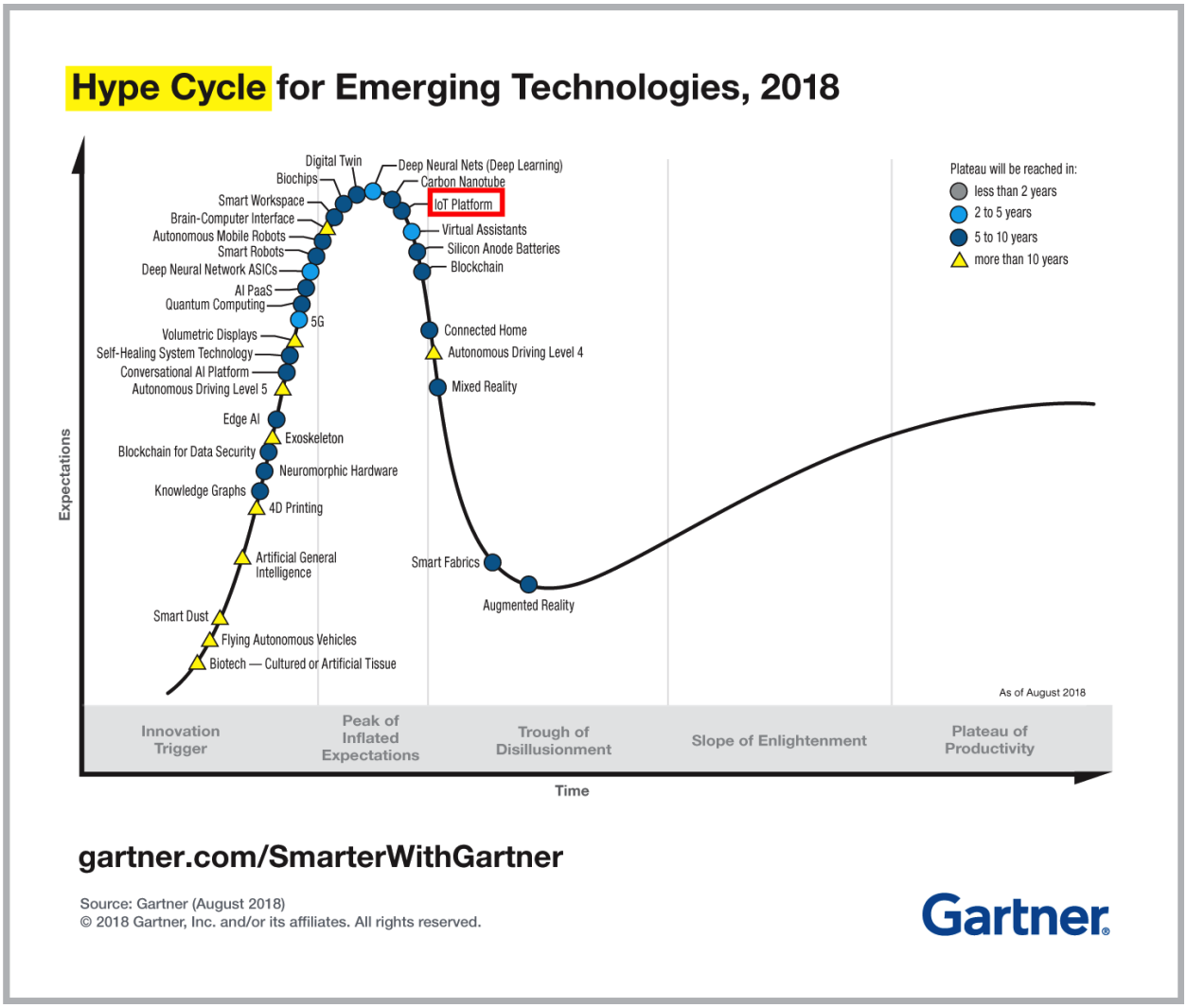

Figure 2.1: Hype Cycle for Emerging Technologies, 2018 [1]

is no universally accepted definition for the IoT. However, if we look at its definition only semantically, "Internet of Things" can mean "a world-wide network of interconnected objects uniquely addressable, based on standard communication protocols" [5].

In order to understand the concept of IoT clearer, we can approach it from three perspectives: "Internet oriented", "Things oriented" and "Semantic oriented" as shown in Fig. 2.2 where concepts, technologies and standards are grouped according to their best characterization of certain IoT vision [6].

On the forefront of the IoT application, Radio-Frequency IDentification (RFID) tags

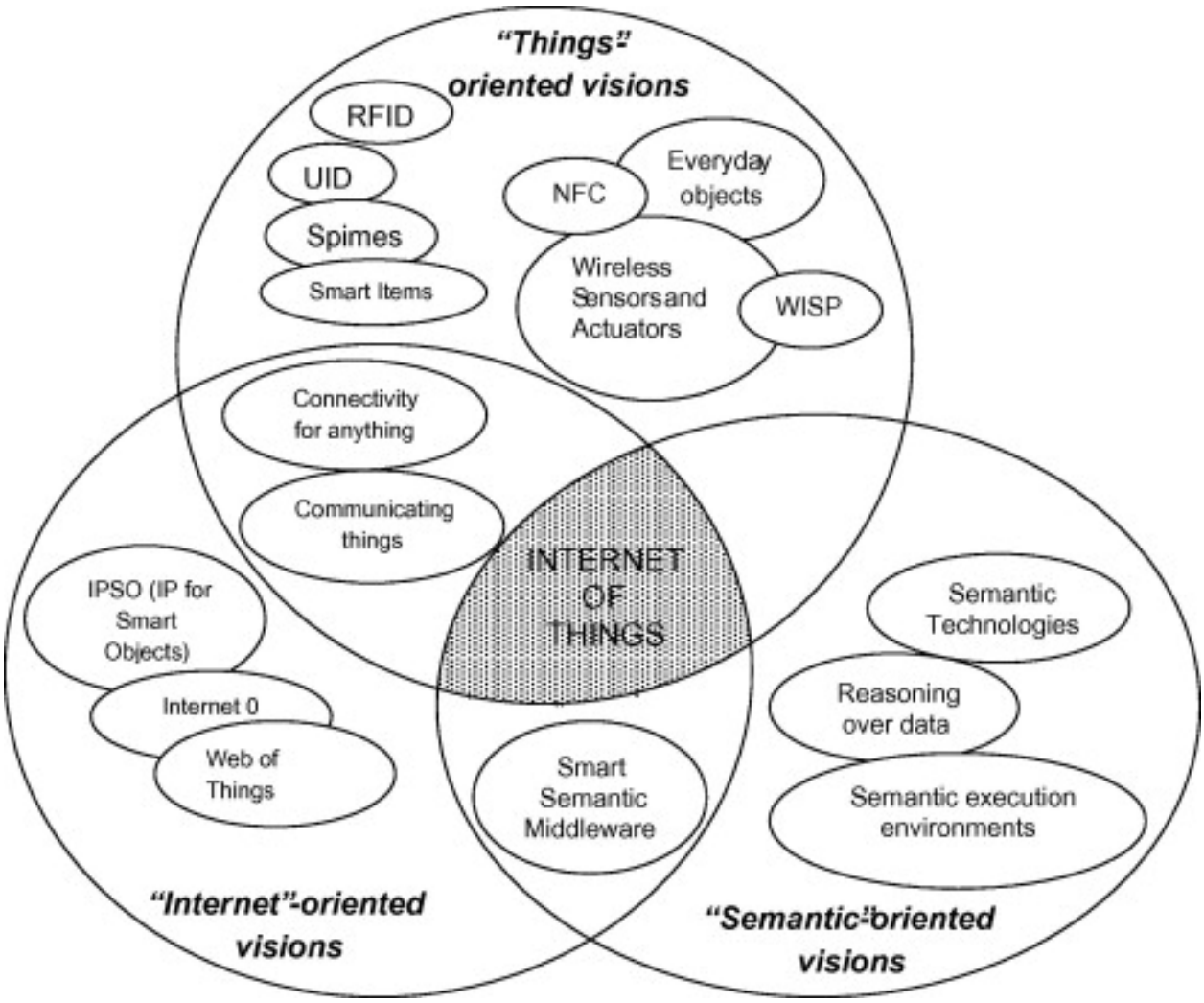

Figure 2.2: Three Perspectives of IoT
[6]

have already been used, for example, in warehouse inventory management system [8]. This technology belongs to "Things" oriented vision. Since we are still in the early stage of IoT development, the biggest challenge right now is how to connect "things" to the internet. The advent of RFID makes that happen even to everyday objects. Similar technologies such as Near Field Communications (NFC) and Wireless Sensor and Actuator Networks (WSAN) are also developed alongside RFID. However, unlike RFID used mostly for identifying items, these two technologies can make use of smart items which are capable of performing complex functions with the assistance of the Internet.

IoT Elements		Samples
Identification	**Naming**	EPC, uCode
	Addressing	IPv4, IPv6
Sensing		Smart Sensors, Wearable sensing devices, Embedded sensors, Actuators, RFID tag
Communication		RFID, NFC, UWB, Bluetooth, BLE, IEEE 802.15.4, Z-Wave, WiFi, WiFiDirect, , LTE-A
Computation	**Hardware**	SmartThings, Arduino, Phidgets, Intel Galileo, Raspberry Pi, Gadgeteer, BeagleBone, Cubieboard, Smart Phones
	Software	OS (Contiki, TinyOS, LiteOS, Riot OS, Android); Cloud (Nimbits, Hadoop, etc.)
Service		Identity-related (shipping), Information Aggregation (smart grid), Collaborative-Aware (smart home), Ubiquitous (smart city)
Semantic		RDF, OWL, EXI

Figure 2.3: IoT Elements and their Technology Examples [7]

After the implementation that "things" are connected to the internet has been realized, "Internet"-oriented visions can be considered to satisfy the ever-growing bookkeeping that come along with all of the "things" online. The advent of IPSO (IP for Smart Objects) Alliance signifies the intention to fulfill "Internet"-oriented visions by promoting Internet Protocol to connect Smart Objects all over the world [9]. Similar approaches such as Internet Φ can be used for the same purposes [10].

Another challenge that comes with IoT is the limited capacity of state-of-the-art search engine and our current search engine has a long way to go in order to provide a satisfying solution. This is where the "Semantic"-oriented visions have been proposed so as to revo-

lutionize the mechanization of search. One of the ways to achieve this vision is to develop semantic technology which provides processable semantic descriptions to the objects that belong to the IoT. By doing so, intelligent search can be achieved without human intervention, which is essential for the scalability of the proposed infrastructure [11].

Although how IoT works is complicated and also depends on specific application, we can in general categorize it into the following elements: identification, sensing, communication, computation, service and semantics as shown in Fig. 2.3. First, identification is used for tagging each "thing" in order to answer the demand of specific service, which includes two sub-elements: naming as for object ID and addressing as for the address for each object ID within a network. Second, sensing means collecting data generated by "things" within a network while communication involves protocols and technologies that help send gathered data through sensing to a warehouse, database or even cloud. Simply gathering data through sensing is not enough, which is why computation has to be included to realize complicated processing. Computation can be achieved through either hardware such as microprocessors, SoCs and FPGAs, or software such as different kinds of operating system(OS) and cloud services developed specifically for IoT.

There are four types of IoT services, which mark different stages of IoT development. Identity-related service is used for realization of identification and it is the most basic and indispensable services. Information aggregation service is based on the data collected through sensing and communication technologies make this service available for different IoT applications. Collaborative-Aware service is performed after information collection is done and then data computation prompts IoT systems to make decision and react accordingly. Unlike other services, ubiquitous service is the ultimate goal for IoT application since it requires other services to be available anywhere, anytime and to anyone. The final element is semantics, which enables heterogeneous systems to interact with each other in order to produce the required service while occupying relatively as little resource as possible.

2.2 Cloud Computing

Cloud Computing, though not showing up in the Hype Cycle report for emerging technologies, has reached the phase of "slope of enlightenment", which signifies its movement towards mainstream adoption next [12]. The inception of this technology, however, can be dated back to 1960s when John McCarthy predicted that "computation may someday be organized as a public utility" [13]. Nevertheless, his vision does not match exactly to the development of cloud computing but is more in line with the concept of utility computing. Unlike cloud computing, utility computing doesn't have to involve virtualization and the locations where computation is performed can be as few as one data center or even one supercomputer, which is similar to the way electricity is distributed as utility [14].

There is also a technology called "grid computing", which shares lots of similarities with cloud computing. Grid computing, the technology that helps customers to utilize computer capability on demand, was first introduced in the mid 1990s. By requesting computing power through standardizing specific protocols, researchers working in this field have developed large-scale federated systems (TeraGrid, Open Science Grid, caBIG, EGEE, Earth System Grid) that provide on-demand service for computing power, data as well as software. Although grid computing technology shares some similarities with cloud computing, it was imagined without having big data in mind. In addition, with the advancement of IC technology, the computation ability on a single chip has greatly enhanced and the cost has been immensely reduced. Last but not least, behemoth corporations such as Microsoft, Amazon and Google have already invested billions of dollars on building commercial systems which contain but are not limited to hundreds of thousands of computers with huge computing capacities [15]. As a result, cloud computing, having much broader and more applications, enjoys the development of the state-of-the-art Information and Communication Technology (ICT) and is supported by large-scale commercial investment.

Due to the increasing amount of applications where cloud computing can be used, there

is little consensus on how to properly define it. However, the concept of cloud computing can be clearer after the discussion of its several fundamentals.

Virtualization allows users to perform computation tasks without relying on one specific physical hardware. Therefore, users have no limitations on the availability of processor, memory and storage resources as well as software environment. This technology comes out mainly due to underutilized hardware, out-of-space data center, green initiatives and the increasing cost of hiring system administrators locally. There are two types of virtualization: server virtualization lets users perform different work under different operating systems using a single virtual environment while storage virtualization enables implementing virtualized storage to store the mount of data not possible physically for one single server [16].

Everything as a service (XaaS) promises a scenario where service-oriented architecture and design supports the development and installation of software applications as services. Cloud computing, which comprises almost half of all proposed "aaS" models, can be defined through its implementation of different "as a Service (aaS) models [17]. For example, cloud architecture, which is designed to implement software applications with the assistance of real-time internet-accessible on-demand service, has four layers and each layer consists of one "as a Service (aaS) model: software as a service (SaaS) model at the top, platform as a service (PaaS), infrastructure as a service (Iaas) model and hardware as a service (HaaS) model at the bottom [18]. SaaS, also referred to as the Application Service Provider (ASP) model, is a platform, which provides software applications to multiple users over a standard protocol such as HTTP. PaaS, platform as a service, enables users to develop, test, deploy and host their applications through a web-based platform containing all the necessary systems and environments. HaaS, hardware as a service, extends pay-as-you-go subscription service towards IT hardware or even a data center, which gets rid of the trouble of building, maintaining and scaling local hardwares for users. IaaS, infrastructure as a service, has extended the service provided by HaaS and provides resources on-demand not only including hardware service but also both networking and storage services.

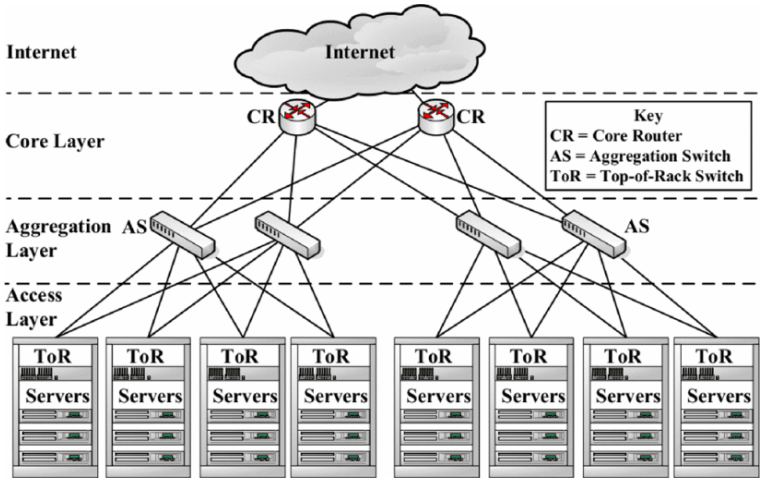

Figure 2.4: Traditional Data Center Network
[20]

Although there are numerous companies that are providing these cloud services, we can categorize them according to how they offer the computing services on the basis of the level of abstraction and management of resources presented to the programmers. Amazon EC2 offers only low-level management services and only supply very basic API. Users will be able to access a low level of virtualization, which is similar to accessing physical hardware directly. Google AppEngine and Force.com, on the other hand, offer computing and storage services specifically for creating applications instead of general-purpose computing. Therefore, Amazon EC2 offers clients flexibility while Google AppEnging and Force.com offer programming convenience. However, Microsoft's Azure lies in between: it supports general-purpose computing but users can't control operating system or runtime; it can perform automatic configuration of network but users have to specify some application properties [19].

2.3 Optical Interconnect for Data Center

A data center is a facility that provides necessary infrastructures for supporting an enterprise business, which includes servers with computational power, storage units, network

devices, power distribution networks and cooling equipment. All contents used in an IT architecture are both generated and passed through the data center [21].

To have a better understanding of the data center, a 3-tier architecture, as shown in Fig. 2.4, can be used as an example of the current data center network. The 3-tier architecture contains core layer, aggregation layer (sometimes referred to as distribution layer) and access layer, which can contain either switches, routers or server. Switches are used to connected multiple devices on the same network while routers connect multiple networks together. Therefore, routers are usually used in the top tier such as the core routers (CR) in the core layer and switches are implemented in the lower tiers such as the aggregation switch (AS) in the aggregation layer and then top-of-rack (ToR) switch in the access layer. In this topology, servers, whose functions is to compute and store data, are located at the bottom of the access layer inside a storage unit named rack. In order for servers to communicate with the Internet, every rack has a ToR switch placed on the top of the access layer. The top tier layer, core layer, contains limited numbers of core routers directly connected to the Internet. In between the core layer and the access layer, there is an aggregation layer containing aggregation switches. Unlike the other two layers, there can be different typologies implemented and we have used the flat layer 2 topology with only layer 2 switches in my example. Also, redundancy can be seen in the aggregation layer: each ToR switch is connected to multiple aggregation switches (2 in my case). It is also worth noting that since aggregate switches combine data from several ToR switches together, they along with core swithces will be operating at much higher data rate than ToR switches.

However, the Global Cloud Index (GCI) shows that global data center traffic growth will triple and reach 20.6 zettabytes per year. Also, 95% of all data center traffic will come from the cloud [22]. In fact, two of the drawbacks from the current data center network structure make it hard to meet the demand mentioned above and thus, current data center network can't be used to create hyper scale data center.

First, there is a latency problem: significant queuing and processing delay happen when

a packet moves from one server to another through switches in different layers.

The second problem comes from the high power consumption of switches in different layers. As more and more servers are implemented and connected together, the topologies of the aggregation layers become more and more complicated and more links are required. Although the development of IC technology has enabled higher throughput from the implementation of multi-core, lower power consumption processors, the amount of power dissipation that a data center could handle can't catch up with the speed of peak performance and bandwidth requirement increment. Besides, as mentioned before that data center has special equipment for cooling purposes, high power consumption of switches will also increase the power consumption of cooling equipment, which will eat up even more power consumption budget for a data center [23].

Although optical interconnect has the advantage of high throughput, low latency and low power consumption, it is unrealistic to replace the whole data center network with optical interconnect since each layer in the network has different design challenges. Thus, let's first start with core networks where optical interconnect is widely implemented for years.

In the core network, there will only be limited numbers of fiber cables and the limited nodes with high capacity will be transmitting highly aggregated traffic. There are two types of core networks that are related with data center interconnect.

First type is inter-data center interconnect in metro network, which has link length limited to less than 100km due to latency requirement. Inter-data center interconnect in wide-area network (WAN) is included, whose two most important parameters are spectral efficiency and reach. Although reach won't be sacrificed as we have upgraded the speed from 2.5G to 10G and to 100G, certain technologies have to be used to increase the reach of 400G system.

Second type is intra-data center interconnect but only includes the part using point-to-point communication, such as server-to-switch and switch-to-switch communication. Multi-mode fiber (MMF) is mostly used for systems whose speed is lower than 40G due to transmission distance constraint. For speed higher than 100G and reach longer than 100-meter,

single-mode fibers will be the focus. Also, multiple parallel fibers can be utilized to achieve higher speed without cost overhead for short reach links [24].

Although researchers are trying to apply flexible and software-controllable optical interconnect technology developed through core network towards data center, it won't be easy due to the following reasons. First, inside the data center, there are much larger number of transmission links because a large number of servers and switches are used and the number will keep increasing in the future. Second, cost and energy efficiency is much more stringent for data centers than for core networks.

On the other hand, even optical interconnect technology based on point-to-point communication needs improvement. First, its low scalability and large latency will cause low power efficiency and high implementation costs. Second, interconnection inside the data center includes more than just transceivers and links. Also, functions such as synchronization, switching, switch control, scheduling, arbitration, signaling as well as managing and routing of data units through the internal interconnection network are necessary.

As one of the promising technologies, optically switched interconnect, which is based on either hybrid or all-optical architecture and utilizes diverse switching technologies, can offer the highest capacity and bandwidth density as well as the potential for lowest latency among all interconnection options. That's why even though this technology is still in its research phase, it seems promising among researchers.

However, there are four different hierarchical system levels inside the internal interconnect within large data centers, supercomputers or routers. The highest hierarchical level is the rack-to-rack interconnection network, whose lengths are from a few meters to several hundreds of meters. The second hierarchical level is within a rack of equipment where different backplanes are realized and the length of intra-rack links are between 15 cm and a few meters. The third hierarchical level is the chip-to-chip interconnects, which provide connections between chips in a single module. One of its implementations is on a board, whose interconnects are typically shorter than 25 cm. The final hierarchical level is on-chip

interconnects, which have a length below two centimeters in general [25].

There are three types of cabling in the data center: passive copper cable, active copper cable and active optical cable. Passive copper cables, functioning as wires only, connect corresponding ends through electrical signals. Active cables, which include both copper cable and optical cable, not only work as wires but also embed optics and/or electronics within the connectors in order to overcome physical distance limit by performing amplification, equalization and restoration. In the rack-to-rack (inter-rack) interconnection level, only active copper/optical cables can be used due to their longer reach. On the other hand, optical cables are better choices for the following reasons. First, optical cable is thinner and lighter, which can provide better configuration flexibility for data center. Second, optical cable has less cooling problems and its airflow consideration is less strict, which might increase the lifespan of the equipment in the data center. Third, optical fibers suffer less from electromagnetic interference (EMI) [26].

Among three layers of data center network, the access layer is responsible for up to 90 percent of the total power consumption of the data center network. The intra-data center interconnect, especially interconnect at top-of-the-rack (ToR), can help to bring down the power consumption of the data center. However, in order to satisfy the traffic requirements such as traffic locality, multicast capacity, variable flow capacity and burstiness, existing switching technology such as optical packet switching (OPS), optical circuit switching (OCS) can no longer be used. Therefore, three types of schemes for passive optical interconnect (POI) are implemented: scheme 1: $N \times N$ arrayed-waveguide grating (AWG)-based POI; scheme 2: AWG + Coupler-based POI and scheme 3: coupler-based POI. As a result, passive optical interconnects are able to achieve a significant reduction of power consumption and maintain cost at a similar level compared to their electronic counterparts [27].

Usually, chip-to-chip interconnects are implemented through the motherboard and are used mostly for relatively long range ($\sim 30 - 100cm$). However, because of the limit of minimum channel pitch achievable on the motherboard and the increasing demand of I/O band-

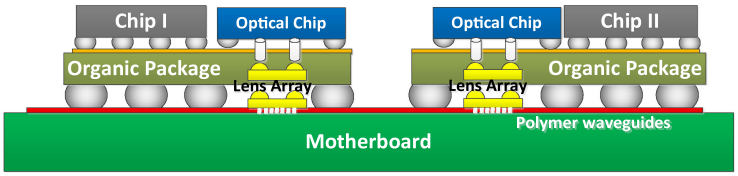

Figure 2.5: Current Chip-to-chip Optical Interconnect Methodology [28]

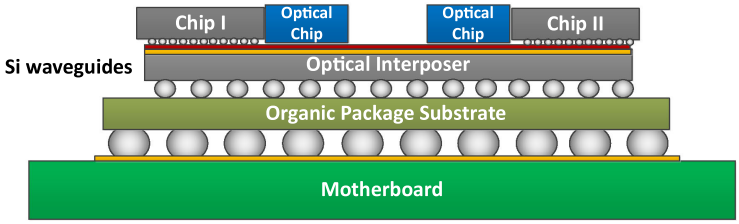

Figure 2.6: Emerging Chip-to-chip Optical Interconnect Methodology [29]

width requirement, traditional electrical interconnect can't possibly keep up while staying low power dissipation. By using wavelength division multiplexing (WDM) to send multiple wavelengths in the same channel, optical interconnect can realize high bandwidth communication between chips in relatively long range. One of the current implementation of optical interconnect in chip-to-chip interconnect can be seen in Fig. 2.5, which shows the schematic of terabus architecture with polymer waveguides at the board level fabricated at a $62.5\mu m$ pitch. The signals from the electrical chips are converted into optical signals through an optical chip, relayed to the motherboard via a lens array and optical couplers, pass the motherboard through polymer waveguide and then are sent to another electrical chip using the same components. The terabus is able to aggregate bidirectional data streams from multiple transmitters to achieve higher bandwidth density. In recent development, optical interposer, which is formed through integration of nanophotonics, has been heavily researched due to its higher bandwidth density, heterogeneous integration and reduction in form factor. One of its implementation examples can be shown in Fig. 2.6. Unlike the example shown in Fig. 2.5, optical interposer can achieve significantly higher bandwidth density as high as 8

Tb/s/mm using fine pitch silicon waveguides [30].

As for the on-chip interconnect, we will discuss it in the next chapter since it is what state-of-the-art silicon photonics research is applied on.

2.4 Pulse-Amplitude Modulation (PAM)-4 and its Application at High Speed Ethernet

When it comes to conventional fiber transmission system with speed as low as 10G, non-return-to-zero (NRZ) modulation is widely used. In NRZ modulation, there are only two optical levels: binary "1" when optical power is strong and binary "0" when optical power is weak. Since it can only transmit two possible optical power levels and only one level at a time, NRZ only carries 1 bit information and can also be called pulse-amplitude modulation (PAM)-2. Also, the symbol rate of NRZ is the same as its bit rate because it transmits single bit per symbol [31].

As the internet traffic has becoming much more crowded and much faster, conventional 10G speed for fiber transmission is no longer enough. As a matter of fact, connections to many servers are already as high as 25 gigabits per second (Gbit/s) and links between switches in large data centers can already reach 100 Gbit/s. In the not so near future, cost-effective 400G modules for links between switches will be demanded, which in fact has already been proposed as 100G single lambda solutions [32].

Physical bandwidth of the data center has become the bottleneck of satisfying the drastic change of fiber transmission speed requirement. This is simply due to the fact that the analog bandwidth of optical and electrical components cannot keep pace with the growth in data traffic. We can add more fibers but it is not a good idea cost wise especially for the long-haul application. Therefore, due to the band limitation of both channels and optical devices, we have to look for another way to increase the speed and one of the available techniques are to pack more bits into single wavelength [33].

Although there are a lot of modulation schemes available, data center architecture has to be totally overhauled in order to change from currently non-return-to-zero (NRZ) modulation or PAM2 to other modulation schemes such as phase modulation or frequency modulation. On the other hand, signal-to-noise ratio can be boosted through circuit techniques such as equalization, amplification and digital signal processing techniques. Therefore, pulse-amplitude modulation (PAM)-4 has become the choice for realizing the following IEEE 802.3bs standards. First, 400GBASE-DR4 use 4 lanes of 100G PAM-4 over 4 parallel single mode fibers for a distance up to 500m. Second, 400GBASE-FR8 uses 8 WDM lanes of 50G PAM-4 and can operate for a distance up to 2km. Third, 400GBASE-LR8 also uses 8 WDM lanes of 50G PAM-4 and these devices can operate up to 10km. Even for standards designed for chip-to-chip/chip-to-module electrical interfaces, PAM-4 modulation is also used. For example, 400GAUI-8 contains 8-lane electrical interface and its encoding scheme 25GBaud PAM-4 is able to achieve each lane with 50Gb/s bit rate [34].

PAM-4, pulse-amplitude modulation 4-level, uses the same PAM scheme as NRZ but has four different levels representing 2bit code 11, 10, 01 and 00. Since it transmits two bits at a time instead of one, PAM-4 has the advantages of having half the Nyquist frequency and twice the throughput for the same Baud rate compared with NRZ. Many benefits are associated with having half the Nyquist frequency: doubling the density of data, achieving higher resolution using the same oversampling rate, and having the same total noise power spread over a wider frequency so that the noise power in bandwidth goes down. However, PAM-4 also has its own disadvantages. First, if the maximum amplitude for the signal is fixed for a channel, the distance between each signal inside PAM-4 is only one third of that inside NRZ. When all nonlinearity effects are added, the SNR loss is approximately 11 dB. Second, PAM-4 will increase the difficulty of implementing transceivers and of realizing better equalization scheme, which will result in higher power consumption. Third, due to its stricter SNR requirements, PAM-4 will only be able to be implemented in short-haul optical system and that's why higher order modulation such as PAM-8 won't be even able

to function in short-haul optical systems, although having even higher throughput [35, 36].

Chapter 3: Silicon Photonics

3.1 Background

As one of the four different hierarchical system levels inside the internal interconnect within large data centers, supercomputers or routers, on-chip interconnect has always depended on copper-based, physical-level electrical interconnects. There are two types of delay on-chip: interconnect delay and gate delay. As the number and the variety of the components that are integrated into system-on-a-chip (SoC) keep increasing, the interconnect between those components will become more and more complicated. As a result, the decreasing of interconnect delay can't keep up with the decreasing of gate delay and thus, interconnect delay will become the main bottleneck for deep-submicron (DSM) technology. Also, the interconnect will also consume most of the power on the SoC. However, this doesn't mean that the semiconductor industry hasn't been working on a solution to deal with this issue. In fact, alternative materials such as low-k dielectrics have been developed to meet the immediate needs but still can't keep up with demands in the long run. Therefore, as we keep pushing for higher and higher data rate on-chip, we need to look for other more future-proof solutions. At the same time, however, the fabrication techniques that this new technology implements have to be compatible with mainstream SoC and system-in-package (SiP) technologies [37].

Before 1947, vacuum tube technology was dominating the electronics industry even though vacuum tubes are fragile, bulky, slow, power hungry, and produce considerable amount of heat. In 1947, the transistor was invented which improved upon all the disadvantages of vacuum tube technology. However, engineers still need to connect diodes, rectifiers and capacitors along with transistors through soldering in order to create a functioning circuit, and all that wiring and soldering can present huge liability and complexity issues. Jack Kilby, during his tenure as an employee for Texas Instrument, began to sketch out his idea of realizing a complete circuit by implementing passive devices using the same materials as actives devices such as transistors in order to form in situ interconnection [38]. From small-scale integration (SSI) where transistor number is fewer than 10, median-scale integration

(MSI), large-scale integration (LSI), very-large-scale integration (VLSI) and ultra-large-scale integration (ULSI) where the number of transistors on-chip has reached over 1 million, Intel has entered the era of processors consisting over one billion transistors [39]. More and more transistors are designed to be incorporated onto a single chip because of the constant scaling of the transistor sizing. Right now, TSMC 5nm technology node has begun production since 2018 [40].

Due to advancement of the IC technology in recent years, it is natural for researchers to come up with the idea of using matured IC technology to solve the delay and power consumption problems for higher data-rate on-chip interconnect. By making it compatible with modern IC technology—just as the idea that Jack Kilby had to realize passive devices using the same materials as transistors—optical on-chip interconnect can provide high-bandwidth data transmission through dense wavelength-division multiplexing (DWDM), ultra-low signal propagation of light in silicon, and relatively distance-independent energy consumption. The technology that implements optical interconnect using currently available IC technology is called silicon photonics, whose fabrication techniques are compatible with mainstream SoC and SiP technologies.

Even though optical interconnect on-chip can be realized using silicon photonics, we need to make changes to the on-chip electrical interconnects architecture, which is where a new field of research Optical Networks-on-Chip (ONoCs) has gained interest in IC design community. Since the signals inside the integrated circuits are electrical and we need optical signals to transmit information on chip, other functionalities are required to implement both optical signals and electrical signals on-chip. The steps to generate and receive an optical signal can be shown in Fig. 3.1.

On the sender side, electronic data is first encoded and conditioned for error correction and signal conditioning purposes. Subsequently, data serialization raises the transmission data rate since electrical circuits with lower data usually have higher power efficiency. Finally, a specialized driver circuit provides an electrical signal to the optical modulator, modulating

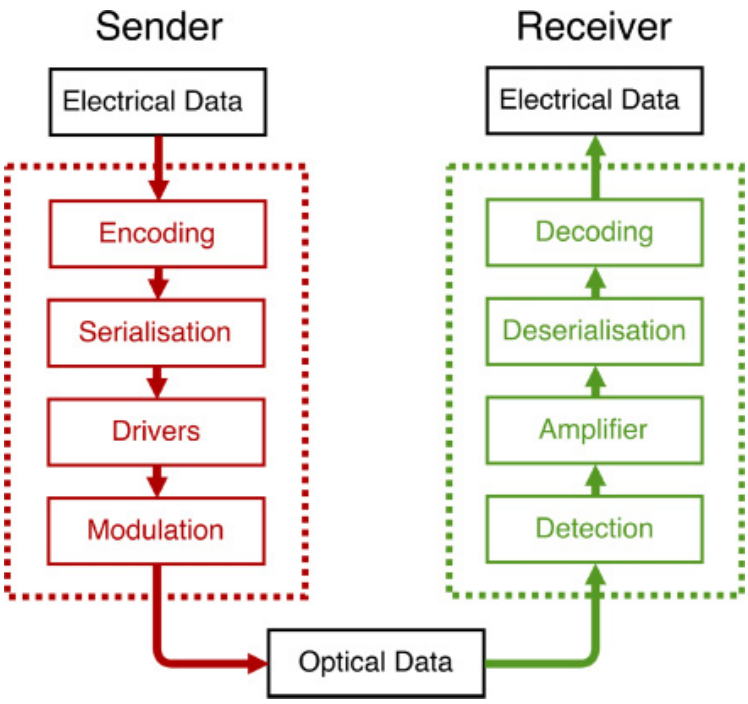

Figure 3.1: Optical Transmission Steps
[41]

bits onto the modulator's optical resonance wavelength. The modulated wavelengths traverse the waveguide until they are filtered at the receiver. Photodetectors are placed right behind the filters and convert optical signals into an electrical current. The electrical currents output by photodetectors are, however, well below the level required to drive voltages for operating digital logic, which is why amplifiers are necessary to regenerate and amplify these currents. The following steps of deserialization and decoding mirror the functionality of the serializer and encoder at the sender side, respectively. Although necessary, these steps do not introduce considerable latency and can typically be executed within one processor clock cycle [42].

3.2 Overview

Silicon photonics, first proposed by Soref back in 1980s, is the technology that is able to reuse the CMOS fabrication infrastructure developed and perfected throughout the years

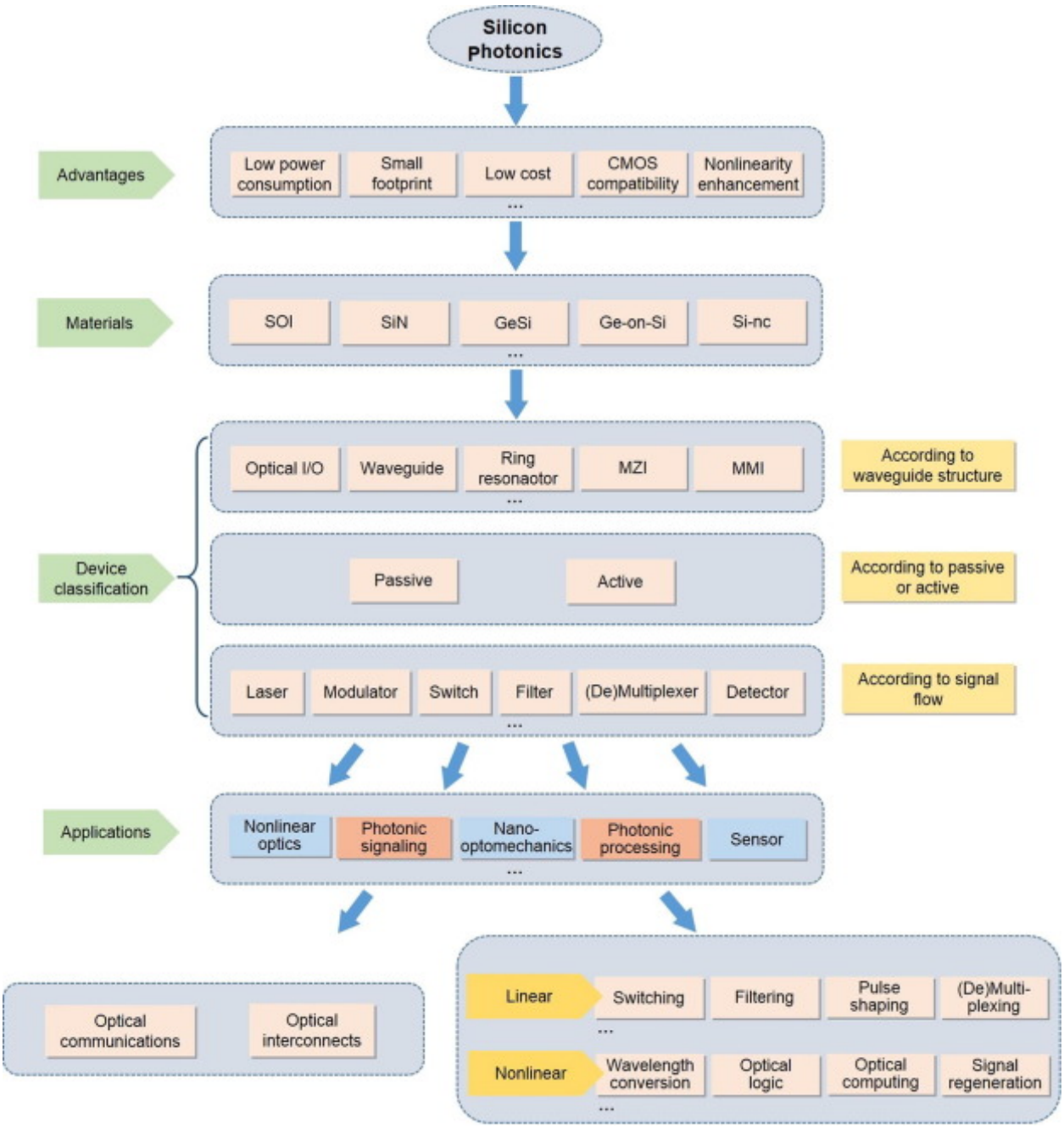

Figure 3.2: Advantages, materials, device classification, and applications of silicon photonics. [43]

to build photonic circuits which are capable of transmitting information seamlessly between the electrical domain and the optical domain [44]. To have a general understanding of the silicon photonics, let's look at the following aspects as shown in Fig. 3.2 [43]: advantages, materials, device classification and applications.

There are five advantages for silicon photonics: low power consumption, small footprint, low cost, complementary metal-oxide semiconductor (CMOS) compatibility and nonlinearity enhancement. Having low power consumption comes from using the optical signals to replace the role of electrical signals for transmission, which has higher bandwidth, consumes less power and consequently dissipates less heat (due to the high thermal conductivity $149 W m^{-1} K^{-1}$ of the silicon). By being compatible with the CMOS technology, silicon photonics can utilize the latest technology advancement to its advantage and even use the state-of-the-art foundry for its own fabrication process, which will help save the cost for developing silicon photonics technologies since researchers don't have to reinvent the fabrication process from ground up. Although the electrical circuits in the Silicon Photonics Technology can directly benefit from the scaling of transistor size, silicon photonics still cannot be of small footprint if the optical circuits are bulky. However, since the the refractive index of silicon is about 3.5 at telecommunication wavelengths such as 1550nm, which is greatly larger than silica (~ 1.414) of the silicon waveguide, light can be confined inside of silicon waveguides so that the integration of a large amount of optical devices can be realized in a millimeter scale. Another advantage of silicon photonics is its nonlinearity enhancement, which is realized by the small cross-section of the high index contrast silicon waveguides or photonics crystals where the photons are made to strongly interact with the medium where they propagate. As a result, the following applications can be achieved: frequency generation, frequency conversion, frequency-comb generation, supercontinuum generation, soliton formation, temporal imaging and time lensing, Raman lasing, and comb spectroscopy [45].

Although Silicon Photonics Technology is based on silicon, silicon compounds rather than silicon alone are used instead for different purposes. There are five types of silicon compounds that are used widely in Silicon Photonics Technology: silicon-on-insulator (SOI), silicon-nitride (Si_3N_4), silicon-germanium (GeSi), germanium-on-silicon (Ge-on-Si) and silicon-nanocrystals (Si-nc). SOI is a semiconductor structure consisting of a layer of single crystalline silicon separated from the bulk substrate, which is a silicon wafer, by a thin

layer of insulator, which is usually a thermal silicon oxide (SiO_2) layer. The thickness of the film can be different depending on the applications [46]. Since SOI has already been widely used in modern IC, silicon photonics also commonly use SOI. Si_3N_4 was traditionally used in standard CMOS processes to insulate individual transistors, known as local oxidation of silicon (LOCOS). As for silicon photonics application, Si_3N_4 is used in optical waveguides as the core layer, which is surrounded by silicon dioxide (SiO_2) as the cladding layer. The refractive index of the cladding at $1.55\mu m$ wavelength (1.98 for SiO_2) and core (1.45 for Si_3N_4) allows for designs that range from low- to high-contrast waveguides with low propagation losses in the range of 0.3 dB/m to 1.0 dB/cm over the range from $\sim$ 400 to $\sim$ 2350 nm [47]. The electro-absorption (EA) effect, known as the Franz-Keldysh (FK) effect in bulk semiconductors and the quantum confined Stark effect (QCSE) in quantum-well (QW) structures, is strong in the GeSi or Ge material system and is an ultrafast process capable of realizing high-speed modulation [48]. Due to the pseudo-direct gap behavior of Ge and compatibility with CMOS technology, Ge-on-Si can be used to implement Waveguide-integrated photodetectors, which are able to achieve full responsivity even at 0 bias (photovoltaic mode) because of the large built-in electric field [49]. Since Si-ncs embody two photoluminescence (PL) features—high efficiency and tunable emission wavelength, which result from quantum confinement effects—si-ncs can be used to realize light emitters as well as waveguides, resonators and solar cells [50].

There are mainly three ways of categorizing silicon photonics devices. First, just as electrical devices, it can be classified into two: passive devices are used for transmission, filtering and polarization/mode/wavelength manipulation while active devices can be utilized for modulation or other nonlinearity functionalities. Second, if we categorize them in terms of waveguide structure, there are optical I/O, waveguide, ring resonator, Mach-Zehnder interferometer (MZI) and multi-mode interferometer (MMI). Third, according to signal flow, light is first generated by a laser source, then it can be modulated by a modulator, processed through switched by a switcher, filtered by a filter, (de)multiplexed by a (de)multiplexer and

finally, it will be detected by a detector.

There are mainly five applications for silicon photonics. The first application is the nonlinear optics. Because of the extremely large third-order nonlinear-optical susceptibility of single-crystal Si, along with strong optical confinement, effective optical nonlinearity can become very strong even when only supplied by relatively low optical power or realized through very short devices with lengths on the order of a few hundred microns to millimeters [51]. The second application is the nano-optomechanics. Nano-fabrication technology, which uses the manufacturing technologies mostly developed for modern day integration circuit design and microcontroller design, has been improved over the years. As a result, nano-fabrication technology paves the ways for developing nano-optomechanics, which make use of optical force such as attraction or repulsion between beams of lights to design devices for photonics integration circuits [52]. The third application is the sensor. Having the advantages of being amenable to chip integration and miniaturization, waveguide-based optical sensing technology has enabled the following types of sensors: grating-coupled waveguide sensors, interferometric waveguide sensors, photonic crystal waveguide sensors and resonant optical microcavity sensors [53].

The final two applications, photonics signaling and photonics processing, are also the most dominant. Photonics signaling can be divided into optical communications and optical interconnects. Although both of them are related with data transmission, each represents a different distance. Optical communication ranges from deep-space mission to network access while optical interconnect is used in data centers and high-performance computing applications ranging from rack-to-rack to on-chip communication. Photonics processing, unlike electrical signal processing, is mostly used for overcoming the bottleneck posed by electrical interconnects in order to satisfy the ever growing bandwidth requirement for high-data rate communication. There are two types of photonics signals processing, linear and nonlinear. Linear photonic signal processing includes switching, filtering, optical pulse shaping, differentiation, wavelength/mode/polarization (de)multiplexing etc. Unlike linear photonics

signal processing, nonlinear photonics signal processing uses different optical materials platforms, such as highly nonlinear fibers (HNLFs), semiconductor optical amplifiers (SOAs), chalcogenide waveguides, and periodically poled lithium niobate (PPLN) waveguides etc., to realize the following functionalities: optical multiplexing and demultiplexing, wavelength conversion, optical logic and computing, signal regeneration, equalizer, optical switch, optical memory, and so on [43].

3.3 IMEC Silicon Photonics Platform (iSiPP) Overview

Silicon photonics platform (iSiPP) from IMEC, based on silicon-on-insulator (SOI), has integrated a wide variety of both passive and active components, which can provide a competitive edge for photonics integrated circuits used for short-reach optical interconnects. There are three different platforms available for commericial use: iSiPP200: 200mm (8") full platform; iSiPP50G: 200mm (8") simplified platform; iSiPP300: 300mm (12") full platform. While iSiPP200 can be accessed through shared run, iSiPP50G utilizes the access model multi-project wafer (MPW) services, which is most used in IC design industry. MPW service combines different integrated circuit designs from different designers or institutions together on a single microelectornics wafers using shared masks in order to save cost. That's why in my implementation, we have chosen iSiPP50G platform for my photonics chip fabrication.

Here are several key technology features. First, silicon-on-insulator is used as the basic structure for the substrate with 220nm Silicon and 2000nm buried oxide (BOX) layer. Second, there are three levels of silicon and one level of poly-silicon, which are patterned using 193nm lithography. Third, six levels of silicon doping are implemented in order to realize different doping for heaters, mach-zehnder modulators (MZM) and microring modulator (MRM) and two levels of germanium doping are used for implementing either germanium option photodiodes or silicon germanium option photodiode and electroabsorption modulator (EAM). Fourth, germanium on silicon (Ge-on-Si) is fulfilled through Remote Plasma-enhanced Chemical Vapor Deposition (RPCVD) epitaxy. Fifth, interconnects are realized

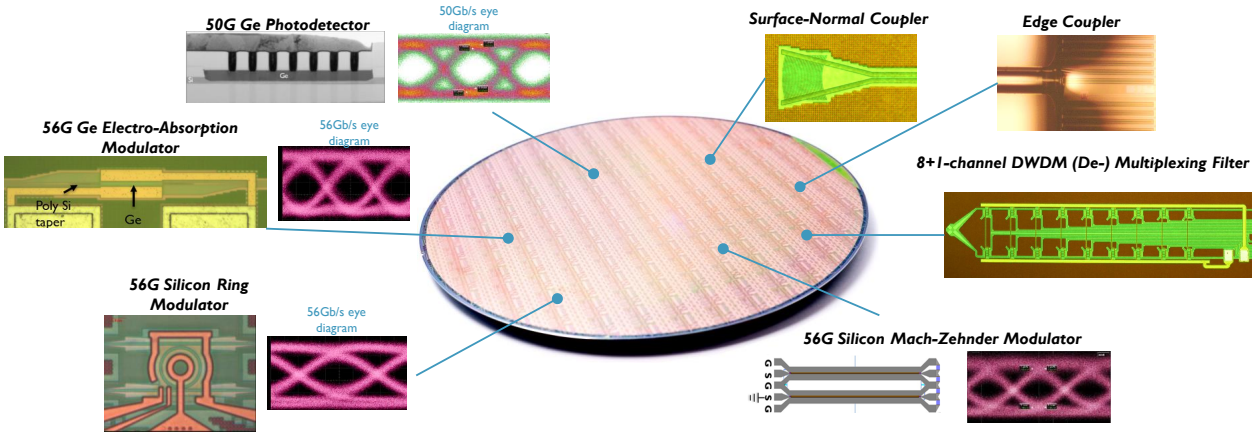

Figure 3.3: 50G Silicon Photonics Integrated Circuit Technology [55]

through two levels of copper while aluminum is the metal choice for bondpads. Sixth, deep reactive-ion etching (DRIE) is implemented specifically for edge coupling, which can achieve a large operating bandwidth.

There are mainly seven types of devices that are available from iSiPP50G, as shown in Fig. 3.3: traveling-wave Mach-Zehnder p-n modulator (TWMZM); GeSi Electro-absorption modulator (EAM); microring p-n modulator (MRM); waveguide-based Ge-on-Si detectors; two types of fiber coupling, vertical "raised" grating and Conventional band (1530nm to 1560nm) edge coupler; integrated heaters and passive waveguide-based devices such as filters, multi-mode interferometers (MMI) etc. However, most of those devices are only provided as standard building blocks and their parameters can't be altered if users want to use them by their device marker [54].

3.4 Basic Devices

3.4.1 Silicon Waveguide

Just as crucial as wires for electrical circuit, waveguide is used in optical circuits to transmit optical signals. Just like wires which require careful design for the dimensions and certain choices for different materials when certain transmission speed has been met, optical

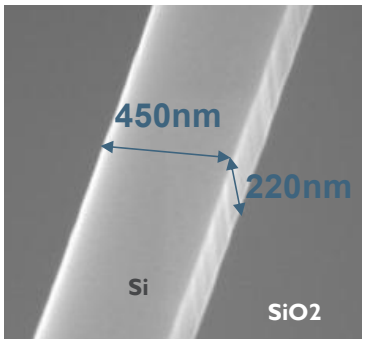

Figure 3.4: A Waveguide used in iSiPP50G technology [55]

waveguide has to be designed according to the property of the optical signals. As shown in Fig. 3.4, IMEC's iSiPP50G platform has implemented the strip waveguide using silicon with SiO_2 as its substrate, which has a width of 450nm and a thickness of 220nm.

In order to have a better understanding of the optical silicon waveguide, let's first perform the 3-D simulation using Lumerical FDTD as shown in Fig. 3.5. The discussed 3-D strip waveguide structure can be seen through XY view, XZ view, YZ view and perspective view. FDTD simulator, which is a must for performing simulation, works as either a plane (2D simulation) or a box (3D simulation). Only the area inside the simulator will be simulated and the simulation precision depends on the mesh cell sizes, which is crucial for attaining correct result without wasting too much computing resources and time. Although there are seven types of boundary conditions such as metal, periodic, symmetric and anti-symmetric, Bloch and perfect magnetic conductor (PMC), we have chosen the perfectly matched layer (PML) boundary condition so that the boundary can absorb light waves (both propagating and evanescent) with minimal reflections. There are two materials used in this structure: silicon and silicon dioxide. The real part of their refractive index and permitivity can be seen in Fig. 3.6, where the fitted curve is based on experimental results with fit tolerance of 0.001 and max coefficients of 100. Since the refractive index for the SiO_2 is on average 1.45 and that for the Si is 3.47, this high contrast in the refractive index makes compact photonic circuits possible.

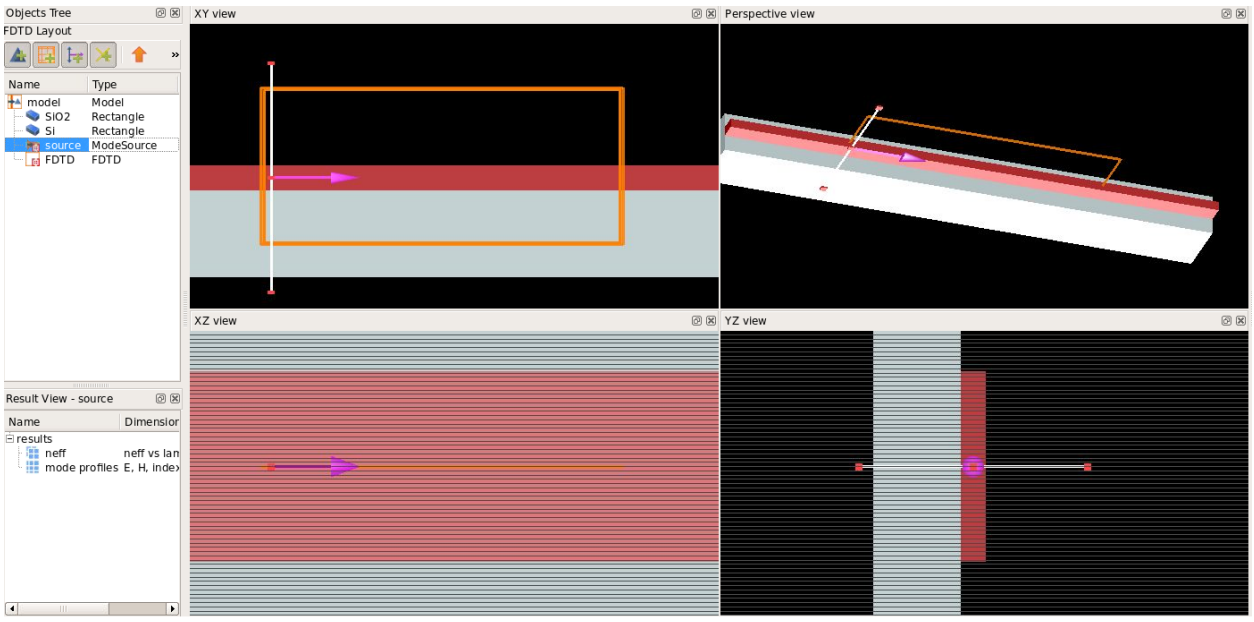

Figure 3.5: Silicon Waveguide FDTD Simulation GUI

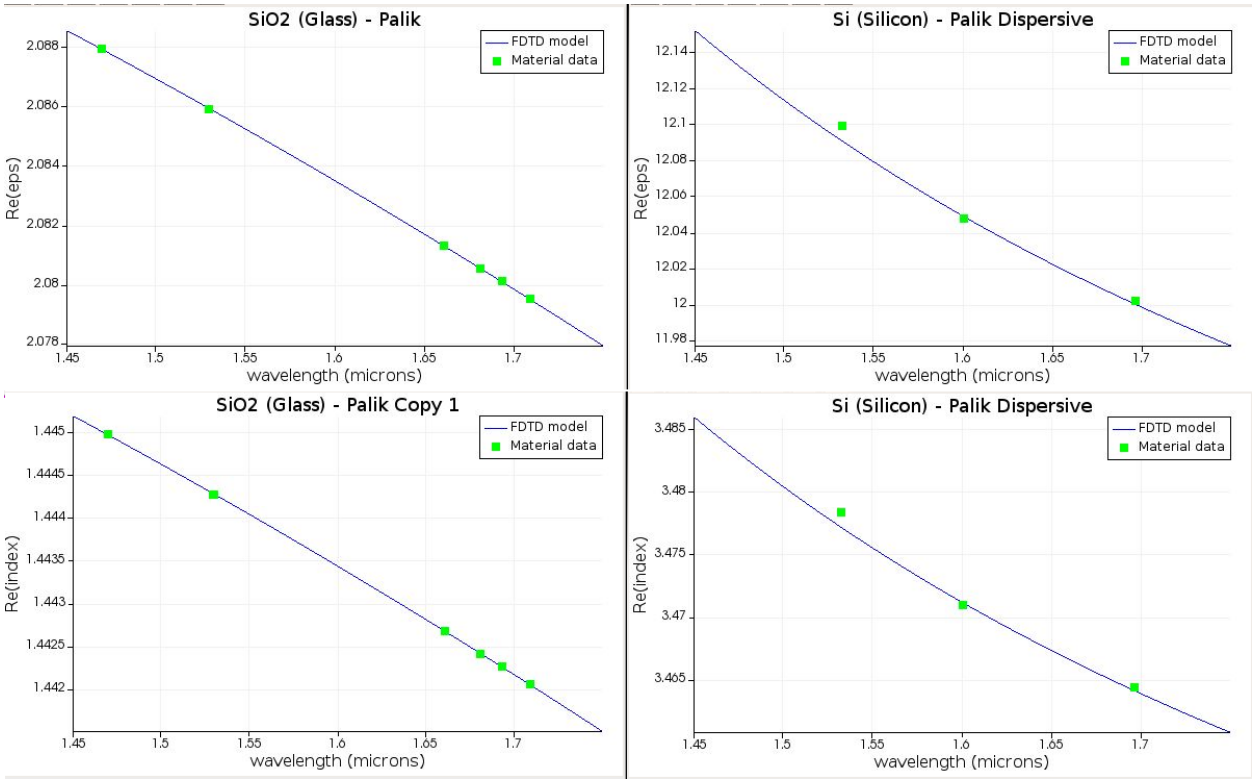

Figure 3.6: Refractive Index for Silicon and Silicon Dioxide

The wire-like phenomena for the silicon waveguide can be demonstrated through the FDTD simulation result as shown in Fig. 3.7. The optical signal source uses the fundamental

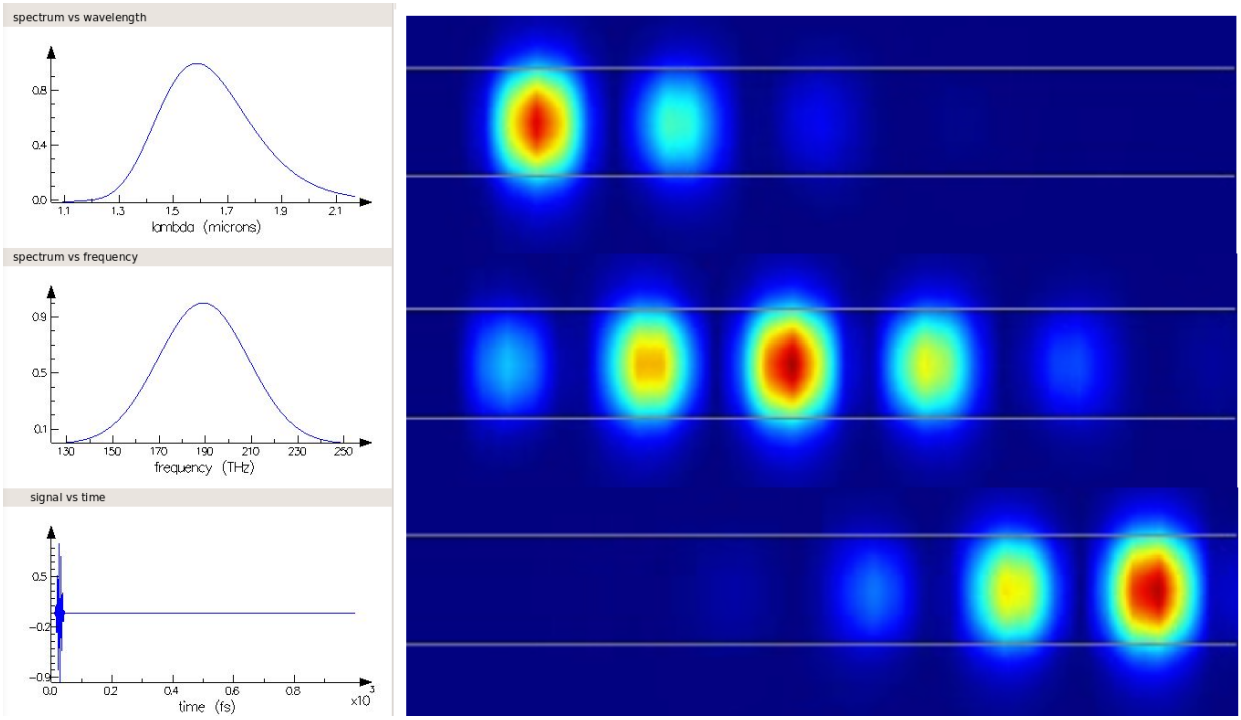

Figure 3.7: Silicon Waveguide Transient Simulation Result

mode and its spectrum/signal waveform can be seen on the left. The transient simulation result shows the passage of the source signal inside of the silicon waveguide where the highest intensity is shown as the color red.

Although FDTD simulation can provide the full picture for the device, it has the disadvantage of taking too much resources and time. Besides, FDTD simulation cannot possibly provide a concise picture of mechanics for the device. Since the optical simulations performed in my thesis work will finally be used for realizing optical mechanism inside the electrical circuit design tools, we need another simulator which can provide clearer pictures so that some of the simulation result can directly contribute to my work later. As a result, Mode solution simulator will be utilized next.

The mode solution UI can be seen in Fig. 3.8. Just like the FDTD simulator, we need to build the silicon waveguide 3D model first with the correct dimension. However, unlike FDTD simulator, we don't need an optical source but only a finite difference eigenmode solver (FDE) is required. The FDE solver doesn't have the 3D box as in FDTD and only

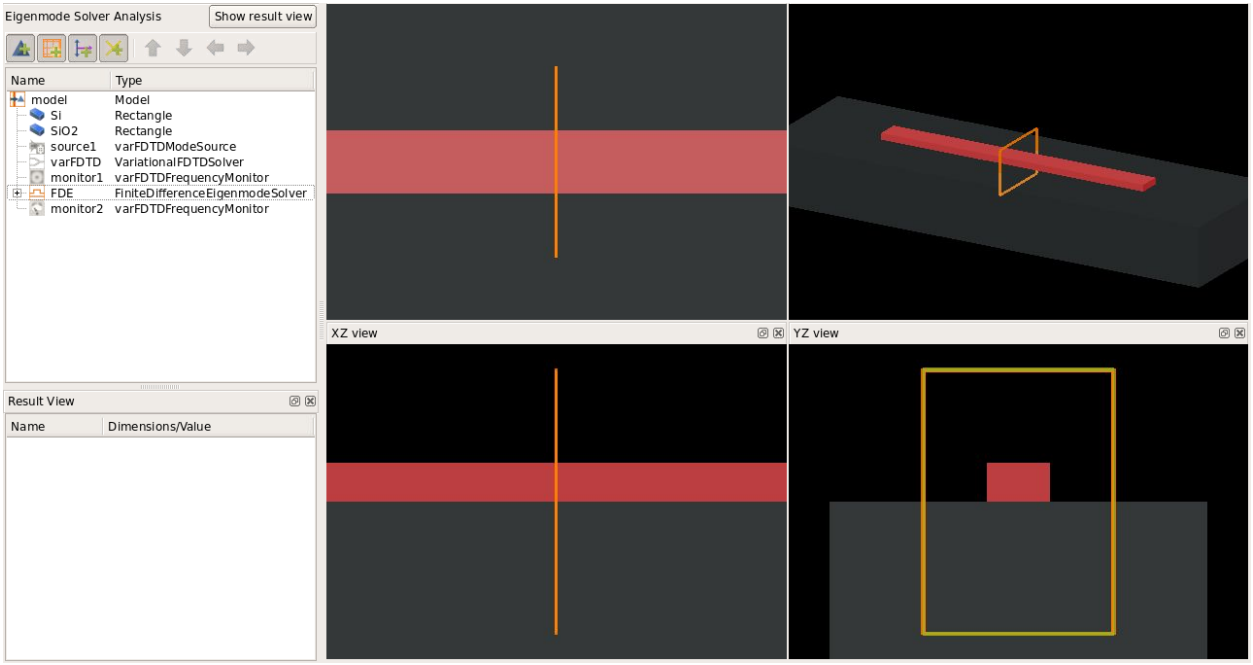

Figure 3.8: Mode Solution UI

the 2D plane and then 1D line can be used. As in my simulation, we have implemented 2D X normal type, which occupies plane YZ and is perpendicular to the direction of light transmission. Just like FDTD simulator, FDE has mesh precision setting and boundary conditions. However, FDE can provide much faster simulation speed and consumes much less computing resources even compared to 2D FDTD under the same mesh precision.

The simulation result using FDE solver can be shown in Fig. 3.9. First, we have set the wavelength to be 1550nm and have chosen the number of trial modes to be 20. The simulation result for performing modal analysis is shown in Fig. 3.9. In the mode list, we can see the effective index (both real and imaginary part), loss in dB/cm, TE polarization fraction (Ey) and waveguide TE/TM fraction (%), where both the derivation and optical properties of the effective index will be discussed in the appendix A. Although there will be more than 20 modes, as we increase the mode number, we can see that the effective index of those modes will become negligible. According to the following equation:

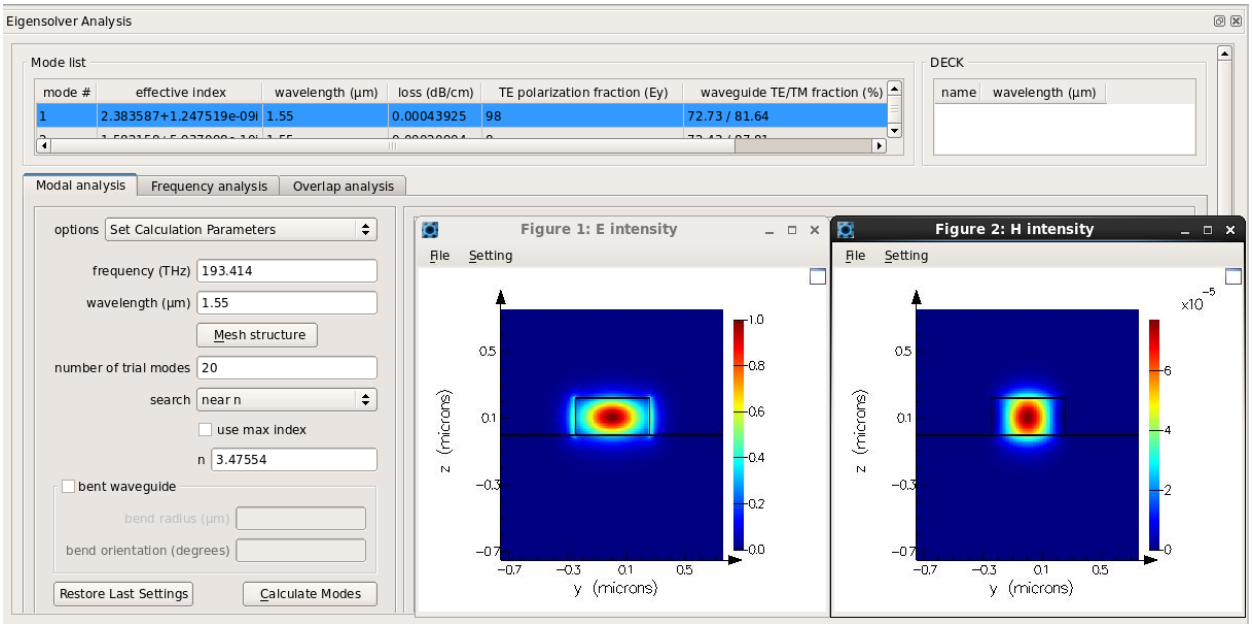

Figure 3.9: Finite Difference Eigenmode Solver

$$n_{eff} = \frac{\beta}{\kappa_0} \tag{3.1}$$

effective index is proportional to β, the propagation coefficient along the z direction, and is inversely proportional to κ_0, the vacumm wavevector of the light. As we decrease the effective index, the propagation coefficient will decrease and will result in the slower propagation of the light. Therefore, we only need to focus on the first mode instead. Mode number 1 has effective index of 2.3836 in real part with negligible imaginary part and has loss of 0.00043925dB/cm. If we look at the electrical field intensity and magnetic field intensity in amplitude, electrical field intensity is almost 10^4 times higher than that of magnetic field, which matches the 98% TE polarization result. Therefore, the mode 1 is mostly transversal electric (TE) mode.

Using FDE simulator, we can also perform frequency analysis. The following optical parameters in terms of frequency can be plotted as shown in Fig. 3.10: real and imaginary part of effective index, loss with the unit of dB/cm, group index, group delay with the unit

of ps/km, group velocity with the unit of m/s and dispersion with the unit of ps/nm/km.

Let's take a look at those optical parameters one by one, except effective index, which will be discussed in Appendix A. Since mode 1 is mostly TE mode and we assume optical wave is propagating in the xoz plane, the electric field will be in the y axis and can be described as follows:

$$E_y(x) = E_0 e^{-\gamma x} = E_0 e^{-\frac{2\pi\kappa x}{\lambda_0}} \tag{3.2}$$

where γ is the attenuation coefficient, κ is the imaginary part of effective index and λ_0 is the wavelength. Loss in the unit of dB/m can be described as follows:

$$loss = -20log_{10}^{[\frac{E_y(x=1m)}{E_y(x=0)}]} \tag{3.3}$$

Combining both equations, we can see that loss is correlated with the imaginary part of the effective index.

Group velocity describes energy traveling speed of an electromagnetic wave and can be depicted as follows where c is the speed of light, n is the effective index and λ is the wavelength:

$$v_g = \frac{c}{n - \lambda\frac{dn}{d\lambda}} \tag{3.4}$$

Group velocity is the same as phase velocity c/n when the change of effective index with respect to wavelength is zero. Since group delay is defined as the time for a light pulse to travel a certain distance, the group delay is just the inverse of group velocity.

By definition, group index describes how much the group velocity is reduced comparing

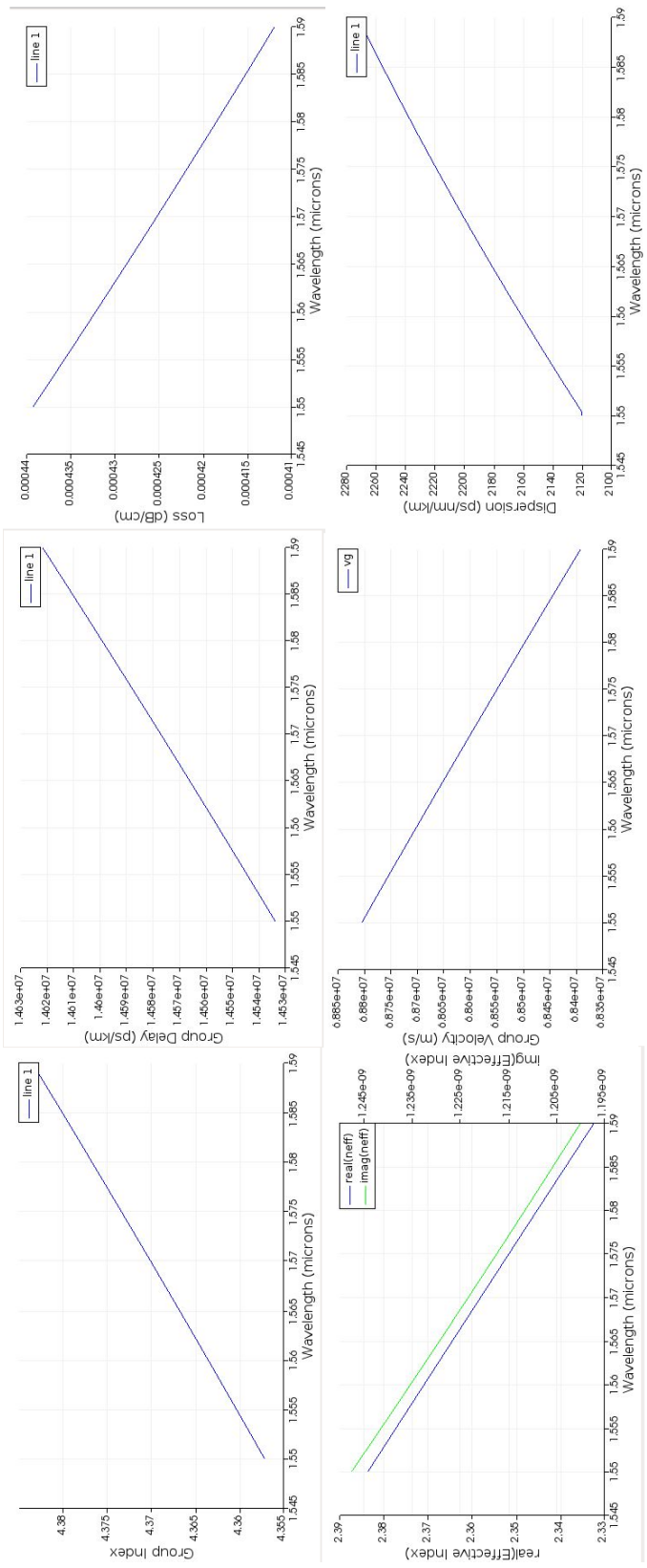

Figure 3.10: Optical Parameters Results from FDE Simulator

to speed of light in a vacuum and thus, the group index n_g is the denominator of the equation (3.4) and is shown as follows:

$$n_g = n - \lambda \frac{dn}{d\lambda} \tag{3.5}$$

Except in some anomalous dispersion regions, group index n_g will always be larger than effective index because $\frac{dn}{d\lambda}$ will be negative. It makes sense since group velocity should always be smaller than the speed of light in a vacuum.

After having passed through dispersive channels, due to the bandwidth limitation, short optical pulses will spread in time and become overlapping with each other. This phenomenon is called dispersion. Although there are three types of dispersions—material dispersion, modal dispersion and waveguide dispersion—the dispersion shown in Fig. 3.10 is group velocity dispersion, one of the material dispersion. Since group velocity dispersion results in different group velocities for different wavelengths, there will be pulse spread for different wavelengths, which can be shown as follows:

$$\Delta\tau = \frac{L}{c}(n_g(\lambda_1) - n_g(\lambda_2)) = \frac{L}{c}\frac{dn_g}{d\lambda}\Delta\lambda = -\frac{L}{c}\lambda\frac{d^2n}{d\lambda^2}\Delta\lambda = DL\Delta\lambda \tag{3.6}$$

where $D = -\frac{\lambda}{c}\frac{d^2n}{d\lambda^2}$ is called materials dispersion and it is the dispersion curve as shown in Fig. 3.10.

3.4.2 Directional Coupler

The coupled-mode theory discussion can be seen in appendix B [56]. Directional coupler is one of the special couplers where the energy of one waveguide will keep depleting itself until its energy is totally transferred to another one and energy transfers won't happen backward. Also, the energy transfer won't cause phase shift. As a result, we can derive the following

equations:

$$\beta_1 > 0, \beta_2 > 0, \kappa_{12} = \kappa_{21}^* = \kappa_{21} \tag{3.7}$$

If we apply the following initial conditions: $A(0) = A_0$ and $B(0) = 0$, the coupled-mode wave equation B.9 in appendix B can be solved and the result is shown as follows:

$$\begin{aligned} A(z) &= A_0[\cos\psi z + \frac{j\delta}{\psi}\sin\psi z]e^{-j\delta z} \\ B(z) &= -A_0\frac{j\delta}{\psi}\sin\psi z e^{j\delta z} \end{aligned} \tag{3.8}$$

where

$$\begin{aligned} \psi &= \sqrt{\kappa^2 + \delta^2} \\ \delta &= \frac{\beta_2 - \beta_1}{2} \end{aligned} \tag{3.9}$$

The power of the wave in each waveguide can be seen as follows:

$$\begin{aligned} \frac{|A(z)|^2}{A_0^2} &= 1 - F\sin^2(\psi z) \\ \frac{|B(z)|^2}{A_0^2} &= F\sin^2(\psi z) \end{aligned} \tag{3.10}$$

where maximum coupling coefficient is F and can be seen as follows:

$$F = (\frac{\kappa}{\psi})^2 = \frac{1}{1 + (\frac{\delta}{\kappa})^2} \tag{3.11}$$

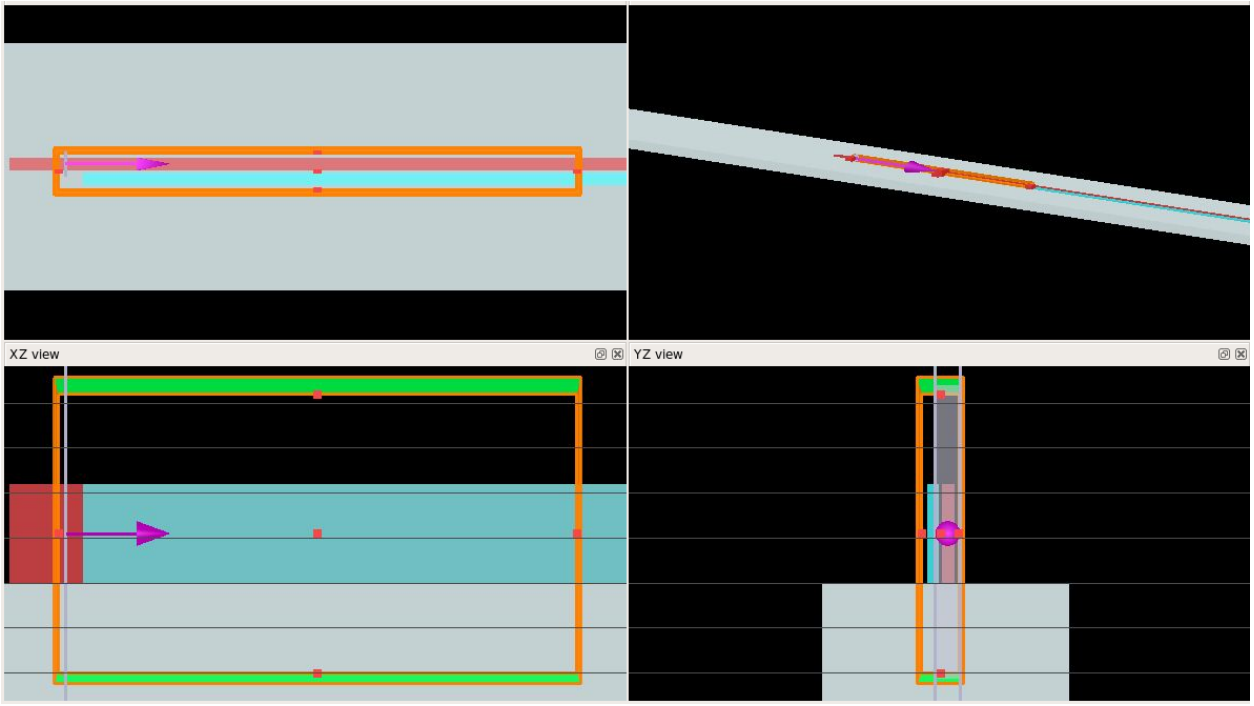

Figure 3.11: 3D FDTD simulation for Directional Coupler

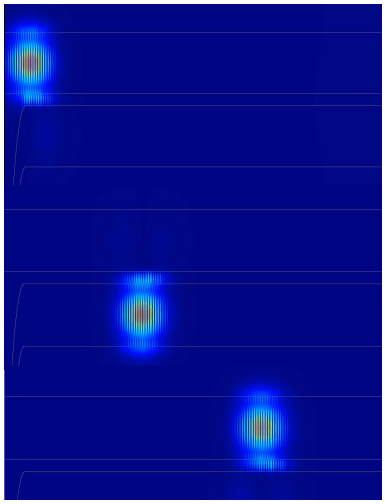

Figure 3.12: Energy Oscillating between Two Waveguides

From the resulting equations, we can see that the power can travel back and forth between two waveguides with 100 percent transfer efficiency and the power of each wave shares the same sine waveform.

To put the above equations into perspective, let's put the directional coupler structure into FDTD simulator, as shown in Fig. 3.11. The source is put into one of the waveguides

and its propagation is in the x direction. Also, we have chosen the fundamental TE mode for the source with wavelength ranging from $0.4\mu m$ to $0.7\mu m$. The resulting optical energy flow can be seen in Fig. 3.12 where the optical energy is oscillating between two waveguides with almost no energy loss visible to naked eye.

3.4.3 Phase-Shifter

Phase-shifters in optical circuits are based on the linear electrooptic effect named Pockel's effect, where the change of index of refraction happens when an external electric field is applied to a crystal. Let's look at this effect through the general modified-index ellipsoid as follows [57]:

$$(\frac{1}{n^2})_1 x^2 + (\frac{1}{n^2})_2 y^2 + (\frac{1}{n^2})_3 z^2 + (\frac{1}{n^2})_4 2yz + (\frac{1}{n^2})_5 2xz + (\frac{1}{n^2})_6 2xy = 1 \tag{3.12}$$

where $(\frac{1}{n^2})_i$ is the dielectric tensor term along the regular cartesian coordinates. If x', y' and z' are the principal axis, equation (3.12) will become

$$(\frac{1}{n^2})_1|_{E=0} = \frac{1}{n_x'^2}, (\frac{1}{n^2})_2|_{E=0} = \frac{1}{n_y'^2}, (\frac{1}{n^2})_3|_{E=0} = \frac{1}{n_z'^2} \tag{3.13}$$

and

$$(\frac{1}{n^2})_4|_{E=0} = (\frac{1}{n^2})_5|_{E=0} = (\frac{1}{n^2})_6|_{E=0} = 0 \tag{3.14}$$

The two equations above show that when there is no external electric field applied, the indices along the principle axes are uncoupled. After the electric field is applied, the change of the index ellipsoid can be described in terms of electrooptic coefficient r and is shown as

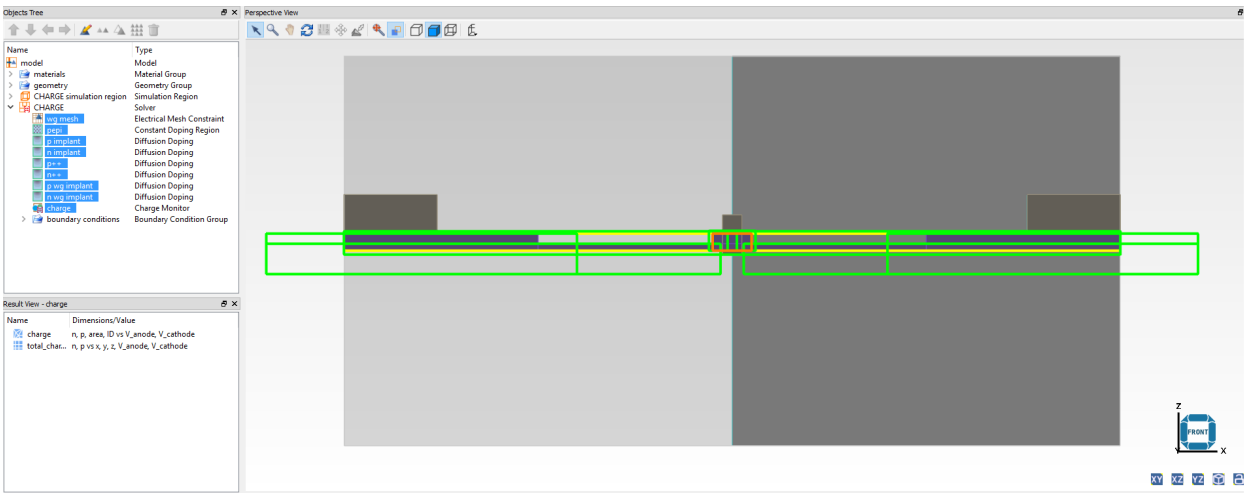

Figure 3.13: Energy Oscillating between Two Waveguides

follows:

$$\begin{bmatrix} \Delta(\frac{1}{n^2})_1 \\ \Delta(\frac{1}{n^2})_2 \\ \Delta(\frac{1}{n^2})_3 \\ \Delta(\frac{1}{n^2})_4 \\ \Delta(\frac{1}{n^2})_5 \\ \Delta(\frac{1}{n^2})_6 \end{bmatrix} = \begin{bmatrix} r_{11} & r_{12} & r_{13} \\ r_{21} & r_{22} & r_{23} \\ r_{31} & r_{32} & r_{33} \\ r_{41} & r_{42} & r_{43} \\ r_{51} & r_{52} & r_{53} \\ r_{61} & r_{62} & r_{63} \end{bmatrix} \bullet \begin{bmatrix} E_1 \\ E_2 \\ E_3 \end{bmatrix} \tag{3.15}$$

where the matrix r_{ij} is called the electrooptic tensor.

In silicon photonics, phase-shifters are usually implemented using pn junctions. Since there is doping involved, we can't use FDTD or Mode simulator. Therefore, the pn junction phase-shifter can only be simulated in details using the new Lumerical Charge simulator as shown in Fig. 3.13, where we have different doping regions, electric mesh constraints, boundary conditions and the charge monitor. The boundary condition is able to set up anode/cathode for the pn junction in any specific block where both steady state and transient voltages can be applied. Even surface recombination effect can be considered in the set up for boundary condition. Charge monitor is used to plot the n-doping and p-doping inside

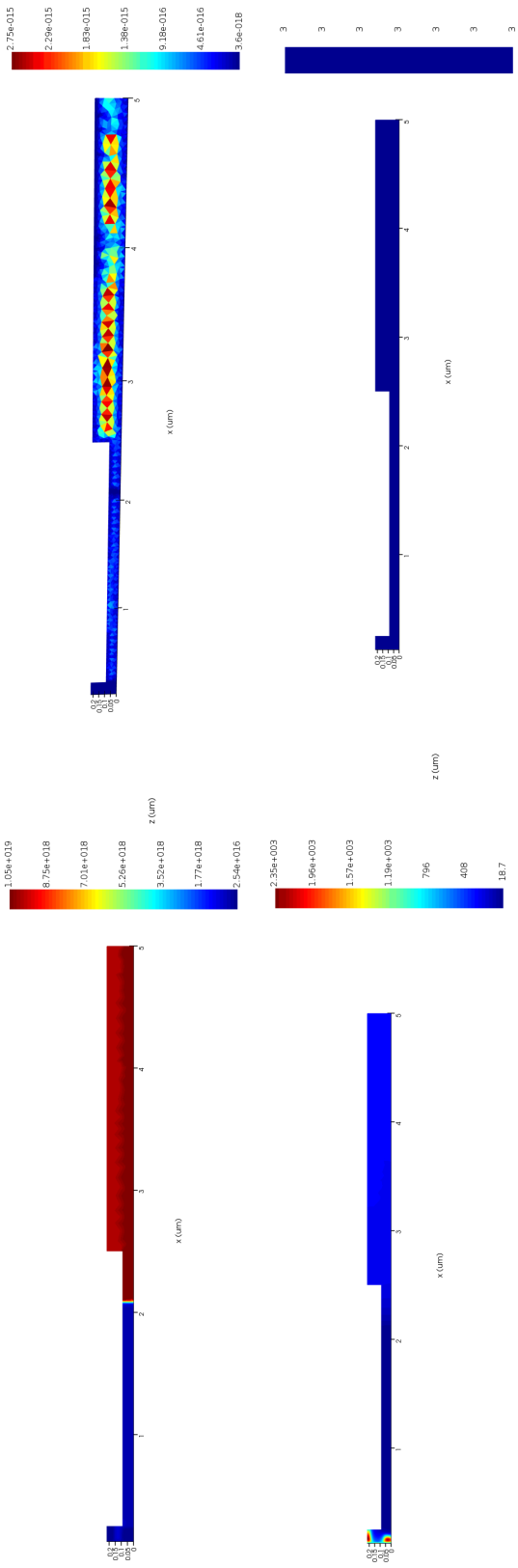

Figure 3.14: Charge Simulation Result for PN Junction

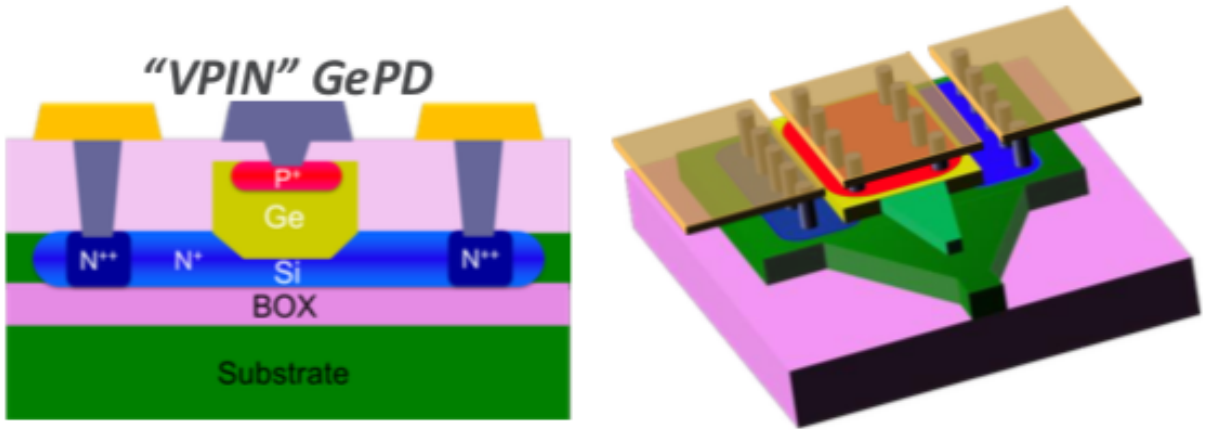

Figure 3.15: Ge Waveguide Photodiode
[55]

the pn junction according to the voltage biasing condition listed in the boundary conditions. The simulation result with anode biased at 1V can be seen in Fig. 3.14 including n doping, p doping, charge distribution and current through the pn junction. Junction resistance can be derived since current is known through the pn junction and junction capacitance can be derived since charge is known too.

3.4.4 Photodetector

Photodetectors are the devices used to convert the optical signals into electrical signals. As shown in Fig. 3.15, Ge waveguide p-i-n photodiode is one of the common variations of the photodiode used in optoelectronic devices and is available in iSiPP50G platform.

The mechanics that most detectors are based on is internal photoeffect where a photon creates a free carrier, an electron in conduction band or a hole in valence band. The resulted excess free carriers are able to change the conductivity and junction voltage. Junction current can be created by free carriers being swept away through biasing voltages applied to anode or cathode or both.

P-i-n photodiode, on the other hand, introduces intrinsic region. Under the same reverse biasing condition, intrinsic region has larger area than the regions with higher doping. By

creating larger areas, more incident radiation can be absorbed and then more free carriers can be generated. As a result, higher responsitivity can be achieved for photodetectors. Also, since photodetector is reversely biased, a larger depletion region also reduces the junction capacitance.

In order to detect the optical signals, certain signal to noise ratio is required for the p-i-n photodiode. The main noise for the photodiode is the shot noise and the shot noise is directly related to current. There are two types of mechanisms for generating current. First, since photodiode can't be in the temperature of absolute zero, there will be spontaneous electron generation through thermal excitation. Second, due to the carrier gradient inside of the p-i-n junction, there will be carrier diffusion and it will produce current. The dark current, one of the parameters used for photodiode, is the junction current when a photodetector is strongly reverse-biased.

3.5 Modulators

3.5.1 Electro-Absorption Modulator

When the photon energy becomes so high that band-to-band transition happens, light will begin to be absorbed by the semiconductor, which is when absorption discontinuity or absorption edge appears. If we apply an external electric field to the semiconductor, a linear band-bending will occur near the surface for both conduction band and valence band. As a result, the electrons will be able to tunnel to the conduction band and it will lead to the redshifting of the absorption edge. This effect is called Franz-Keldysh effect [58]. Although there is another effect called quantum-confined stark effect (QCSE), which can produce even higher absorption coefficient, the QCSE has the absorption area in terms of the same of quantum well while Franz-Keldysh effect has much longer absorption area without the limitation of quantum well. As a result, optical devices based on Franz-Keldysh effect have much higher absorption coefficient than those based on quantum-confined Stark effect.

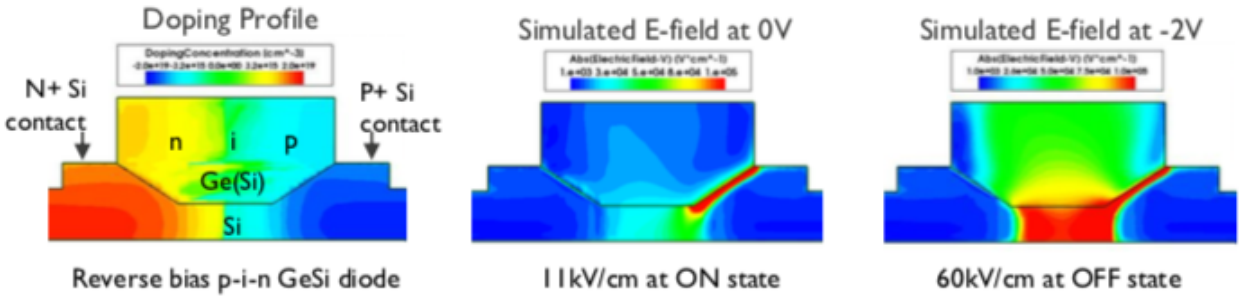

Figure 3.16: Electro-absorption Modulator used in iSiPP50G Platform [55]

The electroabsorption modulator used in iSiPP50G platform can be seen in Fig. 3.16. The device used here is the p-i-n GeSi diode and the figure shows its cross section where the light is propagating perpendicularly. Its doping profile can be seen in Fig. 3.16(a) and the other two sub-figures show the electric field during the on and off state of the device where the on state happens when zero electric field is applied and the off state occurs when reverse electric field is implemented.

Fig. 3.17 shows the different absorption coefficients in terms of wavelength under different biasing conditions. Under the same wavelength, the higher the reverse biasing voltage, the higher the absorption. The electro-optic S_{21} response can be seen in Fig. 3.18 and we can see that the 3dB bandwidth is larger than 50GHz, which is the reason why the electro-absorption modulator is attractive.

3.5.2 Mach Zehnder Modulator

The Mach Zehnder modulator (MZM) is based on the Mach Zehnder interferometer (MZI) but how phase-shift is achieved is different for both devices. Let's look at how to achieve MZI using discrete optical components, as shown in Fig. 3.19. The light is split into two paths, path a and path b, through the beam splitter (BS_c). Although two paths have the same route distance, path a has a phase-shifter. The mirrors can change the propagation direction of the light. As a result, when the beam splitter (BS_q) is present, the interference pattern will appear in detector D_a and D_b.

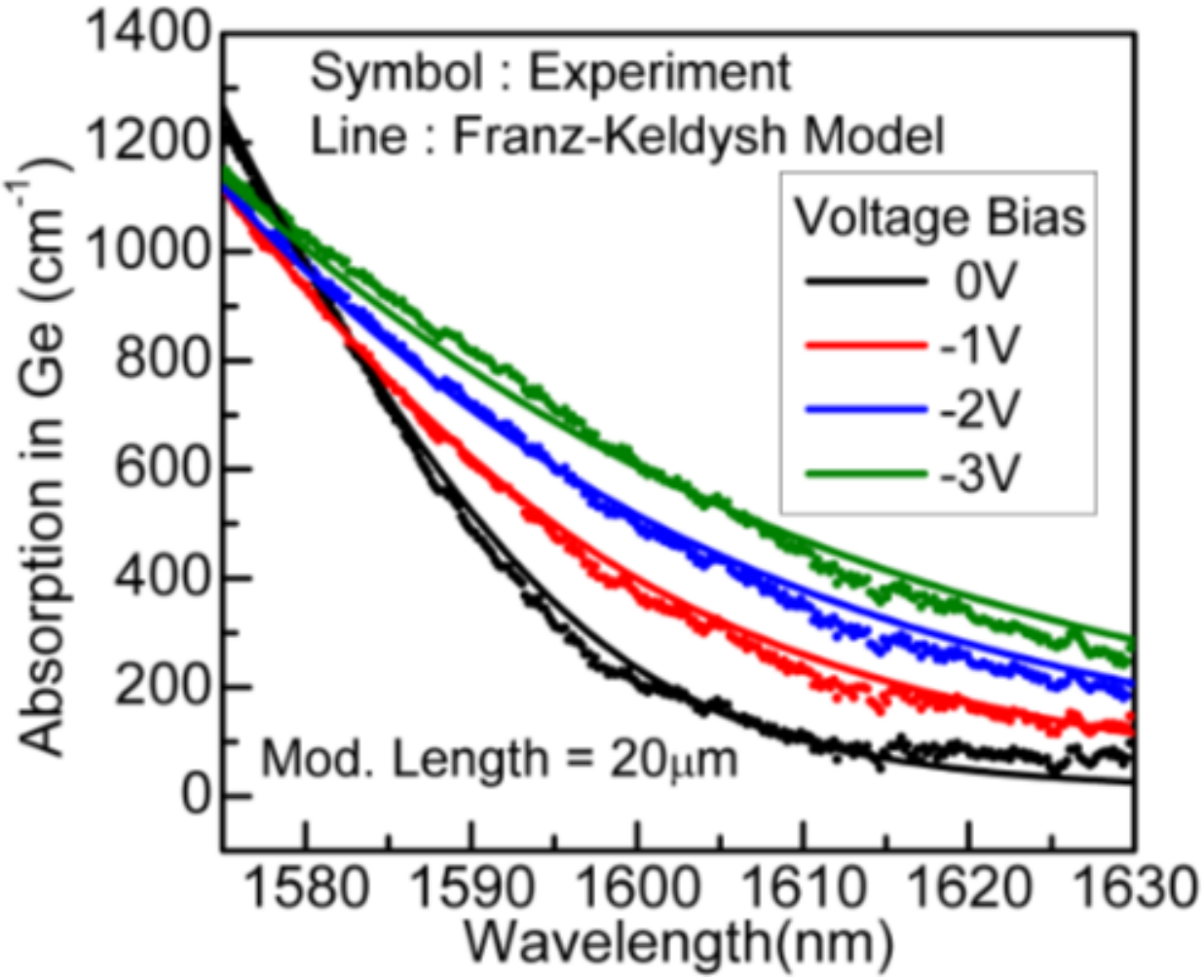

Figure 3.17: Absorption Coefficient of Electro-absorption Modulator under Different Biasing Conditions
[55]

In order to implement Mach Zehnder modulator using Silicon Photonics Technology, we have to find a way to realize the functions of mirrors, beam splitters and phase-shifters used in discrete optical components. As a result, the implementation of MZM using silicon photonic technology can be presented in Fig. 3.20. First, there are no mirrors to guide the light. Instead, light is guided through silicon ridge waveguide. Second, beam splitting is realized through a Y splitter/combiner, which shares the same architecture and their difference lies in difference of the light propagating direction. Also, we can see from both figures, there is radiation and reflection involved for both splitting and combining light, which will be

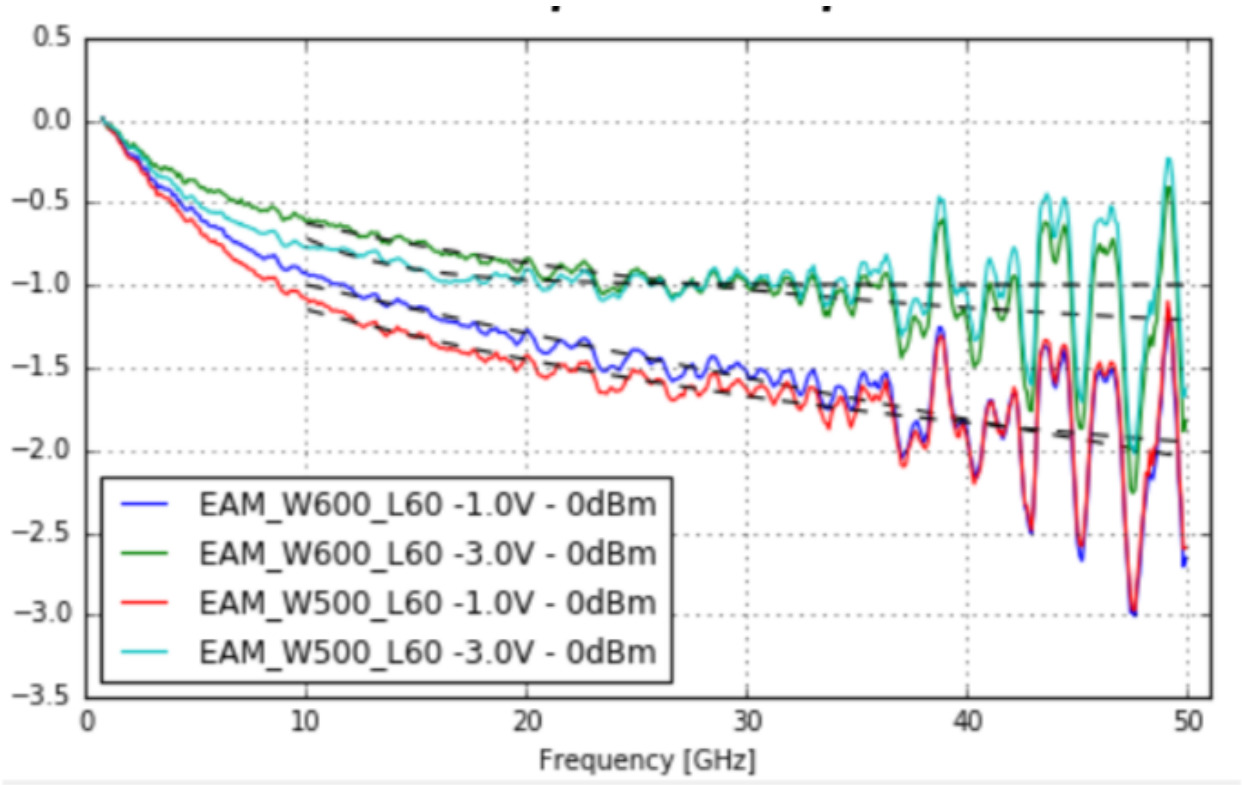

Figure 3.18: Electro-Optic S_{21} Response
[55]

translated into loss.

One of the most important features for the Mach Zenhder modulator is to introduce phase-shift between two paths, which is realized through phase-shifters. However, according to Fig. 3.20, where no additional blocks are inserted like Fig. 3.19, phase-shifter is implemented through the same waveguide but with different doping profiles as discussed in the phase-shifter chapter.

One of the ways to depict the light wave is to think of it as an electric field $Ee^{-i\phi}$ with field amplitude of E and phase of ϕ. Since the Y splitter evenly diverts the light wave into two paths, the amplitude of the electric field for both paths is the same while there will be phase difference introduced between two paths because of the phase-shifter. If we assume the phase of the electric field for the up path and down path before entering the Y combiner is ϕ_1 and ϕ_2 respectively and the amplitude of the electric for both paths is E, the output

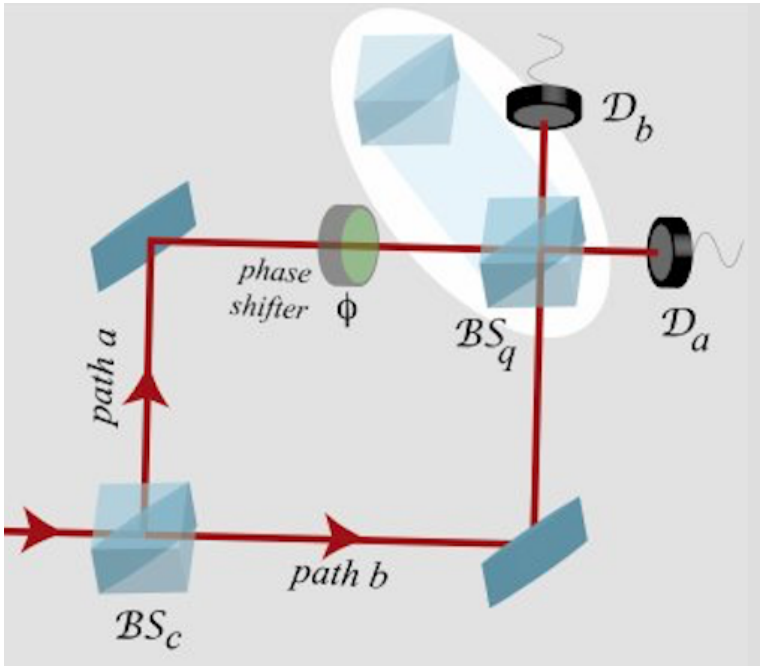

Figure 3.19: Schematic Diagram of the Mach Zehnder Interferometer [59]

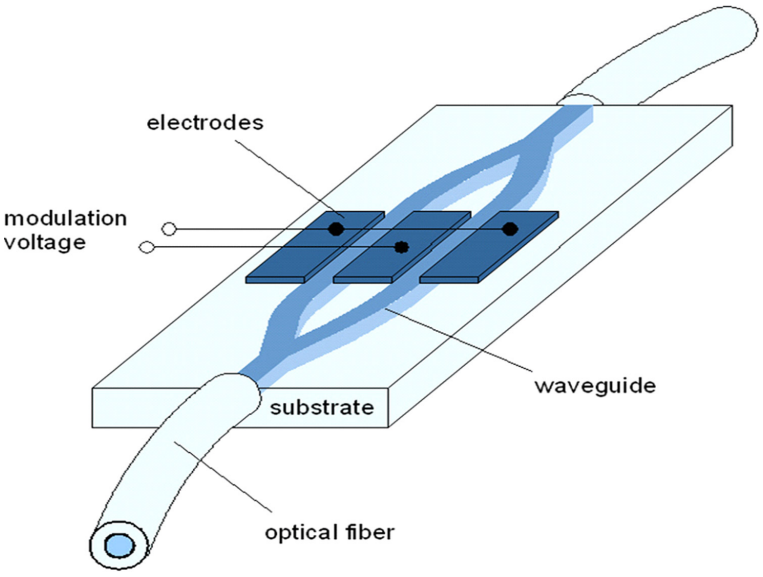

Figure 3.20: Silicon Photonics Implementation of the Mach Zehnder Modulator [60]

light intensity of the MZM is

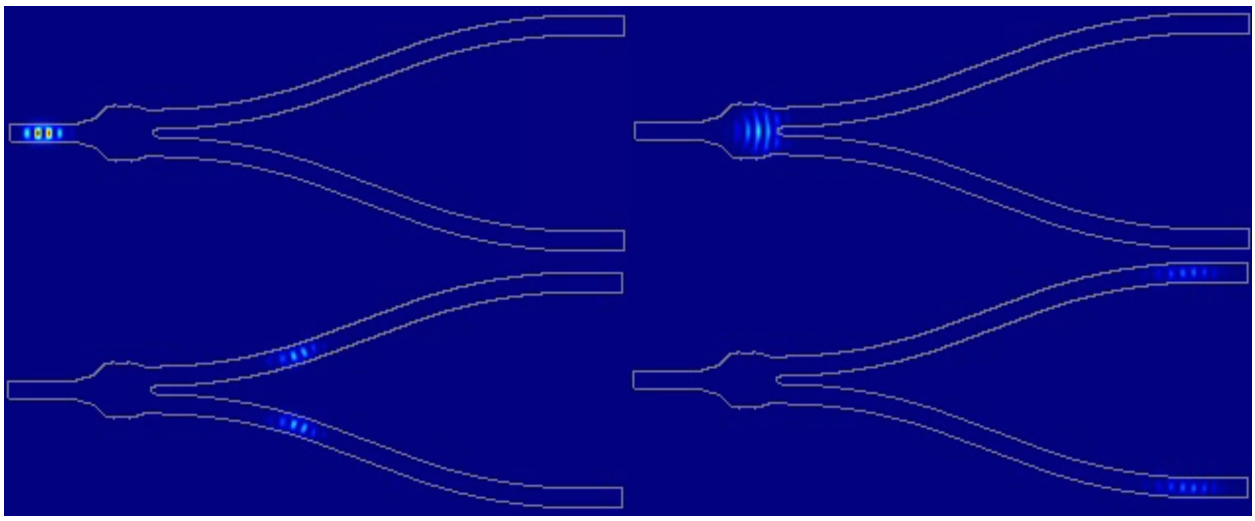

Figure 3.21: Y-junction Splitter

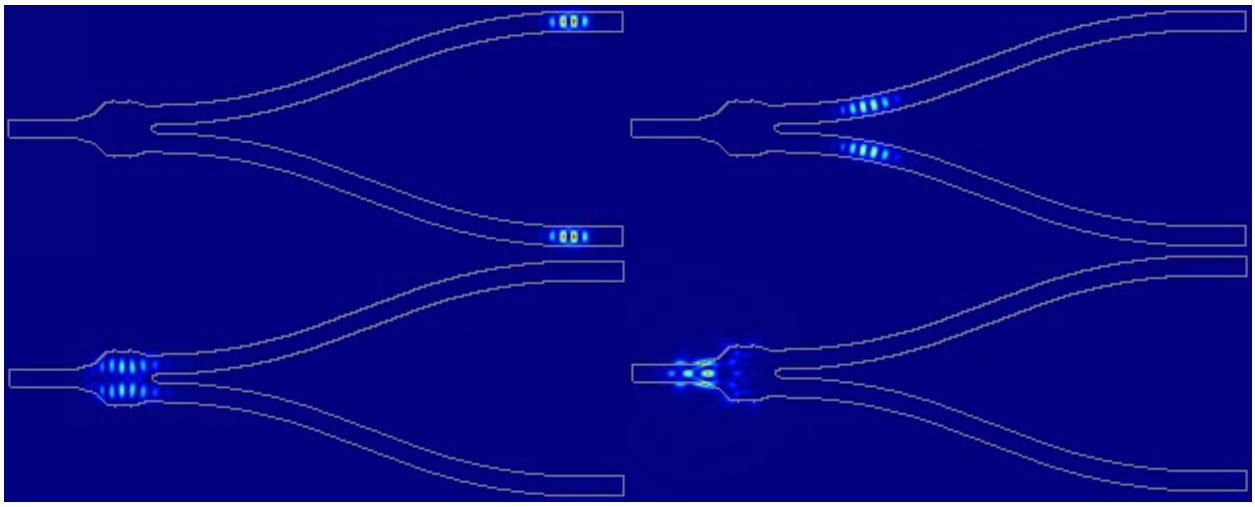

Figure 3.22: Y-junction Combiner

$$I_{output} \propto \left| \frac{1}{\sqrt{2}} E e^{-i\phi_1} + \frac{1}{\sqrt{2}} E e^{-i\phi_2} \right|^2 = \frac{1}{2}(1 + \cos\Delta\phi) I_{input} \tag{3.16}$$

where $\Delta\phi$ is the phase-shift between two paths.

The transmission curve of the MZM can then be derived as follows:

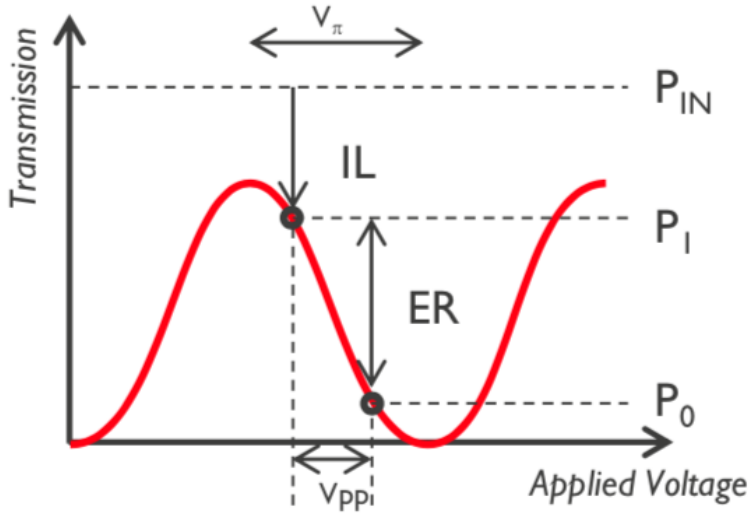

Figure 3.23: MZM Transmission Curve
[55]

$$Transmission = \frac{I_{output}}{I_{input}} = \frac{1}{2}(1 + \cos\Delta\phi) \tag{3.17}$$

Then, the transmission curve can be plotted as shown in Fig. 3.23. One of the parameters used in MZM is V_π, describing the biasing voltage for achieving π phase shift between two paths. However, since the longer the phase-shifter is, the lower voltage V_π can be, it can only represent the modulation intensity of each device. Also, considering the phase-shifter is realized through different dopings and each Silicon Photonics Technology has its doping profiles, there should be a parameter reflecting the modulation efficiency, which will only be technology dependent. That's why the modulation efficiency is considered and in the case of MZM, the modulation efficiency is $V_\pi L_\pi$.

Fig. 3.24 shows the electro-optic S_{21} response and we can see that 3dB bandwidth is only approximately 20GHz, which is much smaller than that of EAM discussed before. One of the reasons is that the long phase-shifter has the equivalent impedance of 50Ω, which has to be impedance matched and thus, more parasitic capacitance is introduced in the process. EAM, on the other hand, has mostly capacitive impedance, the same as microring modulator

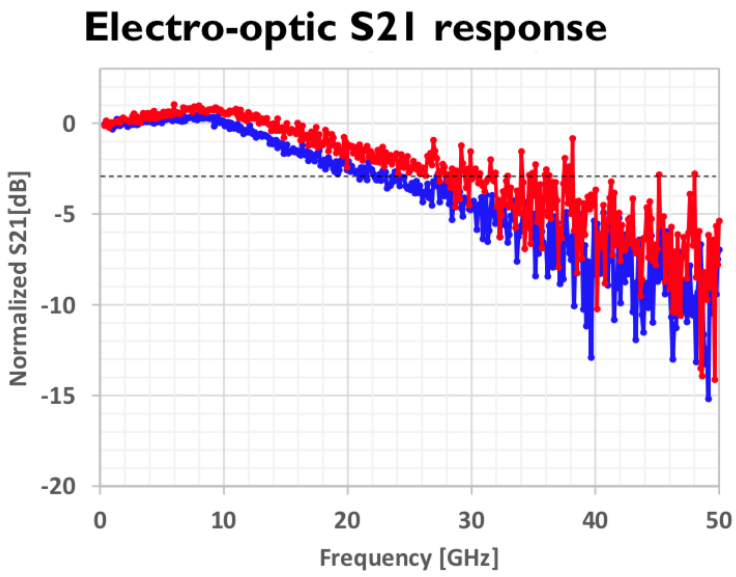

Figure 3.24: Electro-optic S_{21} Response
[55]

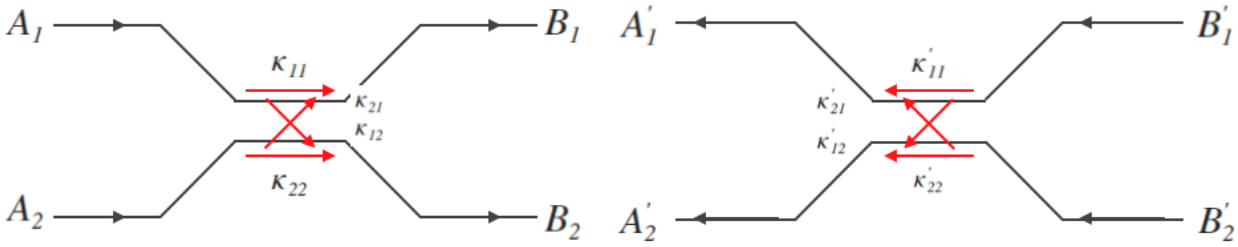

Figure 3.25: Simplified Point Coupler Model

(MRM).

3.5.3 Microring Modulator

Just like Mach-Zehnder modulators that are based on MZI, microring modulator has its origin in microring resonator. Therefore, in order to understand the optical properties of microring modulator, let's first look at those of microring resonator. Since point coupling is used in microring resonator, we will discuss it first.

The simplified point coupler model can be seen in Fig. 3.25. On the left, light is passing from left to right with two inputs A_1/A_2 and two outputs B_1/B_2. On the right, light is passing from right to left with two inputs B_1'/B_2' and two outputs A_1'/A_1'. Thus, the coupling action

can be described by the following transmission matrix:

$$\begin{pmatrix} B_1 \\ B_2 \end{pmatrix} = \begin{pmatrix} \kappa_{11} & \kappa_{21} \\ \kappa_{12} & \kappa_{22} \end{pmatrix} \begin{pmatrix} A_1 \\ A_2 \end{pmatrix} = X \begin{pmatrix} A_1 \\ A_2 \end{pmatrix}$$
$$\begin{pmatrix} A_1^{'} \\ A_1^{'} \end{pmatrix} = \begin{pmatrix} \kappa_{11}^{'} & \kappa_{21}^{'} \\ \kappa_{12}^{'} & \kappa_{22}^{'} \end{pmatrix} \begin{pmatrix} B_1^{'} \\ B_2^{'} \end{pmatrix} = X^{'} \begin{pmatrix} B_1^{'} \\ B_2^{'} \end{pmatrix} \tag{3.18}$$

Due to the time reversal symmetry, we can derive the following:

$$\begin{pmatrix} B_1 \\ B_2 \end{pmatrix} = \begin{pmatrix} B_1^{'} \\ B_2^{'} \end{pmatrix}^*$$
$$\begin{pmatrix} A_1 \\ A_2 \end{pmatrix} = \begin{pmatrix} A_1^{'} \\ A_1^{'} \end{pmatrix}^* \tag{3.19}$$

Then,

$$X^{'} X^* = I \tag{3.20}$$

where the asterisk denotes the conjugate transpose of the matrix and I is the identity matrix. If we again impose the principle of reciprocity (it means that the coupling coefficients are independent of propagation direction), we have the following equation:

$$X^{'} = \widetilde{X} \tag{3.21}$$

As a result,

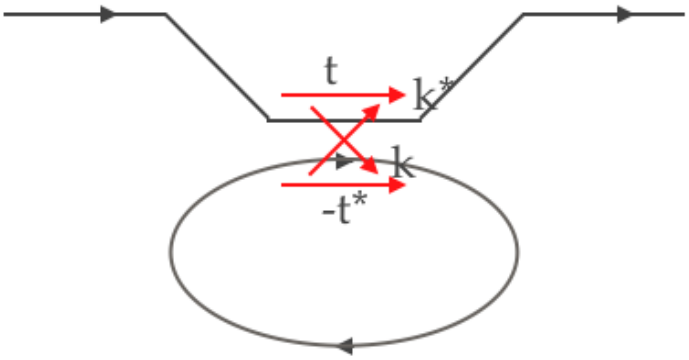

Figure 3.26: Further Simplified Point Coupler Model

$$XX^{\dagger} = I \tag{3.22}$$

where $X^{\dagger}$ is the Hermitian conjugate of X and thus, X is Unitary matrix. And if we choose the determinant of X to be -1 and also define κ_{11} as t and κ_{12} as κ, the matrix X can be represented as follows and the coupling model can be depicted in Fig. 3.26:

$$X = \begin{pmatrix} t & \kappa^* \\ \kappa & -t^* \end{pmatrix} \tag{3.23}$$

There are two types of ring resonators: add-drop and all-pass. Since we are going to use microring modulator based on all-pass ring resonator, only all-pass one will be discussed here. To derive the mathematical model for microring resonator, we can plot the most basic microring resonator model as shown in Fig. 3.27. The electric field transmission result of the all-pass ring resonator can be seen as follows:

$$\frac{E_{t1}}{E_{i1}} = \frac{-A + te^{-i\delta}}{-At^* - e^{-i\delta}} \tag{3.24}$$

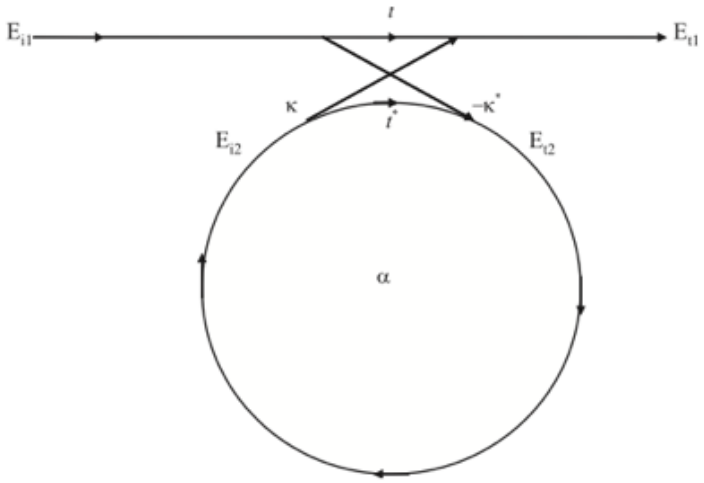

Figure 3.27: All-pass Microring Mathematical Model
[61]

where A is the round-trip amplitude loss and δ is round-trip phase shift, which can be defined in the following equation:

$$E_{i2} = e^{-\frac{\alpha}{2}2\pi R} e^{i\kappa 2\pi R} E_{t2} \equiv A e^{i\delta} E_{t2} \tag{3.25}$$

If we define T_R as the round-trip traveling time, we have the following equation:

$$\delta = \omega R \tag{3.26}$$

Thus, δ is also called normalized phase detuning and can be plotted in Fig. 3.28. We can see that as we decrease the coupling coefficient (increasing t), the center slope decreases, which signifies the decreasing of phase sensitivity. Under the lossless condition, the slope of the center is the same as the intensity buildup in the ring resonator. Also, the group delay T_D can be shown as follows:

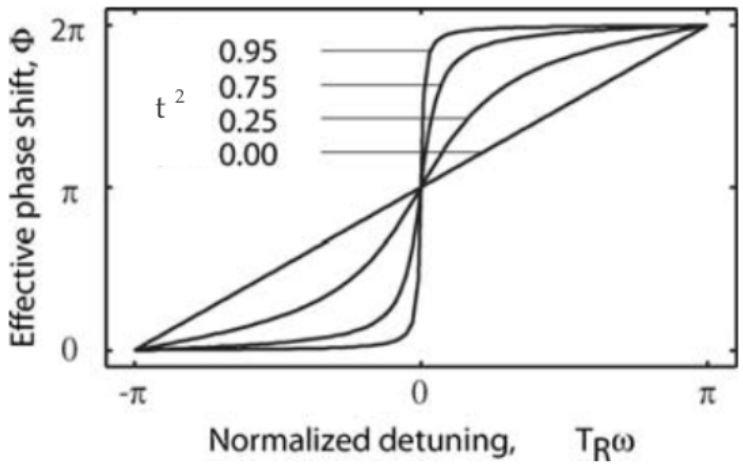

Figure 3.28: Normalized Phase Detuning
[61]

$$T_D = -\frac{d\Phi}{d\omega} = \Phi' T_R \tag{3.27}$$

where T_R is the cavity transit time. Therefore, the group delay is the cavity transit time enhanced by phase sensitivity and is equal to cavity life time. Also, the phase sensitivity is the effective number of round-trip that light transverses in the resonator.

There are three types of coupling conditions. Critical coupling happens when the microring resonator transmission intensity is zero. Since at the resonance, $\delta = 2\pi m$ and m is integer, we have the coupling coefficient for the critical coupling derived through the following equation:

$$|\kappa| = \sqrt{1 - t^2} = \sqrt{1 - |A|^2} \tag{3.28}$$

Thus, undercoupling happens when the coupling coefficient is less than that in the critical coupling scenario while overcoupling happens when the coupling coefficient is larger than that in the critical coupling coefficient. However, in both scenarios, the transmission intensity

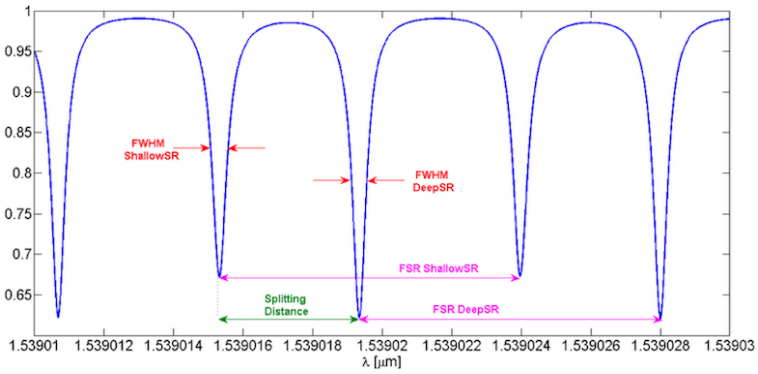

Figure 3.29: Transmission Curve for the Microring Resonator [62]

will be bigger than zero.

To understand the parameters for the microring resonator, let's look at the transmission curve with regard to the wavelength as shown in Fig. 3.29.

First, the transmission curve is periodic. The period is called free spectrum range (FSR), which can be expressed through either wavelength $\Delta\lambda$ or frequency $\Delta\upsilon$ as shown below:

$$\begin{aligned} \Delta\upsilon &= \frac{c}{2\pi R n_{eff}} \\ \Delta\lambda &= \frac{c}{2\pi R n_{eff}} \frac{\lambda^2}{c} \end{aligned} \tag{3.29}$$

where R, n_{eff} are the radius and the effective index of the microring respectively.

For each dip in the transmission curve due to ring oscillation, there is a parameter named full width at half maximum (FWHM) linewidth expressed through wavelength $\Delta\lambda_{1/2}$ or frequency $\Delta\upsilon_{1/2}$, as shown in the following equations:

$$\begin{aligned} \Delta\upsilon_{1/2} &= \frac{c}{2\pi R n_{eff}} \frac{1-tA}{\pi\sqrt{tA}} \\ \Delta\lambda_{1/2} &= \frac{\lambda^2}{2\pi R n_{eff}} \frac{1-tA}{\pi\sqrt{tA}} \end{aligned} \tag{3.30}$$

The intensity buildup B can be derived, which is disproportional to the coupling coeffi-

cient:

$$B \equiv \left|\frac{E_{i2}}{E_{i1}}\right|^2 = \frac{4}{|\kappa|^2} \tag{3.31}$$

One of the unique parameters used in optical circuit is called finesse F and can be presented as follows:

$$F = \frac{\Delta\lambda}{\Delta\lambda_{1/2}} = \frac{\Delta\upsilon}{\Delta\upsilon_{1/2}} = \frac{\pi\sqrt{tA}}{1-tA} \approx \frac{2\pi}{2\pi R\alpha + |\kappa|^2} \tag{3.32}$$

where

$$tA \equiv e^{-2\pi R\alpha_{tot}} = e^{-[\frac{\alpha}{2}2\pi R - \ln t]} = te^{-\frac{\alpha}{2}2\pi R} \tag{3.33}$$

Just like in electrical ring resonator, the parameter quality factor can also be used in microring resonator and can be derived as follows:

$$Q = \frac{\omega_0}{\Delta\omega_{1/2}} = \frac{\omega_0}{\Delta\omega}F = \frac{2\pi R n_{eff}}{\lambda_0}F = \frac{2\pi R}{\lambda}F \tag{3.34}$$

If we define m as $2\pi R/\lambda$, m is representing the order (azimuthal number) of a particular resonance ω_0, which is the measurement of the number of wavelength within the microring circumference. Also, the order is also the indicative of the m^{th} peak in the spectrum and directly relates with the quality factor to the finesse. If we define N as the number of round-trips required to reduce the energy to 1/e of the initial value due to internal loss and bus waveguide, we get $F = 2\pi N$ and $Q = \omega_0 T_R N$, which results in $F = Q/m$. Quality factor

Q represents the number of oscillations inside the microring before the circulating energy is depleted to 1/e of the initial energy. Since it takes more than one round trip for an oscillation to disappear, there is an energy buildup inside of the ring. Therefore, light interacts with the coupling interface for a F number of times while interacting with the cavity of microring for a Q number of cycles.

As mentioned in the previous chapter, the waveguide has an effect called dispersion where the effective index of the waveguide is wavelength dependent. Therefore, the free spectrum range is not constant across all the wavelengths for microring resonator, which is comprised of ring-shape waveguide and a coupler. If we simplify the dispersion effect by linearizing the relationship between effective index and wavelength around my microring resonant wavelength of interest, the parameter FSR has to be modified accordingly.

Since each resonant wavelength of interest has two adjacent resonant wavelengths due to its periodicity, there are two FSRs. Therefore, we can average out those two FSRs so that the dispersion effect is included. As a result, we can derive the following equation:

$$\frac{4\pi c}{L} = n_3\omega_3 - n_1\omega_1 \tag{3.35}$$

then,

$$\frac{4\pi c}{L} = \omega_3(n_2 + \frac{\Delta\omega}{2}\frac{dn}{d\omega}|_{\omega=\omega_2}) - \omega_1(n_2 - \frac{\Delta\omega}{2}\frac{dn}{d\omega}|_{\omega=\omega_2}) = \Delta\omega(n_2 + \omega_2\frac{dn}{d\omega}|_{\omega=\omega_2}) \tag{3.36}$$

where L is the circumference of the microring, n_2 is the effective index of the resonance wavelength of interest, n_1/n_3 are the effective index of the two adjacent resonant wavelength.

Therefore, the FSR in terms of frequency can be shown as follows:

$$\Delta\upsilon = \frac{\Delta\omega}{2 \times 2\pi} = \frac{c}{L(n_2 + \omega_2 \frac{dn}{d\omega}|_{\omega=\omega_2})} = \frac{c}{Ln_g} \tag{3.37}$$

where the term $n_2 + \omega_2 \frac{dn}{d\omega}|_{\omega=\omega_2}$ is defined as group index of the waveguide at the resonant wavelength and is denoted as n_g.

If we compare equation 3.37 with 3.29, both are similar except effective index is replaced with group index. Similarly, FSR in terms of wavelength can be expressed as follows:

$$\Delta\lambda = -\frac{\lambda_2^2}{Ln_g} \tag{3.38}$$

where

$$n_g = n_2 - \lambda_2 \frac{dn}{d\lambda}|_{\lambda=\lambda_2} \tag{3.39}$$

The discussion above is only about microring resonator but microring modulator has almost the same optical characteristics except that the ring waveguide is replaced with ring phase-shifter. Since the effective index (both real and imaginary part) of the phase-shifter is depending on the biasing voltage, the transmission curve will be biasing voltage dependent and one of the examples can be seen in Fig. 3.30. The y-axis shows the output intensity of microring modulator with the unit of dBm, which is the same as the transmission curve when its input is 1mW. When the phase-shifter is reversely biased, the transmission curve is shifting to the right (redshift) and the wavelength shift distance is called modulation efficiency.

Usually, microring modulator is used in narrowband and thus, we are only interested in a single wavelength. At single wavelength, there are two P_{out}, P_1 and P_2 since there are two

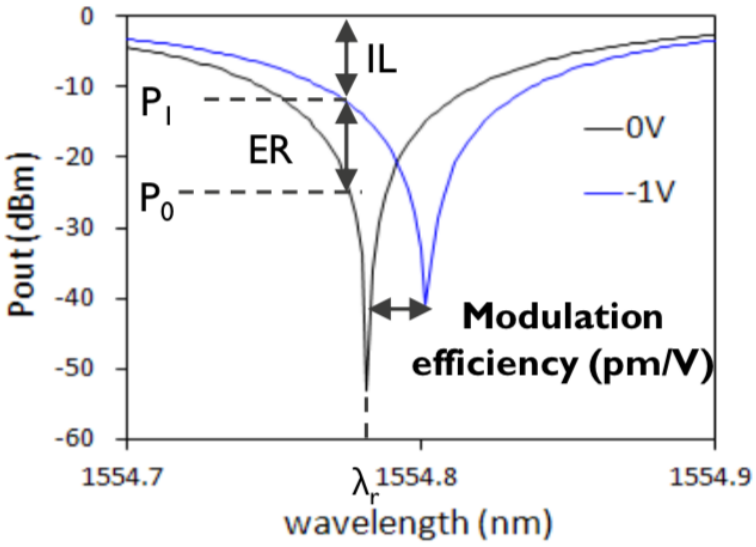

Figure 3.30: Transmission Curve for Microring Modulator under Different Biasing Conditions [61]

biasing voltages. There are two parameters, extinction ratio and insertion loss. Extinction ratio (ER) represents the power difference between P_1 and P_2 as shown as follows:

$$ER = 10 \log_{10} \frac{P_1}{P_0} \tag{3.40}$$

Insertion loss (IL) shows how much power is lost in the microring modulator when the output power of the microring modulator is at maximum level of certain wavelength and can be seen as follows:

$$IL = -10 \log_{10} P_1 \tag{3.41}$$

Chapter 4: Silicon Photonics Device Modeling Based on IMEC iSiPP50G Technology

4.1 Verilog-A Modeling

Verilog HDL is one of the hardware discriptive languages that is widely used to design FPGA and other configurable logic-based devices. Each building block in Verilog HDL is named module, described through its input/output ports and external parameters applied to the module. However, Verilog HDL has limitations and only can be used for designing logic-based circuits, which is not applicable for either analog or mix-signal integrated circuit design.

Verilog-AMS HDL, on the other hand, is based on Verilog HDL but has extended the hardware descriptive language applications towards both analog circuits and mixed-signal circuits design by implementing a continuous-time simulator, which is able to solve differential equations used in analog systems. As a result, Verilog-AMS HDL not only can describe high-level behaviors but also is able to depict the structural details such as interconnections between sub-components of the circuits.

However, the applications of the Verilog-AMS HDL is not limited to the electrical systems. Since Verilog-AMS HDL is based on continuous-time simulator, which is able to solve differential equations, it can be used in other disciplines which are continuous systems such as mechanical systems, fluid dynamic systems, thermodynamics systems and in my case, optical systems. More specifically, Verilog-AMS HDL is based on the law of conservation and it is the natural extension of analog circuits: the generalized form of Kirchhoff's Potential and Flow Laws (KPL and KFL) used in analog circuits is the extension of the law of conservation, whose definition is set up through the quantities such as voltage and current associated with the analog behaviors [63].

In order to define an optical system using Verilog-AMS HDL, we need to define its nature, access, discipline and potential.

A nature is a set of attributes, which define certain characteristics of the nature. Attributes can include but are not limited to abstol (provides a tolerance metric for convergence), access (identifying the name of the accessed function), idt_nature (the time integral of the nature), ddt_nature (the time derivative of the nature) and unit of the nature, where both idt_nature and ddt_nature are optional. For example, both voltage and current are natures. According to the definition of current in electrical system, its access is "I", its unit is "A", its idt_nature is charge and its abstol depends on the simulation precision.

A discipline describes a realm where a collection of natures are bound to and a domain type is defined. The definition of the discipline doesn't have to be limited to broad concepts such as electrical or optical and either voltage or current can be defined as a discipline. However, when electrical is defined as a discipline, it is a conservative discipline, which contains the nature voltage as potential and the nature current as flow. When either voltage or current is defined as a discipline, voltage and current are both potentials and thus, we call it a signal-flow discipline.

In my design, if we define optical as my discipline, we have to decide whether it is either a signal-flow discipline or a conservative discipline. Also, we need to define natures that are bound to my optical discipline.

Although optical signals can be described through electric field and magnetic field with different optical modes, we can't include all of the information into my Verilog-AMS model since the simulation time will be too long once extraction simulation is required to verify my designed circuits. Therefore, we need to simplify the optical signals as much as possible. According to the simulation result of the FDE solver from Lumerical's Mode Solution, the first mode of optical signals inside of silicon ridge waveguide is dominantly TE mode and can be described through only the electric field. According to the axis setup of Fig. 3.8, the TE mode has its electric field transverse to the light propagating plane. Since the light propagating plane is zox, the electric field of the TM mode will be in the y axis. Besides, with the implementation of effective index method [64], the electric field will also be equal

in the zox plane and thus, can be described as $E_y(x)$. Thus, the electric field can be seen as a one-dimensional signal similar to the voltage signal in electrical circuits. Therefore, we have defined a signal-flow discipline named "optical" with a defined nature named "Efield" as its attribute. The nature "Efield" has the unit of "V/m", abstol of 1^{-6} and access of "E".

However, for the Verilog-AMS language, the nature has to be a real number and thus, electric field can't be represented by single signal with nature Efield since it contains both amplitude and phase information or real and imaginary parts. Therefore, for each electric field signal, we need two signals with the nature Efield to represent it. Those two signals can depict either real and imaginary parts of the electric field or amplitude and phase information of the electric field. We don't have to choose only one way to represent the electric field as long as we have a block that can convert those two between each other.

Also, in my Verilog-AMS model, Efield in each block will only be in one direction and then, the optical signal flow in every block should be predetermined.

4.2 Continuous-Wave Laser Modeling

A continuous-wave (CW) laser steadily pumps out light. Since its light emission is based on single or multiple resonant modes, it can emit light which contains either single or multiple frequencies. As mentioned in the previous section, light can be defined by the one-dimensional electrical signal similar to voltage signal in electrical circuits. Therefore, the light source is functioning like a sine-shaped one-dimensional electric field, which can be described by the combination of amplitude and phase information. But unlike electrical signals, light source usually has extremely high frequency: the C-band wavelength, 1550nm, is equivalent to frequency approximately 193THz, which is much higher than the currently highest frequency 56GHz in electrical simulation as far as we know. As a result, the simulator that is designed for electrical circuit simulations is not suitable for simulations operating at such high frequency and thus, it will take a really long time to finish one transient simulation. However, as mentioned in the previous chapter, the bandwidth of the optical devices such

as microring resonator is much smaller than its frequency and its transmission curve is also periodic. Thus, we don't need to know all the information from DC to 193THz and only frequencies around oscillation frequency are important for the simulations.

In my Verilog-A model, we have first introduced a parameter named reference frequency, which is similar to the concept DC frequency used in electrical circuits and all of the frequencies can be expressed through the reference frequency and a frequency offset. As a result, all the paremeters used in optical devices will first be derived through the reference frequency/wavelength and then, the simulator will use both parameters calculated at reference frequency and the frequency offset to derive the results at any targeted frequency. In fact, the concepts mentioned above are not unfamiliar to circuit designers since what have we proposed is similar to ac analysis: parameters at reference frequency are similar to DC operating point and frequency offsets are similar to ac frequency of the ac stimulus. It is worth mentioning that both my simulation and ac analysis are linear since each frequency is independent of each other and there is not frequency mixing involved. Therefore, the offset frequency works like a parameter that can be swept in the simulation to derive the frequency response of optical devices.

However, unlike the light inside MZM only experiencing static response, the light source inside the microring modulator will first experience transient response and then settle into static response due to its feedback structure. Therefore, we have to run the transient simulation in order to characterize the performance of the microring modulator. As a result, frequency offset has to be implemented into the model of cw laser and has to work as a stimulus in transient simulation.

Since the light source can be represented by a one-dimensional electric field, the cw laser model can be expressed by the magnitude and phase of the electric field as follows:

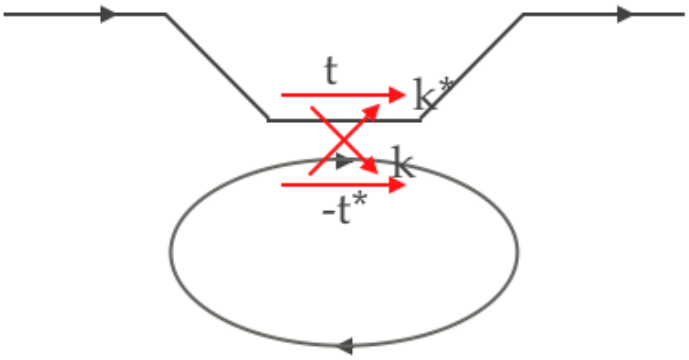

Figure 4.1: Further Simplified Point Coupler Model

$$E_{out} < 1 > \quad = \quad E_{amp} \tag{4.1}$$

$$E_{out} < 0 > \quad = \quad \int_0^t 2\pi\Delta f d\tau \tag{4.2}$$

The magnitude of the electric field will be supplied externally by a DC voltage source through defining a node with electrical as its discipline. Since the ground or the reference node in electrical discipline is always zero, we don't have to define the electrical ground in my Verilog-a modeling. However, in our user-defined optical discipline, we have to define an optical ground since the nature Efield is defined as potential. The phase of electric field is the time integration of angular frequency offset with its lower bound at t=0, which is implemented using a time integral operator. Also, π is a constant, which will be referred from a file defining all other constants used in my Verilog-a models.

4.3 Coupler Modeling

As discussed in the previous chapter, the point coupler model can be further simplified into Fig. 4.1 and accordingly, the transmission matrix X for the point coupler that is derived from this model can be shown in (4.3):

$$X = \begin{pmatrix} t & \kappa^* \\ \kappa & -t^* \end{pmatrix} \tag{4.3}$$

where t is the straight-through coupling coefficient and κ is the cross-coupling coefficient. Specifically in my Verilog-a model, both are field magnitude coefficient. And if we assume there is no loss for the point coupler, we have the following relationship between those two coupling coefficients:

$$|\kappa|^2 + |t|^2 = 1 \tag{4.4}$$

Therefore, the transmission matrix X can be further categorized into two matrices with the left one representing conjugate case and the right one representing non-conjugate case as shown in (4.5):

$$\begin{bmatrix} i\kappa & \sqrt{1-\kappa^2} \\ \sqrt{1-\kappa^2} & i\kappa \end{bmatrix} \quad or \quad \begin{bmatrix} -i\kappa & \sqrt{1-\kappa^2} \\ \sqrt{1-\kappa^2} & -i\kappa \end{bmatrix} \tag{4.5}$$

However, the elements in the matrix are complex numbers, which contain both real and imaginary part. Thus, we have to separate one matrix into the real part and the imaginary part of the matrix, which will also result in separating optical signals into both real and imaginary parts. Therefore, each of the two inputs and two outputs of the coupler will be represented by two signals, which are real and imaginary parts respectively. Accordingly, we will also treat each element inside the matrix X as two optical signals with real and imaginary parts. Since those elements are defined as optical disciplines, we also have to define an optical ground in order to assign them values.

Since the output signals of the matrix X is derived from the multiplication of input signals and the elements from matrix X is defined as an optical signal, we have to define a function for performing multiplication between two complex signals with both real and imaginary parts and then giving rise to another two complex signals with both real and imaginary parts. We have also defined a function to perform addition between two complex signals both with real and imaginary parts.

It is worth mentioning that the coupler model is one-dimensional where the optical signal is passing from left to right and the light inputs have to come from left, which means we have to define the optical signal transmission directions before we place my coupler model in a new model such as microring modulator model.

4.4 Photodiode Modeling

Photodiodes are the optical devices that are used to convert optical signals into electrical signals, specifically current. In the IMEC technology, the photodiode belongs to the class of silicon doped vertical PIN diode, where "I" is referred to as the intrinsic region. In fact, it is not surprising that IMEC technology has used PIN diode as its photodiode. PIN diode as a photodetector has a high quantum efficiency as high as 0.9 since the intrinsic region is usually thick enough to absorb all the incident radiations.

Since optical signals will be converted into electrical signals through photodiodes, the photodiode Verilog-a model can be expressed through its electrical models entirely, which is shown in Fig. 4.2. There is an external biasing voltage V, which is usually negative since the photodiode is working under reverse biasing condition. Except series resistance R_s and parallel capacitor C, all other electrical components can be expressed as follows [65]:

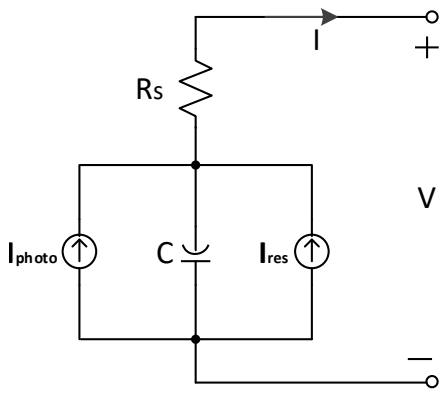

Figure 4.2: Photodiode Electrical Model

$$\begin{aligned} I_{photo} &= R_{spv}|E_{in}|^2 + \frac{V}{R_{dark}} \\ I_{res} &= I_s(e^{\frac{V}{V_t}} - 1) \\ I_{cap} &= \frac{d}{dt}(CV) \end{aligned} \tag{4.6}$$

Since we are modeling my photodiode based on IMEC technology, all of the parameters used will be derived from either the library handbook or photodiode Lumerical Interconnect model both provided by IMEC. The responsitivity of the photodiode R_{spv} is chosen as 0.91 Amps/Watt (A/W) according to the conservative estimation from the library handbook [66].

According to the Lumerical Interconnect simulation result, if we change the reverse biasing voltage of the photodiode without injecting light into the photodiode by setting $E_{in} = 0$, current "I" and its fitting result can be both shown in Fig. 4.3.

Since the current curve is exponential-shaped and the current is negative when the biasing voltage is zero, this current "I" includes two currents from the previous equations, I_{photo} and I_{res}. I_{cap} is not included because the current is derived through DC simulation. However, even if we use transient stimulus in the Lumerical Interconnect simulator, the current output of the photodiode did not show any capacitive effect and thus, we can't possibly derive either

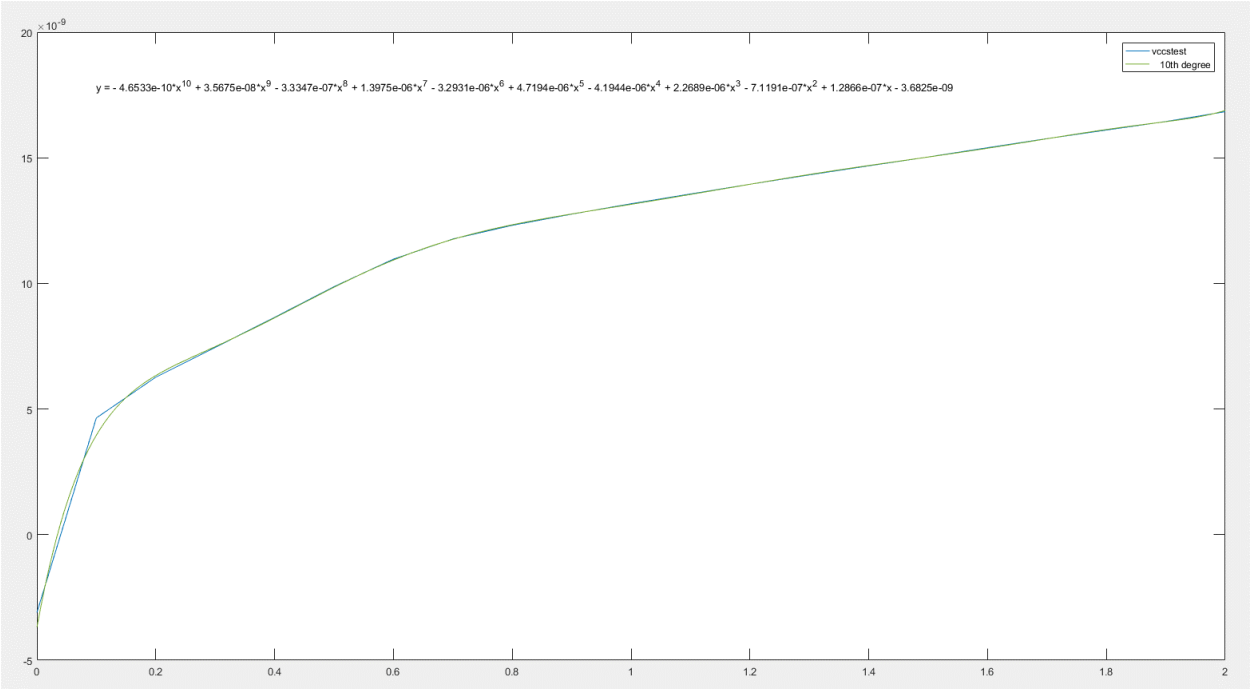

Figure 4.3: Photodiode Current I and its fitting results

series resistor R_s or capacitor C from Interconnect simulator. As a result, we have to refer to the library handbook once again, which shows conservatively that the bandwidth is 32.8GHz when the biasing voltage is set as -2V. If we set $I_{res} = 0$ and dark current as zero, the step response of the photodiode can be expressed as follows:

$$I(t) = u(t)(1 - e^{-\frac{t}{RC}}) \tag{4.7}$$

where the bandwidth is proportional to $\frac{1}{RC}$ and u(t) has the same unit as I(t). If we set R as 1000Ω, the resulting capacitor is $4.8523fF$.

As a result, the sum of I_{photo} and I_{res} can be expressed as follows:

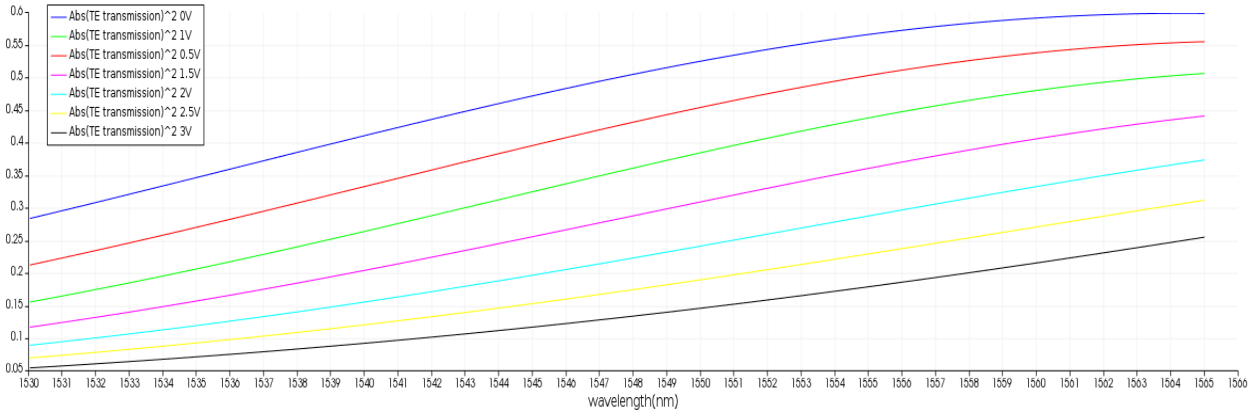

Figure 4.4: Electro-Absorption Modulator Lumerical Interconnect Simulation Result

$$
\begin{aligned}
I_{photo} + I_{res} = R_{sp} \times |E_{in}|^2 - 3.6825 \times 10^{-9} A + 1.2866 \times 10^{-7} A \times |V/R_0| \\
-7.1191 \times 10^{-7} A \times |V/R_0|^2 + 2.2689 \times 10^{-6} A \times |V/R_0|^3 - 4.1944 \times 10^{-6} A \times |V/R_0|^4 \\
+4.7194 \times 10^{-6} A \times |V/R_0|^5 - 3.2931 \times 10^{-6} A \times |V/R_0|^6 + 1.3975 \times 10^{-6} A \times |V/R_0|^7 \\
-3.3347 \times 10^{-7} A \times |V/R_0|^8 + 3.5675 \times 10^{-8} A \times |V/R_0|^9 - 4.6533 \times 10^{-8} A \times |V/R_0|^{10}
\end{aligned}
\tag{4.8}
$$

where $R_0 = 1\Omega$ and V has a unit of $\sqrt{Watt}$ or Volt.

The other current derived from resistor R_S and capacitor C can be included through the implementation of the Verilog-a model of R_s and C.

4.5 Electro-Absorption Modulator Modeling

Like other standard optical devices, IMEC has provided the Lumerical Interconnect model for electro-absorption modulator(EAM). Unlike other standard optical modulators, IMEC doesn't provide its electric model and thus, we can't reliably design its driver using the given information. However, we can implement its DC performance in my Verilog-a model. As shown in Fig. 4.4, the transmission curve of the electro-absorption modulator(EAM) is plotted in terms of wavelength and different biasing voltages. Since the EAM is used mostly around 1550nm wavelength, we will curve-fit the transmission intensity coefficient,$|T|^2$,in

terms of biasing voltage at the wavelength of 1550nm and its result is shown as follows:

$$\begin{aligned} |T|^2 = 0.72472 - 0.1062 \times |V/V_0| + 0.034636 \times |V/V_0|^2 - 0.1161 \times |V/V_0|^3 \\ +0.23035 \times |V/V_0|^4 - 0.2728 \times |V/V_0|^5 + 0.17919 \times |V/V_0|^6 - 0.065005 \times |V/V_0|^7 \\ +0.012433 \times |V/V_0|^8 - 0.0010395 \times |V/V_0|^9 \end{aligned} \quad (4.9)$$

where $V_0 = 1\sqrt{Watt}$ and V has a unit of $\sqrt{Watt}$ or Volt.

Both the input and output of the EAM use the discipline Efield and thus, we need to assign an optical ground to both of them. Also, both of them will be represented by two signals each: one for its real part and another for its imaginary part. Since the transmission intensity coefficients only have real part, both the real and imaginary part of the input will be multiplied by the same square root of transmission intensity coefficient.

4.6 Waveguide and Phase-Shifter Modeling

As mentioned in the previous chapter, according to the simulation result from FDE simulator, the light that is propagating inside a 3-D strip waveguide is mostly transversal electric (TE) mode. With the implementation of the effective index method (EIM), representation of the light inside the waveguide can be further simplified to a one-dimensional electric field as follows:

Although we can use Efield as the discipline to represent the equation above, we can't use the absolute wavelength since it would take too much time to perform transient simulation using Verilog-A model. Also, it is not necessary since only the simulation result within certain bandwidth is important. Besides, as discussed in the Verilog-A model for CW laser, each frequency will be expressed through the addition of reference frequency and frequency offset. In order to make both compatible with each other, the waveguide model is based on the following equation instead:

$$\tilde{E}_{shift}(L,t) = e^{-\alpha_A L} e^{-j\beta(\omega_R)L} \tilde{E}_{shift}(0, t - \frac{Ln_g}{c}) \tag{4.10}$$

$$E_y(x) = E_0 e^{-\gamma x} = E_0 e^{-\frac{2\pi\kappa x}{\lambda_0}} \tag{4.11}$$

where L is length of the phase-shifter and α_A is the attenuation coefficient with the unit of m^{-1}. $\beta(\omega_R)$ can be expressed as follows:

$$\beta(\omega_R) = \frac{2\pi f n_{eff0}}{c} = \frac{2\pi n_{eff0}}{\lambda} \tag{4.12}$$

n_{eff0} is the effective index at the reference frequency and λ is the reference wavelength. Thus, $\beta(\omega_R)$ is the spatial frequency at the reference frequency.

$\tilde{E}_{shift}(z,t)$ is the electric field whose DC frequency is shifted from 0Hz to reference frequency. As a result, the frequency component inside $\tilde{E}_{shift}(z,t)$ is intrinsically frequency offset instead of absolute frequency.

According to the segmented microring modulator layout, which will be discussed in the next chapter, the waveguide part of the microring is similar to its phase-shifter part but with some differences. Both waveguide and phase-shifter share the same waveguide core and waveguide cladding structure but with different doping profile. The doping profile of the phase-shifter used in IMEC technology can be seen in Fig. 4.5. Only cathode of the microring will be segmented and the waveguide won't include the doping layer N1, N2 and N+, which results in disappearing of the PN junction. Although it is not exactly the same, we have implemented the waveguide model through the phase-shifter model with zero biasing applied to its pn junction. Therefore, the waveguide model is similar to the phase-shifter

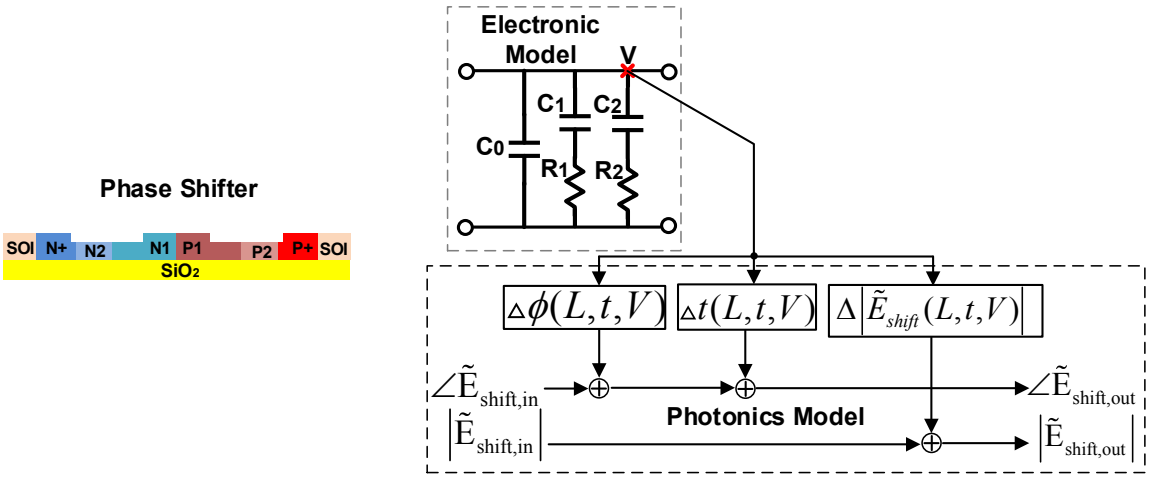

Figure 4.5: Electronics/Photonics Model of Phase-shifter

model as shown in Fig. 4.5 but has some differences. First, since there is zero bias applied, there is no electronic part in the waveguide model. Second, the photonics part of the model is also different: all voltage components "V" of the model will be set to zero.

After setting voltage components "V" to zero, the three parts of the photonics model as shown in Fig. 4.5 can be represented by equation (4.10). The first term is electric field magnitude attenuation after light passing through waveguide, which is shown as $\Delta \left|\tilde{E}_{shift}(L,t,0)\right|$. The magnitude attenuation is related with imaginary part of the effective index and the attenuation coefficient can be expressed as follows:

$$\alpha_A = \frac{2\pi f}{c} Im[n_{eff}] \tag{4.13}$$

The second term is the initial phase shifter related with real part of the effective index at reference frequency as seen in equation (4.12) and is represented as $\Delta\phi(L,t,0)$. The third term, represented as $\Delta t(L,t,0)$, is the time delay, which is related with the group index of the waveguide. Although both the second and the third term of the equation will introduce phase shift to the waveguide, they are not the same: the second term will also introduce

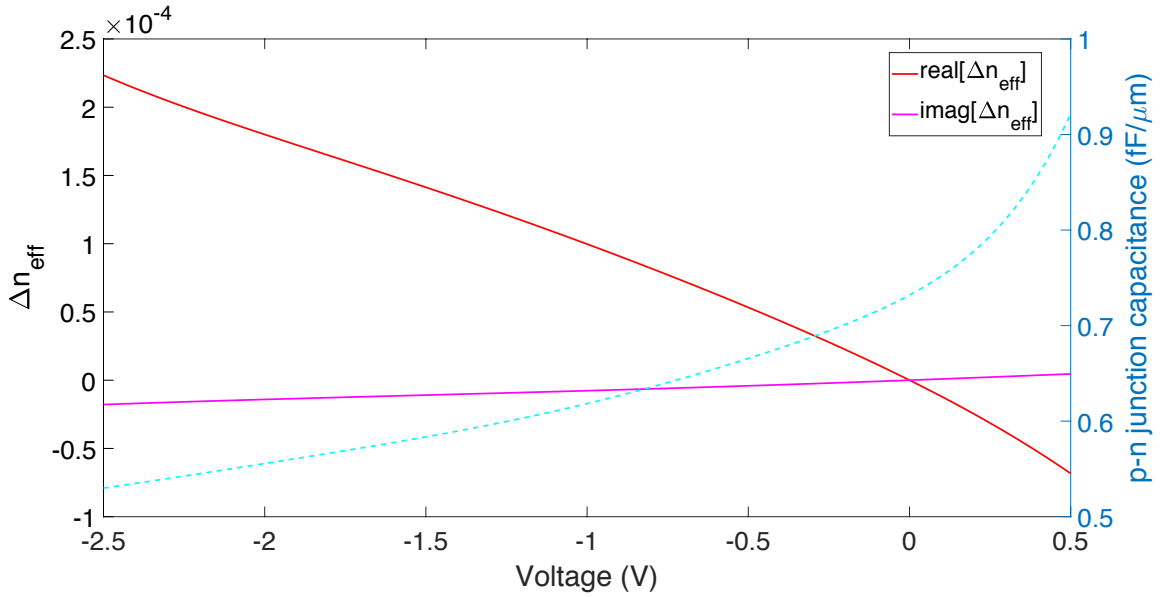

Figure 4.6: The change of Effective Index and Capacitance of Phase-Shifters with Respect to Biasing Voltage Based on IMEC Technology

the same phase-shift regardless of the input stimulus; the third term will introduce different phase shifts with different input frequency since phase output from laser is time integral of frequency offset although it always results in the same delay.

Although we can model waveguide and phase-shifter into two separate Verilog-A models, it is not necessary since waveguides are just phase-shifters under zero biasing conditions. As a result, we only need one model for phase-shifters, which can be seen in Fig. 4.5, and waveguide model can be derived by applying zero biasing voltage to phase-shifter model. In fact, since we have introduced several equations describing how the waveguide model is derived, we only need to discuss the difference between those two models.

Here is the first difference. Since the shifted electric field $\tilde{E}_{shift}(z,t)$ is biasing voltage dependent for phase-shifter, we need to find out which parameters in equation (4.10) will be voltage-dependent. First, group index n_g is mostly constant and is only depending on the reference frequency that it is based on. Second, since attenuation coefficient α_A and spatial frequency $\beta(\omega_R)$ are dependent on the imaginary and real part of the effective index respectively, both of them will be voltage-dependent. The dependency of real and imaginary

part of the effective index can be seen in Fig. 4.6. It is worth mentioning that the effective index referred here is based on reference frequency and if we change the reference frequency, we have to plot the dependency once again. On the other hand, how the frequency offset is reflected in the model comes from the delay term in equation (4.10).

The second difference comes from the electronic model. Since waveguides won't be driven by a dynamic voltage, there is no transient response in its electrical domain. The electrical model of the phase-shifter can also be seen in Fig. 4.5, where C_0 is the capacitance of metal pads, C_2/R_2 is substrate capacitance and resistance and C_1/R_1 is capacitance and resistance of the phase-shifter PN junction. Unlike other two capacitors, pn junction capacitor C_1 is voltage dependent and is also plotted in Fig. 4.6.

4.7 Microring Modulator Modeling

After implementation of the Verilog-A models for blocks such as CW laser, coupler and phase-shifter etc., the microring modulator can be modeled as shown in Fig. 4.7. Although microring modulator alone should only include two blocks, the coupler and the phase-shifter, we can't perform the transient simulation without the other two blocks. First, we need the CW laser to provide the input light source. The second block is placed at the output of the microring modulator, which is used to convert the light signals in cartesian coordinates into light signals in polar coordinates. Since the Verilog-A models for CW laser and phase-shifter are based on their physical meanings, both models have to use light signals in polar coordinates. On the other hand, the Verilog-A model for the coupler will be based on light signals in cartesian coordinates. In my model, we have chosen cartesian coordinates as the standard coordinates when Verilog-A blocks are communicating with each other and as a result, we have to implement the block for converting polar coordinates into cartesian coordinates inside the Verilog-A model for both the phase-shifter and laser source. However, light output of the microring modulator in cartesian coordinates makes less sense than that in polar coordinates since the latter represent magnitude and phase information of the electric

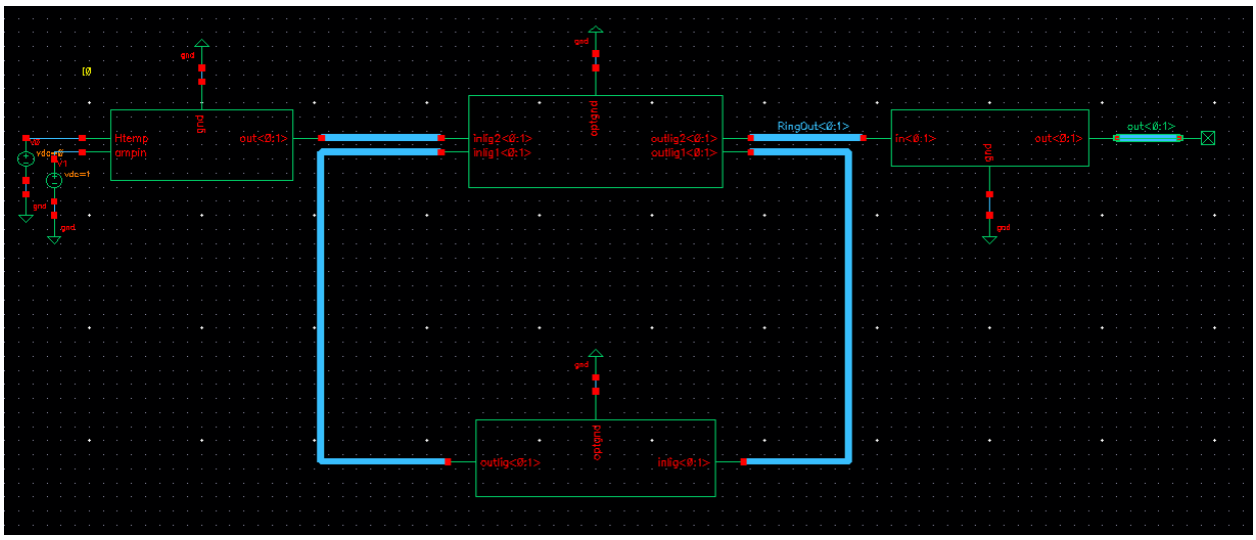

Figure 4.7: Microring Modulator Block Diagram in Cadence Virtuoso

field. Besides, the magnitude square for the light signal when the cw laser input has the power of 1W is the transmission intensity of the microring modulator. It is worth noting that model for the microring modulator is in one direction, where the light signal propagates from left to right. Also, the optical grounds of the microring modulator are all connected to the electrical ground.

After combining several blocks together to form the Verilog-A model for the microring modulator, we need to find out all the parameters used in each block of the model that are based on IMEC technology.

Although IMEC has provided parameters for the Verilog-A model based on testing results, they are not necessarily suitable for my model. Instead, we have made use of the Lumerical Interconnect model for the standard microring modulator provided by IMEC and compare its transmission result with the one from my model. Although we can export the transmission results from Lumerical Interconnect, it is easier to replicate the proposed model from Verilog-A model into equivalent Lumerical Interconnect model. As a matter of fact, Lumerical Interconnect has provided the blocks such as coupler, waveguide and phase-shifter, which will generate the same result as my proposed model. The microring modulator model used in Lumerical Interconnect can be seen in Fig. 4.8. Unlike the microring modulator model

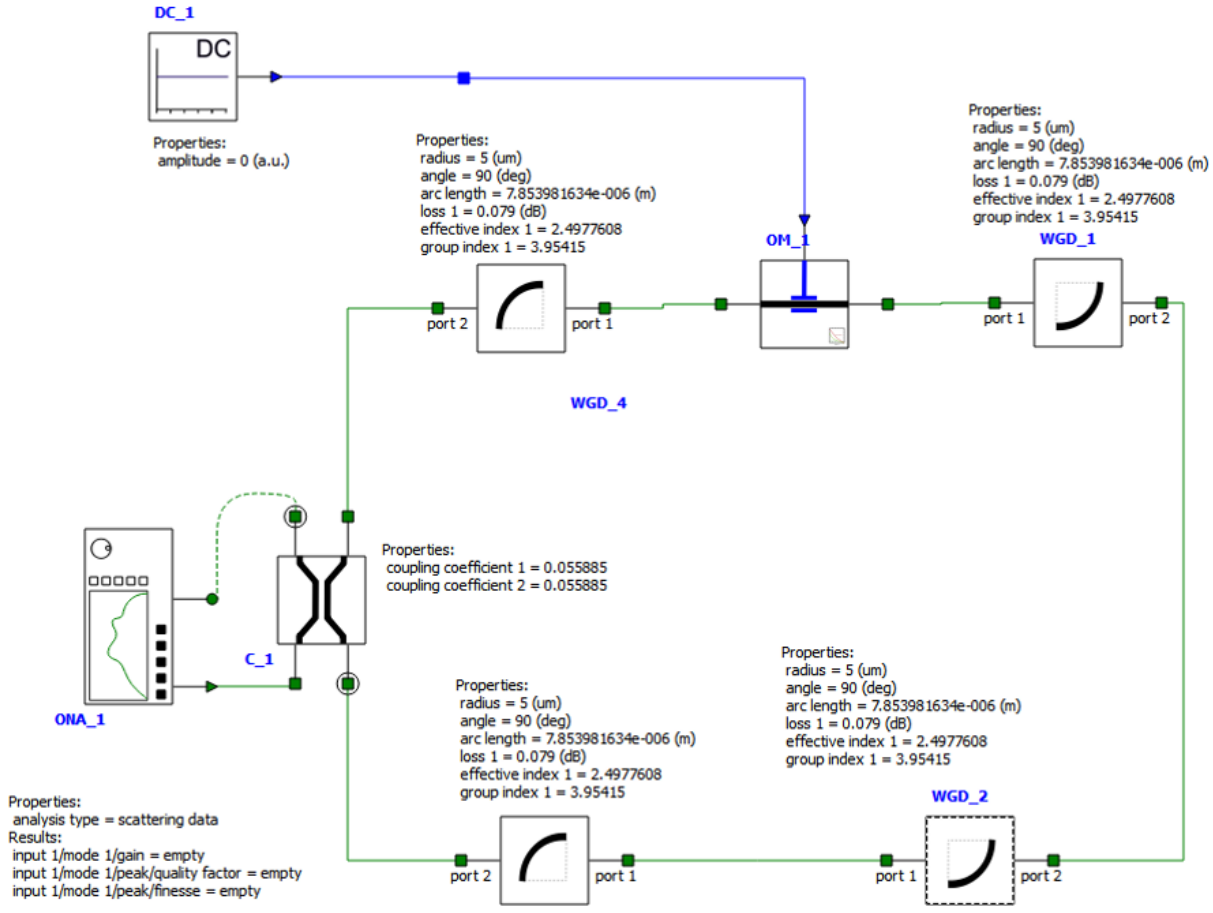

Figure 4.8: Microring Modulator Block Diagram in Lumerical Interconnect

used in Cadence, the models for phase-shifter and waveguide are separate and thus, we have broken up the waveguide into four parts. Also, since the waveguide model has the delay components, we have placed the phase-shifter model in between in order to reduce the skew in the final eye-diagram results, which comes purely from the modeling.

In order to derive the parameters used in my microring modulator Verilog-A model, which is based on IMEC-ePIXfab SiPhotonics ISIPP50G technology, we will implement the same microring modulator structure as the standard $5\mu m$ radius microring modulator provided by IMEC and compare the transmission results of both models. The microring modulator used in my model will be operating under the C-band so we have chosen 1550nm as my reference wavelength. Since there are several sets of parameters capable of resulting in the

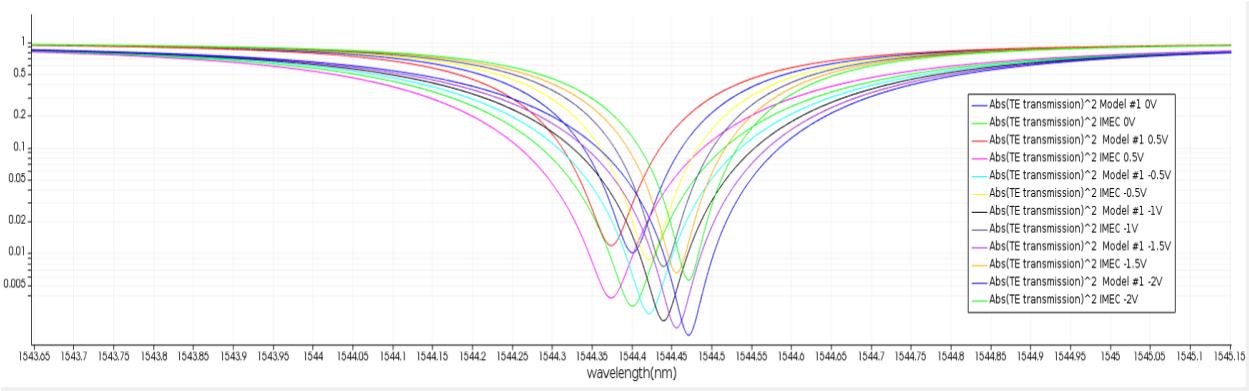

Figure 4.9: Lumerical Interconnect Simulation Results Comparison Between Standard IMEC Model and my Proposed Model

same transmission curve, we have chosen to use coupling loss provided by IMEC as the field amplitude coupling coefficient κ so that only one set of parameters will be derived later. Group index n_g can be derived through the matching of resulting free-spectrum range(FSR) between two models.

How the rest of the parameters are derived can be seen in Fig. 4.9. First, by matching oscillation frequencies, the real part of the effective index n_{eff} can be decided. If we sweep the biasing voltage to the phase-shifters, the effective index in terms of biasing voltage can be derived. In my model, we denote the real part of the effective index when biasing voltage is zero as the effective index at reference frequency and the difference between that and the real part of the effective index under different biasing conditions as $Re[\Delta n_{eff}]$, whose result can be seen in Fig. 4.6. Second, by matching bandwidths, the imaginary part of the effective index can be derived. The same method is used to decide $Im[\Delta n_{eff}]$, whose result is also shown in Fig. 4.6. Also, it is worth noting that due to the limitation of my proposed model, we can't match the insertion loss as well as the bandwidth.

Besides all the parameters used in optical models, the parameters used in electronic models are provided by the IMEC library handbook. However, they are provided as the values for the standard microring modulator and thus, we have to calculate their values in terms of unit length in order to implement them into a phase-shifter model, whose length can vary. Unlike other parameters that are voltage-independent, pn junction capacitor C_1 is

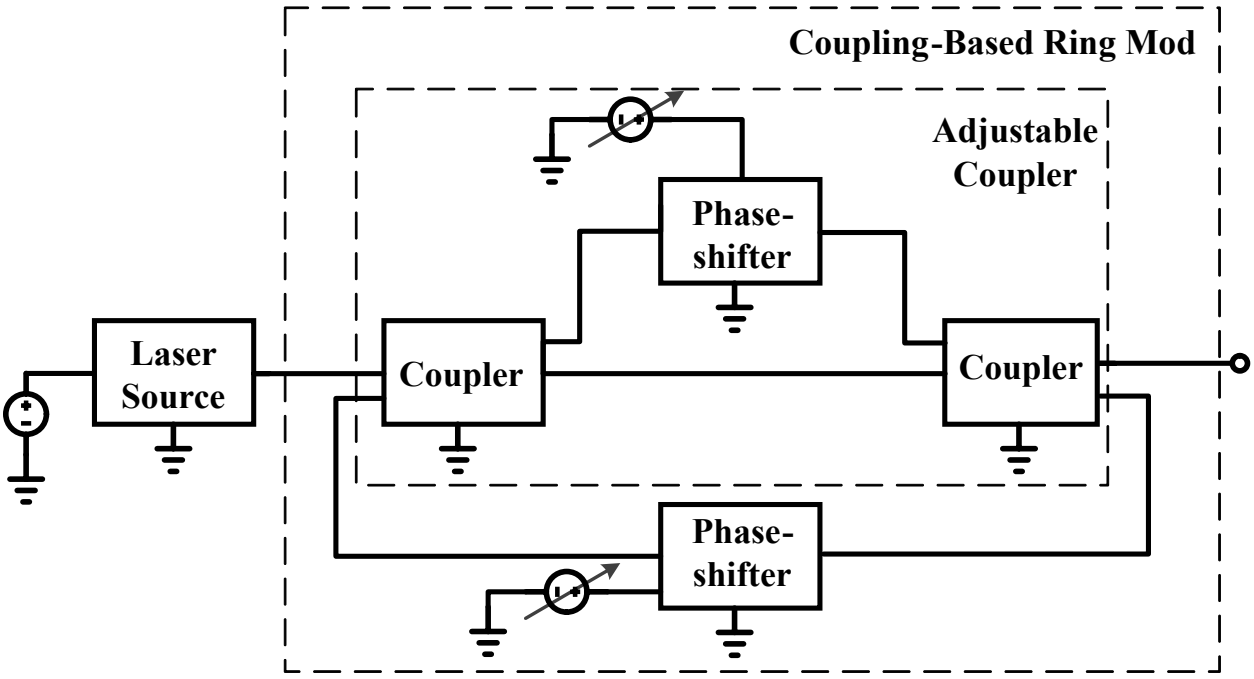

Figure 4.10: Coupling-Based Microring Modulator Block Diagrams

voltage-dependent and has to be modeled separately: its value under zero biasing condition is listed in the library handbook; its voltage-dependency is derived through IMEC technology, whose result is seen in Fig. 4.6.

4.8 Coupling-Based MRM Modeling and its Result

After finishing building the Verilog-A models for each optical block, we can also use them to develop new optical devices. In my case, a coupling-based microring modulator is proposed, whose Verilog-A model is shown in Fig. 4.10. Unlike a regular ring modulator which has constant coupling coefficient, a coupling-based ring has an adjustable coupler, whose coupling coefficient can be modified. The adjustable coupler is realized through two couplers and one phase-shifter between them. Although we can put one phase-shifter in each path between two couplers to boost extinction ratio of the microring modulator even further, the phase-shifter inside the microring path will be affecting the resonant waveguide of the whole structure. Besides, the extra phase-shifter inside the ring will also increase ring length

and result in lower quality factor, which will reduce the extinction ratio for the modulator instead of increasing it.

Instead of using another phase-shifter inside the adjustable coupler, my structure has chosen to replace the microring waveguide with a microring phase-shifter in order to further increase the extinction ratio. As a result, the total extinction ratio comes from both coupling coefficient change and oscillation frequency shift.

Due to different functionalities of these two phase-shifters, however, we can't use both of them for modulation. In my design, we use the phase-shifter inside the ring for modulation while using the one in the adjustable coupler for a brand new type of tuning: coupling coefficient tuning.

Because of fabrication imperfections, the coupling-coefficient of the ring modulator will vary and the extinction ratio will be affected. Therefore, the introduction of coupling-coefficient tuning in the ring modulator with minimum structure change is important in PIC design.

In my model, coupling-coefficient tuning is electrical tuning since the tuning comes from the phase shift. Also, the coupling coefficient affects the transmission result just like temperature variation influencing resonant wavelength, so coupling coefficient tuning like thermal tuning is working at much lower frequency than modulation frequency. With the new tuning scheme, my coupling-based ring modulator can be working near the critical coupling point, which will render the highest extinction ratio.

Here, we will discuss one example of using the Verilog-A model developed above to design a Coupling-Based Ring Modulator and the parameters used are derived from the microring modulator section.

First, we have chosen to set the reference frequency as 1550nm and then both the effective index and group index at this reference frequency along with voltage dependency of the effective index will be the same as the ones that we are using for the microring modulator. Second, we choose $6\mu m$ as the ring radius. Third, we replace the adjustable coupler with

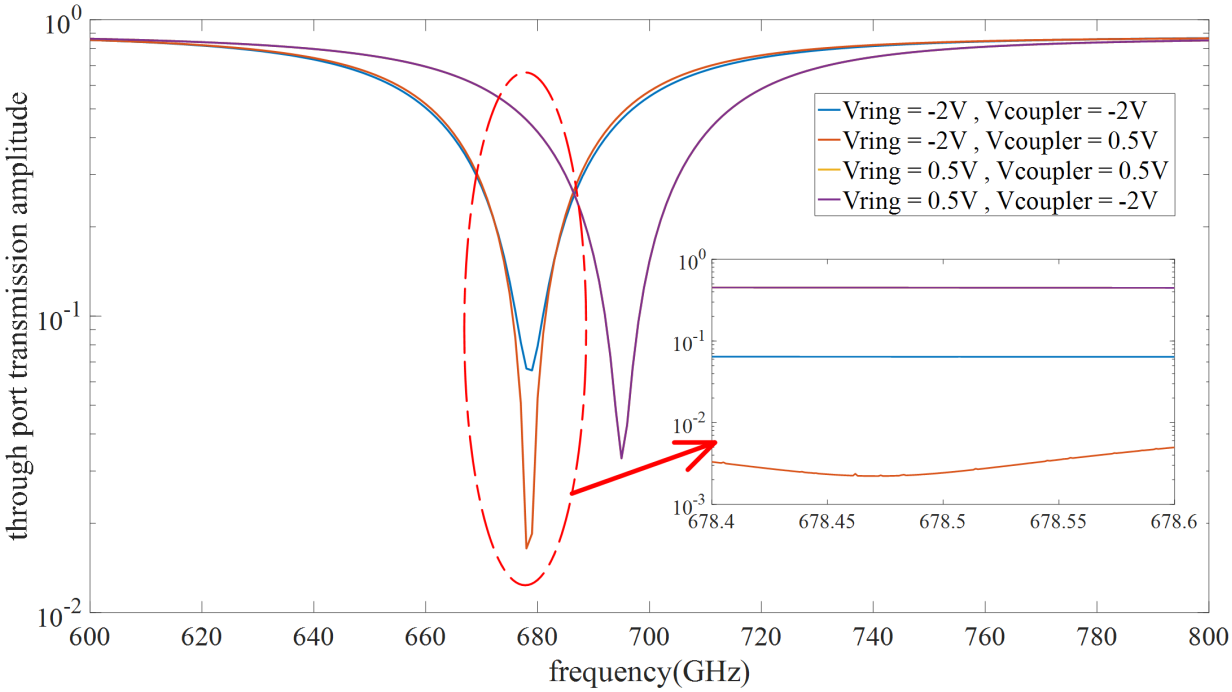

Figure 4.11: Transmission Result of Coupling-Based Microring Modulator

a single coupler and find a coupling coefficient that can result in the highest extinction ratio for the microring. Then, the frequency offset that corresponds to resonant wavelength of my ring modulator can be found, which is 679GHz in this example. Fourth, we match the coupling coefficient of the adjustable coupler to the one derived above by adjusting the coupling coefficient of the two couplers inside. As a result, κ for both couplers is 0.1927434. Finally, Since the IMEC microring modulator model is only precise when its phase-shifter is biased between -3V and 0.5V (from -3V to -10V, the data is derived through curve-fitting), we fix the frequency offset to be 679GHz, sweep the voltage applied to the phase-shifter in the adjustable coupler by this voltage range and also sweep its length at the same time to find the largest extinction ratio. As a result, the length that renders my coupling-based ring modulator the largest extinction ratio is 99.2μm.

The transmission result can be plotted as shown in Fig. 4.11. The main figure is the course frequency offset sweeping result from 600GHz to 800GHz with increments of 1GHz and the subset is the precise sweeping around oscillation frequency with frequency increment of

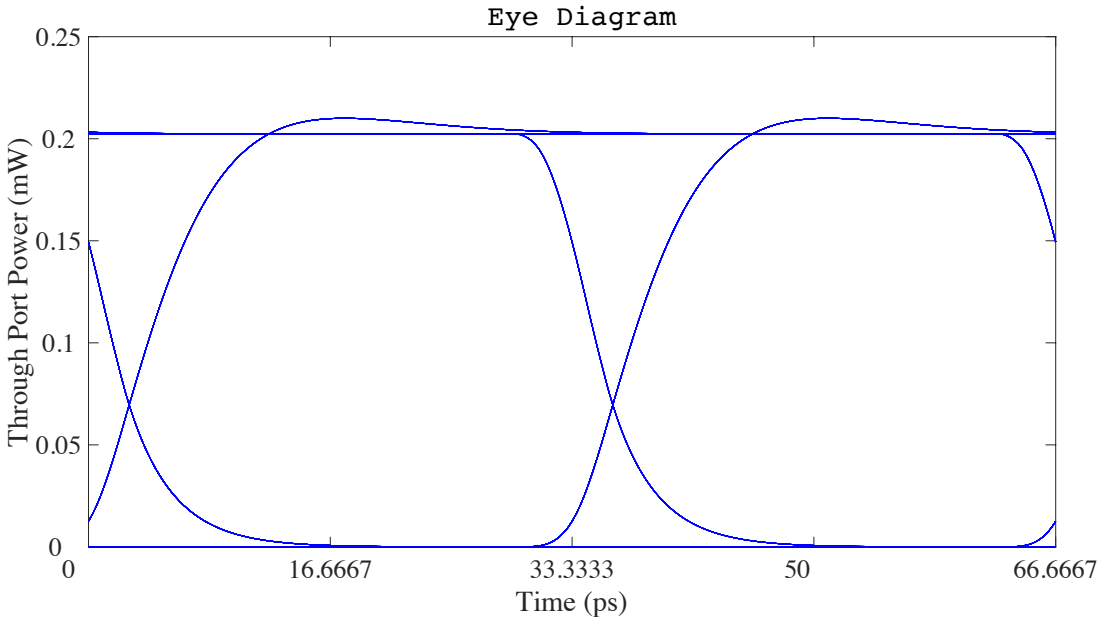

Figure 4.12: Eye Diagram of Coupling-Based MRM at the Data Rate of 30GS/s

0.2GHz. The y-axis is the magnitude of the through port transmission curve of the coupling-based ring plotted in log scale. The four curves correspond to two biasing voltages (-2V and 0.5V) applied to the phase-shifter inside the coupler. From the figure, we can see that the insertion loss has negligible difference for both voltages and 0.5V bias gives rise to the highest extinction ratio. Therefore, my proposed coupling-coefficient tuning scheme results in higher extinction ratio without introducing extra insertion loss.

In this coupling-based ring modulator design example, the precise oscillation frequency offset is at 678.47GHz. The extinction ratio results under different biasing conditions are concluded in table 4.1.

From the transmission result, we see that frequency offset 678.47GHz corresponds to resonant wavelength λ_0 and choosing bias voltage as 0.5V for the 99.2μm long phase-shifter inside the coupler will result in the highest extinction ratio. Only the phase-shifters in the microring will be biased by the dynamic PRBS signals while the one in the adjustable coupler is biased by the DC voltage 0.5V. In my transient simulation, if we apply 1mW to the laser source and set the data rate for PRBS voltage source to be 30GHz, the eye diagram of

the through port transmission power output can be plotted as shown in Fig. 4.12, whose extinction ratio is 46dB, the same as the one shown in table 4.1.

Table 4.1: Extinction Ratio Results for Different Conditions

Conditions	Coupling-Coefficient Tuning Only	Resonant Wavelength Shift Only	Applying Both Simultaneously
Extinction Ratio	16dB	29dB	46dB

Chapter 5: Silicon Photonics Chip: Layout and Testing

5.1 Optical Devices Layout

After finishing the modelings and simulations of the silicon photonics devices based on IMEC iSiPP50G technology, the next step is to implement those silicon photonics devices that we have proposed using my models in IMEC iSiPP50G technology so that we can measure the performance of those proposed structures under more realistic conditions. Therefore, in this chapter, we will discuss the layout of the photonics chip that we are going to fabricate and then, will describe our proposed testing setup and testing plans as well as prospective testing results.

There are a couple of differences between photonics layout and integrated circuit layout realization. First, one of the maturities on IC layout part is reflected by its abilities to parameterize almost every single component used in each technology both in schematic and layout (However, the maturity levels among analog/mixed-signal, power electronics and digital IC layout also differ). Photonics layout, at least from our experience with the commercially available IMEC technology, can't be changed from the standard cell without treating it as a completely different block, which makes the available experimental results of the standard cell limited in predicting its newly modified version. Second, the extraction simulation result of photonics layout is not possible to our knowledge. Third, although the components in photonics layout are hard to build up even when they are based on standard cells due to their lack of usable parameterized models, the global routing that is used to connect each component is much easier to implement than that of traditional integration circuit layout. Therefore, we need to figure out solutions to realize each optical component, whether derived from either a standard cell or a newly created structure built from scratch.

One of the most popular ways of realizing photonics components layout is through a software named IPKISS. By using Python script interface, IPKISS is able to create any user-defined photonics component layout. For example, Python code in IPKISS can be used for generating the GDSII file of a simple ring resonator as shown in Fig. 5.1.

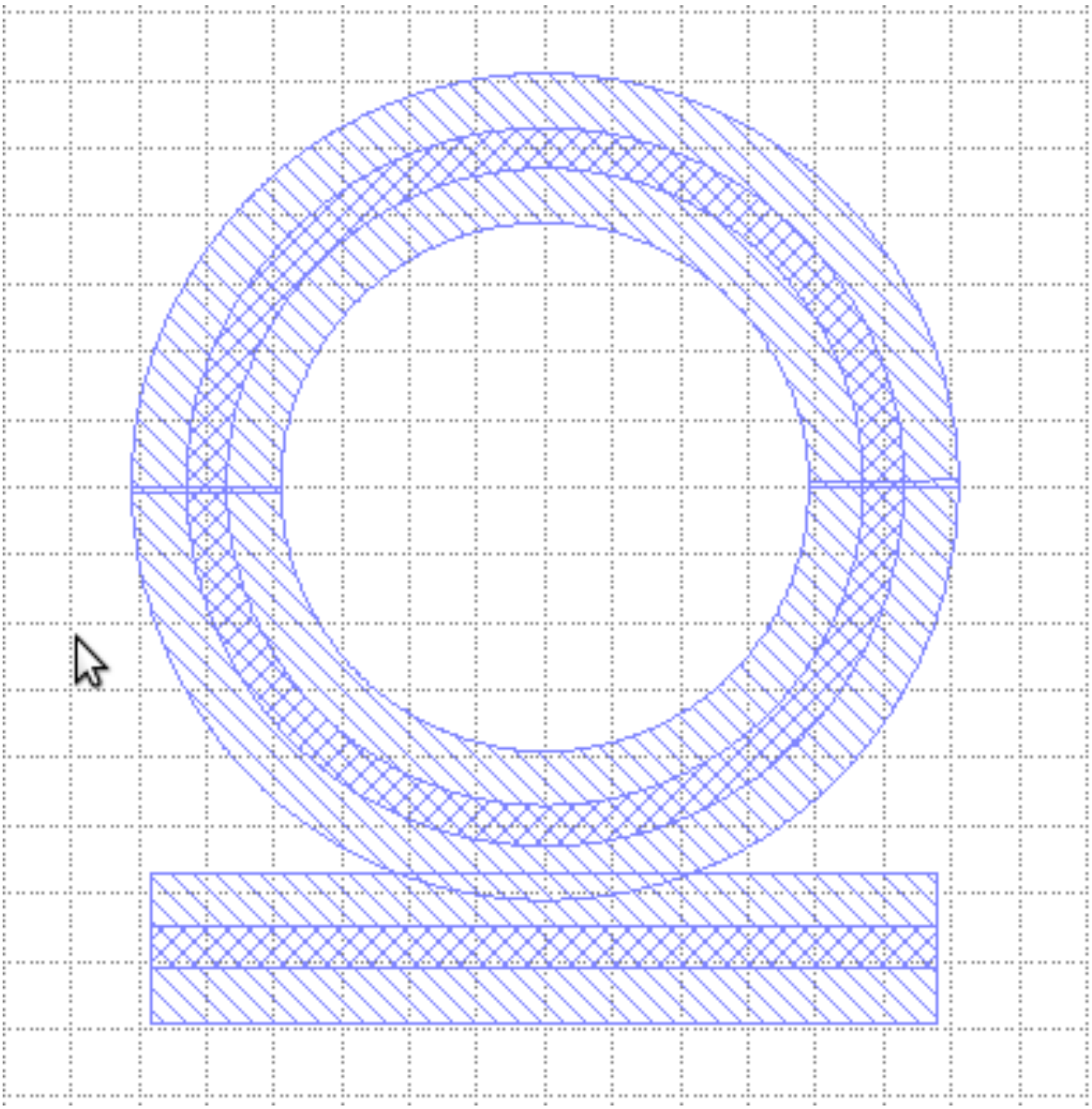

Figure 5.1: Simple Ring Resonator Created by IPKISS
[67]

However, there are several drawbacks for this method. First, since we have to build up the code from scratch, it is always dangerous to use this method if we did not have any previous experience with fabricating photonics chips. Therefore, we have to do a few trials and errors before we can comfortably test my proposed architectures. Also, it is very likely that we won't be able to include all the necessary layers since we don't have either DRC, LVS

or extraction simulation in my current photonics design tools to verify my new structure. Second, since the main target of my photonics chip is to test my proposed three-segment microring modulator, which is based on the standard microring modulator cell provided by IMEC, it is safer for my first photonic chip to modify the standard cell instead of creating a new one instead. Besides, it would help us to reduce the time for the process of fabricating photonics chips.

For drawing the layout of my proposed three-segment microring modulator, we have chosen another method in my design instead of using Python code: just use the tool Klayout. Generally, Klayout is used for creating layouts for transistors, resistors or other electrical components without referring to any specific technology. However, its function to create layout is limited since it is based mostly on polygons, which are hard to use for creating different structures without using programming. Besides, the tools such as Virtuoso Layout Suite and Pyxis have many more functionalities and are more suitable for producing complicated integrated circuit layouts. Since photonics layout will have many more circular shapes than integrated circuit layout, Klayout will be much more ill-equipped in this application. However, the above limitation for Klayout is based on its application for creating a brand new electrical and optical layout from scratch.

In my design specifically, the above limitations of Klayout don't affect my design for the three-segment microring modulator. First, my proposed three-segment microring modulator is based on the standard $5\mu m$ radius microring modulator provided by IMEC, whose layout is readily available to view and edit in Klayout. Second, there are only a few differences between the standard microring modulator and my proposed three-segment microring modulator and those differences can be easily realized using Klayout, which will be discussed later. On the other hand, using Klayout will not only bring the benefit of speeding up the process of building my proposed microring modulator but also can generate a new structure with minimum changes from the standard cell, which can minimize the risk of building a completely new optical structure. As a result, we have chosen Klayout to generate my

proposed three-segment microring modulator.

In order to understand how do we derive my proposed three-segment microring modulator, let's first take a look at the standard microring modulator layout provided by IMEC as shown in Fig. 5.2. There should be two major differences between this standard microring modulator and my three-segment microring modulator.

First, since drivers in my design are driving the cathodes of the microring modulator while its anode is connected to the ground, we need to dissect the cathode of the standard microring modulator while keeping its anode intact. According to the layer information of IMEC technology, we need to dissect the following layers: NBODY for N-type body implant, N2 for N-type doping engineered for ring modulator, SAL for local silicide, NPLUS for N-type contact implant and M1_DRW for implementing metal one of copper damascene. Also, PCON for Tungsten Contact Plugs has to be modified since it is providing the connections to N-type doping layers. On the other hand, the layers for implementing ring waveguide and other optical parts won't be changed at all. Since the three segments in my design has a specific length ratio, we have to dissect the aforementioned layer accordingly. However, not all of those layers that need to be dissected are equally important. The N2 layer, which has the most doping, directly decides the characteristics of the phase-shifter and thus, has to be dissected as close to proposed length ratio as possible. Also, other layers that need to be dissected have to be closely matching the N2 layer. Due to the margin of error even in the layout fabrication phase, we might not be able to generate the phase-shifters with exact length ratio and thus, performing simulations with length variations for three phase-shifters have to be done in order to verify the adaptability of my proposed scheme and transmitter structure.

Second, the standard cell only has one cathode and one anode while in my design, there are three cathodes and one anode. Therefore, we need to add at least two more pads for the cathodes.

After understanding the aforementioned two differences, we have built my proposed three-

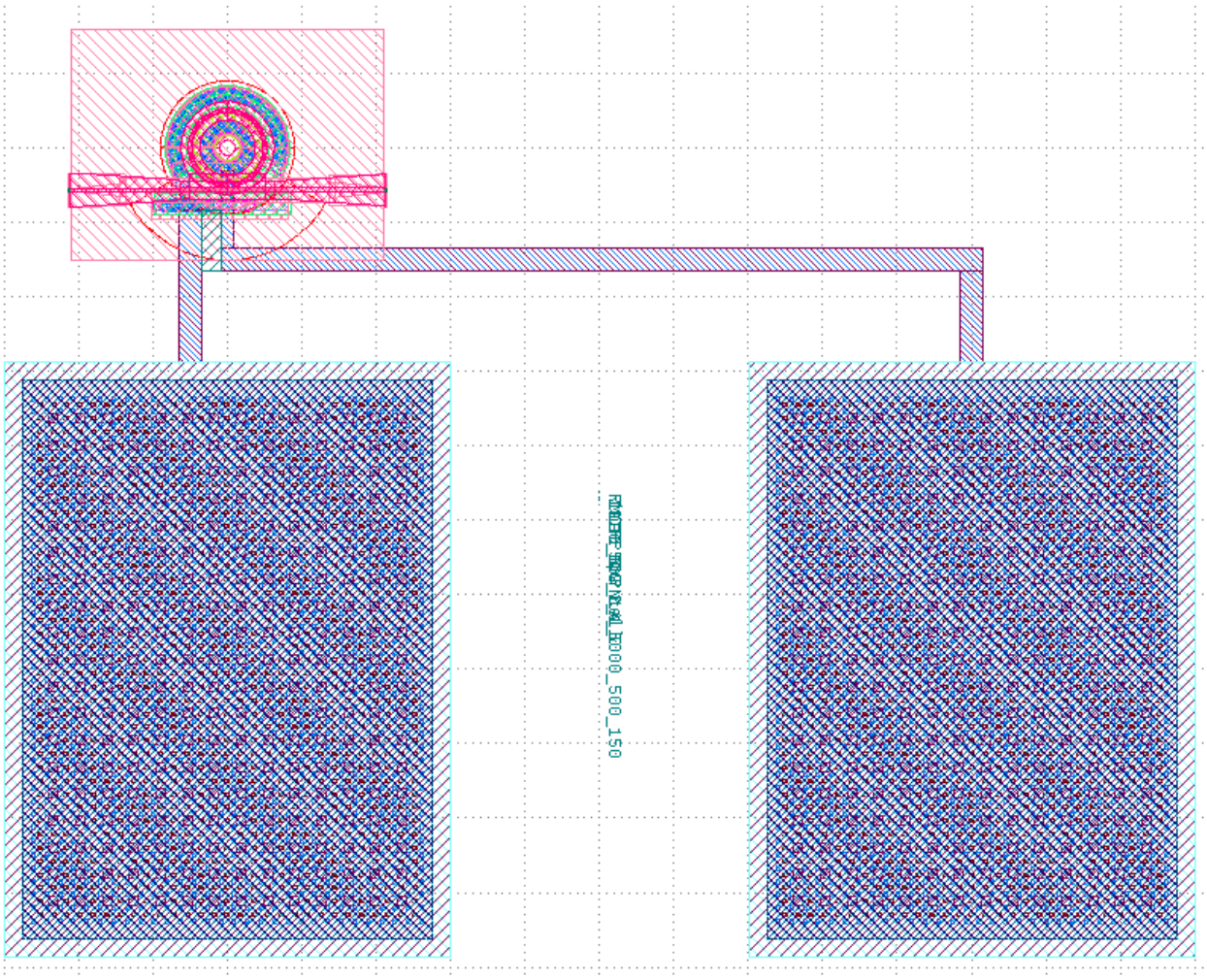

Figure 5.2: Standard Microring Modulator Cell from IMEC Technology

segment microring modulator using Klayout and its final layout is shown in Fig. 5.3. In fact, we have added three more pads compared to the standard microring modulator from IMEC technology: one for ground and two for two segments of the microring modulator. Although we don't have to add another ground pad functionally, adding an extra ground pad as well as putting it outside the three pads for connecting the three cathodes can create ground/signal/ground (GSG) routing, which can both create a balanced microring modulator layout structure and provide better return paths for the ground signals. Besides, the GSG routing is commonly used in photonics layout design such as Mach-Zehnder modulator (MZM).

If we zoom in to the microring waveguide part alone, my proposed three-segment microring modulator can be shown as Fig. 5.4. We have built two different three-segment

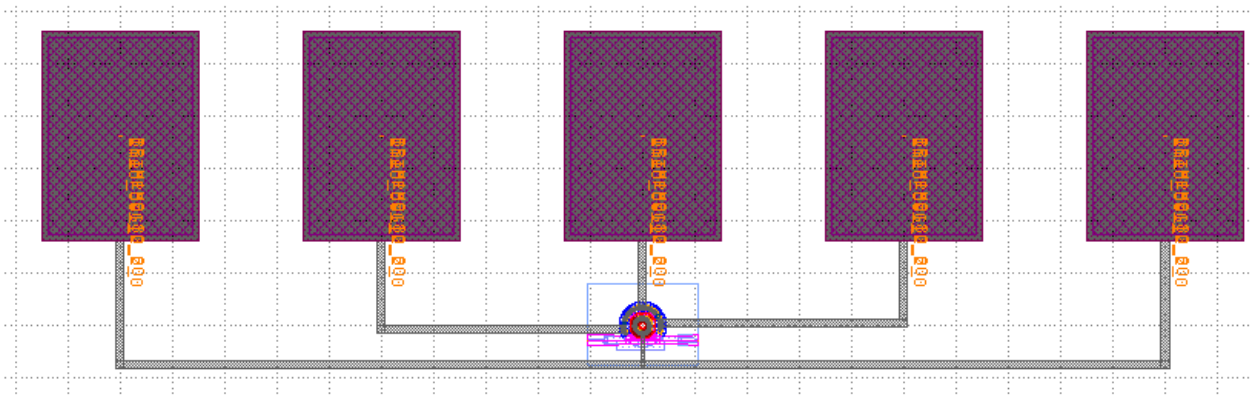

Figure 5.3: Proposed Three-segment Microring Modulator Built using Klayout

microring modulators using Klayout. Although both layouts have the same length ratio of 1:2:4 and are based on the standard 5-μm radius microring modulator provided by IMEC-ePIXfab SiPhotonics ISIPP50G technology, the one on the right (we call it first version) has the central angle of 30° : 60° : 120° and the one on the left (we call it second version) has the central angle of 45° : 90° : 180°. The first version has the longest achievable phase-shifter lengths without violating the design rules for photonic chips using IMEC-ePIXfab SiPhotonics ISIPP50G technology. Thus, this version will result in the highest extinction ratio among all the possible implementations of the three-segment microring modulator. The second version has shorter phase-shifter length and thus has lower extinction ratio. Although it has sacrificed the extinction ratio, the second version has avoided putting n-type doping onto the coupling region between ring and straight waveguide so that the electrical signals won't affect the coupling coefficient of the microring. At the same time, the extra space from the gap can be used for implementing thermal tuner in the future work. By building two different three-segment microring modulators, we have better chance of successfully overcoming the process fabrication imperfection in my layout and it may also help us to understand IMEC technology better.

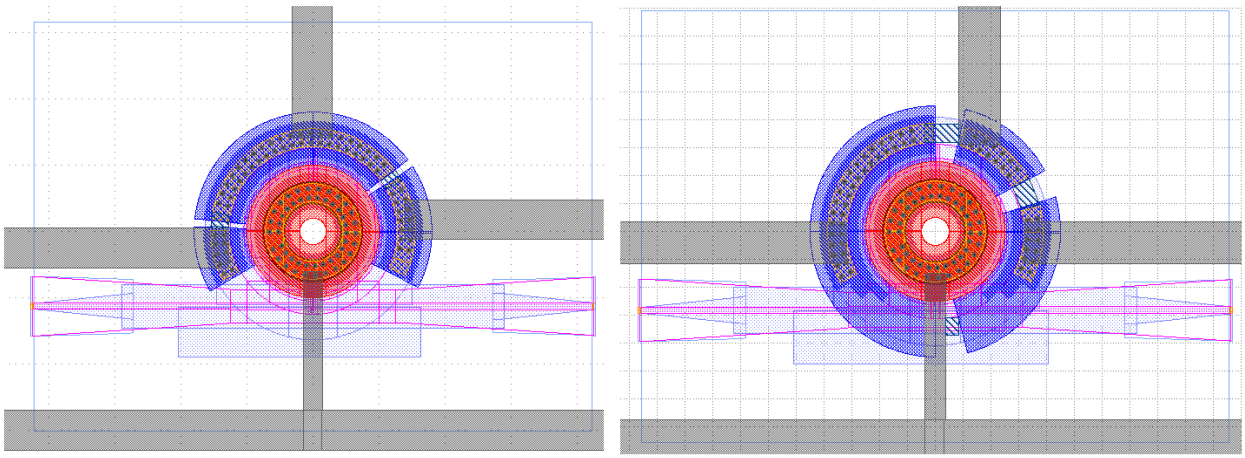

Figure 5.4: A Closer Look at Microring Part of my Proposed Three-Segment Microring Modulator Layout from IMEC Technology

5.2 Global Routing

As mentioned in the previous section, using Klayout to generate photonics circuits is limited except in a few special cases such as generating layout for my proposed three-segment microring modulators. Thus, it would be more difficult to use Klayout to realize connection between optical devices even in my photonics chip which only contains limited number of optical devices. On the other hand, it is possible to use IPKISS to realize the connections between each photonics device since it is based on Python coding. However, there are three problems with this approach. First, implementing global routing with Python code will further complicate the code for photonics devices. Second, in integrated circuit design, global routing is done with the tool Virtuoso and there is no coding involved. Thus, it would be less intuitive for IC designers like us to use coding alone to draw all the layouts. Third, just like in integrated circuit layout design, the routing that is used to connect each device is generally much more complicated and is also prone to change due to the planning for global layout floorplan. Therefore, using coding to implement the global routing will be much less flexible and every change in the global routing will take much longer time to implement compared to the way it is used in state-of-the-art integrated circuit design.

After the discussion above, we have realized that the global routing should not be gener-

ated by using Python code due to several reasons and we need to find a way which is similar to the global layout implementation used in current integrated circuit design. Although in my transmitter layout generation, we have used a schematic driven layout (SDL) tool named Cadence Virtuoso, Virtuoso doesn't provide the functionality to generate optical waveguides. On the other hand, there is another SDL tool called Pyxis Custom IC Design Platform provided by Mentor Graphics, which is mostly used for creating layout and performing layout extraction. Although Pyxis won't be able to compete with Cadence Virtuoso in terms of circuit simulation, my photonics design doesn't need this function at all since all of the photonics circuit simulations will be performed using Cadence Virtuoso instead. However, Pyxis Layout has one advantage that is essential to my photonics layout: there is a generic silicon photonics (GSiP) PDK developed by the University of British Columbia (UBC), which can be implemented in Pyxis Layout for generating the layouts of waveguides [68]. The generic silicon photonics PDK is not related with any technology and can be modified to generate layouts of waveguides that are based on any technology. There are two files that need to be modified according to specific technology: create_GSiP.dofile is used for defining process parameters and all the process layers used in targeted technology as well as their representing colors and patterns in the layout view. It is worth mentioning that process parameters are crucial for later performing design rule check; GSiP_oa_layermap_file defines each layer used in the technology by its layer purpose, layer stream number and datatype stream number.

GSiP provides several functions such as schematic capture, circuit simulation, schematic-driven layout, tilting and electronics/photonics co-design. But in my specific application, we will use these two features: design rule check (DRC) and waveguide routing. Design rule check (DRC) and its application in Pyxis Layout is straightforward since Calibre is known for its layout verification tools. Also, we do not have to create design rule files just like we did with layer defining files mentioned above since it is provided by IMEC technology. Therefore, we don't need to introduce DRC in detail here since it is almost exactly the same as DRC used in integrated circuit design.

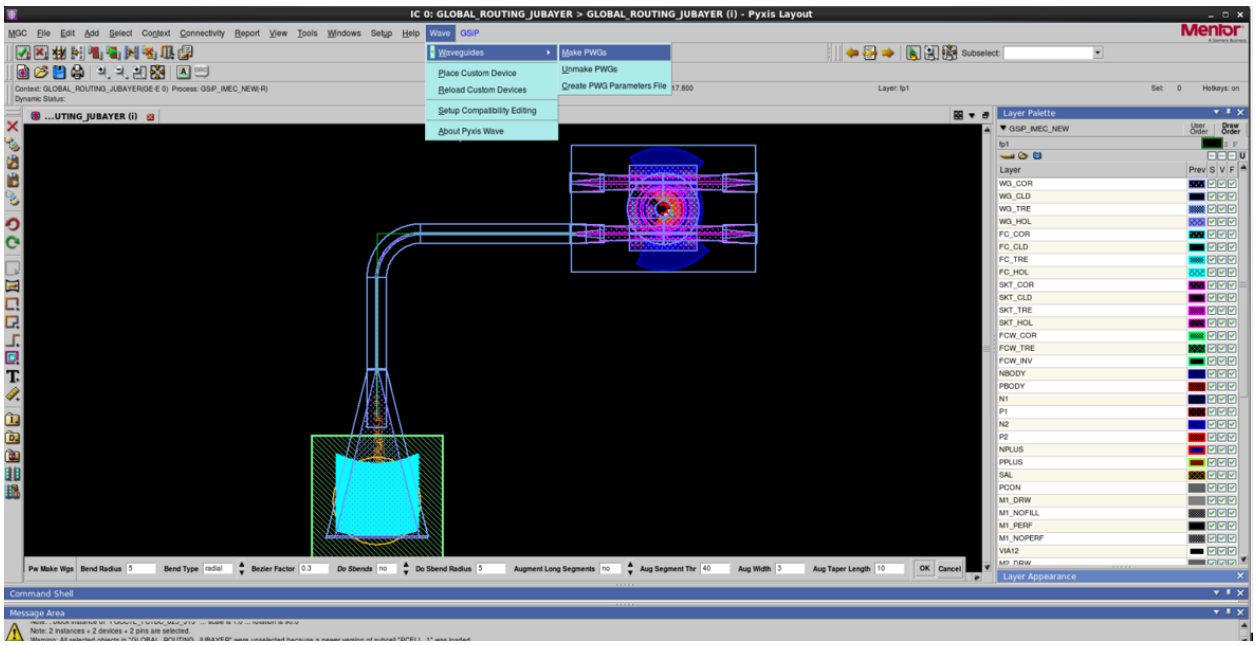

Figure 5.5: Waveguide Routing in Pyxis Layout

On the other hand, the second feature, waveguide routing, has to be discussed in the thesis since it is not implemented in integrated circuit layout generation and is the main attraction for using GSiP PDK. The waveguide routing feature is able to be implemented in Pyxis layout because the file folder pyxwave is included. Let's take a look at one example for performing waveguide routing as shown in Fig. 5.5. On the right, we can see the layer palette, which includes all the layers defined in file create_GSiP.dofile. There are two new drop-down menus, Wave and GSiP, which are not included in the generic Pyxis layout menu. The first new menu, Wave, is used to generate waveguide by clicking on Make PWGs. Just like generating paths in integrated circuit layout, waveguides can be generated by first clicking on the layer used in waveguides from the layer palette, then clicking on the starting point and finally clicking on the final point to finish the routing. In between, if we need to make turns, we can click on the turning point and drag again towards the next turning point or final point of the waveguide. Since an optical waveguide has to have smooth turning points, the waveguide generator provided by GSiP includes the parameter setting for bend radius, bend type etc. The way to change the width of waveguide is the same as that used in integrated

circuit layout. Also, the ruler function can also assist alignment between waveguides and other photonics devices. Finally, it is worth mentioning that all of the individual photonics devices will be put in the same directory and we will use them just like integrated circuit layout blocks by inserting their layouts into my global layout.

5.3 Chip Floorplan Analysis

After understanding how to generate both photonics device layout and global routing, we have generated a photonic chip using IMEC technology as shown in Fig. 5.6. Unlike integrated circuit layout, photonics circuit layout is usually not generated for realizing a single function but has implemented several photonics devices in order to realize or test different functionalities. The same can be said about my generated photonics layout. That's why we have segmented the whole chip into four different parts and thus, each segment will be explained in terms of its functionality and design details.

Before we start to talk about each segment, let's look at some design key points for the global floorplan. First, when designing for a multi-project wafer(MPW), we have to choose a template provided by IMEC, which is able to fit all of my proposed layouts. Since larger template size will cost more and my layout is generated to test the microring modulator, We have chosen the smallest template available with block size of $2500\mu m$ by $2500\mu m$. The template includes the following layers: TRENCH layer is the drawing layer for representing deep trench; WG_CLD layer is the waveguide cladding drawing layer; DOC layer is the documentation layer to show other documentation information; PAYLOAD_DRW layer is the marking layer for showing outline of my designed block; EXPO layer is the drawing layer for presenting back end of the line (BEOL) etch for waveguide exposure. In the template, the most noticable part is the rectangular block on the left, which is the trench layer and is used to define the deep etch. Also, edge couplers can be created through the trench layer. Second, unlike external signal supplies for integrated circuits that are coming from either bondwires or solder bumps, external signal supplies for photonics circuits, mostly light source

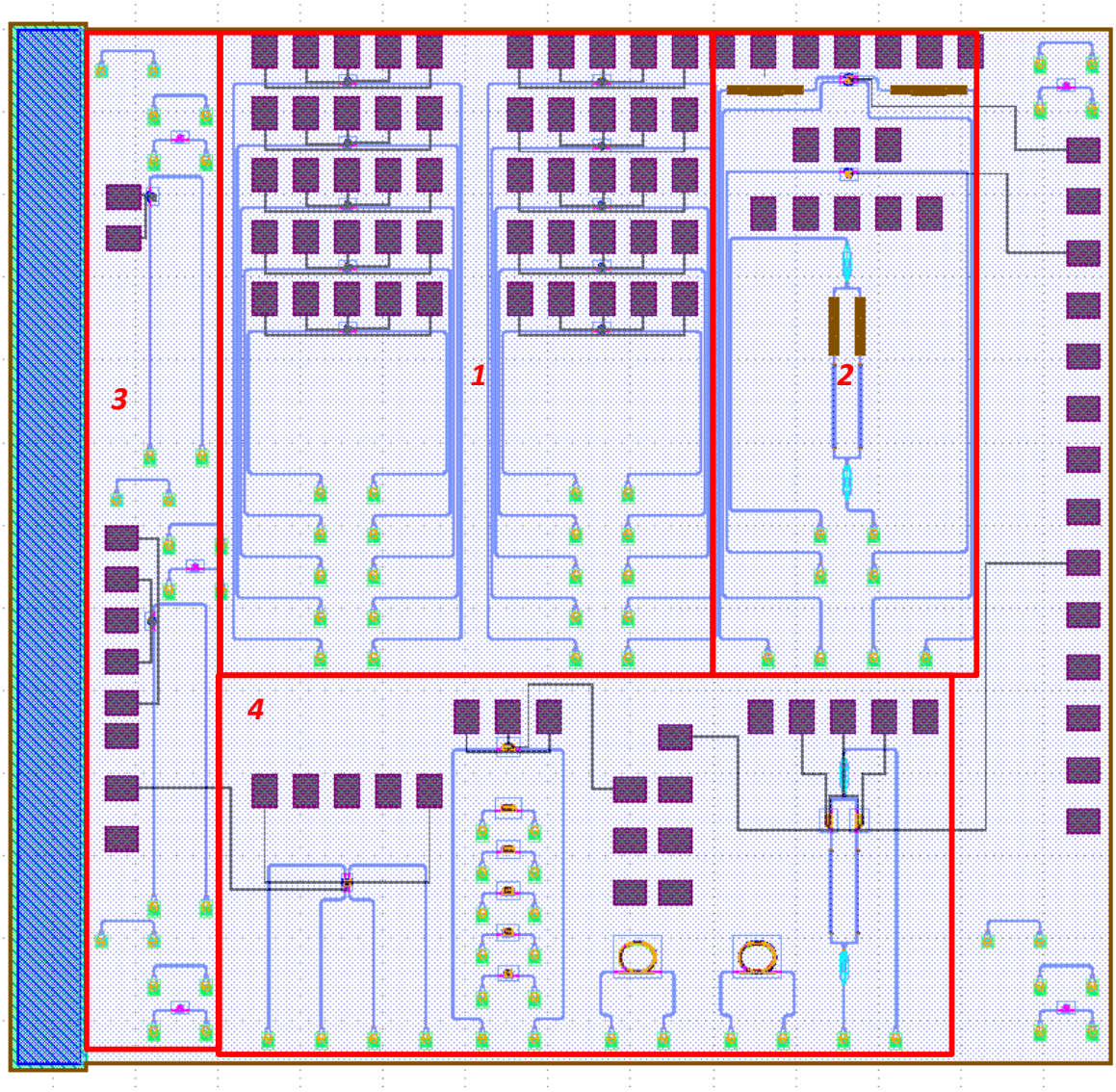

Figure 5.6: Photonic Chip Layout

from the continuous-wave laser, has to be provided through fiber array. In order to bring the light from the fiber array into the photonics chip and pass the light from the photonics chip into the fiber array, grating couplers are implemented in state-of-the-art photonics chip design. In my photonics layout, there are lots of different photonics devices: some of them are different photonics devices for realizing different functionalities while some of them are the same photonics device but with different parameters for testing purposes. For each

photonics device,a pair of grating couplers—one for bringing in light and one for passing light into fiber array—are needed. Since it takes a long time to align the fiber array with grating couplers, we have decided to align all of the grating couplers from different photonics devices together so that we only need to align once for each testing. In order to ensure that fabrication imperfection won't affect the alignment, we have placed four pairs of grating couplers on four corners of the chip for alignment purposes instead of choosing the grating couplers of either photonics devices on the chip. In fact, only three pairs of grating couplers on three corners of the photonics chip will be enough for alignment.

The first segment of the photonics layout includes two versions of my proposed three-segment microring modulator: the five on the left have the central angle of $30° : 60° : 120°$ and the five on the right have the central angle of $45° : 90° : 180°$. Among those five microring modulators, the pitch between the microring and straight waveguide is different so that the coupling coefficients of those five microring modulators are also different. The pitches of those five microring modulators are $150nm$, $180nm$, $200nm$, $250nm$, $300nm$ respectively and $150nm$ is the pitch used in the standard microring modulator provided by IMEC. By implementing different pitches, we can have better chance of finding the right coupling coefficient so as to generate the high extinction ratio possible even under fabrication imperfection. In real life, the fiber array has its own size and thus, if the grating couplers are placed too close to bondpads of the microring modulator, we might not be able to successfully probe the bondpads or the bondwires will become too close to the fiber array so as to introduce non-negligible interference. As a result, the closest distance between grating couplers and bondpads in my design is $450\mu m$. Also, the five pairs of grating couplers are placed together for two reasons: first, electrical signals and optical signals are separated so that they are not interfering with each other; second, it is easier to move fiber array when grating couplers are close to each other.

The second segment includes a single-bus microring modulator, double-bus microring modulator and electro-absorption-modulator-assisted Mach-Zehnder interferometer. The

double-bus microring modulator is generated using Python coding and its cathode is not segmented. Also, there is a heater inside to characterize the temperature effect for the microring modulator in the IMEC technology. Two standard phase-shifters are also included in the structure to provide more ways to compensate for the fabrication imperfections. Since there are four ports in the double-bus microring modulator, it will need four grating couplers and all four of them will be aligned on one horizontal line. The single-bus microring modulator has the same doping and segment scheme as those of the double-bus microring modulator including a heater but there are no extra phase-shifters included. Although both double-bus and single-bus microring modulators have one cathode and one anode, we have added one extra dummy pad on the left side of the cathode bondpad to form the pattern Ground/Signal/Ground(GSG). The electro-absorption-modulator-assisted Mach-Zehnder interferometer (MZI) is based on the structure of MZI but on each path, the phase-shifting is performed using an electro-absorption modulator. Also, a thermo-optic phase shifter will be added to each path to provide another source of phase-shifting in order to compensate for the fabrication imperfection. Due to the balanced structure between two electro-absorption modulators, their bondpads will also be placed together with their common ground attached to the single ground pad in the middle, which has resulted in five bondpads placed together with the same distance between them. Since the two thermo-optic phase shifters are separated from two EAMs, their bondpads will also be placed separately and are located on the right side of the chip instead. As you can see from the layout, the bondpads and grating couplers are also separated to avoid interference for testing convenience.

The third segment includes a standard microring modulator and a two-segment microring modulator. The inclusion of the standard microring modulator helps us to compare the experimental data provided by IMEC with my experimental result so that my Verilog-A model can be verified. The two-segment microring modulator is the optical structure used in one of my references and we can compare its result to those from my proposed three-segment microring modulator in order to find out the pros and cons between two structures. Since

we are going to compare the two-segment microring modulator and three-segment microring modulator, the two-segment microring modulator will be generated in Klayout instead of using Python code.

The fourth segment includes the other testing structures: an optical circulator with a heater inside, a race-track ring modulator with a heater inside, seven race-track ring resonators with two different sizes and a ring-assisted Mach-Zehnder interferometer(RAMZI) with the same structure as that of the aforementioned electro-absorption-modulator-assisted Mach-Zehnder interferometer (MZI). Also, it is worth mentioning that since the signals that are controling the heaters are DC signals, their pads can be placed far away from the photonics devices without negatively affecting their performances, which can save spaces for those pads passing high-speed signals. All of those structures above are generated using Python codes. Although their implementations are riskier than those generated using Klayout, it is the first step towards building up a user specific photonics device library.

5.4 Testing Setups for the Three-Segment MRMs and Prospective Testing Results

Among the four segments on the photonics chip, only the photonics devices in the first segment are proposed by the author and the others are used for testing the experimental performances of IMEC technology in my custom test setup and for extracting parameters for our future photonics chip design. Also, when driving three-segment MRMs with ground/signal/signal/signal/ground as their five pads, generic probes can't be used due to their non ground/signal/ground signaling. As a result, only the testing setups for the ten three-segment MRMs in the first segment will be discussed in this section.

As will be mentioned in chapter 6, my three-segment MRMs are designed to convert electrical PAM-4 signals into optical PAM-4 signals with my proposed scheme, where optical PAM-4 signals at their through ports will be detected and used as my criteria to compare

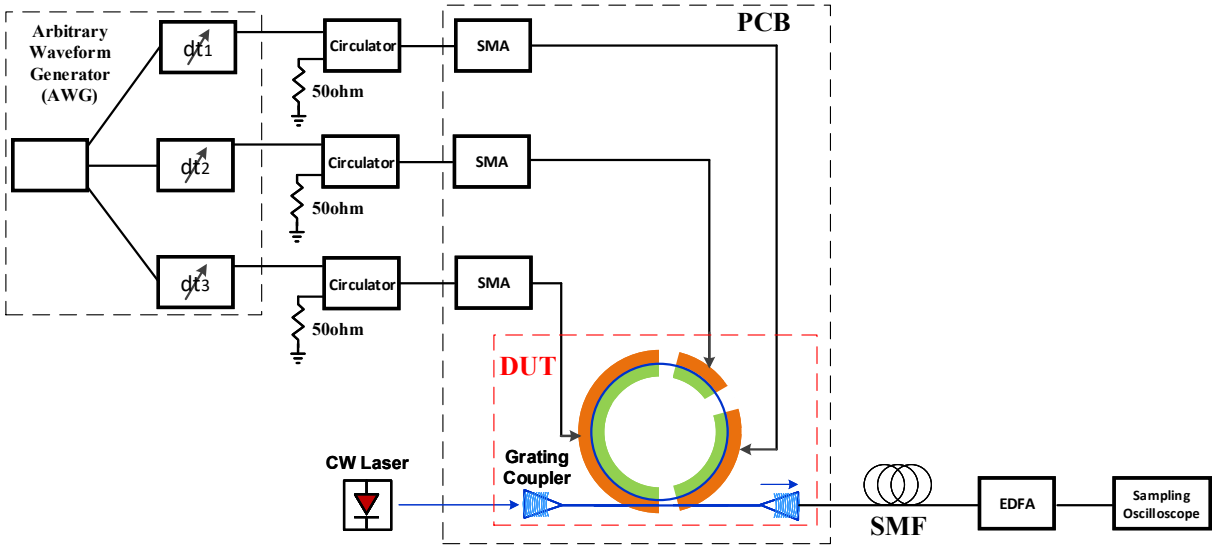

Figure 5.7: Experiment Setup for testing On-chip Three-Segment Microring Modulators

different three-segment MRM designs. Since we can't use RF probes to inject the electrical signals into my three-segment MRMs, we have proposed a different transmission experimental setup as shown in Fig. 5.7.

Light generated by a continuous-wave laser source with tunable wavelength is coupled into a three-segment microring modulator under test through a fiber-to-chip grating coupler, are coupled out through another grating coupler into a single-mode fiber and then, pass through an EDFA in order to compensate for the insertion losses of two back-to-back grating couplers as well as the three-segment MRM. Lights will finally go into the optical input port of a sampling oscilloscope, where its optical eye-diagram can be demonstrated. A laser source that is capable of finely tuning its wavelength is necessary since the resonant wavelength of the microring modulator is sensitive to the temperature and the wavelength of the tunable laser can be adjusted accordingly to compensate for its change. my design under test (DUT) includes two back-to-back grating couplers and a three-segment MRM, which are all fabricated on my photonics chip shown in Fig. 5.6.

Since there are three electrical driving signals (one for each phase-shifter in the microring), we have fabricated a high-speed PCB board instead of using probes for proper driving

signal injections as mentioned before. On the board, there are three 27GHz end launch SMA connectors each with with ground/signal/ground signaling, which are used for injecting electrical signals onto the board. Those three electrical signals will then pass through three high-speed transmission lines separately and later into the three phase-shifters of the three-segment microring modulator through bondwires. Since the characteristic impedance of both SMAs and transmission lines is 50Ω and the equivalent load of the phase-shifters is capacitive, there will be reflections on the interface between microring and transmission line, which results in loss of injected power. Although we can increase the injected power level, it will also produce more power reflection and thus, cause damage to the testing equipment. In order to avoid damaging the equipment, a circulator is inserted in between and the reflected electrical power can be diverted into a 50Ω termination resistor instead.

According to the voltage-tuning scheme to be discussed in chapter 6, the three electrical driving signals are not three uncorrelated PRBS signals and are different depending on the photonics fabrication results. Thus, we have to use arbitrary waveform generator(AWG), in my case Agilent M8195A, to generate more flexible electrical signals that can accommodate microring modulators with different fabrication results. Also, due to the nature of three input signals, their transmission lines on the PCB are hard to design to be of the same length. Thus, we have to introduce tunable delays for three input electrical signals, which can be done in AWG with unit delay as small as 100fs and ranges from -100ps to 100ps.

There are two steps for determining those three driving voltages. Step one, three uncorrelated PRBS signals will be generated by using a PC with both software M8070A and M8195A soft front panel to control my AWG via a USB bus or LAN, which will result in non-equispaced optical PAM-8 signals. Through the result of optical PAM-8 signals, we can choose four optical levels which is closest to achieve equispaced optical PAM-4 signals and the three binary signal streams to generate them can be determined. The process above is called coarse tuning and will be discussed in the next chapter. Step two, we need to use M8195A to generate those three binary signal streams and apply them to the three-segment

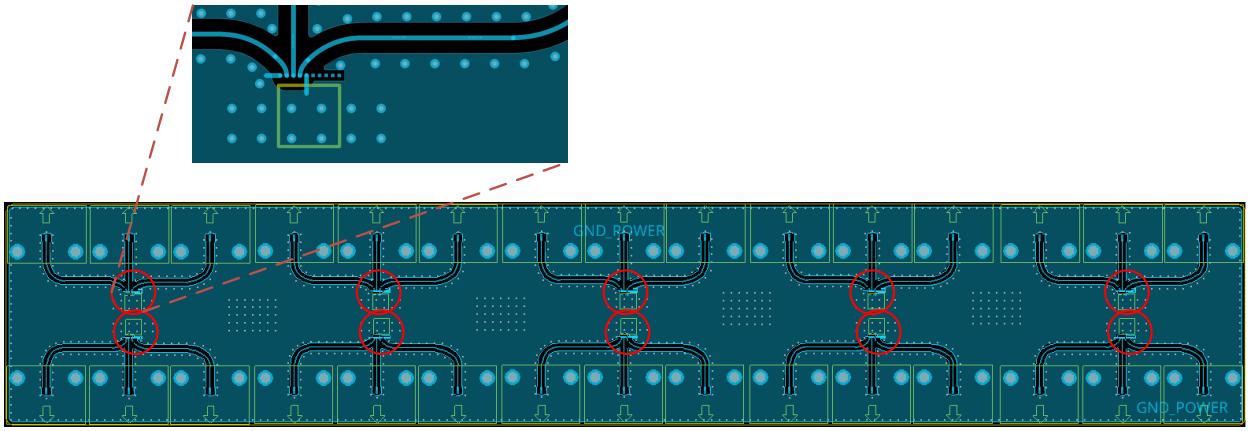

Figure 5.8: PCB Design

microring modulator to make sure that the optical output signals are close to equispaced PAM-4 signals. Then, we will finely tune the voltage levels of those three signals in order to generate equispaced optical PAM-4 signals with a high percentage of level separation mismatch ratio. The step above can be described as precise tuning and also be discussed in the next chapter.

One of the ways that we are using M8195A to generate random binary signals is through .csv file with my desired voltage values programmed in. However, M8195A uses first-order hold to connect nodes so we have to use several duplicated nodes to represent one node. Luckily, M8195A has much higher sampling rate than we need: it has sampling rate of 62.5GSa/s so that we can use five nodes in total to represent one node with the data rate of 12.5GSa/s. The transition point can be smoothed out with the low-pass filtering effect from my connecting cables. The bandwidth of M8195A is 25GHz, which is enough in my scenario. Just in case we need higher bandwidth for my AWG, we can use different ones: M8194A has the sample rate of 120GSa/s with analog bandwidth of 45GHz and M8196A has the sample rate of 92GSa/s with analog bandwidth of 32GHz.

The PCB that we have designed for the testing is shown in Fig. 5.8. There are ten same testing structures fabricated on one PCB board and each consists of three end launch SMA connectors, three transmission lines with characteristic impedance of 50Ω and one slot for placing my photonics chip. Since we only have single plane PCB boards, we can't wirebond

all ten three-segment MRMs on a single chip to my board simultaneously. Therefore, we simplify my wirebonding procedures by putting ten chips on one PCB board and wirebonding only one three-segment MRM from one chip, which results in ten slots for ten chips on a single PCB board. Although three transmission lines don't have equal length in my PCB and can cause skews between them, their skews can be compensated using tunable delay building blocks within AWG. Fig. 5.8 also provides the zoom-in view of each red circle in the figure. Since the signaling of SMA is ground/signal/ground and we have to combine three of those signalings into ground/signal/signal/signal/ground, the transmission lines at the far end will still maintain the signaling of ground/signal/ground and only one of its ground paths will recede when it comes close to the slot of the chip. Thus, at the near end of chip slot, there will only be five pads for wirebonding with the signaling of ground/signal/signal/signal/ground. It is worth noting that since there will be wirebonding involved, my PCB has to use ENEPIG (Electroless Nickel Electroless Palladium Immersion Gold) final finish for the following reasons: first, it offers great strength that wirebonding needs; second, it reduces porosity and shields copper layer beneath; finally, it is a must for high-frequency circuits since it can prevent nickel from interference at high frequency [69].

Although we can't actually perform the experiment at the moment, we can predict my testing results through simulations. Due to the complexities of the circuit-level designs in order to generate optical PAM-4 signals through driving a three-segment microring modulator, all the simulations will be performed using Cadence Virtuoso where the optical devices are modeled with Verilog-A instead of using simulation tools such as Lumerical Interconnect [70].

In order to simulate the two sets of three-segment microring modulators with five different gaps between straight waveguide and microring fabricated on the first segment of my photonics chip, we have simulated two sets of three-segment microring modulators with five different coupling coefficients. Although we can't precisely determine the exact coupling coefficients for five different gaps, we can choose five different coupling coefficients and study their effects on the extinction ratio (ER) of the microring modulator. According to the

Table 5.1: Extinction Ratio Results for Five Different Coupling Coefficients of Two Versions of Three-Segment Microring Modulator

Phase-Shifters Angles / Coupling Coefficient	$\pi : \pi/2 : \pi/4$	$2\pi/3 : \pi/3 : \pi/6$
0.2	4.9 dB	3 dB
0.2364	11.3 dB	8.4 dB
0.3	7.2 dB	4.8 dB
0.4	1 dB	0.6 dB
0.5	0.4 dB	0.22 dB

testing results provided by IMEC-ePIXfab SiPhotonics ISIPP50G technology handbook, the coupling coefficient of the standard microring modulator is 0.2364 when the gap is 150nm while in my photonics chip, five gaps–150nm, 180nm, 200nm, 250nm and 300nm–are implemented. As a result, five coupling coefficients–0.2, 0.2364, 0.3, 0.4, 0.5–are chosen in my simulation and their resulting extinction ratios for two sets of microring modulators can be seen in table 5.1.

According to table 5.1, the extinction ratios (ERs) for both sets are larger than 3dB when the coupling coefficient is between 0.2 and 0.3 with the largest ER at 0.2364, which suggests that in the experiment, we are likely to see a large extinction ratio in at least one of the five microring modulators in one set. Also, simulation results also show that version one with the longer phase-shifters has larger extinction ratio but their differences might not be prominent during testing.

As mentioned before, the purpose of implementing a three-segment MRM is to produce optical PAM-4 signals at its through port and one of the criteria is to quantify the eye-diagrams of this optical PAM-4 signals. Since five different MRMs are designed to find the ones closest to working at critical coupling condition, we can use the one with the coupling coefficient closest in that situation, which is 0.2364. Thus, we have plotted the eye-diagrams for MRMs with the coupling coefficient of 0.2364 in Fig. 5.9 with the right figure representing the version one three-segment MRM and the left figure representing the version two three-segment MRM. The resulting level separation mismatch percentage of version one

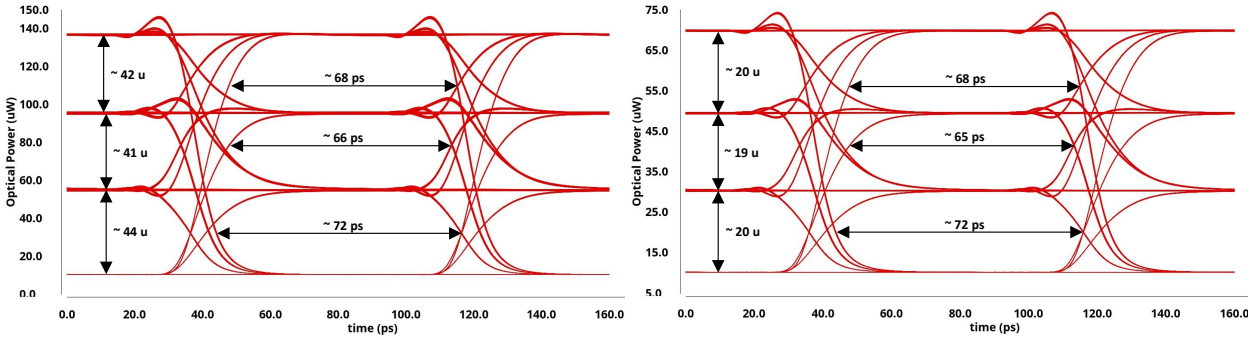

Figure 5.9: (Right) Simulated 12.5GS/s Optical Eye-diagram of Version One Three-Segment Microring Modulator (Left) Simulated 12.5GS/s Optical Eye-diagram of Version Two Three-Segment Microring Modulator

three-segment MRM is 96.6% and that of version two three-segment MRM is 96.8%. The simulation results above show that both can achieve PAM-4 data rate of 25Gb/s with high percentage of level separation mismatch and with scheme discussed in the following chapter, three-segment MRMs can generate optical PAM-4 signals with high linearity.

This chapter discusses the layout implementation of my fabricated photonics chip, which is different from traditional IC layout designs and thus, is important to IC layout engineers also interested in fabricating photonics chips. Later, this chapter uses my proposed photonics layout implementation method to produce a new photonics chip with IMEC 50G technology and then, proposes a setup to test the fabricated chip. Finally, prospective testing results of the chip can be derived from the simulations performed in Cadence Virtuoso.

Chapter 6: A Scheme to Realize Optical PAM-4 Based on Three-Segment MRM

6.1 Three-Segment Microring Modulator Verilog-A Modeling and its Result

In this section, we will analyze how to use the three-segment microring modulator to realize optical PAM-4 but first, let's take a look at the Verilog-A modeling for my proposed three-segment microring modulator. The layout of my proposed three-segment microring modulator is derived from that of the standard microring modulator fabricated with IMEC-ePIXfab SiPhotonics ISIPP50G technology. The surrounding optical devices of my proposed modulator include a CW laser, two grating-couplers and the straight waveguide from the microring modulator extended to connect two grating couplers as shown in Fig. 6.1(a). The three-segment microring modulator chosen in this case is the one on the right of Fig. 5.4, which has the radius of $5\mu m$ and those three phase-shifters inside the microring have the central angle of $45° : 90° : 180°$, which results in the length ratio of 1:2:4. Both the microring and the straight waveguide are based on the silicon-on-insulator (SOI). Aside from the three phase-shifters, there are three equal length gaps in between in order to provide enough space to separate those three phase-shifters so as to adhere to the layout design rule of IMEC technology.

A Verilog-A block diagram for three-segment microring modulator can be seen in Fig. 6.1(b), which contains three phase-shifters, one waveguide, one coupler and one laser source. The grating coupler is not modeled since it only provides amplitude attenuation, which can be realized through changing the amplitude of the CW laser output. The waveguide models the combinations of three gaps in between three phase-shifters and thus, the length sum of three phase-shifters and one waveguide is the circumference of the microring. The waveguide model is the same as the phase-shifter model with its anode and cathode both biased to ground. A voltage source V_{laser} determines the output power of the laser source:

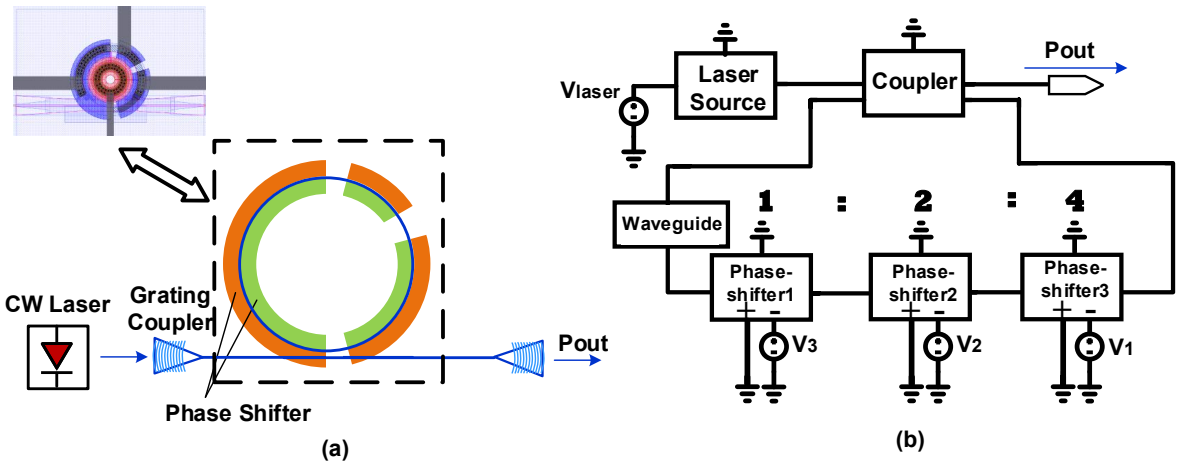

Figure 6.1: Three-Segment Ring Modulator and its Verilog-A Block Diagram

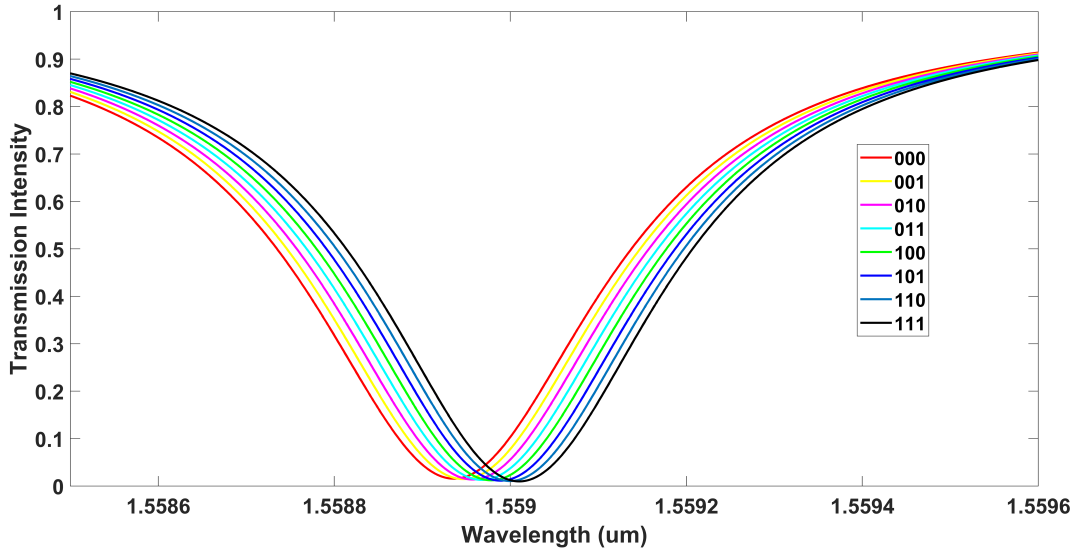

Figure 6.2: Transmission Intensity Result of Three-Segment Ring Modulator

DC voltage 31.62278mV corresponds to 1mV output power.

If we apply two different voltages, 0V and 2.4V, to the biasing voltages V_1, V_2 and V_3 of the three phase-shifters, we can derive eight transmission curves as shown in Fig. 6.2. The "1" and "0" shown in the legends of the figure represents 2.4V and 0V respectively. As we increase the biasing voltages, the transmission curve will be shifting to the right where the wavelength is increasing and thus, it is called red-shifting. Although transmission curves

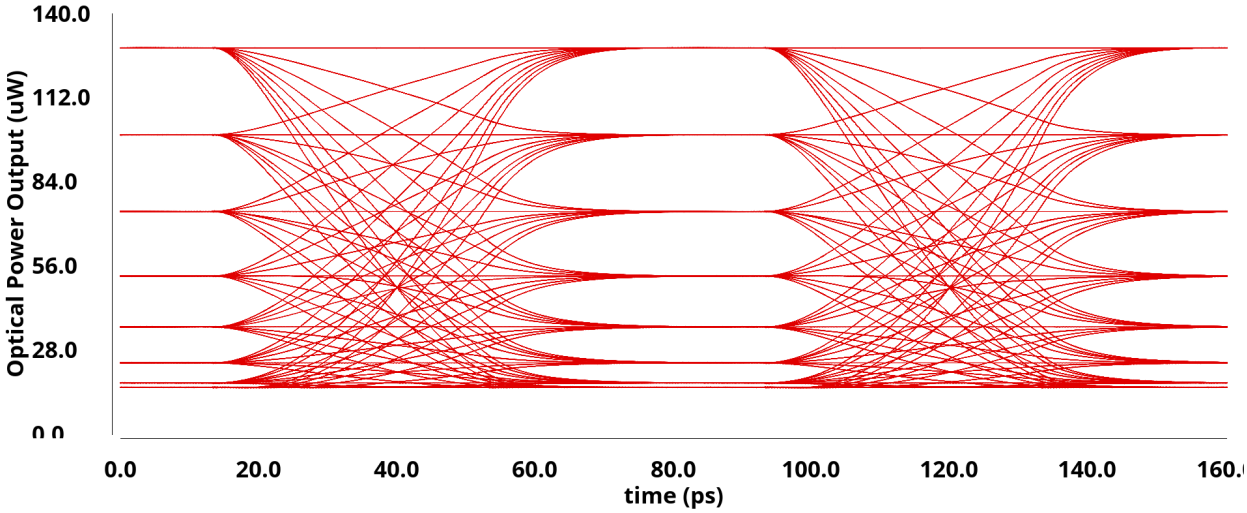

Figure 6.3: Eye Diagram of P_{out} at Symbol Rate of 12.5GS/s

can demonstrate some characteristics of the microring modulator, modulators are usually operating at one wavelength at a time and thus, we need to find out the wavelength where the extinction ratio can be maximized. In the transmission curves, there are two wavelengths that fit the description above: the resonant wavelength of logic "000" and logic "111". Due to its thermal stability, however, the resonant wavelength of logic "000" is used, which is $1.55884\mu m$ corresponding to the frequency offset of -1.1088THz. If we inject the wavelength of $1.55884\mu m$ with the power of 1mW into the three-segment microring modulator through the CW laser, the resulting eye-diagram of the optical power output P_{out} can be seen in Fig. 6.3. It is much clearer to see through the eye-diagram that the three-segment microring modulator can't produce equispaced PAM-8 signals.

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6.2 Proposed Scheme Analysis

According to the Verilog-A simulation result of three-segment MRM, if we apply three uncorrelated PRBS signals to the three phase-shifters of the MRM, we have in total eight different transmission curves. If we inject the optical signal with a single wavelength (commonly using the resonant wavelength of the microring under zero biasing condition) and

detect the optical power output of the modulator, there will be in total eight optical power levels.

On the first thought, we might want to use my proposed three-segment microring modulator to realize optical PAM-8. However, there are several of reasons that would go against it. First, those eight optical levels are not naturally equally spaced. Second, if we can change the lengths of those three phase-shifters, their total lengths are constant and thus, those eight levels are not uncorrelated, which means that when one of the levels is changed, the others will be different too. Third, even if we have been able to find out the correct lengths for realizing equally-spaced PAM-8, due to the fabrication related imperfections, the simulation result and the testing result will be different and it would render using three-segment MRM to realize PAM-8 unreliable.

Therefore, if we can't use my three-segment MRM to realize optical PAM-8, we have decided to find a scheme that is able to realize optical PAM-4 instead. Since we can choose four optical levels from eight total optical levels, using three-segment MRM instead of the two-segment has much better flexibility. As a result, there are two ways of realizing optical PAM-4 using three-segment MRM. First, we can change the lengths for three phase-shifters. We only need to choose four levels out of eight and thus, adjusting the lengths of those three phase-shifters can always realize optical PAM-4. However, once the MRM is fabricated, the length of the three phase-shifters is fixed and thus, this method is intolerant of fabrication imperfection. The second method is to use a fixed length for three phase-shifters and change their biasing voltages instead. Although the second method has shifted the design burden towards the electrical domain, which requires designing a driver that is able to produce biasing voltages that are not power supply or ground, it won't suffer from the fabrication imperfection of the optical circuits. Since electrical integrated circuits have developed much more than photonics circuits and driver design is relatively more mature, putting burden onto electrical circuit is justifiable.

In my design, we have chosen the second method: using a fixed length for three phase-

shifters and designing the drivers, which can realize different biasing voltages. On the other hand, we have to choose four levels instead of using all eight levels. In fact, those two aspects are similar but not the same: both of them will decide the biasing voltage for each phase-shifter. However, the first aspect is to decide which binary code, either logic "1" or logic "0" will be used for biasing voltage. Then, the second aspect will decide which voltage will be used for either 'logic '1" or logic "0". Therefore, we have named the first aspect of my scheme, the coarse tuning since we can only choose four levels out of eight possible levels. We have named the second aspect of my scheme, the precise tuning since designed drivers will be able to generate much higher precision for voltage than simply choosing from eight possible levels.

In order to explain my scheme by showing how to achieve equally spaced optical output power intensity, we can by definition use the MRM optical output power P_{out}. However, since the optical output power is proportional to optical power input fed into the microring modulator, its y-axis will change accordingly. At the same time, the transmission intensity of the microring won't change with regard to the optical power input and thus, we will use it in my explanation for my proposed scheme.

First, let's denote $|T|^2 (V_1, V_2, V_3, \lambda)$ as the transmission intensity of my three-segment MRM. In this denotation, T stands for transmission, V is the symbol for representing voltage and λ is wavelength injected into the MRM by continuous-wave laser. V_1, V_2, V_3 are the three biasing voltages applied to the three phase-shifters with the length ratio of 4 to 2 to 1. Since my microring modulation will be used in its depletion mode only, its biasing voltage will not be greater than zero and thus, we have chosen to denote V_1, V_2, V_3 as the reverse biasing voltages. Therefore, the real biasing voltages will be $-V_1, -V_2, -V_3$ and these reverse biasing voltages can be produced through applying the voltages to the cathodes of phase-shifters while keeping anodes grounded. On the other hand, a positively biased voltage can be generated by applying voltages to anodes of phase-shifters while keeping their cathodes grounded.

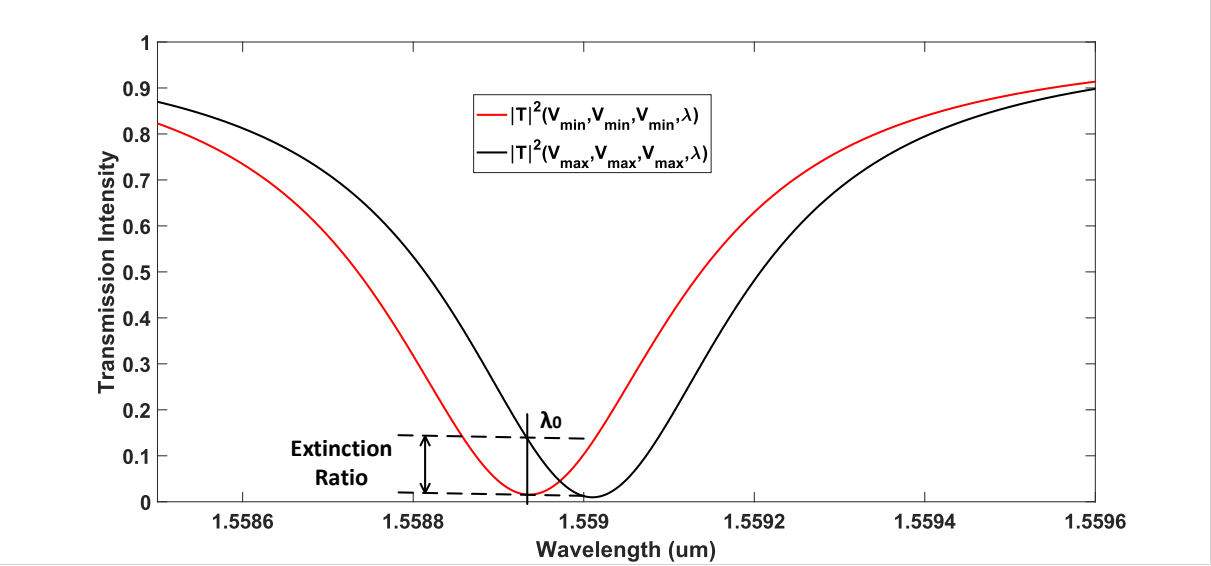

Figure 6.4: Transmission Intensity Curves under Two Reverse Biasing Conditions

Although the actual biasing voltages for phase-shifters will vary due to my driver design, there will be a range for the biasing voltages. The largest reversely biased voltage happens when the power supply is applied to the cathodes of phase-shifters and the smallest reversely biased voltage happens when the power supply is applied to the anodes of phase-shifters. However, in order to generalize my scheme derivation, we have chosen to denote the smallest reverse biasing voltage to be V_{min} and biggest reverse biasing voltage to be V_{max}. Therefore, the three biasing voltages can be expressed as $V_{1,2,3} \in [V_{min}, V_{max}]$. Since V_{max} is bigger than V_{min} and both of them are the voltages applied to the cathodes, the transmission curve will be redshifted (wavelength is increasing) from $|T|^2(V_{min}, V_{min}, V_{min}, \lambda)$ to $|T|^2(V_{max}, V_{max}, V_{max}, \lambda)$ as shown in Fig. 6.4. One of the parameters that are used to characterize the microring modulator is the extinction ratio and according to the transmission intensity curve shown here, the extinction ratio at the resonant wavelength λ_0 can be expressed as follows:

$$ER = \frac{|T|^2(V_{max}, V_{max}, V_{max}, \lambda_0)}{|T|^2(V_{min}, V_{min}, V_{min}, \lambda_0)} \tag{6.1}$$

The extinction ratio here is the maximum given the range of my biasing voltages, which is according to the design of my drivers since the drivers won't necessarily be able to generate two power supplies with different polarities. As will be discussed later, once the precise tuning is enabled, the largest biasing voltages that can be generated by my driver design will be reduced. That's why we have introduced a precise tuning disable signal, which is able to disable precise tuning when the PAM-4 signals are either "11" or "00". As a result, my design can achieve the highest extinction ratio given my power supply and my driver design. Therefore, the transmission intensity to achieve logic "11" and "00" can be expressed as follows:

$$\begin{aligned} |T_{11}|^2 &= |T|^2(V_{max}, V_{max}, V_{max}, \lambda_0) \\ |T_{00}|^2 &= |T|^2(V_{min}, V_{min}, V_{min}, \lambda_0) \end{aligned} \tag{6.2}$$

where V_{max} and V_{min} are the maximum biasing voltage and the minimum biasing voltage respectively that can be generated through my proposed drivers and possible power supplies.

Since the transmission intensity of the optical PAM-4 should be equally spaced, the transmission intensity to achieve logic "10" and "01" can be shown as below:

$$\begin{aligned} |T_{10}|^2 &= (|T_{11}|^2 - |T_{00}|^2) \times \frac{2}{3} \\ |T_{01}|^2 &= (|T_{11}|^2 - |T_{00}|^2) \times \frac{1}{3} \end{aligned} \tag{6.3}$$

Through the equations above, we can calculate the required driving voltages $V_{1,2,3}$ for both $|T_{10}|^2$ and $|T_{01}|^2$. As a result, the driving voltages $V_{1,2,3}$ for $|T_{11}|^2$, $|T_{10}|^2$, $|T_{01}|^2$ and $|T_{00}|^2$ are all different. However, they are sharing the same resonant wavelength λ_0.

Unlike discrete circuits where you can tune your voltages as needed, integrated circuits won't be able to fine-tune the voltages arbitrarily. Therefore, we have chosen to discretize the driving voltages according to the simple circuit model as shown in Fig. 6.5. There are

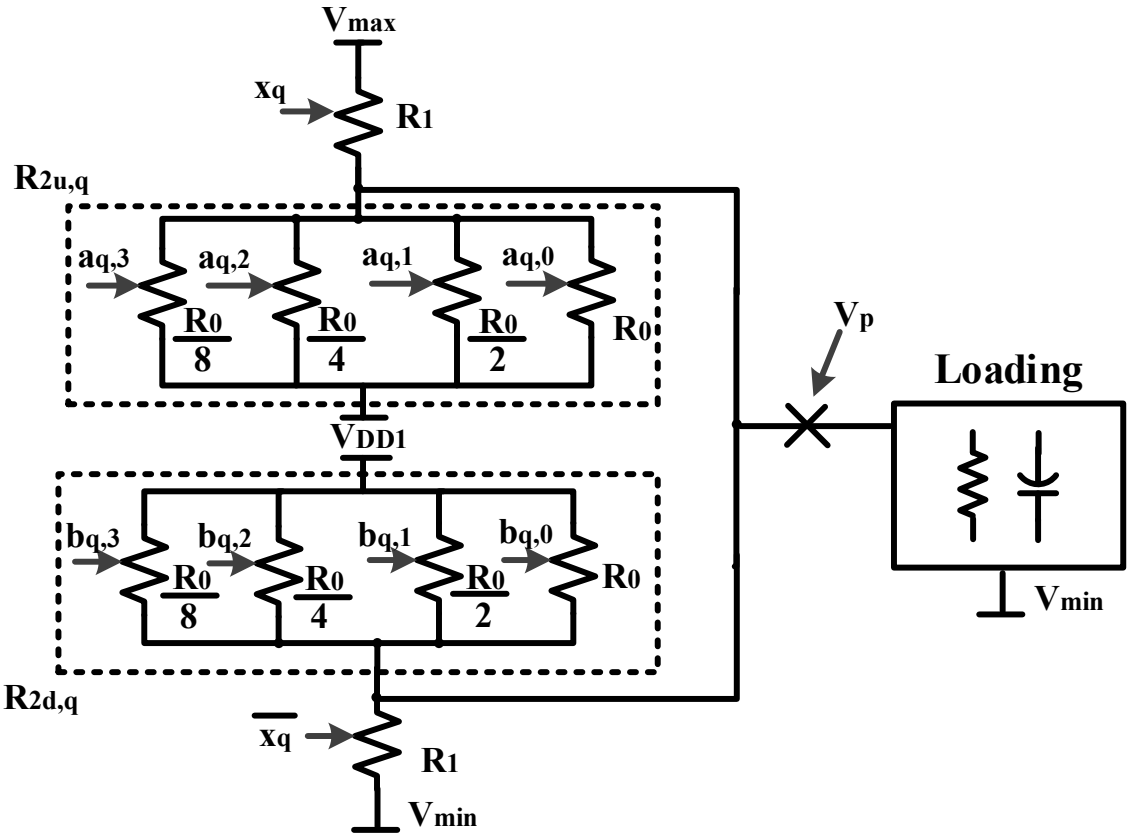

Figure 6.5: Equivalent Circuit for Discretizing Voltages V_p where $p = 1, 2, 3$

two branches to drive the loading (to supply the biasing voltage V_p): pull-up branch and pull-down branch. Both branches are controlled by one resistor R_1 and four resistors with resistance of R_0, $R_0/2$, $R_0/4$ and $R_0/8$ respectively. The pull-up branch has the supply voltage of V_{max} and uses V_{DD1} as ground while the pull-down branch has the supply voltage of V_{DD1} and uses V_{min} as its ground. Both resistors R_1 in the pull-up and pull-down branch are controlled by signal x_q but with different polarities since R_1 in the pull-up branch is realized using the PMOS transistor and R_1 in the pull-down branch is realized using the NMOS transistor. The four resistors in the pull-up branch with a ratio of 8 to 4 to 2 to 1 are controlled by $a_{q,0}$, $a_{q,1}$, $a_{q,2}$ and $a_{q,3}$ respectively and the four resistors in the pull-down branch with ratio of 8 to 4 to 2 to 1 are controlled by $b_{q,0}$, $b_{q,1}$, $b_{q,2}$ and $b_{q,3}$ respectively. As

a result, if we denote the equivalent resistance of those four resistors in the pull-up branch as $R_{2u,q}$ and of those four resistors in the pull-down branch as $R_{2d,q}$, they can be expressed as follows:

$$\frac{1}{R_{2u,q}} = \sum_{m=0}^{3} \frac{2^m}{R_0} \times a_{q,m} \tag{6.4}$$

$$\frac{1}{R_{2d,q}} = \sum_{m=0}^{3} \frac{2^m}{R_0} \times b_{q,m} \tag{6.5}$$

The loading is the equivalent circuit model of the phase-shifter and it is mostly capacitive but large resistance. Also, since the lowest voltage of the equivalent circuit is denoted as V_{min} instead of ground or zero volt, the ground for the loading will also be V_{min}. Consequently, the driving voltage V_p for the loading is shown as follows:

$$V_p = \begin{cases} \frac{V_{max}-V_{DD1}}{R_1+R_{2u,q}} \times R_{2u,q} + V_{DD1} when \quad x_q = \text{“1”} \\ \frac{V_{DD1}-V_{min}}{R_1+R_{2d,q}} \times R_1 + V_{min} \quad when \quad x_q = \text{“0”} \end{cases} \tag{6.6}$$

Since the loading is one of the three phase-shifters and we denote their driving voltages as V_1, V_2 and V_3, p can be either 1 or 2 or 3. As for q, since we want to distinguish them, we assign either i or j or k to it. Since either x_q or $a_{q,3:0}$ or $b_{q,3:0}$ are used to turn on/off the resistors, they can be represented by binary codes “1” and “0”. Therefore, we denote the biasing voltages that are generated by drivers as $V_1(x_i, a_{i,3:0}, b_{i,3:0})$, $V_2(x_j, a_{j,3:0}, b_{j,3:0})$ and $V_3(x_k, a_{k,3:0}, b_{k,3:0})$, where each biasing voltage is controlled by one binary code and two sets of 4-bit codes. We name my scheme voltage tuning since all those bits are used to tune the driving voltage. In order to understand the mechanism of my proposed scheme, we have first categorized it into two different sub tuning schemes: coarse tuning and precise tuning.

6.2.1 Coarse Tuning Scheme

Equation 6.6 describes the combination of both coarse tuning and precise tuning. If we assume that $a_{q,3:0}$ = "0000", $b_{q,3:0}$ = "0000", $R_{2u,q} \to \infty$ and $R_{2d,q} \to \infty$, the following equation can be described:

$$V_p = \begin{cases} V_{max} \quad when \quad x_q = \text{“1”} \\ V_{min} \quad when \quad x_q = \text{“0”} \end{cases} \tag{6.7}$$

Since V_p can be either V_1 or V_2 or V_3 and each voltage has two possible values according to x_q, there can be eight possible voltage combinations to choose from to drive three phase-shifters and we can denote the combination as (V_1,V_2,V_3). Eight possible combinations are much fewer than the number of combinations we will be using in the precise tuning scheme. That's why we can call this coarse tuning.

However, since the purpose of my scheme is to realize optical PAM-4 signals, those eight levels can't be used at the same time. As a matter of fact, the driving signals of my proposed scheme has to be two uncorrelated PRBS signals, which are able to realize electrical PAM-4 to begin with. Therefore, it is inevitable that my scheme requires a mapping algorithm, that is able to find out the corresponding 3 bit signals to the 2 bit signals including $|T_{11}|^2$, $|T_{10}|^2$, $|T_{01}|^2$ and $|T_{00}|^2$.

In order to realize the highest extinction ratio, $|T_{11}|^2$ has to be the combination where $(V_1, V_2, V_3) = (V_{max}, V_{max}, V_{max})$ corresponding to $x_i x_j x_k$ = "111", which is equal to mapping logic "11" to "111". $|T_{00}|^2$ has to be the combination where $(V_1, V_2, V_3) = (V_{min}, V_{min}, V_{min})$ corresponding to $x_i x_j x_k$ = "000", which is equal to mapping logic "00" to "000". As for the other two optical levels $|T_{10}|^2$ and $|T_{01}|^2$, there are six optical levels left from 3 bit signals to choose from: $x_i x_j x_k$ = "110", $x_i x_j x_k$ = "101", $x_i x_j x_k$ = "100", $x_i x_j x_k$ = "011", $x_i x_j x_k$ = "010" and $x_i x_j x_k$ = "001". Because $|T_{10}|^2$ will always be larger than $|T_{01}|^2$, the 3 bit

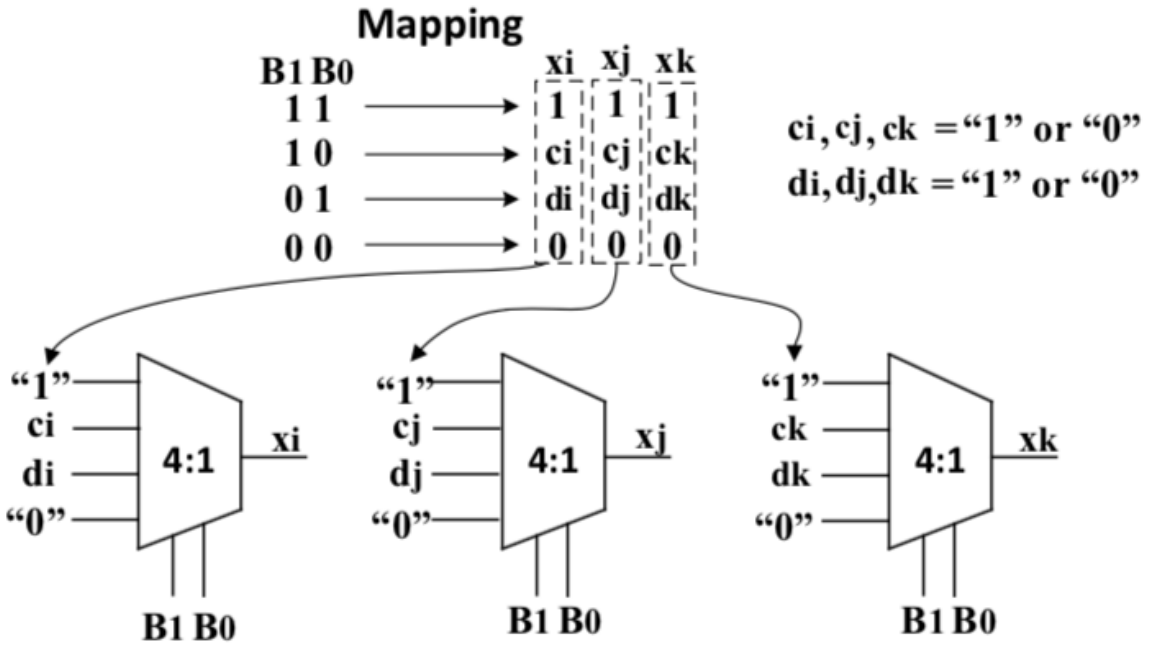

Figure 6.6: Block Diagram for Realizing Coarse Tuning

signals chosen by $|T_{10}|^2$ will also always be larger than those chosen by $|T_{01}|^2$. As a result, there will only be 15 different mapping possibilities: when $|T_{10}|^2$ is mapped to $|T_{110}|^2$, $|T_{01}|^2$ can be mapped to $|T_{101}|^2$, or $|T_{100}|^2$ or $|T_{011}|^2$ or $|T_{010}|^2$ or $|T_{001}|^2$; when $|T_{10}|^2$ is mapped to $|T_{101}|^2$, $|T_{01}|^2$ can be mapped to $|T_{100}|^2$ or $|T_{011}|^2$ or $|T_{010}|^2$ or $|T_{001}|^2$; when $|T_{10}|^2$ is mapped to $|T_{100}|^2$, $|T_{01}|^2$ can be mapped to $|T_{011}|^2$ or $|T_{010}|^2$ or $|T_{001}|^2$; when $|T_{10}|^2$ is mapped to $|T_{011}|^2$, $|T_{01}|^2$ can be mapped to $|T_{010}|^2$ or $|T_{001}|^2$; when $|T_{10}|^2$ is mapped to $|T_{010}|^2$, $|T_{01}|^2$ can be only mapped to $|T_{001}|^2$.

Logically, the aforementioned 2-to-3-bit mapping can be realized through three 4-to-1 selectors as shown in Fig. 6.6. B_1B_0 represents two uncorrelated PRBS signals that can generate electrical PAM-4 signals and their transmission intensities can be denoted as $|T_{B_1B_0}|^2$. $x_ix_jx_k$ is the mapping result and its transmission intensity can be denoted as $\left|T_{x_ix_jx_k}\right|^2$. The mapping is basically trying to find out $x_ix_jx_k$ for the closest $\left|T_{x_ix_jx_k}\right|^2$ towards $|T_{B_1B_0}|^2$. Each column of the mapping results represents the codes to generate either x_i or x_j or x_k and those codes are the inputs of the respective selector. Those codes are logic signals

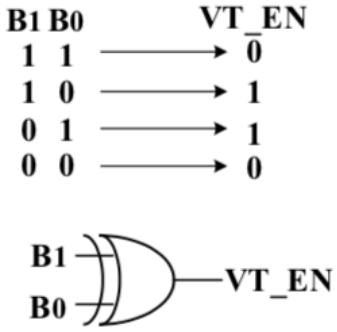

Figure 6.7: Precise Tuning Disable Signal Generator

as well as DC signals where "1" represents power supply and "0" represents ground while B_1B_0 are dynamic signals instead. As a result, the three output signals of the three 4-to-1 selectors are dynamic signals just like B_1B_0 but are not correlated like B_1B_0.

6.2.2 Precise Tuning Scheme

After the coarse tuning is achieved, the mapping $\left|T_{x_ix_jx_k}\right|^2$ from $|T_{B_1B_0}|^2$ when B_1B_0 = "10" and B_1B_0 = "01" will be decided. However, tuning doesn't end there. If we consider Fig. 6.5, what the coarse tuning has accomplished is to decide either V_p will be driven by the pull-up branch or the pull-down branch. Since there are four resistors for either pull-up or pull-down branch, they can realize 16 different voltages in a range of $[\frac{V_{max}-V_{DD1}}{(15R_1)/R_0+1}+V_{DD1}, V_{max}]$ when x_q = "1" and in a range of $[V_{min}, \frac{V_{DD1}-V_{min}}{1+R_0/(15R_1)}+V_{min}]$ when x_q = "0". For each mapping result $\left|T_{x_ix_jx_k}\right|^2$ from either $|T_{B_1B_0}|^2$ where B_1B_0 = "10" or $|T_{B_1B_0}|^2$ where B_1B_0 = "01", 16 possible voltage levels for one of the three bits will result in 4096 possible levels($16\times16\times16$) and that is only one of the two PAM-4 levels that can generate this many possible optical levels. Thus, we call this precise tuning since the coarse tuning is only able to achieve 15 different possibilities.

Just like the inputs of 4-to-1 selectors, two sets of inputs $a_{q,3:0}$ and $b_{q,3:0}$ of the equivalent circuit for discretizing voltage V_p are also binary DC signals and as a result, are two 4-bit binary vectors. However, the tuning above only happens when B_1B_0 = "10" or B_1B_0 = "01".

Since both $a_{q,3:0}$ and $b_{q,3:0}$ are DC signals, which won't change when B_1B_0 changes, $|T_{11}|^2$ and $|T_{00}|^2$ will be affected as long as $a_{q,3:0}$ and $b_{q,3:0}$ are not "0000" and thus, the extinction ratio will be reduced. Therefore, we need to generate another signal to disable precise tuning when either B_1B_0 = "11" or B_1B_0 = "00". The signal mentioned above is called precise tuning disable signal VT_{EN} and can be realized through a XOR gate as shown in Fig. 6.7. In my design, voltage tuning disable signal will be used to control two sets of four resistors in both the pull-up and pull-down branches by bypassing the signals $a_{q,3:0}$ and $b_{q,3:0}$. One of the ways to implement that is to put a NAND/NOR gate in front of those resistor sets and apply both signals $a_{q,3:0}/b_{q,3:0}$ and VT_{EN} to them. Accordingly, we will have to generate the opposite polarities of VT_{EN} since both branches require VT_{EN} and the resistors in those two branches are realized through PMOS and NMOS, respectively.

6.2.3 Lower "1" and Higher "0" Tuning

If we combine both precise tuning and coarse tuning together, the mechanism of my tuning scheme will be hard to comprehend and thus, we have categorized the combination of those two tuning schemes into two sub-schemes: lower "1" tuning and higher "0" tuning.

According to the connotation of biasing voltage V_p, $V_p(x_q, a_{q,3:0}, b_{q,3:0})$, where $p = 1, 2, 3$, $q = i, j, k$, we can see that this connotation has included both the coarse tuning and precise tuning together. If we set $b_{q,3:0}$ = "0000" and use $a_{q,3:0}$ for precise tuning, there will be 16 possible voltages for V_p when x_q = "1" and V_p will always be V_{min} when x_q = "0". Since V_p will be lower than V_{max} when x_q = "1", we have categorized this scenario as lower "1" tuning. On the other hand, if we set $a_{q,3:0}$ = "0000" and use $b_{q,3:0}$ for precise tuning, there will be 16 possible voltages for V_p when x_q = "0" and V_p will always be V_{max} when x_q = "1". Since V_p will be higher than V_{min} when x_q = "0", we have categorized this scenario as higher "0" tuning.

Now that $b_{q,3:0}$ is set as "0000" when lower "1" tuning is enabled and $a_{q,3:0}$ is set as "0000" when higher "0" tuning is chosen, we can further simplify the denotation of V_p under these

two tuning scenarios: for lower "1" tuning, V_p is denoted as $V_{pL}(x_q, a_{q,3:0})$ while for higher "0" tuning, V_p is denoted as $V_{pH}(x_q, b_{q,3:0})$.

Since lower "1" tuning and higher "0" tuning are the combination of both precise tuning and coarse tuning, both tuning methods can generate more than 4096 possible optical PAM-4 levels. According to coarse tuning, only $|T_{10}|^2$ and $|T_{01}|^2$ need to be mapped, which will result in only 15 different mappings with coarse tuning alone. For each set of mapping result mentioned above, precise tuning can produce two different amounts of PAM-4 optical levels for either lower "1" tuning or higher "0" tuning.

For lower "1" tuning, let's take a look at one of the mapping results where $|T_{10}|^2$ is mapped to $|T_{110}|^2$ and $|T_{01}|^2$ is mapped to $|T_{101}|^2$. First, there will always be one scenario where $a_{q,3:0}$ = "0000" representing no lower "1" tuning is performed. Second, since only logic "1" can be tuned and "110" and "101" have at least one logic "1" in either their MSB, MSB-1 or LSB, there will be 15 possible levels when either only $a_{i,3:0} \neq$ "0000" or only $a_{j,3:0} \neq$ "0000" or $a_{k,3:0} \neq$ "0000"; there will be 225 (15×15) possible levels when either only $a_{i,3:0}$ = "0000" or $a_{j,3:0}$ = "0000" or $a_{k,3:0}$ = "0000"; there will be 3375 ($15 \times 15 \times 15$) possible levels with all three $a_{i,3:0} \neq$ "0000", $a_{j,3:0} \neq$ "0000" and $a_{k,3:0} \neq$ "0000". As a result, the scenario when there are 15 possible levels happens three times; the scenario when there are 225 possible levels happens three times and the scenario when there is one possible level happens once, which amounts to 4096 possible levels. There are five other coarse tuning mapping results that will amount to 4096 possible levels: $|T_{10}|^2$ is mapped to $|T_{110}|^2$ and $|T_{01}|^2$ is mapped to $|T_{011}|^2$ or $|T_{001}|^2$; $|T_{10}|^2$ is mapped to $|T_{101}|^2$ and $|T_{01}|^2$ is mapped to $|T_{011}|^2$ or $|T_{010}|^2$; $|T_{10}|^2$ is mapped to $|T_{100}|^2$ and $|T_{01}|^2$ is mapped to $|T_{011}|^2$. Therefore, there are in total 24576 possible PAM-4 levels.

As for the 9 remaining coarse tuning scenarios, since there is logic "1" in two out of three bits of the mapped results, there are two scenarios having 15 possible PAM-4 levels and one scenario having 225 possible PAM-4 levels. Along with one scenario where lower "1" tuning is disabled, there are 256 possible PAM-4 levels. Therefore, there are in total 2304 possible

PAM-4 levels.

If we combine the aforementioned 15 coarse tuning scenarios together, we have in total 26880 possible PAM-4 levels for lower "1" tuning alone.

For higher "0" tuning, we should have the same 26880 possible PAM-4 levels. However, the following six mappings will have 4096 possible levels: $|T_{10}|^2$ is mapped to $|T_{110}|^2$ and $|T_{01}|^2$ is mapped to $|T_{001}|^2$; $|T_{10}|^2$ is mapped to $|T_{101}|^2$ and $|T_{01}|^2$ is mapped to $|T_{010}|^2$; $|T_{10}|^2$ is mapped to $|T_{100}|^2$ and $|T_{01}|^2$ is mapped to $|T_{011}|^2$ or $|T_{010}|^2$ or $|T_{001}|^2$; $|T_{10}|^2$ is mapped to $|T_{010}|^2$ and $|T_{01}|^2$ is mapped to $|T_{001}|^2$. The remaining 9 coarse tuning scenarios will have 256 possible PAM-4 levels.

6.3 Ideal Transmitter Design using Transistor-Level Voltage-Mode Drivers

In the first step towards proving the validity of my proposed scheme, we will first design an ideal transmitter that is implementing my scheme to realize equispaced optical PAM-4. However, the ideal transmitter will also include transistor-level block: the driving signals for the three drivers will be generated through ideal blocks and the driver design itself will be at the transistor level using TSMC 65nm technology. The final proof of my proposed scheme will be presented using the optical power output of the three-segment microring modulator and its four optical levels have to be equispaced.

Since ideal circuits are used to supply the input signals for the driver, we will address the design of my driver first.

Unlike the Mach-Zehnder Modulator, the loading of the microring modulator is mostly capacitive and thus, the driver used in my design is a voltage-mode driver. As mentioned in Section 6.2, the equivalent circuit presented in Fig. 6.5 shows one of the ways to implement voltage-mode driver. Therefore, we have based my voltage-mode driver design on that aforementioned equivalent resistor model and the final voltage-mode driver circuit can

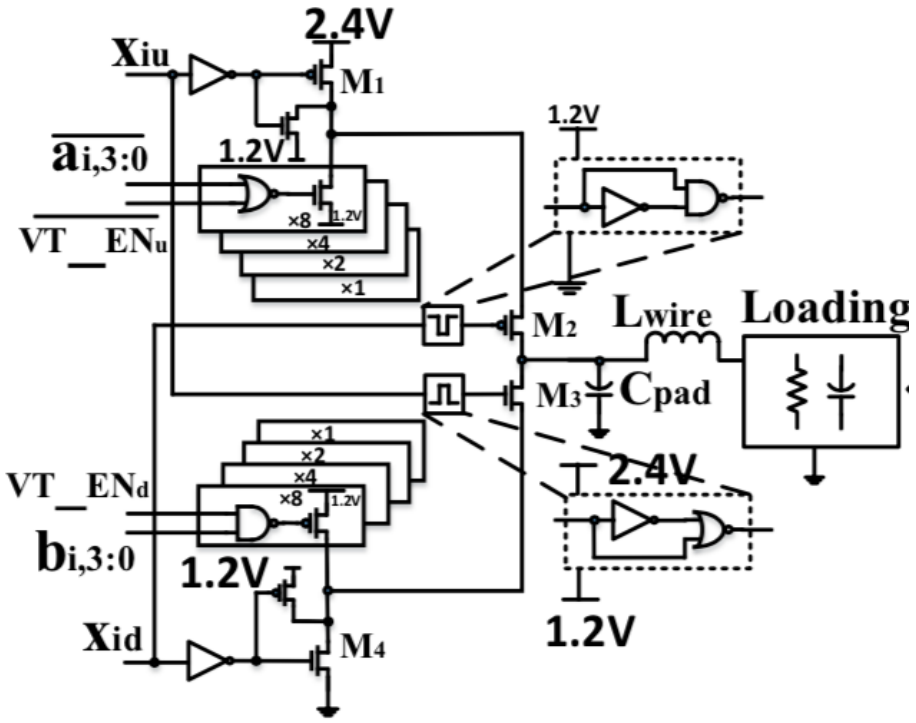

Figure 6.8: Voltage-Mode Driver with Tunability

be seen in Fig. 6.8. Also, my voltage-mode driver will be implemented using TSMC 65nm technology with the nominal power supply of 1.2V. Besides, since the voltage-mode driver and the microring modulator are not on the same chip (we are using a heterogeneous integration method), we have a bondwire model in-between to model their connections, which includes parallel capacitor C_{pad} and series inductor L_{wire}. Loading of the driver consists of pad capacitor, bondwire inductance, and the R-C load offered by both the phase-shifters and their pads.

First, the power supply for the voltage-mode driver is 2.4V and the ground is 0V, which correspond to the voltage V_{max} and V_{min}, respectively. The power supply in between, V_{DD1}, is 1.2V, which is half the power supply voltage of my driver.

Second, although the resistor R_1 is in both the pull-up and pull-down branches, it will be implemented using different types of transistors where R_1 in the pull-up branch and the pull-down branch is realized through NMOS M_4 and PMOS M_1 transistors respectively. Since the logic to turn on/off NMOS and PMOS are reversed, the $\overline{x_q}$ controlling PMOS in the

pull-down branch can produce the same logic result as x_q controlling NMOS in the pull-up branch. Therefore, since the resistor R_1 is supposed to produce the opposite logic result for the pull-up and pull-down branches, the control signal for both branches should be the same. However, since the pull-up branch has a power supply of 2.4V and a ground of 1.2V while the pull-down branch has a power supply of 1.2V and a ground of 0V, the signal to drive transistor M_1 and M_4 has different power supplies and grounds and that's why we have denote them differently: signal x_{iu} that is used to drive transistor M_1 has power supply of 2.4V and ground of 1.2V while signal x_{id} that is used to drive transistor M_4 has a power supply of 1.2V and a ground of 0V. Also, since the drain of the transistor always has the opposite polarity as its gate, we have inserted an inverter in between transistor M_1/M_4 and signal x_{iu}/x_{id}. Different from the equivalent resistor model, there is a NMOS transistor having its drain, gate and source connected to the drain of M_1, gate of M_1 and 1.2V respectively and there is a PMOS transistor having its drain, gate and source connected to the drain of M_4, gate of M_4 and 1.2V respectively. Since M_1 and M_4 will have their drains floating when they are off, the two transistors mentioned above will keep the drain of transistors M_1 and M_4 at 1.2V when those two are off.

Third, the two sets of four resistors in the pull-up and pull-down branches can be represented by a set of four PMOS transistors and a set of four NMOS transistors respectively. Both sets of four transistors have a length ratio of 8 to 4 to 2 to 1, which is inversely proportional to the resistance of the four resistors that they represent. Also, both sets of four transistors have their sources connected to a 1.2V power supply.

The inputs of those two sets of four transistors, however, can not directly feed signals such as $a_{i,3:0}$ or $b_{i,3:0}$ since as mentioned before, we need to disable precise tuning when the logic is either "11" or "00" so as to not sacrifice extinction ratio for voltage tuning. If we use the XOR gate logic $VT\_EN = B_1 \bigoplus B_0$ to represent voltage-tuning disable signal VT_EN, VT_EN will become logic "0" when voltage tuning should be disabled.

For the pull-up branch, the control signals for those four PMOS transistors can be ex-

pressed by the following logic:

$$\overline{\overline{a_{i:3:0}} + \overline{VT\_EN_u}} \tag{6.8}$$

where the logic can be realized using a NOR gate.

Since the NOR gate is used in the pull-up branch, its power supply and ground should be 2.4V and 1.2V respectively. At the same time, the two inputs of the NOR gate should also have the 2.4V as power supply and the 1.2V as ground and that's why we denote voltage tuning disable signal for the pull-up branch as $\overline{VT\_EN_u}$.

As for the pull-down branch, the control signals for those four NMOS transistors can be expressed as the following logic:

$$\overline{b_{i:3:0} \wedge VT\_EN_d} \tag{6.9}$$

where the logic can be realized using NAND gate.

Since the NAND gate is used in the pull-up branch, its power supply and ground should be 1.2V and 0V respectively. At the same time, the two inputs of the NOR gate should also have 1.2V as the power supply and 0V as the ground and that's why we denote the voltage tuning disable signal for the pull-up branch as VT_EN_d.

All the circuits mentioned above can be found in the equivalent circuits as shown in Fig. 6.5. On the other hand, there are other circuits implemented so as to satisfy the circuit design requirements. Since the voltage between power supply and ground is 2.4V, the voltage close to 2.4V will be added to either transistor M_1 or M_4 if transistors M_2 and M_3 don't exist. Thus, transistors M_1 or M_4 will be close to their avalanche limit since their transistor nominal voltage is only 1.2V. Therefore, we need to insert a PMOS transistor M_2 to the pull-up branch and a NMOS transistor M_3 to the pull-down branch so that two transistors

in either branch will be turned on at the same time to share 2.4V together.

There are two edge-triggered pulse generating circuits that are connected to the gate of transistor M_2 and M_3. The purpose is to keep the V_{DS} of the transistor M_2 and M_3 within the technology nominal power supply voltage so that there will not be V_{DS} overstressing with the cascode transistors [71].

Let's first look at the edge-triggered pulse generating circuit at the gate of transistor M_2. Although it is driving the pull-up branch, the power supply and the ground of the edge-triggered pulse generator is 1.2V and 0V respectively. When x_{id} is either constant "1" or "0", the edge-triggered pulse generator output is always logic "1", which is 1.2V. However, when x_{id} changes its logic level, the generator output will change: when x_{id} changes from logic "1" to logic "0", its output will stay logic "1" due to the NAND gate; when x_{id} changes from logic "0" to logic "1", this signal will directly go to the input of NAND gate and thus, its output will jump to logic "0". But after the logic "0" passes the inverter and becomes logic "1" at another input of NAND gate, its output will return to logic "1". Therefore, when x_{id} jumps from logic "0" to logic "1", the generator output will have a dip at 0V. Since x_{id} jumping from logic "0" to logic "1" will make the pull-up branch turned on, the dip at 0V will increase the voltage V_{SG} of transistor M_2 and makes charging the loading with the pull-up branch faster.

Let's then look at the edge-triggered pulse generating circuit at the gate of transistor M_3. Although it is driving the pull-down branch, the power supply and the ground of the edge-triggered pulse generator are 2.4V and 1.2V respectively. When x_{iu} is either constant "1" or "0", the edge-triggered pulse generator output is is always logic "0", which is 1.2V. However, when x_{iu} changes its logic, the generator output will change: when x_{iu} changes from logic "0" to logic "1", its output will stay logic "0" due to the NOR gate; when x_{iu} changes from logic "1" to logic "0", this signal will directly go to the input of NOR gate and thus, its output will jump to logic "1". But after the logic "0" passes the inverter and becomes logic "1" at another input of NOR gate, the output of NOR gate will return

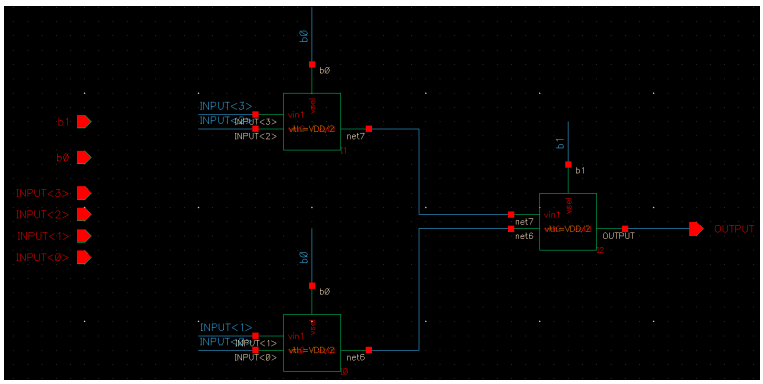

Figure 6.9: Ideal 4-to-1 Selector Schematic

to logic "0". Therefore, when x_{iu} jumps from logic "1" to logic "0", the generator output will have a jump at 2.4V. Since x_{iu} jumping from logic "1" to logic "0" will make pull-down branch turned on, the jump at 2.4V will increase the voltage V_{GS} of transistor M_3 and makes discharging the loading with pull-down branch faster.

After finishing the design of voltage-mode driver, we can use its input and output signals to design the other circuits in the transmitter.

Let's first look at the inputs of the proposed driver. Among all the input signals of the driver, only $\overline{a_{i,3:0}}$ and $b_{i,3:0}$ are DC signals while x_{iu}, x_{id}, VT_EN_d and $\overline{VT\_EN_u}$ are all depending on the two uncorrelated input NRZ data streams B_1 and B_0, which are dynamic signals instead. Therefore, we don't need to build a circuit to generate the DC signals $\overline{a_{i,3:0}}$ and $b_{i,3:0}$. Since there are totally three drivers in order to drive three phase-shifters, the same can be applied to $\overline{a_{j,3:0}}$, $b_{j,3:0}$, $\overline{a_{k,3:0}}$ and $b_{ik,3:0}$.

As mentioned before, signal x_{id} and x_{iu} share the same waveform but have different power supply and ground. Therefore, we don't have to generate two separately. Instead, we can use level shifter to shift their power supply and ground separately, which is what we have done in chapter 7. The same can be done for signal VT_EN_d and $\overline{VT\_EN_u}$ but we also have to realize their opposite polarities. Therefore, all we need to do is to generate either x_{id} or x_{iu}, VT_EN_d or $\overline{VT\_EN_u}$ and then level-shift the outputs of those signal generators. Since the ground is usually assigned as 0V, we have chosen to generate signals x_{id}, VT_EN_d and

$\overline{VT\_EN_d}$, which have 1.2V as their power supply and 0V as their ground.

The logic to realize signal x_{id} can be seen in Fig. 6.6, where a 4-to-1 selector is required. In my ideal circuit, the 4-to-1 selector will be realized using blocks from library "ahdlLib" provided by Cadence. The block diagram of the 4-to-1 selector can be seen in Fig. 6.9. All three blocks used are the cell analog_mux with their parameters vth set as half the power supply 1.2V. The PRBS signals are fed to the port "vsel" while the DC input signals for the selectors such as c_i or d_i are fed to the port vin1 and vin2. The block diagram of the three 4-to-1 selectors, which represent the ideal schematic of those in Fig. 6.6, can be seen in Fig. 6.10. We have created a cell named PLUT (programmable logic under test) to include those three 4-to-1 selectors. Its inputs include two uncorrelated PRBS signals and six DC codes to represent c_i, c_j, c_k, d_i, d_j and d_k. Its outputs include three 4-to-1 selectors output x_i, x_j and x_k.

Even though the PLUT design is ideal, we have to implement D-type flip-flops to align its three outputs as shown in Fig. 6.11 in order to reduce simulation-induced glitches. The block is from the library "ahdlLib" and its cell name is "d_ff". The outputs of PLUT will be connected to the port D of the D-type flip-flop. Three outputs of the PLUT will be aligned by the clock signal CLK, which has the same power supply and ground as other signals. Also, in order to maximize safety margin for alignment, clock signal will be shifted by half the period of data rate comparing to the two PRBS signals. For example, if the data rate is 12.5G, the time shift for the clock is will be 1/25G.

As mentioned before, although we have generated the signal x_{id}, we have to generate the signal x_{iu}, which requires a level shifter. But in my ideal circuit, the cell d_ff can shift its output power supply and ground by setting parameters like vlogic_high and vlogic_low differently. Therefore, we put another ideal d-type flip-flop at the outputs of PLUT and set their parameters differently to perform level-shifting without introducing skew. As a result, the parameters of the cell d_ff for generating x_{id} will be assigned as follows: vlogic_high is set as 1.2V, vlogic_low is set as 0V, vtrans_clk is set as 0.6V, vtrans is set as 0.6V, tdel is

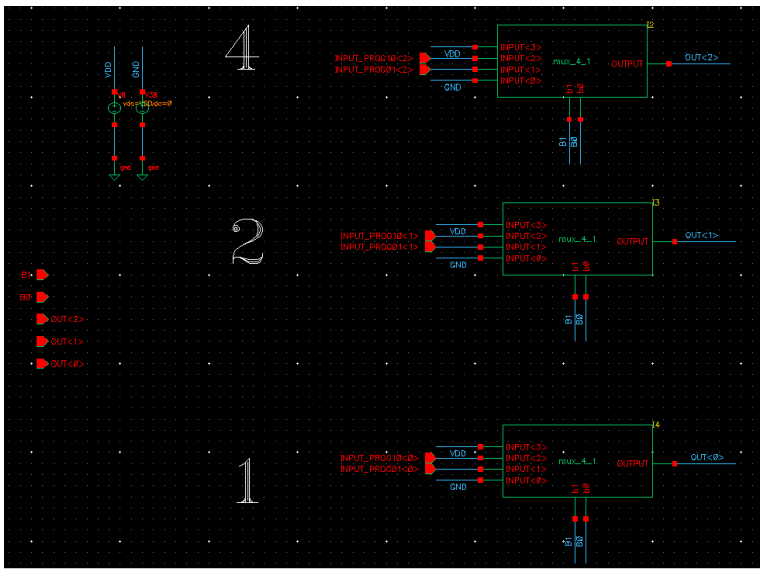

Figure 6.10: Ideal Block for the Three Selectors

set at 0, trise and tfall are set as 5p. The parameters of the cell d_ff for generating x_{iu} will be assigned as follows: vlogic_high is set as 2.4V, vlogic_low is set as 1.2V, vtrans_clk is set as 0.6V, vtrans is set as 0.6V, tdel is set at 0, trise and tfall are set as 5p. Consequently, there are six d-type flip-flops connected to the three outputs of PLUT and their output port Q will be connected to the driver inputs.

The ideal circuit for generating voltage tuning disable signal can be seen in Fig. 6.12. The XOR gate uses the cell xor_gate from ahdlLib and has its parameters set as follows: vlogic_high is set as 1.2V, vlogic_low is set as 0V, vtrans is set as 0.6V, tdel is set at 0, trise and tfall are set as 5p. Its two input signals are two uncorrelated PRBS signals. After the XOR gate, there are two ideal d-type flop-flops connected and their parameters setting is the same as those after the PLUT. Unlike x_{id} or x_{iu}, VT_EN_d and $\overline{VT\_EN_u}$ have different polarities besides having different power supply and ground. Having different power supply and ground makes using two d-type flip-flops at the output of XOR gate necessary. Signal VT_EN_d can be generated at the port Q of the lower d-type flip-flops while signal $\overline{VT\_EN_u}$ can be generated at the port $\overline{Q}$ of the upper d-type flip-flops.

It is worth noting that the implementation of the d-type flip-flop can also align the three

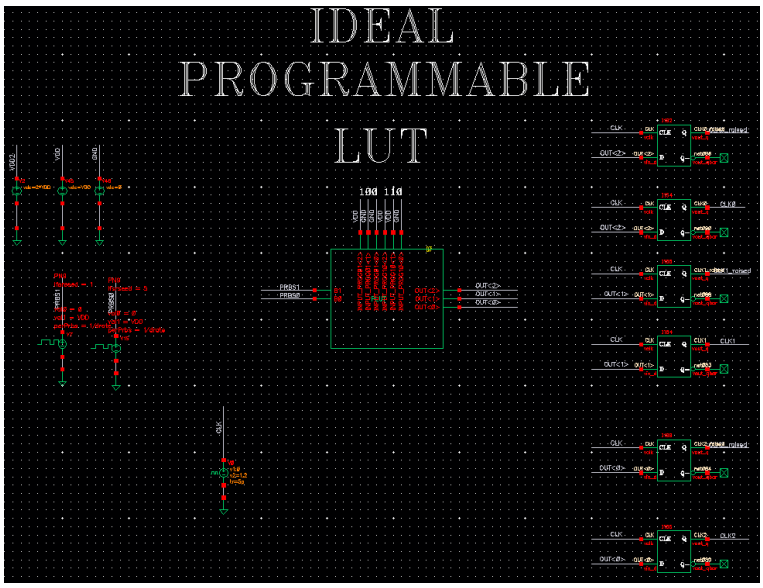

Figure 6.11: Ideal PLUT and its Alignment Circuit

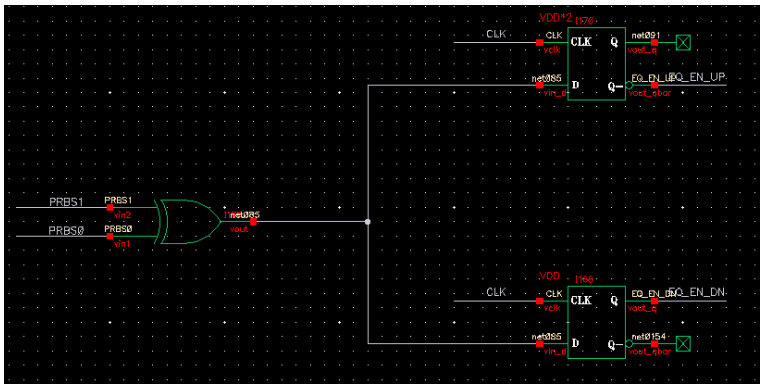

Figure 6.12: Ideal Voltage-Tuning Disable Signal Generator

outputs of PLUT as well as the voltage-tuning disable signal. It is important because all of those signals are injected at the same plane of the driver and their skew should be minimized.

After the implementation of driver input signal generation circuits is finished, we can have a look at the circuits that are connecting to my proposed voltage-mode drivers.

First of all, the three drivers will directly connect to the bondwire. In order to verify the proposed scheme only, we have chosen to set the inductor L_{wire} as 0H, which won't affect the driver schematic design at all. On the other hand, we have set the capacitor C_{pad} as 70fF, which is important since it will affect the driver circuit design.

After the bondwire, the three output signals of the drivers are connected to the three

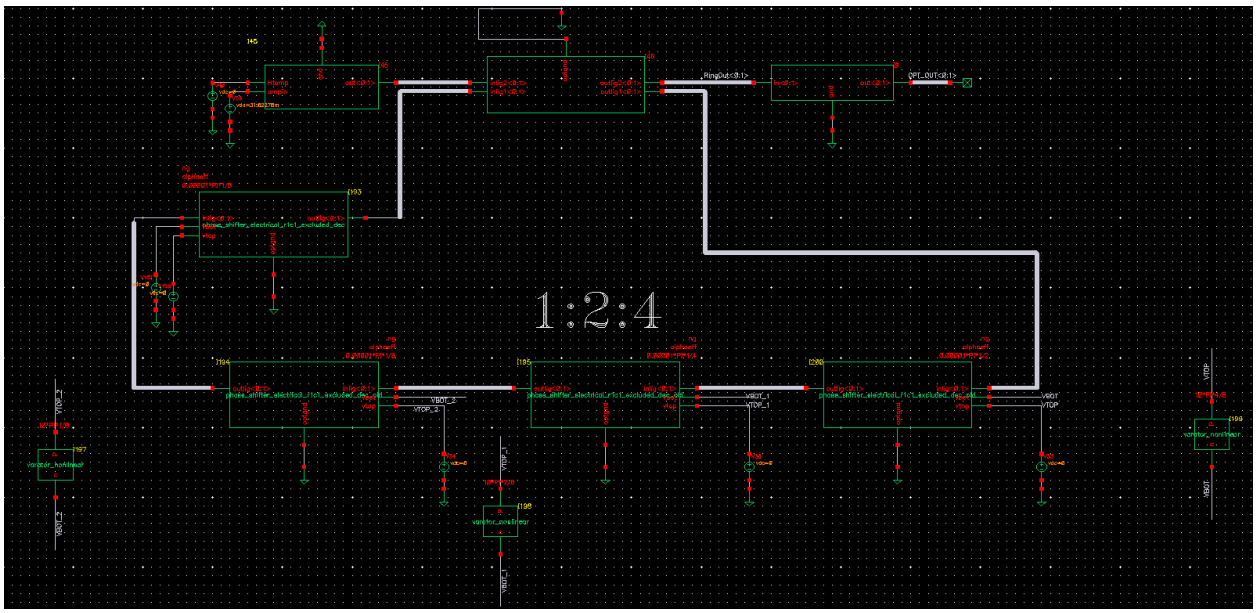

Figure 6.13: Three-Segment Microring Modulator Schematic

phase-shifters of the three-segment microring modulator, which can be seen in Fig. 6.13. Since the microring modulator is working in the depletion mode, its biasing voltage will never be bigger than zero. Granted that my drivers will only supply voltages that are bigger than zero, their output voltages will be applied to the cathodes of the three phase-shifters while the anodes of those phase-shifters are grounded as 0V. As mentioned in the modeling, the gap between three phase-shifters is modeled using a single phase-shifter with both its anode and cathode grounded. In my design, we did not implement all of the electrical model of the phase-shifter into a single block. Instead, its nonlinear varactor part of the electrical model is singled out and is modeled as block varactor_nonlinear. Since the capacitor inside of the nonlinear varactor model is voltage-dependent and is also sensitive to the polarities of the biasing voltage, we have to connect its anode and cathode to the anode and cathode of the phase-shifter model respectively. On the other hand, since the gap modeled by the phase-shifter won't be biased by the driving output and is actually biased by the DC voltage, we don't have to add nonlinear varactor model to it. Also, if we are only going to use the three-segment microring modulator model to derive the DC transmission curve, we don't have to add the nonlinear varactors since it will be open circuit under DC biasing condition.

Thus, only when we need to perform transient simulation, we need to add the nonlinear varactor model to the phase-shifter model.

6.4 Schematic Simulation Result using TSMC 65nm Technology and its Adaptability Analysis

In order to verify that my scheme and transmitter design can achieve equispaced optical PAM-4 signal at the output of the proposed three-segment microring modulator, we must derive the eye-diagram of the optical power output of the MRM so that transient simulation is required. Thus, we will discuss the parameters used in my transient simulations in order to derive equispaced optical PAM-4 signals.

First, there are two power supplies: 2.4V and 1.2V. There is only one ground, 0V. The two PRBS signals are set as follows. Both of them have 0V as their zero value and 1.2V as their one value. Their bit periods are both 1/12.5G with both of their rising time and falling time as 0.05/12.5G. Their transition reference is set as 10 to 90% and edge type set as halfsine. Their trigger type is internal and their LFSR mode is PN9. The first PRBS signal has the seed of 1 and the second PRBS signal has the seed of 5. The clock signal that is used to align three PLUT outputs and one XOR gate output is set as follows. Voltage 1 is set as 0V, voltage 2 is set as 1.2V, period is set as 1/12.5G, delay time is set as 1/25G, rise time and fall time is set as 5ps and pulse width is set as $1/25G - 10ps$.

Second, let's inspect the parameters used in the Verilog-A model for the three-segment microring modulator. Since the continuous laser power is going to use 1mW and DC voltage of the voltage source controlling the CW laser model is the square root of the power according to the CW laser Verilog-A model, the DC voltage is set as 31.62278mV. We have also set the voltage source controlling the port Htemp as 0V since we won't consider the temperature effect of the CW laser. The continuous-wave laser can generate different wavelengths and the parameter used to denote the specific wavelength is offsetfreq, which is set as -1108.6GHz.

The actually wavelength of the CW laser is the combination of both reference wavelength and offsetfreq, which is 1558.935um. The coupling coefficient of the coupler is set as 236.4m. There are four phase-shifter models used in the three-segment microring modulator Verilog-A model including three phase-shifters and one waveguide realized through phase-shifter model with both its anode and cathode grounded. All four phase-shifter models have the following parameters: group index n_g is set as 3.954, attenuation coefficient alphaeff is set as 1119.193, effective index at reference wavelength 1550nm is set as 2.5019019, capacitance coefficients ct0 and ct2 are set as 5e-15 and 1.7507e-09 respectively and resistance coefficient rt2 is set as 0.043354. The length L for the three phase-shifters with their length ratio as 1 to 2 to 4 is set as $0.00001 * \pi * 1/8$, $0.00001 * \pi * 1/4$ and $0.00001 * \pi * 1/2$ respectively where π is the global parameter set in the v̇ams constant file. The gap modeled using the zero biasing phase-shifter model has a length L of $0.00001 * \pi * 1/8$. The three varactor models have the same resistor parameter r set as 2042.04 and its length L is set to be the same as the phase-shifters that they are connecting to.

Third, here is the setting for transient simulation. Since the frequency offset is as high as -1108.6G, the accuracy setting even at that conservative level can't be precise enough. Therefore, we have to set the maxstep in the transient simulation setting to be as low as possible without slowing down the simulation too much. In my simulation, we have set the maxstep as 0.01ps, which is equivalent to the frequency of 100THz and is much higher than the absolute value of my offset 1108.6G. Also, in order for my simulation to be able to settle, we have set the stop time of my simulation to be 100ns, which is equivalent to 1250 periods of data rate. Since the simulation where the transmitter is not settled is not as important, we have set the parameter "outputstart" as 50ns, which can help us to save the hardware required to perform simulations.

The final simulation result can be seen in Fig. 6.14. The optical power output for the four levels are 131.5uW, 94uW, 55.21uW and 15.47uW respectively. One of the criteria of equispaced optical levels is the level separation mismatch ratio R_{LM} and in our case, it can

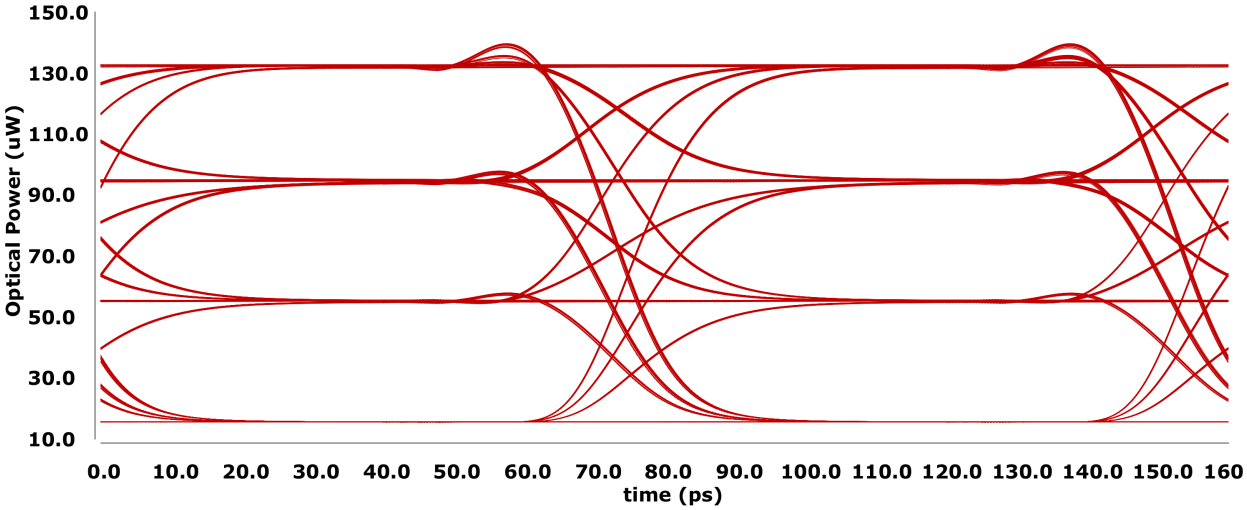

Figure 6.14: Ideal Transmitter Eye-Diagram at Symbol rate 12.5GS/s

be derived as shown in (6.10):

$$R_{LM} = \frac{131.5 - 94}{131.5 - 15.47} = 97\% \tag{6.10}$$

Thus, my scheme can achieve high percentage of level mismatch ratio. The extinction ratio in my simulation result is 9.3dB.

The above simulation result is realized through lower "1" tuning scheme with $a_{i,3:0}$ = "0000", $a_{j,3:0}$ = "1111" and $a_{k,3:0}$ = "0000". Also, $|T_{10}|^2$ is mapped to $|T_{110}|^2$ and $|T_{01}|^2$ is mapped to $|T_{100}|^2$.

One of the benefits of my proposed scheme is its ability to tolerate optical device fabrication nonideality. Therefore, we can change the parameters of the three-segment microring modulator model to test the adaptability of my scheme. Although there are a lot of parameters such as coupling coefficient, group index, effective index at the reference wavelength, changing them will only scale the optical output power of the microring modulator and thus, they won't affect the parameters such as $a_{i,3:0}$, $a_{j,3:0}$ or $a_{k,3:0}$ or the mapping results from either $|T_{10}|^2$ or $|T_{01}|^2$.

Therefore, in my design, we will instead examine the effect of length variation for the

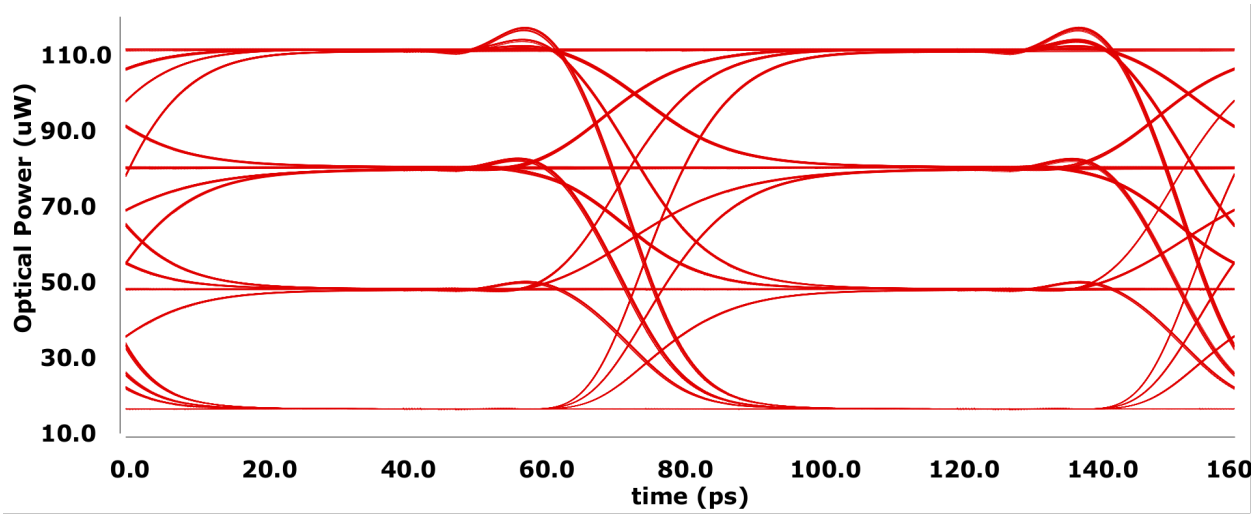

Figure 6.15: Ideal Transmitter Eye-Diagram For the Second Variation at Symbol rate 12.5GS/s

three phase-shifters, where the total length of the microring is the same but each phase-shifters inside have different lengths. We have proposed two variations: the first has three 10% longer phase-shifters and the second has three 10% shorter phase-shifters. The first variation with longer phase-shifters has three phase-shifters with length of 10
$pi \times \frac{1.1}{8}$, $10\pi \times \frac{1.1}{4}$, $10\pi \times \frac{1.1}{2}$ respectively and one waveguide with length of $10\pi \times \frac{3}{80}$, all in the unit of μm. The second variation with shorter phase-shifters has three phase-shifters with length of $10\pi \times \frac{0.9}{8}$, $10\pi \times \frac{0.9}{4}$, $10\pi \times \frac{0.9}{2}$ respectively and one waveguide with length of $10\pi \times \frac{17}{80}$, all in the unit of μm.

The final simulation result for the second variation can be seen in Fig. 6.15. The optical power output for the four levels are 110.7uW, 79.7uW, 48.1uW and 16.3uW respectively. One of the criteria of equispaced optical levels is the level separation mismatch ratio R_{LM} and in my case, it can be derived as shown in (6.11):

$$R_{LM} = \frac{110.7 - 79.7}{110.7 - 16.3} = 98.5\% \tag{6.11}$$

Thus, my scheme can achieve a high percentage of level mismatch ratio. The extinction

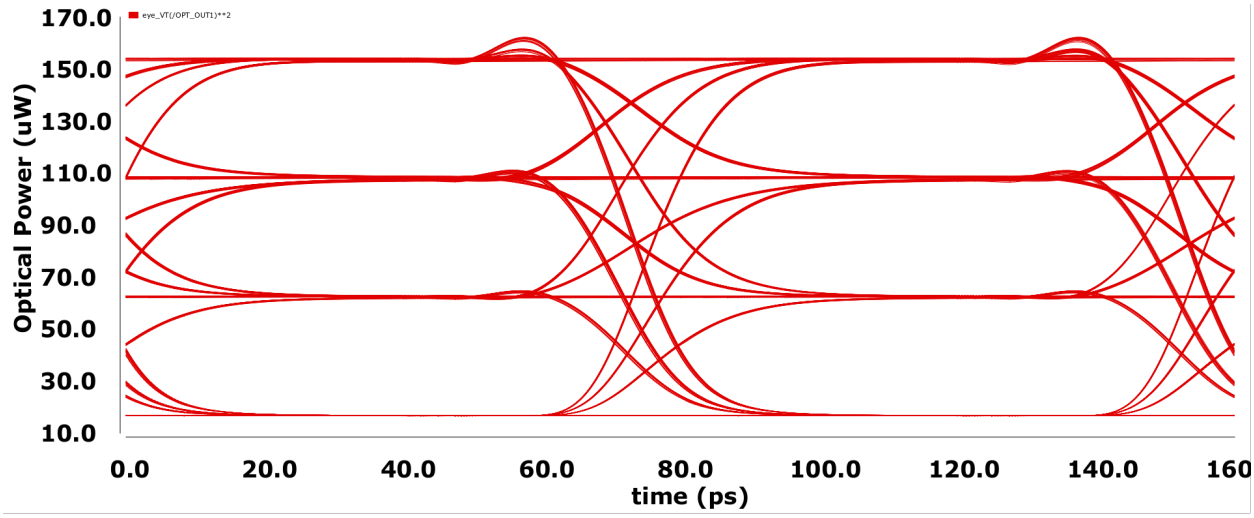

Figure 6.16: Ideal Transmitter Eye-Diagram for the First Variation at Symbol rate 12.5GS/s

ratio in my simulation result is 8.3dB.

The above simulation result is realized through lower "1" tuning scheme with $a_{i,3:0}$ = "0000", $a_{j,3:0}$ = "1111" and $a_{k,3:0}$ = "0000". Also, $|T_{10}|^2$ is mapped to $|T_{110}|^2$ and $|T_{01}|^2$ is mapped to $|T_{100}|^2$.

The final simulation result for the first variation can be seen in Fig. 6.16. The optical power output for the four levels are 152.7uW, 107.4uW, 62.5uW and 15.6uW respectively. One of the criteria of equispaced optical levels is the level separation mismatch ratio R_{LM} and in my case, it can be derived as shown in (6.12):

$$R_{LM} = \frac{107.4 - 62.5}{131.5 - 15.6} = 98.2\% \tag{6.12}$$

Thus, my scheme can achieve high percentage of level mismatch ratio. The extinction ratio in my simulation result is 9.9dB.

The above simulation result is realized through lower "1" tuning scheme with $a_{i,3:0}$ = "0000", $a_{j,3:0}$ = "1111" and $a_{k,3:0}$ = "0010". Also, $|T_{10}|^2$ is mapped to $|T_{110}|^2$ and $|T_{01}|^2$ is mapped to $|T_{100}|^2$.

Chapter 7: Transmitter Design Based on Proposed Scheme

7.1 Transmitter Structure Overview

In the previous chapter, we discussed the proposed scheme for using three-segment microring modulator to realize equispaced optical PAM-4. In order to verify the scheme, we implemented the voltage-mode driver design in the transistor level and other parts of the transmitter using ideal building blocks from ahdl library. Although the method above is useful for verifying my proposed scheme, it did not show that my scheme can be successfully implemented in the circuits. Therefore, we have to further justify the proposed scheme by implementing the circuit design for the whole transmitter besides the voltage-mode driver. The final transmitter structure block diagram for driving three-segment microring modulator after replacing ideal circuit models with nonideal circuit designs can be seen in Fig. 7.1.

Although there are three voltage-mode drivers for driving three segments of the microring modulator, each driver and the circuits that are supplying its inputs such as its predriver and 4-to-1 selector share the same circuit structure and thus, only one of the drivers and its corresponding inputs supplying circuits need to be shown in order to clarify the transmitter structure without making the transmitter block diagram too hard to read. As a result, in my transmitter block diagram, we are showing a generic path [q] to represent one of three paths and thus, $q = 1, 2, 3$. For each path [q], voltage V_q will be generated to drive one of the three phase-shifters from my proposed three-segment MRM. Each path contains one voltage-mode driver, two inverter-based predrivers, two CML-to-CMOS converters, one CML 4-to-1 selector and one CML D-type flip-flop. Since the function of other circuits is to provide input signals for the driver, the whole structure of the transmitter is based on the drivers themselves. Therefore, the transmitter design is usually starting from its driver and then continues with the circuits that are providing its input signals.

The driver has CMOS logic inputs x_{qu} and x_{qd} along with two 4-bit DC inputs $a_{q,3:0}$ and $b_{q,3:0}$. On the other hand, the two uncorrelated NRZ streams B_1B_0, acting as selecting signals for 4-to-1 selectors in order to realize coarse tuning, come from external Bit-Error-

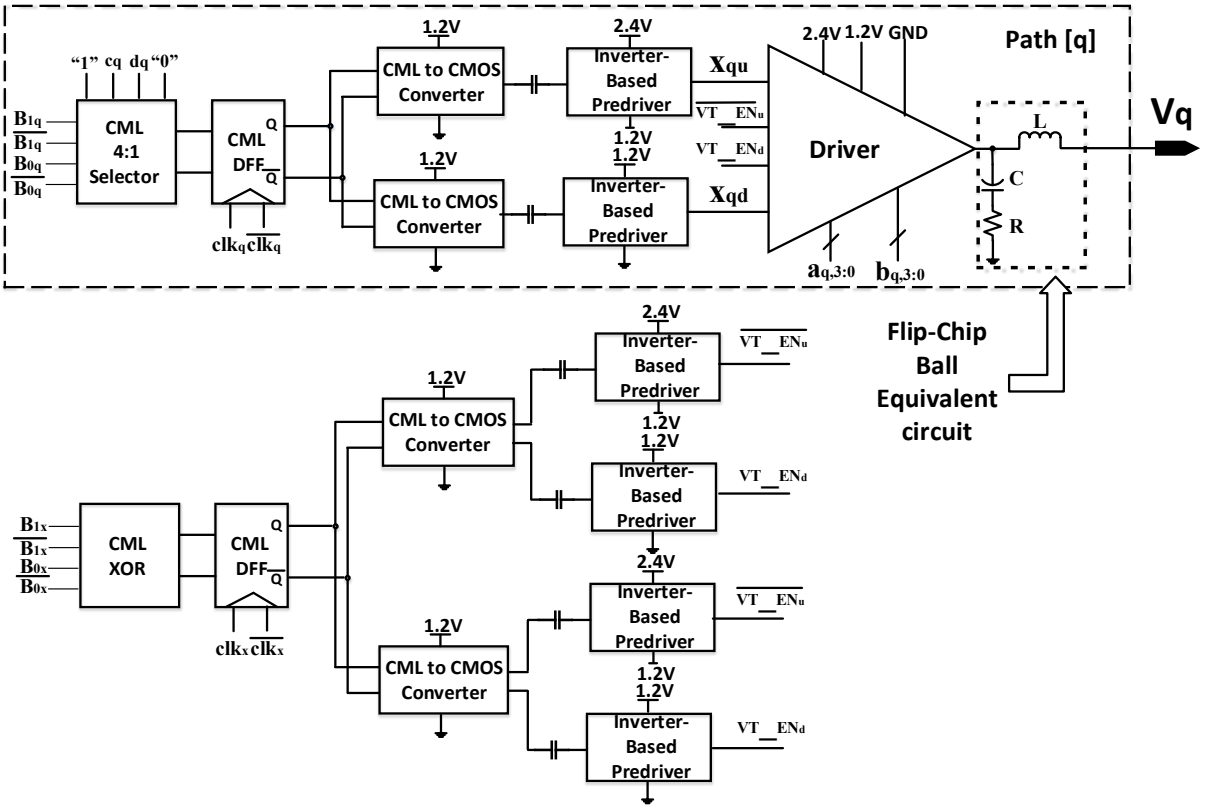

Figure 7.1: Transmitter Block Diagram

Rate-Tester(BERT). Although regular BERT will provide signals with different logic output, the only logic that is able to achieve data rate as high as 12.5Gb/s has to be current-mode logic (CML). Since the drivers' inputs are CMOS logic, we can add CML-to-CMOS directly after the input CML signals from BERT. However, we have to implement 4-to-1 selectors using inverters, which are not able to achieve data rate as high as 12.5Gb/s. As a result, the 4-to-1 selector has to use CML logic and there has to be a CML-to-CMOS converter before the driver and after the selector. The driver sets V_{max} as 2.4V, V_{DD1} as 1.2V and V_{min} as 0V while all the circuits with CML logic including CML-to-CMOS converter use 1.2V as their V_{DD} and 0V as their ground.

There are two pairs of binary inputs for the driver. The first pair, x_{qu} and x_{qd}, comes from the output of CML-to-CMOS converter. Since x_{qu} and x_{qd} drives the pull-up and pull-down branch of the driver respectively, they should share the same waveform but have different

power supply and ground: x_{qu} has a power supply voltage of 2.4V and uses 1.2V as its ground while x_{qd} has a power supply voltage of 1.2V and uses 0V as ground. Also, inverter-based predriver has to be inserted after CML-to-CMOS converter so that there will be enough driving capacity for the driver inputs. To drive both pull-up and pull-down branch of the driver, we have used two predrivers: one with 2.4V as power supply and 1.2V as ground and one with 1.2V as power supply and 0V as ground. By putting ac-coupling capacitors before two predrivers with different power supplies and grounds, their respective CML-to-CMOS converters can share the same power supply and ground, 1.2V and 0V respectively. Therefore, ideally, we can use one CML-to-CMOS converter for each path since it has the same power supply and ground for driving pull-up and pull-down branch. However, due to the ac-coupling capacitor used in front of inverter-based predriver, the output of the single CML-to-CMOS converter will be connecting to two ac-coupling capacitors, which will result in charge sharing between those two connected capacitors since the two predrivers connecting to those two capacitors have different power supplies and grounds. In order to avoid charge sharing mentioned above, we have used one CML-to-CMOS converter for each predrive even though they have the same power supply and ground.

Another pair of the driver input, VT_EN_d and $\overline{VT\_EN_u}$, are the signals for disabling precise tuning when two uncorrelated NRZ streams B_1B_0 are either "11" or "00". Due to the structure of the driver mentioned in the previous chapter, the binary input pair for disabling precise tuning as well as the binary input pair from the output of CML 4-to-1 selector has to arrive at the same plane of the driver at the same time. Thus, the path for creating precise tuning disabling signals has to share as many same block diagram as path [q] as possible in order to minimize the skew among all the binary input signals for the driver. Therefore, the block diagram, whose functions also include generating precise tuning disable signals, contains one CML XOR gate, CML D-type flip-flop, two CML-to-CMOS converters and four inverter-based predrivers. Although functionally we only need to use one inverter-based predriver for VT_EN_d and for $\overline{VT\_EN_u}$ respectively, their outputs have

to drive three drivers instead of one like the signal x_{qu}. As a result, we have chosen to add two more predrivers so that there will be enough driving capacities for three drivers without introducing extra loading to the signal path. As elaborated in the Section 7.2, CML XOR gate uses exactly the same structure as CML 4-to-1 selector and their only difference is the inputs, which has made CML XOR gate as the special case for CML 4-to-1 selector. As a result, both CML block will have the same skew and thus, the signal flow goes like this: two uncorrelated PRBS signals will pass through one CML 4-to-1 selector, one CML d-type flip-flop, one CML-to-CMOS converter, ac-coupling capacitors and inverter-based predriver before arriving at the inputs of the voltage-mode driver.

In the transmitter, there are three paths for driving three phase-shifters and one extra path for supplying the signals for disabling precise tuning. As mentioned above, we can make sure there are minimum skew between them by making each path both containing the same blocks and having the same loading. At the same time, there is another technique called synchronization implemented in my transmitter design in order to reduce jitter and even skew in the transmitter: inserting a CML D-type flip-flop before CML-to-CMOS converter and after either a CML 4-to-1 selector or a CML XOR gate. By inserting a CML D-type flip-flop before two parallel CML-to-CMOS converters and after either one CML 4-to-1 selector or one CML XOR gate, the signal outputs coming from three CML 4-to-1 selectors and one CML XOR gate can be aligned or synced by a clock signal applied to the inputs of CML d-type flip-flop. If we let those four CML blocks themselves to define their own skew and jitter, those two nonidealities will be affected by process variations and even in some cases can be signal dependent. Instead, clock synchronization technique can make final outputs only dependent on clock signal alone. At the same time, the CML d-type flip-flop can reduce their outputs jitter. As can be seen in the simulation result, my proposed CML 4-to-1 selector has non-negligible jitter since it is formed through the combination of three 2-to-1 selectors and that's why CML d-type flip-flop is even more necessary in my specific transmitter design. In order to reliably realize the synchronization technique, the most crucial element is to

generate "clean" clock signals CLK_q where $q = i, j, k, x$ for the CML D-type flip-flop since any nonideality of this clock signal will directly affect the CML D-type flip-flop output. The "clean" clock signals can be achieved through robust design of clock distribution network. Also, it is worth noting that since the original clock signals also have to come from external BERT just as B_1B_0 and the delay between clock signal and B_1B_0 can be adjusted on the panel of BERT, that skew adjustment can be used to compensate for the system skew in my transmitter design. In my simulation, we can adjust the delay between my two uncorrelated PRBS signal generators and the synchronization clock signal generator, which is justified by the real-life application of BERT.

Just like clock signals CLK_q as the inputs for CML D-type flip-flops, two NRZ bit streams B_{1q} and B_{0q} where $q = i, j, k, x$ are the input signals for four CML circuits: three CML 4-to-1 selectors and one CML XOR gate. Additionally, their original signals CLK, B_1 and B_0 are all coming externally from bit-error-rate tester, BERT. As a result, we have chosen to implement two distribution networks, which is similar to the clock distribution network mentioned above, to generate B_{1q} and B_{0q} where $q = i, j, k, x$ respectively.

As for the heterogeneous connection between my proposed three voltage-mode drivers and three-segment MRM, we have chosen to implement flip-chip bonding in order to reduce more power consumption for driving optical modulator than using wirebonding as shown in the previous chapter. Therefore, we have added flip-chip ball equivalent circuit at the loading of each driver and values of circuit parameters R, L and C come from reference [72].

The remaining sections of this chapter will discuss the circuit implementation of each block in my proposed transmitter structure. The final section will discuss the extraction simulation results for my proposed transmitter design.

7.2 CML 4-to-1 Selector and CML XOR Gate

Even in deep sub-micron technology, such as $0.18\mu m$ and $0.13\mu m$ technology, the power supply will be as low as 1.2V. In the technology node such as 90nm and 65nm that we are

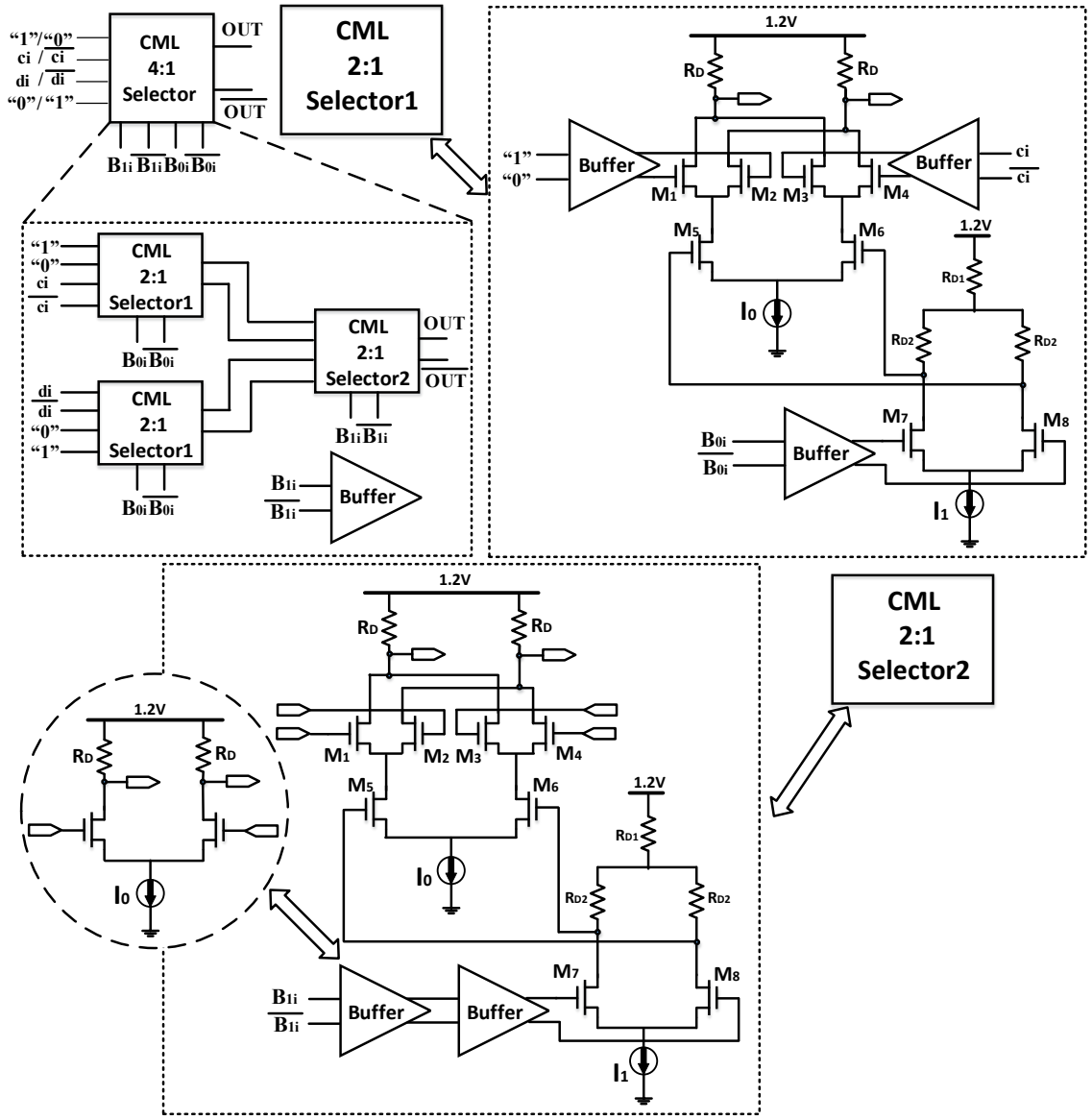

Figure 7.2: Current-Mode Logic 4-to-1 Selector Block Diagram

using in my design, its power supply can be as low as 1V. Furthermore, in my high speed interconnect application, the transistors are targeted to be biased in the region of velocity saturation, which can produce the highest bandwidth available to certain technology. As a result, voltage V_{DS} of the transistors, which are used in signal path of my proposed circuits, have to be as high as possible to maximize its speed and thus, the speed requirement and low supply voltages won't make it possible to stack more than four transistors from power

supply to ground.

Therefore, although we can in theory realize CML 4-to-1 selector with one circuit, we have chosen to implement CML 4-to-1 selector by combining three CML 2-to-1 selectors together, which is exactly the same as my proposed ideal 4-to-1 selector mentioned in chapter6. However, in non-ideal circuit design, there are several issues that are important for designers. First, three 2-to-1 selectors are not the same. The inputs for the first two 2-to-1 selectors are DC signals while the inputs of the sequential selector are the outputs of those first two 2-to-1 selectors. Thus, inputs of the sequential 2-to-1 selector can be either DC signals or dynamic signals and we have to design it accordingly. Second, the two uncorrelated PRBS signals can be interchangeable and the design of my selector should not be affected. However, from the block diagram of the 4-to-1 selector, we can see that the loading of the two PRBS signals are different. In high speed circuit, if the loading is different, the rise/fall time of the signals will be affected and the different rise/fall time will introduce more skew and jitter into my circuits. With the above two issues in mind, we have proposed the current-mode logic 4-to-1 selector as shown in Fig. 7.2, where two 2-to-1 selector1s sit at the front with their inputs provided off-chip by DC supply/ground and one 2-to-1 selector2 with its inputs fed by the outputs of two 2-to-1 selector1s.

As mentioned in the previous section about the transmitter design, all of the CML circuits will follow the same logic, which means that we assumed 1.2V as my CML logic "1" and 0.8V as my CML logic "0" with DC operating point as 1V. Since the outputs of the CML 2-to-1 selector1 control the input transistors M_1 to M_4 of the CML 2-to-1 selector2, they should share the same DC operating point 1V. Thus, the input transistors M_1 to M_4 of the CML 2-to-1 selector1 should also have the same DC operating point. Therefore, the DC inputs of CML 2-to-1 selector1 have to be converted by a buffer to CML logic before fed into the input transistors M_1 to M_4 of the CML 2-to-1 selector1. The buffer ends up having 400Ω loading resistor R_D and $1mA$ tail current I_0. The loading resistors and tail currents of the Gilbert cells inside both types of 2-to-1 selectors share the same value as those buffers.

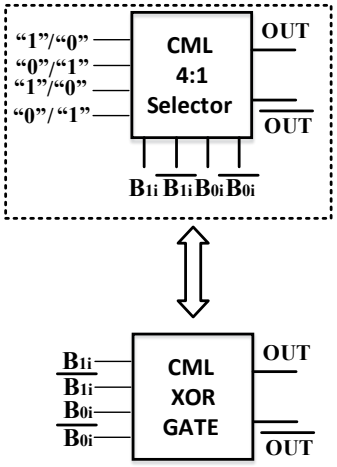

Figure 7.3: Current-Mode Logic XOR Gate Block Diagram

Since the drains of transistors M_5 and M_6 are connected to the sources of transistors M_1 to M_4, selecting signals B_{1i} and B_{0i} have to be shifted to lower DC operating point 0.7V before applying to transistor M_5 and M_6, which is realized by level-shifter with the loading resistor R_{D1} of 200Ω, R_{D2} of 350Ω and tail current I_1 of $1mA$. Due to limited voltage headroom, transistors from M_1 to M_8 are all low-threshold voltage transistors (lvt).

According to the schematic of CML 4-to-1 selector, selecting signal B_{0i} has passed through a level-shifter and a Gilbert cell before arriving at the inputs of CML 2-to-1 selector2, while selecting signal B_{1i} has only passed a level-shifter. Since signal B_{0i} and B_{1i} are synced, one buffer, which has the same delay as the Gilbert cell, has to be inserted after signal B_{1i} to compensate the skew.

However, different loading will also act as another source of skew: signal B_{0i} drives two level-shifters while signal B_{1i} only drives one buffer. Therefore, we have inserted one buffer after signal B_{0i} and added another one in cascade with the existing one after signal B_{1i}. Also, one dummy buffer is added directly after signals B_{1i}. As a result, both signal B_{1i} and B_{0i} drive two buffers.

According to the proposed transmitter structure, the outputs of both CML 4-to-1 selector and CML XOR gate has to be synced. Therefore, instead of proposing a different structure,

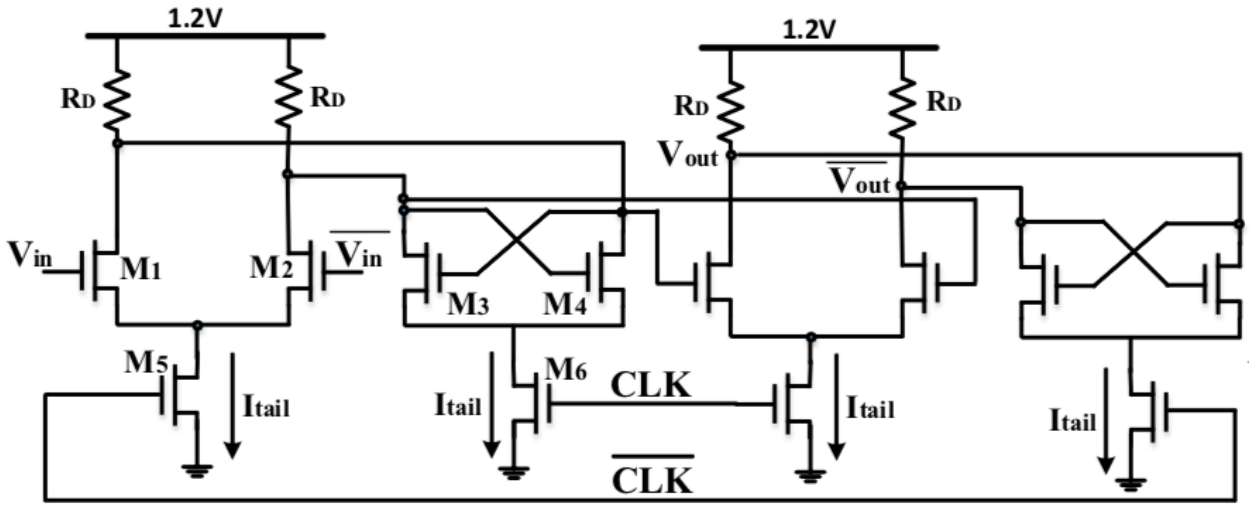

Figure 7.4: Current-Mode D-type Flip-Flop Schematic

we have implemented CML XOR gate using CML 4-to-1 selector as shown in Fig. 7.3 by using signal B_{1i} and B_{0i} as two selecting signals and using DC input "1", "0", "1" and "0" as four selector inputs, which corresponds to 1.2V, 0V, 1.2V and 0V respectively.

7.3 CML D-type Flip-Flop

As mentioned in the transmitter structure chapter, the d-type flip-flop is used to sync the output signals of three CML 4-to-1 selectors and one CML XOR gate since they will all go into the inputs of the drivers, which share the same plane and are supposed to align to avoid jitter and skew.

Logically, we can realize d-type flip-flop using only digital logic to reduce the power consumption of my transmitter, which is usually well-established and can even be done using only hardware description language(HDL). The only change we need to make in my transmitter design is to put the cml-to-cmos converter before d-type flip-flop. Besides, d-type flip-flop can even align the output of cml-to-cmos converters, whose skew and jitter will also be corrected. However, the data rate 12.5Gb/s cannot be achieved under 65nm technology. As a result, we have to implement current-mode logic instead although it will consume more power.

In my CML D-type flip-flip design as shown in Fig. 7.4, we have implemented the design where two CML D-latches are in cascade with the first D-latch synced by $\overline{CLK}$ and the second by CLK. The operation of d-type flip-flop works like this. When the signal $\overline{CLK}$ is high, the amplifier of the first d-latch is on and the signal from the output of either CML 4-to-1 selector or CML XOR gate will be amplified. Since the positive-feedback latch is off, the output of the amplifier will closely follow the outputs of either CML 4-to-1 selector or CML XOR gate depending on which block d-type flip-flop is following. At the same time, the amplifier of the second d-latch is turned off and thus, the unstable output (since it is following the changing inputs of first amplifier) won't be able to pass through the second d-latch. After the signal $\overline{CLK}$ becomes low, amplifier of the first d-latch will be turned off and thus, the signals from either CML 4-to-1 selector or CML XOR gate won't be able to pass through even the first d-latch. But the signal inputs at the moment when $\overline{CLK}$ becomes low will be further amplified, which is turned on by CLK and signals outputs of the first d-latch will reach my assigned CML logic level through positive feedback latch. Meanwhile, amplifier of the second latch will be turned on and its output will closely follow output of the first d-latch and amplifies it at the same time. However, the second latch will be turned off and thus, the output of the D-type flip-flop won't reach my assigned CML logic. Finally, after the signal $\overline{CLK}$ returns to high, the second positive-feedback latch will be turned on and the outputs of the d-type flip-flop will reach the assigned CML logic level. As a result, the d-type flip-flop will pass the signal from either CML 4-to-1 selector or CML XOR gate when the $\overline{CLK}$ jumps from low to high and that's why we call this d-type flip-flop rising edge triggered.

After understanding the timing and logic aspect of the CML d-type flip-flop, we will talk about its circuit design aspect. For each D-latch, transistor M_5 and M_6 with width of $10\mu m$ are switched by clock signals from 0 to $2 \times I_{tail} = 2.4mA$, which results in $0.24mA/\mu m$ current density, which is close to the peak f_T current density of n-MOSFETs.

Although my d-type flip flop is based on CML logic and we have assigned specific voltage

to its logic "1" and logic "0", we can make some changes to voltages as long as other parts of the circuits are not negatively affected. In fact, by changing its voltage, we will have some positive impact on my circuit design. In my specific design case, we have chosen to achieve larger single-ended output amplitude of $600mV_{pp}$. When larger amplitude is implemented, rise/fall time of the signal will also be reduced. In the noisy circuits, the smaller the rise/fall time, the less jitter will be produced due to the voltage variation. Since output of the CML d-type flip-flop is CML-to-CMOS converter, larger amplitude can facilitate the jitter reduction of CML-to-CMOS converter. Besides, since the d-type flip-flop can also realize amplification, we don't have to add an extra amplifier in order to achieve higher amplitude. The resulting loading resistor R_D is set as 250Ω. In order to improve the speed of the latch, we have also chosen transistors of different V_T for signal path and clock path: M_1, M_2, M_3 and M_4, which are in the signal path, are low-V_T transistors while M_5 and M_6, which are in the clock path, are high-V_T transistors. By using high-V_T transistors in the clock path, the input pair of amplifiers that feed the clock signals from the clock distribution network will be biased close to the velocity saturation region by having larger V_{DS}. As mentioned before, biasing transistors in the velocity saturation region will increase its bandwidth. Although its gain is sacrificed, requirement for the clock path is focusing on providing higher speed instead. By using low-V_T transistors in the signal path, larger g_m can be achieved with the same tail current and as a result, higher gain can be achieved with the same power consumption.

7.4 CML-to-CMOS Converter

Since the input PRBS signals from external equipment have to use CML logic in order to achieve speed as high as 10GHz and my voltage-mode driver inputs are designed to use CMOS logic, a CML-to-CMOS logic is inevitable. Functionally, the CML-to-CMOS converter is just an amplifier that is also able to level shift the DC operating point since the CMOS logic has DC operating point of 0.6V and single-ended amplitude of $600mV_{pp}$. However, unlike regular linear amplifier, CML-to-CMOS logic has no specific requirement for linearity. On

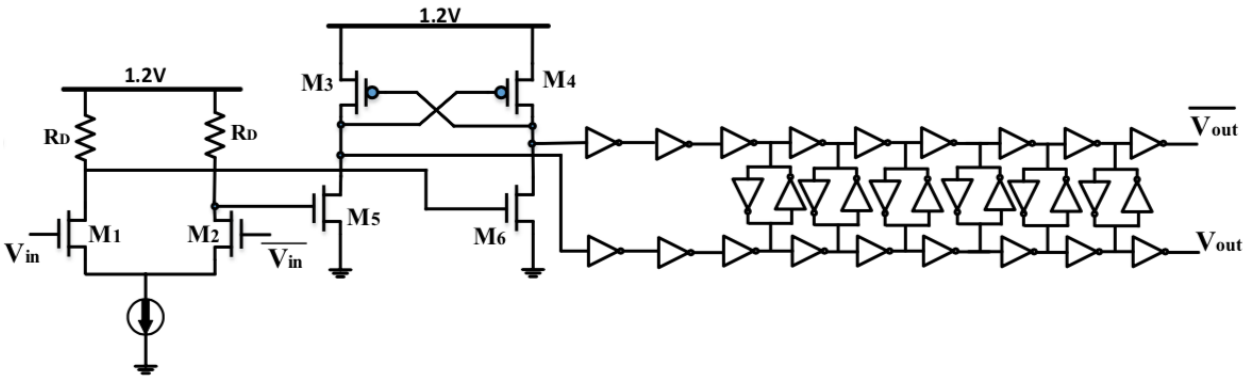

Figure 7.5: CML-to-CMOS Converter

the other hand, the CMOS logic does require low rise/fall time, which demands high skew rate of my design. Therefore, we can use regular linear amplifier for out CML-to-CMOS converter. But the power consumption is going to be too large and will also be a waste due to its low linearity requirement to begin with. Another way to realize amplification without using linear amplifier is to use positive feedback latch used in comparator circuit and my CML d-type flip-flop. Comparing with utilizing linear amplifier, the second method is more power efficient in my scenario.

Using the second method, my proposed CML-to-CMOS converter, as shown in Fig. 7.5, contains a linear amplifier, an inverter using Differential Cascade Voltage Swing Logic (DCVSL) and two inverter chains whose outputs are connected through six back-to-back inverter pairs.

Due to high DC operating point of the CML logic in my design and in order to ensure lower-jitter performance for CML-to-CMOS converter, we will further amplify the output signals from CML D-type flip-flop and also lower their DC operating point before feeding them into DCVSL so that the outputs of DCVSL can achieve rail-to-rail. Before the amplifier in the CML-to-CMOS converter, the DC operating point of the signals is 0.6V. If we directly pass this low DC voltage to the gates of DCVSL, transistor M_5 and M_6 are both turned off even at DC operating point, which will shift their drain voltages toward power supply instead of the ideal 0.6V. The amplifier, as a result, has its single-ended amplitude reaching

$800mV_{pp}$ with DC operating point of 0.8V.

After the amplification, we use DCVSL to convert CML logic to CMOS logic. This logic uses positive feedback latch as loading and its pull-down network (PDN) can be realized by two simple NMOS transistors which are driven by the differential outputs of the amplifier. Using this logic, the CML to CMOS converter output can reach the amplitude as large as rail-to-rail, which is essential to reduce the jitter of the inverter chains.

As shown in my transmitter schematic, only one of the differential outputs of CML to CMOS converter will be fed to the predrivers. Besides, upon arriving to the same output node of DCVSL, differential output signals of the amplifier will pass through different numbers of transistors and thus, the output of DCVSL transitioning from high to low is faster than the transitioning from low to high. Therefore, there will be duty cycle distortion after passing through DCVSL. To correct the duty cycle distortion, we have added another inverter chain at the other output of DCVSL and also added back-to-back connected inverters between those two inverter chains. Since the transition from high to low is always faster and two inverter chains after differential outputs of DCVSL have opposite polarities, the two back-to-back inverters that connect those two inverter chains can average out the skew between two transition states and thus correct the duty cycle distortion. In my design, we have chosen to add six of them along with nine inverters in cascade so that the output of the inverter chains has sufficient inverters to both correct the duty cycle and supply enough driving capacity for predrivers. It is worth mentioning that this decision is based on my extraction simulation result instead of schematic simulation results since only two will be needed in the latter case.

7.5 Clock and PRBS Signals Distribution Network

If we only perform the transmitter simulation using its schematic view, we don't have to design clock or prbs signal distribution network at all since there will be no distance between three 4-to-1 selectors and one XOR gate at all. However, since each CML logic block has large layout, there will be non-negligible delay between each one of them and it will become

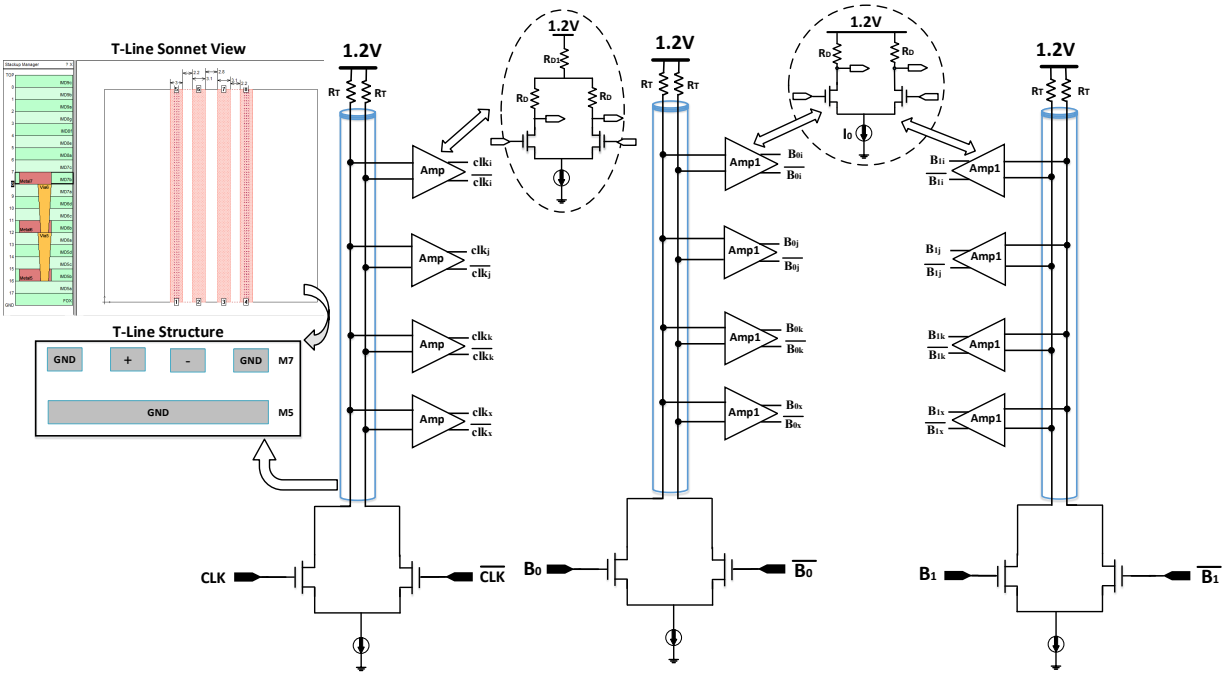

Figure 7.6: Clock and NRZ Bit Stream Distribution Network

even more significant when they are working under higher data rate. Besides, those four blocks are sharing the same PRBS and clock signals, which is the reason why a PRBS or clock signal distribution network is necessary for my transmitter design.

There are three types of clock distribution networks: transmission line, inverter chain and CML logic. Among these three, transmission line has the best balance between jitter and power dissipation and this is why we have chosen to implement it in my design. Also, the skew between different output nodes on the same transmission line will be minimized, which will result in minimizing the skew among CLK_q, B_{1q} and B_{0q} themselves where $q = i, j, k, x$. Therefore, the three distribution networks that are used to generate the clock signal CLK_q and two uncorrelated PRBS signals B_{1q}/B_{0q} where $q = i, j, k, x$ as mentioned in the transmitter design, are based on transmission line, which are shown in Fig. 7.6.

Differential clock signal inputs from external BERT are modeled by two 12.5GHz differential sine waves CLK and $\overline{CLK}$ with single-ended amplitude of $300mV_{pp}$ and DC operating point of 1V. The clock signals pass through an open-drain amplifier, which is used for dis-

tributing clock signals by driving transmission line as its loading. Normally, the T-Line is designed to have characteristic impedance of 50Ω and thus, we need to use 50Ω as the termination resistor for the T-Line in order to minimize reflection. However, with such low termination resistor, we need a significant amount of power to provide the same gain as using higher termination resistors. As a result, we use 125Ω as the termination resistor R_T to balance between power and reflection, which results in using $4mA$ in tail current so as to render the same gain and DC operating point as using $1mA$ tail current and 500Ω loading resistor. Since the transmission line is supposed to drive the tail transistors M5 and M6 of CML D-type flip-flop, we need four amplifier "AMP"s to both shift transmission line output DC operating point and further increase its amplitude. As a result, the final amplifiers have loading resistors R_{D1} of 50Ω, R_D of 334Ω and tail current of $1.5mA$, which results in single-ended output of $300mV_{pp}$ and DC operating point of 0.875V.

Two pairs of differential NRZ bit streams $B_1/\overline{B_1}$ and $B_0/\overline{B_0}$ from external BERT are modeled by two pairs of differential PRBS voltages with single-ended amplitude of $300mV_{pp}$ and DC operating point of 0.9V. Both bit streams using PN8 as their LFSR mode and $seed = 1$ but with B_0 delayed for 85 period compared to B_1. Unlike clock distribution network, there is no level shifting for NRZ bit stream distribution network and a simple buffer as shown in Fig. 7.6 is sufficient. The buffer, as a result, has the loading resistor R_D of 400Ω and the tail current of $0.75mA$.

The transmission line structure we have used in my design is differential microstrip with coplanar shields routed in metal 7 (M7) and metal 5 (M5). Instead of using Virtuoso to simulate transmission line effects too, we have implemented the following procedures using more specialized electromagnetics tool SONNET:

- Import the thickness/resistivity/dielectric constant of both dielectric layers and metal layers used in TSMC 65nm technology into the SONNET stackup manager.
- Build four parallel microstrips on metal 7 and one microstrip on metal 5. Then connect the outer two microstrips on metal 7 to the microstrip on metal 5 through multiple

vias since those three microscrips are all connected to ground. The placing of the vias needs to satisfy the DRC of TSMC 65nm technology.

- Design the widths for four microstrips and distances between them in order to render the characteristics impedance of the transmission line to be 50Ω.

- SONNET has provided N-coupled line model, which extracts the RLCG values for a unit length of a multi-conductor planar transmission line system and can produce RLGC matrix for Cadence Virtuoso Spectre. Using this model, we have created four input ports and four output ports for my transmission line, and the extraction result is exported as .dat file.

- Using mtline block from analoglib library, the extracted .dat file can be implemented in Cadence. In order to use it, we need to specify some CDF parameters: num of lines is set to be 4 and type of input is set to be RLGC. We can change the physical length according to my layout floorplan.

- In schematic, the reference ports of mtline are set to ground. Since each transmission line distribution network will drive four CML blocks, we are using five mtlines in cascade. For the mtline closer to the open-drain amplifier, its two inner inputs are connected to the drains of open-drain amplifier, and two outer ports are connected to the ground. For the mtline closer to the termination resistors R_T, which are three terminal n+ poly resistor with salicide, its two inner inputs are connected to two termination resistors, and two outer ports are connected to the ground terminals of the termination resistors. Other three mtlines will be connected with each other by corresponding ports.

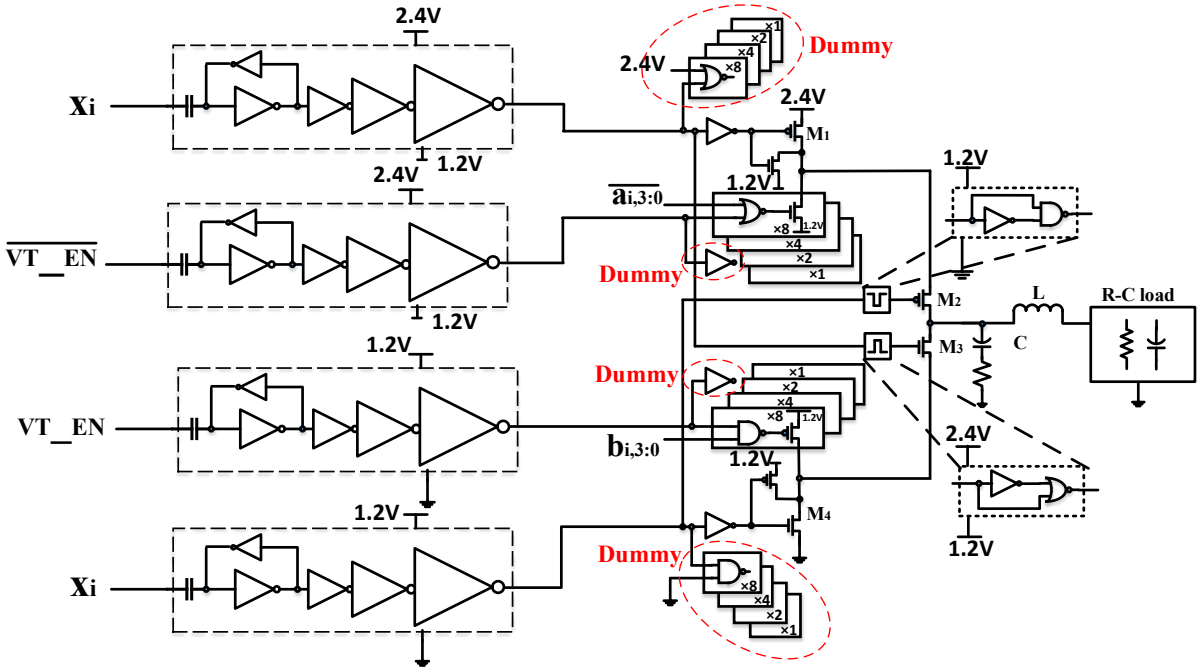

Figure 7.7: Driver and Predriver Schematic

7.6 Predriver and Driver

After the CML-to-CMOS converter, the high-speed signal has become CMOS logic instead of CML logic and thus, we can add digital circuits right after the CML-to-CMOS converter instead of analog circuits to save energy consumption of my proposed transmitter. Although inputs of the proposed voltage-mode driver, other than the DC codes, follows the CMOS logic, we can't directly feed the output signals from the CML-to-CMOS logic to those inputs of the driver for the following reasons. First, although those CMOS logic inputs for the driver have the same amplitude of 1.2V and they also share the same waveform, they have different power supplies and grounds for pull-up branch and pull-down branch. That's why we will need level-shifters after the CML 4-to-1 selectors and CML XOR gate. Second, drivers are usually large in size and that's why they will need strong digital signals to drive so as not to introduce large jitter for the driver outputs. As a result, a predriver is usually needed in between CML-to-CMOS converter.

With the aforementioned reasons, we have added predrivers with other auxiliary circuits right before the drive and their combined schematic, which can be seen in Fig. 7.7. There are six inputs for each driver: two from outputs of one CML 4-to-1 selector and two from outputs of one CML XOR gate as well as two sets of 4-bit DC code $\overline{a_{i,3:0}}$ and $b_{i,3:0}$. The first four are NRZ bit streams requiring predrivers to build up their driving capacity, which is mentioned as the second reason why we need a predriver after CML-to-CMOS converter. The latter two are DC voltages and can be applied directly to the driver inputs. As shown in the figure, the input signals for the four predrivers are X_i, $\overline{VT\_EN}$, VT_EN and X_i and their resulting output signals of the four predrivers are X_{iu}, $\overline{VT\_EN_u}$, VT_EN_d, X_{id} respectively.

In addition to building up driving capacity, a predriver can also achieve level-shifting, which is the first reason why we need to implement a predriver after a CML-to-CMOS converter. The level-shifting is realized through an ac-coupling capacitor and two back-to-back inverters in front of a series of inverters in cascade with a fanout of 2. The ac-coupling capacitor and the capacitive loading from two back-to-back inverters have formed a high-pass filter together where only dynamic signals sans its DC operating point can pass through. DC operating point of the predriver will be decided by the power supply and ground of the two back-to-back inverters. Also, the inverter in the feedback path is usually smaller and has a larger turn-on resistor than the one in the signal path so that those two back-to-back inverters will be able to realize the same self-biasing function as an amplifier with a resistor as its feedback. Due to the power supply and ground difference between pull-up and pull-down branch, the two predrivers that drive the pull-up branch of the driver have 2.4V as their power supply and 1.2V as their ground, while the two predrivers that drive the pull-down branch have 1.2V as their power supply and 0V as their ground. Usually, the two back-to-back inverters are supposed to self-bias its DC operating point to the mid-level between its power supply and ground: 1.8V for two predrivers that drive pull-up branch and 0.6V for two predrivers that drive pull-down branch, which can maximize the noise margin of

the inverter chains. However, the above result is based on the assumption that the dynamic signal input is PRBS signal, whose integration over time is the mid voltage between its power supply and ground. But in my situation, after two uncorrelated PRBS signals B_1 and B_0 pass through CML 4-to-1 selector, integration over time of their outputs might not be at the mid voltage between the power supply and ground depending on the DC code inputs of the 4-to-1 selector. Without biasing at the mid voltage, the inverter chain right after the two back-to-back inverters will not function correctly. Since this problem is coming from the DC code inputs of the CML selector, we will first set those DC codes to the values that are able to achieve mid voltage and wait for the predriver output to settle, then we can change those DC codes to the values that are able to achieve equispaced optical PAM-4. As a result, those DC codes will also be dynamic but their changes will be slow and thus, in a sense, they are still slowly changing signals compared to high data-rate PRBS signals.

There is a problem with ac-coupling. When NRZ bit stream contains a string of consecutive identical digits, the voltage at the ac-coupling node will droop, resulting in low-frequency pattern-dependent jitter (PDJ). In my design, since CML 4-to-1 selector outputs might produce signals that are not PRBS signals, the longest possible length for a string of consecutive identical digits will be longer than those of PRBS signals. As a result, when we are using PN8 with delay of 85 period between two NRZ streams, the longest consecutive identical digits are 13 bits. By choosing ac-coupling capacitor to be 2.5pF, the PDJ in my system will be 2.2ps, and it is smaller than 3% of the bit period.

The driver that we are using is the voltage-mode driver with 2.4V as supply and 0V as ground. Between supply and ground, there are four transistors stacked together so that their V_{DS} are no bigger than nominal power supply of 65nm technology. NMOS transistor M5 and PMOS transistor M6 are connected to the sources of transistors M2 and M3 so that when the pull-down branch changes from enabled to disabled, the sources of transistor M3 will be discharged to 1.2V and when the pull-up branch changes from enabled to disabled, the sources of transistor M2 will be discharged to 1.2V. There are two blocks at the gate of

cascode transistor M2 and M3 which can generate edge-triggered pulses. When signal X_{id} jumps from 0V to 1.2V, the gate of M2 will drop to 0V for a short period of time and jump back again to 1.2V, which will increase the V_{SG} of transistor M2 for a short period of time and can accelerate the charging at the driver output; when signal X_{iu} drops from 2.4V to 1.2V, the gate of M3 will rise to 2.4V for a short period of time and drop back to 1.2V, which will increase the V_{GS} of transistor M3 for a short period of time and can accelerate the discharging at the driver output.

The output voltage-tuning is realized through adding four NMOS transistors with the size ratio of 8:4:2:1 to the source of transistor M2 and four PMOS transistors with the same size ratio to the source of transistor M3. Each of the four transistors in the pull-up branch is controlled by NOR gate through signal $\overline{a_{i,3:0}}$ and $b_{i,3:0}$ while each of the four transistors in the pull-down branch is controlled by NAND gate through signal VT_EN_d and $b_{i,3:0}$. The sources of both pairs of transistors will be added to 1.2V.

The above descriptions for the driver design are almost the same as those discussed in the last chapter using schematic view of the voltage-mode driver and ideal view of other parts of the transmitter. However, when the predriver is not ideal, it will have limited driving capacity, which will result in being sensitive to loading differences. If we look at the structure of the driver, we can see that in the pull-up branch, input X_{iu} drives an inverter and input $\overline{VT\_EN_u}$ drives four XOR gates while in the pull-down branch, input VT_EN_d drives four NOR gates and X_{id} drives an inverter. If we directly connect the predrivers, there will be different rise/fall time for each input, which will result in skew between them. Since each time, only one branch either pull-up or pull-down is turned on, only two inputs for either pull-up or pull-down branch need to match in their input capacitance. Therefore, for the pull-up branch, we have added a dummy at the input X_{iu} containing four NOR gates with the same size as those used in front of signal $\overline{VT\_EN_u}$ and have added another dummy at the input $\overline{VT\_EN_u}$ containing one inverter with the same size as that used in front of signal X_{iu}. For the pull-down branch, we have added a dummy at the input X_{id} containing

four NAND gates of the same size as those used in front of signal VT_EN_d and have added another dummy at the input VT_EN_d containing one inverter with the same size as that used in front of signal X_{id}. Although those dummies are adding extra loading to my predriver inputs, it is the only way as far as we have known to solve the different loading problem without sacrificing my transmitter operating speed or introducing extra skew or jitter into my transmitter design.

7.7 Simulation Results Based on Layout Extraction

Using proposed transmitter structure and circuit implementation of each block inside of the transmitter mentioned in the previous sections in this chapter, we have realized a transmitter utilizing TSMC 65nm LP technology that is able to generate equispaced optical PAM-4 signals at the symbol rate of 12.5GSample/s. Also, we have not only taken my simulation one step further than the previous chapter which only implements voltage-mode drivers in transistor level while keeping other parts of the circuits ideal by realizing almost every single part of the transmitter structure in transistor level, but also have drawn the layout for all the circuits that are in transistor level and performed simulation using their extraction results. Unlike the previous chapter whose purpose is to verify my proposed scheme of using three-segment microring modulator to realize equispaced optical PAM-4 signal, this chapter is focusing on how to implement it in the transistor level. Besides, since the target symbol rate of my design is 12.5GSample/s, transistor level design on such high speed is really sensitive to the parasitic capacitors. As a result, we have to use the simulation result of my transmitter based on its layout extraction instead of just schematic result to prove that my proposed transmitter structure can be achieved in transistor level. As for the Verilog-A model used for my proposed three-segment microring modulator, all of its parameters are based on IMEC-ePIXfab SiPhotonics ISIPP50G technology, whose derivation is discussed in the chapter 4.

The final layout used for my extraction view simulation for both proposed transmitter

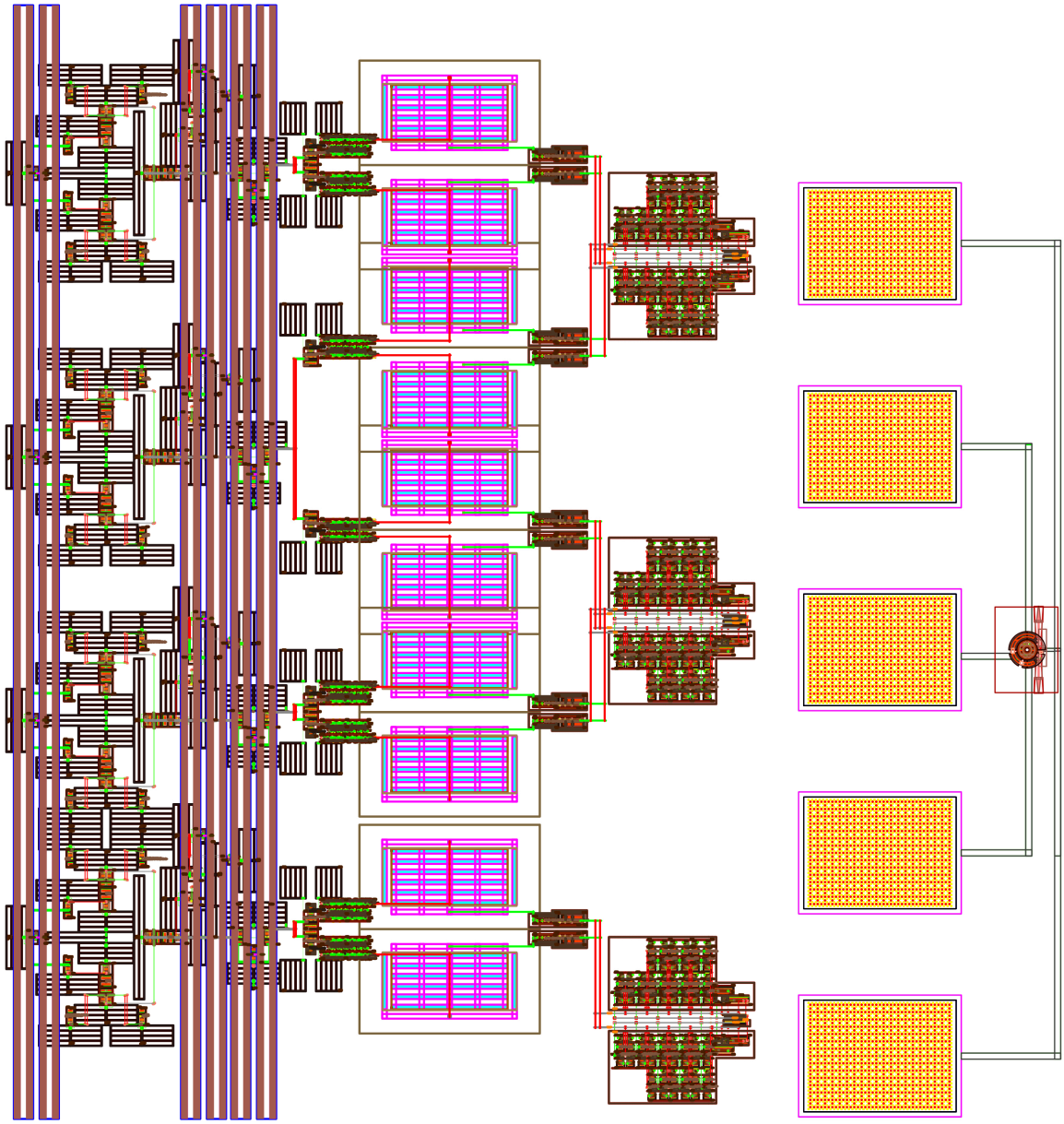

Figure 7.8: Transmitter and Three-Segment MRM Layout

(on the left) and three-segment microring modulator (on the right) can be seen in Fig. 7.8. The transmitter circuit area is $0.1728mm^2$ ($0.48mm$ by $0.36mm$), while the three-segment MRM occupies the area of $0.0705mm^2$ ($0.15mm$ by $0.47mm$).

Although the three paths for supplying three driver voltages are supposed to have the same block diagrams and share the same circuit implementation, the global routing difficulty comes from how to implement the voltage-tuning disable signals since they need to supply three paths at the same time. After carefully placing each block of the transmitter, we have decided not to supply the voltage-tuning disable signal for the third path, which is the LSB of my three-segment microring modulator. Either in the previous simulation where ideal circuits are used or current simulation where extraction simulation is performed, we don't have to realize precise tuning for the LSB in order for my proposed scheme to achieve high percentage of level mismatch. However, we have to supply the coarse tuning for the third path and thus, only change to my transmitter structure is to always disable precise tuning for the third path by giving DC voltage 2.4V to $\overline{VT\_EN_u}$ and DC voltage 0V to VT_EN_d. As a result, the path for creating voltage-tuning disable signals will be placed in between the other two paths of creating MSB and MSB-1 for the three-segment microring modulator, which will make distance of supplying two voltage-tuning disable signals for path MSB and MSB-1 the same. At the same time, since we have decided to only use two predrivers instead of three for supplying voltage-tuning disable signals, using two predrivers to drive two voltage-mode drivers will further reduce the skew coming from the parasitic capacitance unbalance between voltage-tuning disable path and coarse tuning signal generator path.

As can be seen in the transmitter, the ac-coupling capacitor is quite large and that's why we have arranged my transmitter design around it. Therefore, we have chosen the capacitor model mimcap_udd_6m_1p5 in order to achieve a small area and to be voltage-independent at the same time.

There are three more points worth mentioning in my layout design. First, since the transmitter design has three different power supplies and grounds, 2.4V, 1.2V and 0V, there is no common voltage for the ground. Thus, we have to separate the blocks with different power supplies and grounds using guard rings so that their substrate won't be connected together. Second, the layout distance between three voltage-mode drivers has to be the

same. Since MSB path and MSB-1 path are separate from LSB path, we can adjust the distance of LSB path to realize the same distance between three voltage-mode drivers. Also, the predriver output of LSB will be routed to the south so that LSB path won't be too far from the other two paths in order to achieve same distance for three drivers. Third, the clock and PRBS signal distribution network use the same dimension result derived from Sonnet simulator in my layout design. Although we can't use my extraction view simulations for those networks, we have to make sure that the dimension results are able to satisfy the DRC rule, which is crucual for potential future integrated chip fabrication.

The layout of three-segment microring modulator can be seen on the right of figure 7.8. There are five pads connected to the microring modulator and from the top down the pads are connecting to ground, MSB segment of the microring modulator, MSB-1 segment of the microring modulator, LSB segment of the microring modulator and ground respectively. Thus, the pads of microring follow the pattern of GSG, ground/signal/ground.

In order to verify my proposed optical PAM-4 transmitter structure, an eye-diagram of optical power output P_{out} of my proposed three-segment MRM can be used as the main criteria. Eye-diagrams of the two variations of my proposed MRM can be further used to showcase the adaptability of my transmitter structure. Since the optical PAM-4 transmitter has to be working as fast as 12.5GHz in my design, we have drafted the transmitter layout as shown in Fig. 7.8, created its extraction view using $R-C-C_C$ modeling and implemented it into my transient simulation to derive the final eye-diagram of P_{out}.

The transient simulation is performed under the following conditions. First, $1mW$ optical power is injected into my proposed three-segment MRM through laser source, which corresponds to the V_{laser} of $31.6mV$. Second, the frequency offset Δf is set to be -1.232THz, which corresponds to the resonant wavelength of 1559.94 nm. The differential clock signal inputs from external BERT are modeled by two 12.5GHz differential sine waves with single-ended amplitude of $300mV_{pp}$ and DC operating point of 1V, which have the delay of 35ps and 75ps respectively. Two pairs of uncorrelated, differential NRZ bit streams from external

BERT are modeled by two pairs of 12.5GHz differential PRBS voltages with single-ended amplitude of $300mV_{pp}$ and DC operating point of 0.9V. Their settings include transition reference as 10-90%, edge type as halfsine, trigger as internal and LFSR mode as PN8 with seed of 1 but one with no delay and another one with delay of 85 periods. Since outputs of three CML 4-to-1 selectors won't all be PRBS signals and won't be averaged out to zero, the ac-coupling won't be able to achieve the voltage sitting at the middle between power supply and ground for the predriver. In my case, since we have used "110" and "100" to represent logic "10" and "01" respectively, MSB has more logic "1" and LSB has more logic "0". Also in my simulation, we have found that the ac-coupling setting will take about 30ns to settle. As a result, we have chosen to use cell vpwl to supply the inputs for 4-to-1 selectors: before 50ns, we will use logic "111" and "000" to represent logic "10" and "01"; then, logic "111" and "000" will change into logic "110" and "100" to represent logic "10" and "01" respectively.

Just like in the previous chapter where we have used two variations of my proposed three-segment microring modulator to showcase the adaptability of my proposed scheme, we will use the same length variations for verifying that my proposed transmitter structure can also adapt since there are some loading differences between those three scenarios. For the consistency of my thesis, we will reiterate the three variations again. We have modeled both the proposed three-segment $5\mu m$ radius MRM and its two variations, where the first has three 10% longer phase-shifters and the second has three 10% shorter phase-shifters. The proposed MRM has three phase-shifters with length of $10\pi \times \frac{1}{8}$, $10\pi \times \frac{1}{4}$, $10\pi \times \frac{1}{2}$ respectively and one waveguide with length of $10\pi \times \frac{1}{8}$, all in the unit of μm. The first variation with longer phase-shifters has three phase-shifters with length of $10\pi \times \frac{1.1}{8}$, $10\pi \times \frac{1.1}{4}$, $10\pi \times \frac{1.1}{2}$ respectively and one waveguide with length of $10\pi \times \frac{3}{80}$, all in the unit of μm. The second variation with shorter phase-shifters has three phase-shifters with length of $10\pi \times \frac{0.9}{8}$, $10\pi \times \frac{0.9}{4}$, $10\pi \times \frac{0.9}{2}$ respectively and one waveguide with length of $10\pi \times \frac{17}{80}$, all in the unit of μm.

When three phase-shifters are all grounded, the transmission curves for the proposed

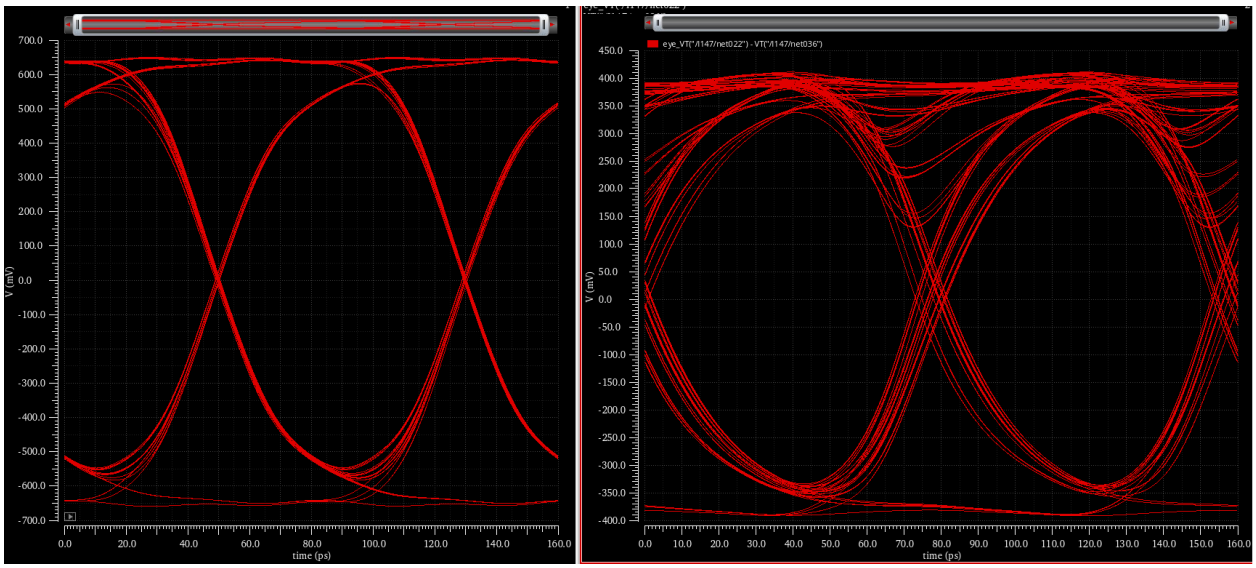

Figure 7.9: Waveform Before and After CML D-type Flip-flop

MRM and its two variations are the same, which is $|T|^2\,(0V, 0V, 0V, \lambda)$. After three phase-shifters are all reversely biased by 2.4V, the transmission curves for the proposed MRM, the first variation and the second variation are $|T_0|^2\,(2.4V, 2.4V, 2.4V, \lambda)$, $|T_2|^2\,(2.4V, 2.4V, 2.4V, \lambda)$ and $|T_1|^2\,(2.4V, 2.4V, 2.4V, \lambda)$, respectively. Their extinction ratios (ER) are 8.7dB, 8.3dB and 9.3dB respectively.

Before we present the eye-diagram for my proposed transmitter structure, let's look at the simulation result from one of the essential structure CML D-type flip-flop in my design as shown in Fig. 7.9. As mentioned before, one of the functions for CML d-type flip-flop is to align the output signals of three CML 4-to-1 selectors and one CML XOR gate, which can be tested through the final eye-diagram result. Its other function, reducing jitter of the output signals, can be seen in the Fig. 7.9: the eye-diagram on the left is derived from the differential output signal of one of the four CML d-type flip-flop and the eye-diagram on the right is derived from the differential input signal of the same CML d-type flip-flop. Therefore, we can see after comparing those two eye-diagrams that the CML d-type flip-flop can not only amplify the output signals of both CML 4-to-1 selectors and CML XOR gate but also is able to reduce the jitter of those output signals significantly.

The eye-diagram of P_{out} at 12.5GS/s symbol rate from my proposed three-segment MRM,

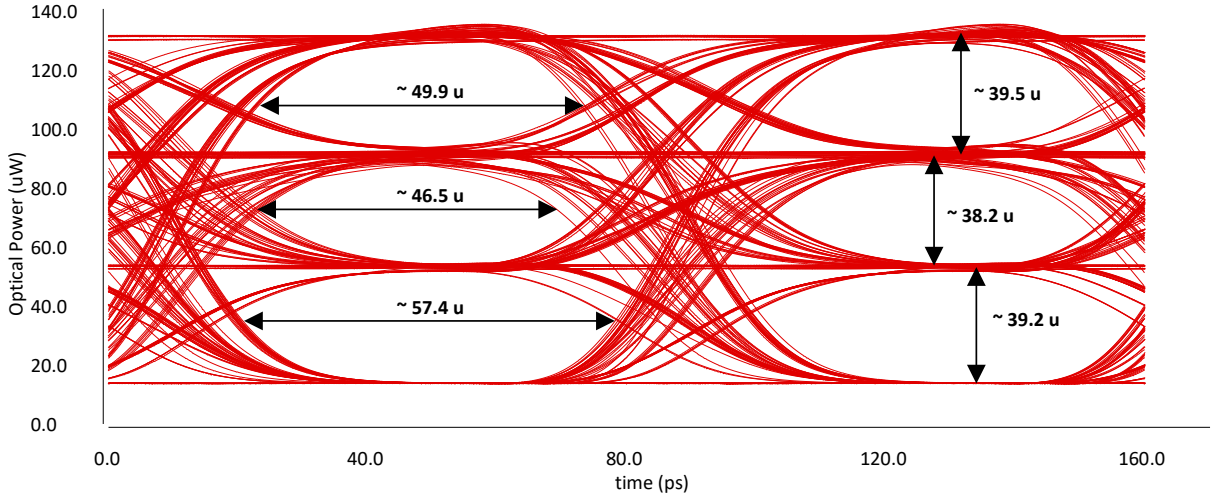

Figure 7.10: Eye-Diagram of P_{out} at 12.5GS/s Symbol Rate Based on my Proposed Three-Segment MRM

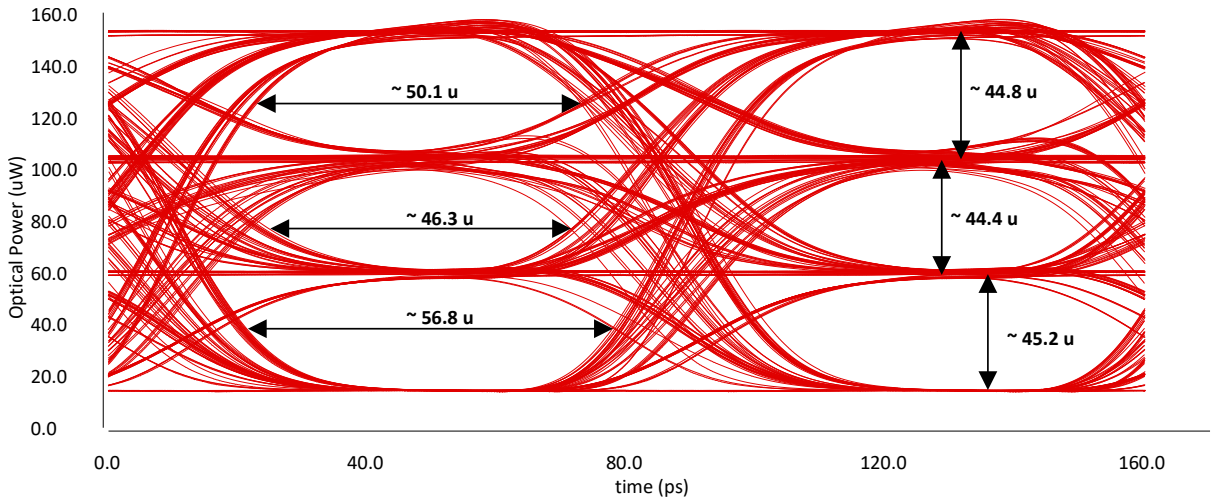

Figure 7.11: Eye-Diagram of P_{out} at 12.5GS/s Symbol Rate Based on the First Variation of my Proposed Three-Segment MRM

which is derived from extraction simulation result of my transmitter structure, can be seen in Fig. 7.10, where all four levels are equally spaced with level mismatch $R_{LM} = 98\%$. The transmission intensity for level "10" and "01" that this eye-diagram is based on can be shown as follows:

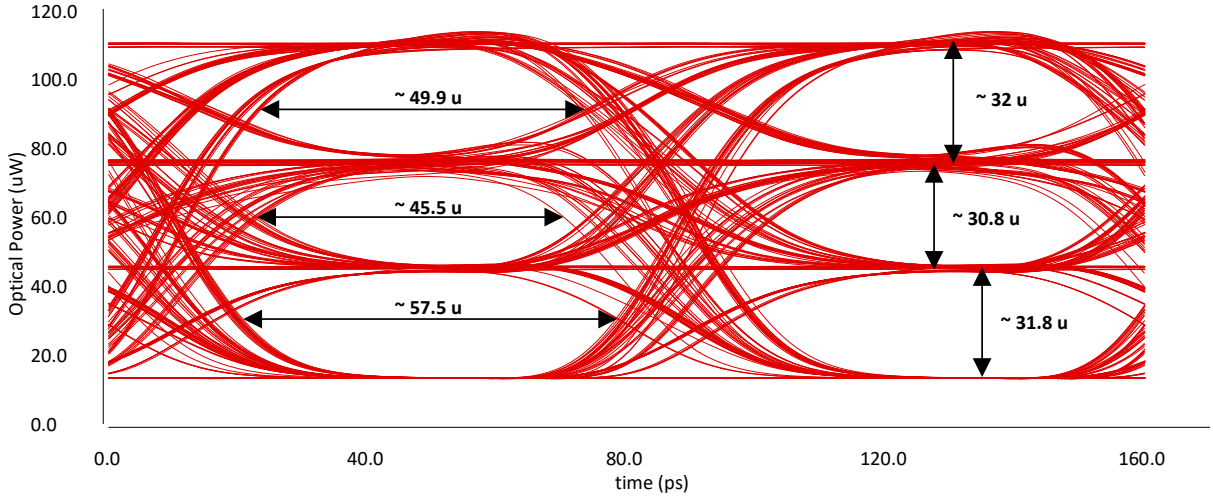

Figure 7.12: Eye-Diagram of P_{out} at 12.5GS/s Symbol Rate Based on the Second Variation of my Proposed Three-Segment MRM

$$|T_{10}|^2 = |T|^2[V_{1L}(1,0000), V_{2L}(1,1110), V_{3L}(0,0000)] \tag{7.1}$$

$$|T_{01}|^2 = |T|^2[V_{1L}(1,0000), V_{2L}(0,1110), V_{3L}(0,0000)] \tag{7.2}$$

The eye diagrams of P_{out} at 12.5GS/s symbol rate from the first and the second variation of my proposed three-segment MRM can be seen in Fig. 7.11 and Fig. 7.12 respectively, where all four levels are equally spaced with level mismatch $R_{LM} = 99.1\%$ and $R_{LM} = 97.7\%$. The transmission intensity for level "10" and "01" that eye-diagrams in Fig. 7.11 and Fig. 7.12 are based on can be shown in Eqn. (7.3-7.4) and Eqn. (7.5-7.6) respectively:

$$|T_{10}|^2 = |T|^2[V_{1L}(1,0010), V_{2L}(1,1110), V_{3L}(0,0000)] \tag{7.3}$$

$$|T_{01}|^2 = |T|^2[V_{1L}(1,0010), V_{2L}(0,1110), V_{3L}(0,0000)] \tag{7.4}$$

$$|T_{10}|^2 = |T|^2[V_{1L}(1,0000), V_{2L}(1,1111), V_{3L}(0,0000)] \tag{7.5}$$

$$|T_{01}|^2 = |T|^2[V_{1L}(1,0000), V_{2L}(0,1111), V_{3L}(0,0000)] \tag{7.6}$$

As discussed in an earlier part of this section, the transmitter structure layout requires that the precise tuning for LSB has to be disabled in order to create equal loading for both the voltage-tuning disable signal inputs of the drivers and coarse tuning inputs of the drivers. Although it might seem to be a compromise in terms of layout, as can be seen from equations above, lower "1" tuning are used for all three scenarios and $V_{3L}(0, 0000)$ showing up in all three scenarios means that precise tuning in the x_k is always disabled. Thus, the compromise in terms of layout won't become a compromise for creating high percentage of level mismatch and equispaced optical PAM-4 signals. Therefore, the two predrivers that are supplying the signals for disabling precise tuning only need to drive the driver for x_i and x_j, which not only simplifies global routing but also reduces the parasitic capacitance coming along with it. On the other hand, by disabling precise tuning in the x_k, lower amount of PAM-4 optical levels will be produced for lower "1" tuning and higher "0" tuning: 6 out of 15 different PAM-4 optical levels have 15 possible PAM-4 optical levels, while 9 out of 15 different PAM-4 optical levels have 256 possible PAM-4 optical levels. As a result, both lower "1" tuning and higher "0" tuning have in total 2400 possible PAM-4 optical levels.

The power consumption of the transmitter is summarized in Table 7.1. There are two power supplies, 1.2V and 2.4V and only predrivers and drivers are using both. The most power is consumed in the CML circuits which include three CML 4-to-1 selectors, one CML XOR gate and four CML D-type Flip-Flops, whose power consumption is 145.9 mW. The CML-to-CMOS converter consumes 28.4 mW while the power consumption of both predriver and drivers combined is 34.45 mW. The energy efficiency of the whole transmitter structure is 8.29 pJ/bit. If we only consider drivers and predrivers, the energy efficiency is 1.37 pJ/bit and if we only consider drivers and modulator, the energy efficiency is as low as 0.5 pJ/bit.

After finishing the extraction simulation of my proposed transmitter structure and having gathered its simulation results, we need to find out the advantages and disadvantages of my proposed scheme and its corresponding transmitter structure. We have summarized the performance of my PAM-4 transmitter in Table II as well as other PAM-4 optical transmitter

Table 7.1: Transmitter Power Consumption Breakdown

Circuit	Supply Voltage [V]	Supply Current [A]	Power Consumption [mW]
CML Circuit	1.2	121.59	145.9
CML-to-CMOS Converter	1.2	23.7	28.4
Predrivers	1.2	1.16	1.39
	2.4	9	21.6
Drivers	1.2	1.83	2.2
	2.4	3.86	9.26
Total Transmitter Power Consumption			208

structures so that we can make a clear comparison. Keep in mind that all other transmitter structure results are from testing results while my result is from extraction simulation results. Although my proposed scheme and structure should be treated with a grain of salt, my result shouldn't be too far off since we have already finished the transmitter layout and its extraction simulation is much better than only schematic simulation results.

First, my design has achieved high extinction ratio compared to other three structures. The high extinction ratio means that under the same signal-to-noise ratio (SNR) requirement, the noise floor can be higher than others, which would reduce the power consumption of the system. Second, my transmitter energy efficiency is low overall but relatively high in terms of modulator and drivers. Although it is not as high as reference [73], that transmitter uses monolithic integration method, which can greatly reduce the loading of the drivers and thus, reduce the power consumption by a great amount. Besides, using 45nm technology will further help with driving down the power consumption of the driver and other parts of the transmitter structure.

Finally, the greatest strength of my proposed scheme and transmitter structure lies in the fact that my design can generate as many as 4800 different PAM-4 optical levels, which shows much better flexibility than the other three transmitter schemes mentioned in the table. The problems with all other transmitters come from the fact that they did not provide the testing results for different variations of photonics modulators as well as corner scenarios. By looking at their number of possible PAM-4 optical levels, we can see there are serious limitations on how to accommodate fabrication imperfections of the photonics modulators. The limitation is even more severe for reference [74] since the length of each segment in the microring modulator is designed specifically from the simulation result alone. Besides, since the silicon photonic fabrication is still not able to reach its mass production level, its fabrication imperfection will be more pronounced than that in traditional integrated circuit fabrication. Thus, my proposed scheme will be useful in dealing with this challenge.

Table 7.2: Comparison with State-of-the-Art Optical PAM-4 Transmitters

	This work	[74]	[73]	[75]
Photonics Circuits	IMEC iSiPP50G with LP 65nm CMOS	130nm SOI with GP 65nm CMOS	45nm CMOS SOI	90nm CMOS SOI
Integration	Flipchip	Wirebond	Monolithic	Monolithic
Wavelength	1550 nm	1550 nm	1280 nm	1300 nm
Driver Supply	2.4V	2.4V	1.55V	1.5V
Modulator Device	Ring-resonator	Ring-resonator	Ring-resonator	MZI
Extinction Ratio	9dB	7dB	3dB	6.3dB
Number of Possible PAM-4 Optical Levels	4800	16	16	1
PAM-4 Data Rate	25Gb/s	40Gb/s	40Gb/s	56Gb/s
PAM-4 Energy Efficiency*	0.5pJ/bit	3.0pJ/bit	0.042pJ/bit	4.8pJ/bit

*Modulator and Driver Energy Efficiency.

Chapter 8: Summary and Future Work

8.1 Summary

Silicon-based Photonics has become a popular technology recently with the purpose of satisfying the ever-increasing demands for high throughput servers and that's why there are a lot of work been done in this field. However, this dissertation provides a different perspective on this technology: how should a traditional IC designers approach the design of Silicon-based Photonics ICs. As a result, this dissertation has offered a self-contained and familiar approach for traditional IC designers to get into the work of this promising field.

The design of photonics ICs starts with the modeling using Verilog-AHDL, which is very similar to the hardware description language such as Verilog or AHDL and both are familiar to IC designers. The goal of modeling photonics devices using Verilog-AHDL is to implement these devices in a way that traditional IC design tool Cadence Virtuoso can understand. The modeling results in a self-contained photonics device toolbox, which can represent certain commercially available photonics technologies such as IMEC-ePIXfab SiPhotonics ISIPP50G technology in my thesis. Also, we can use the created modeling toolbox to propose and simulate new photonics devices such as coupling-based microring modulator and three-segment microring modulator in my case. Furthermore, the modeling can work as my first round of verification for the proposed structures before we implement them in a real photonics chip.

After the verification phase, the design of photonics ICs continues with the implementation of their layout and this dissertation describes how to realize it by using Calibre Pyxis layout tool, which is also used by traditional IC designers to implement electrical layout. The implementation is also specific to IMEC-ePIXfab SiPhotonics ISIPP50G technology as discussed in my thesis but can adjust to other technologies as well. After the photonics ICs are fabricated, the testing of their performances offers the final stage of the verification and is also explored in this dissertation.

Up till now, we have only examined the optical part of the photonics technology but the electrical part is also important. Since we have been able to model photonics devices in the

simulation tool traditionally designed for electrical circuits, both optical part and electrical part of the photonics technology are capable to be simulated together on a same platform, which can facilitate the portraying of the complete mechanism for photonics technology on a platform familiar to traditional IC designers. To describe above process in depth, this dissertation has used a proposed scheme and its corresponding transistor-level transmitter structure based on the three-segment microring modulator to realize equispaced optical PAM-4 signal output using the PDK of TSMC 65nm technology under Cadence Virtuoso platform.

In a nutshell, this dissertation can help IC designers to become familiar with photonics IC designs with the knowledge and tools that they already have by working on the traditional IC designs.

8.2 Future Work

Although we have finished photonics chip fabrication, testing PCB fabrication, Verilog-A modeling for optical devices and driver circuits design for realizing equispaced optical PAM-4, there is still more work that can be done in the future.

- The fabricated photonics chip needs to be tested. Not only my proposed three-segment microring modulators need to be tested using my fabricated PCB, the testing of other structures such standard IMEC microring modulators, two-segment microring modulators are also necessary since this is the first time that we have used this technology and all the parameters used in my simulations are provided by foundries. Thus, the testing of more standard optical structures can help us to improve my Verilog-A models and refine the parameters used in my models. Besides, we can also collect the data for the process variations of those parameters and find their temperature and other dependencies.

- Due to the thermal instability of microring modulator, thermal tuning circuits have to

be implemented in order to provide the complete integrated circuit design for driving microring modulator. Therefore, once we have gained a better understanding of my three-segment microring modulator, we can implement thermal tuner inside of the microring and develop a new thermal tuning scheme that is able to achieve both lower power and fast convergence. Also, the circuits for controlling thermal tuning should be implemented into my old transmitter design to save even more power and space.

- Improve upon the power efficiency of my proposed transmitter design to find a better balance between power consumption and flexibility of the scheme. There is a large gap between the number of different PAM-4 levels my scheme can generate and other state-of-the-art design. After the testing result is available, we should be able to see whether this many different PAM-4 levels are necessary for tolerating process variations. Either way, we should be able to improve upon my proposed scheme to produce a design which is more power efficient and can adapt to process or other variations in the photonics chip.

- Finally, even higher order of pulse-amplitude modulations(PAM-N) can be implemented by proposing new optical structures and its transmitter design needs to be balanced between power efficiency and flexibility. There are two approaches that the author has in mind at the moment. One approach to realize optical PAM-8 signals using my proposed three-segment microring modulator but coming up with a different scheme. Another approach is to propose a differently segmented microring modulator such as four-segment microring modulator and using the similar tuning scheme as the one we proposed in this dissertation.

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Appendix A: Effective Index Method (EIM)

Mathematically, the effective index method is to use the reduced vector-wave equation to approximate the full vector-wave equation. Physically, the effective index method makes use of a slab waveguide with the derived effective index to approximate the rectangular-core waveguide structure.

The transverse electric field Et in an isotropic waveguide with a refractive-index profile n(x,y) satisfies the full vector wave equation:

$$\nabla_t^2 \vec{E_t} + (n^2\kappa^2 - \beta^2)E_t + \nabla_t[\vec{E_t}\frac{\nabla_t(n^2)}{n^2}] = 0 \tag{A.1}$$

where

$$\nabla_t \quad = \quad \frac{\partial}{\partial x}\hat{x} + \frac{\partial}{\partial y}\hat{y} \tag{A.2}$$

Since $\vec{E_t} = E_x\hat{x} + E_y\hat{y}$ and n(x,y) is material index,

$$\nabla_t^2 \vec{E_t} = (\frac{\partial^2}{\partial x^2} + \frac{\partial^2}{\partial y^2})E_x\hat{x} + (\frac{\partial^2}{\partial x^2} + \frac{\partial^2}{\partial y^2})E_y\hat{y} = \nabla_t^2 E_x\hat{x} + \nabla_t^2 E_y\hat{y} \tag{A.3}$$

If we assume

$$\begin{aligned} \frac{\partial}{\partial x}[\frac{E_y}{n^2}\cdot\frac{\partial n^2}{\partial y}] = 0 \\ \frac{\partial}{\partial y}[\frac{E_x}{n^2}\cdot\frac{\partial n^2}{\partial x}] = 0 \end{aligned} \tag{A.4}$$

Equation (A.3) can be simplified to

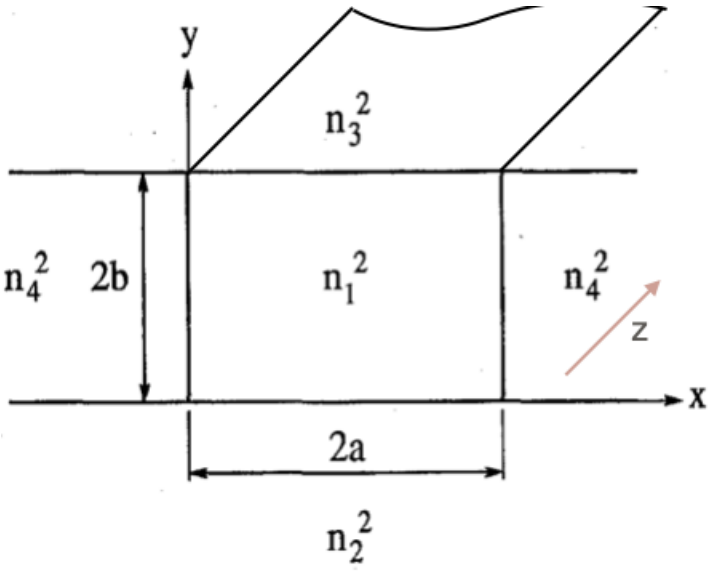

Figure A.1: Rectangular Waveguide Structure

$$\nabla_t^2 E_x + (n^2\kappa^2 - \beta^2)E_x + \frac{\partial}{\partial x}(\frac{E_x}{n^2}\frac{\partial(n^2)}{\partial x}) = 0 \tag{A.5}$$

$$\nabla_t^2 E_y + (n^2\kappa^2 - \beta^2)E_y + \frac{\partial}{\partial}(\frac{E_y}{n^2}\frac{\partial(n^2)}{\partial y}) = 0 \tag{A.6}$$

where both are representing a linearly polarized mode with the first equation as quasi-TE mode and the second equation as quasi-TM mode. Linearly polarized modes are used to approximate the hybrid modes. As long as the guided mode of a rectangular-core waveguide is not close to cutoff, the guided mode does contain the predominant transverse electric field component. It doesn't work when cross-polarization coupling is involved. In the weak-guidance limit—when the relative index difference between core and surrounding medium is small—the modes are always linearly polarized, regardless of the shape of the waveguide.

Let's look at the rectangular waveguide, as shown in Fig. A.1. According to separation of variables, the mode field and profile can be expressed as follows:

$$\begin{aligned} \Psi(x,y) &= \Psi_a(x)\Psi_b(y) \\ n^2(x,y) &= n_a^2(x) + n_b^2(y) \end{aligned} \tag{A.7}$$

By putting equation A.7 into equation A.5, we can derive the following results:

$$\frac{\partial^2 \Psi_b}{\partial y^2} + [n_b^2(y)\kappa^2 - n_x^2\kappa^2]\Psi_b = 0 \tag{A.8}$$

$$\frac{\partial^2 \Psi_a}{\partial x^2} + \frac{d}{dx}[\frac{\Psi_a}{n_a^2 + n_x^2}\frac{d(n_a^2 + n_x^2)}{dx}] + [n_a^2(y)\kappa^2 - n_x^2\kappa^2 - \beta_{x1}^2]\Psi_a = 0 \tag{A.9}$$

where

$$n_b^2(y) = \begin{cases} n_3^2 & 2b < y < +\infty \\ n_1^2 & 0 < y < 2b \\ n_1^2 & -\infty < y < 0 \end{cases} \tag{A.10}$$

and

$$n_a^2(x) + n_x^2 = \begin{cases} n_x^2 & 0 \le x \le 2a \\ n_4^2 & otherwise \end{cases} \tag{A.11}$$

The equation A.8 is the same as TE-wave equation since $\Psi_b(y)$ is E_x and is representing the new equivalent structure as shown in Fig. A.2. The equation A.9 is the same as TM-wave

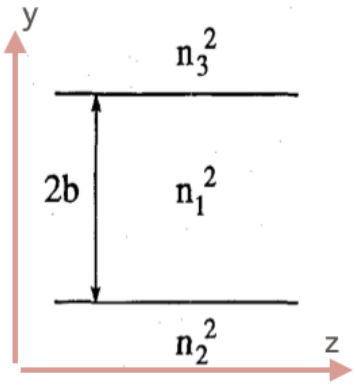

Figure A.2: TE Wave Equivalent Structure for E_x

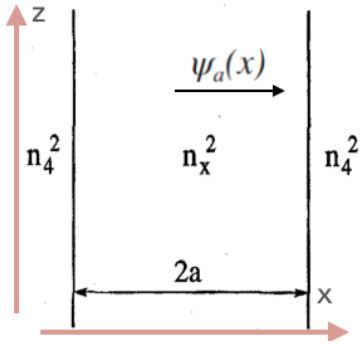

Figure A.3: TM Wave Equivalent Structure for E_x

equation and is able to describe the equivalent structure shown in Fig. A.3. Since $\Psi_a(x)$ is in the plane zox and κ is in the z direction, magnetic field H can only be in the y axis and that's why it is the TM wave. By combining both structures, we can finally solve E_x with the first structure solving $E_X(y)$ and the second structure solving $E_X(x)$.

By putting equation A.7 into equation A.6, we can derive the following results:

$$\frac{\partial^2 \Psi_b(y)}{\partial y^2} + \frac{d}{dx}[\frac{\Psi_b(y)}{n_b^2}\frac{d(n_b^2)}{dx}] + [n_b^2(y)\kappa^2 - n_x^2\kappa^2]\Psi_a = 0 \tag{A.12}$$

$$\frac{\partial^2 \Psi_a}{\partial x^2} + [n_a^2(y)\kappa^2 + n_x^2\kappa^2 - \beta_{y1}^2]\Psi_a = 0 \tag{A.13}$$

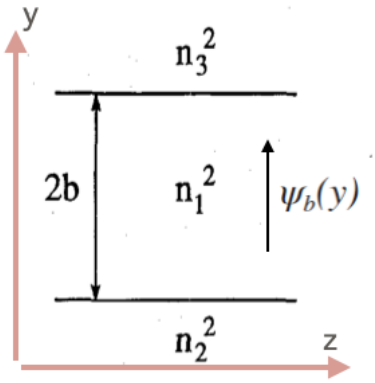

Figure A.4: TM Wave Equivalent Structure for E_y

where

$$n_b^2(y) = \begin{cases} n_3^2 & 2b < y < +\infty \\ n_1^2 & 0 < y < 2b \\ n_1^2 & -\infty < y < 0 \end{cases} \tag{A.14}$$

and

$$n_a^2(x) + n_x^2 = \begin{cases} n_x^2 & 0 \leq x \leq 2a \\ n_4^2 & otherwise \end{cases} \tag{A.15}$$

The equation A.12 is the same as the TM-wave equation since $\Psi_b(y)$ is H_y and is representing the new equivalent structure as shown in Fig. A.4. The equation A.13 is the same as TE-wave equation and is able to describe the equivalent structure shown in Fig. A.5.

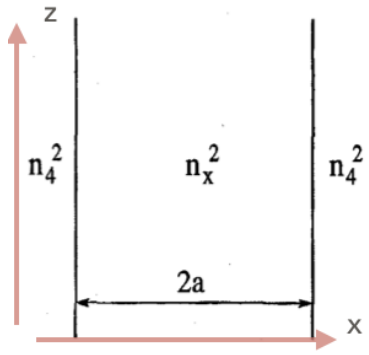

Figure A.5: TE Wave Equivalent Structure for E_y

Appendix B: Coupled Mode Theory

If the amplitude of the first mode is A(z) and the amplitude of the second mode is B(z), the electric field and magnetic field of the optical signal can be expressed as follows:

$$\begin{aligned} \vec{E} &= A(z)\vec{E_1} + B(z)\vec{E_2} \\ \vec{H} &= A(z)\vec{H_1} + B(z)\vec{H_2} \end{aligned} \tag{B.1}$$

Then, the generalized coupled-mode equations can be shown in the following equations:

$$\begin{aligned} &\frac{dA}{dz} + C_{12}\frac{dB}{dz}e^{-j(\beta_2-\beta_1)z} + j\chi_1 A + j\kappa_{12}Be^{-j(\beta_2-\beta_1)z} = 0 \\ &\frac{dB}{dz} + C_{21}\frac{dA}{dz}e^{-j(\beta_2-\beta_1)z} + j\chi_2 A + j\kappa_{21}Ae^{-j(\beta_2-\beta_1)z} = 0 \end{aligned} \tag{B.2}$$

where C_{21} is the butt coupling coefficient, χ_1 is the change in propagation constant and κ_{21} is the mode coupling coefficient. Butt coupling is abrupt and hapens at the end of the waveguide while mode coupling is slow and coupled through evanescent waves over long distance. Since the total power in waveguide p can be expressed as follows:

$$p_p = \frac{1}{2}\int_{-\infty}^{+\infty}\int_{-\infty}^{+\infty}(\vec{E}_p \times \vec{H}_p^*)\hat{z}dxdy \tag{B.3}$$

the denominators of three parameters mentioned above are $4p_p$. If we normalize those denominators, we get:

$$\begin{aligned} C_{21} &= C_{12}^* \\ \chi_p &= \chi_q^* \end{aligned} \tag{B.4}$$

Then, the power in the super mode P is:

$$P = \frac{1}{2}\int_{-\infty}^{+\infty}\int_{-\infty}^{+\infty}(\vec{E}\times\vec{H^*})\hat{z}dxdy = \frac{1}{4}[|A|^2 + |B|^2 + A^*BC_{12}e^{-2j\delta z} + AB^*C_{12}^*e^{-2j\delta z}] \quad \text{(B.5)}$$

where

$$\delta = \frac{\beta_2 - \beta_1}{2} \quad \text{(B.6)}$$

If the power in the super mode is constant in z direction, it means that $\frac{dP}{dZ} = 0$. Then,

$$\kappa_{21} = \kappa_{12}^* + 2\delta C_{12}^* \quad \text{(B.7)}$$

If we also assume two waveguides are identical ($\delta = 0$) and are sufficiently separated (C_{12}^*), then

$$\kappa_{21} = \kappa_{12}^* \quad \text{(B.8)}$$

If we introduce another assumption that there is no butt coupling and the change in propagation constant is zero, the coupled-mode equation can be finally simplified as follows:

$$\begin{aligned}\frac{dA}{dz} &= -j\kappa_{12}Be^{-j(\beta_2-\beta_1)z} \\ \frac{dB}{dz} &= -j\kappa_{21}Ae^{+j(\beta_2-\beta_1)z}\end{aligned} \quad \text{(B.9)}$$