Mixed-Mode S-Parameters Measurements of Power Distribution Networks

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ABSTRACT

To be able to perform the S-parameters measurement procedures, the study of using PNA N5225A, calibration kits, gage kit, connectors, probing station, and microscope were necessary. The short-open-load (SOL) and short-open-load-thru (SOLT) calibration methods were used before the measurements to obtain accurate results. The GS/SG 500 Z-Probes were used to obtain single-ended S-parameters and CSR-5 calibration substrate was used to perform SOL and SOLT calibrations. The printed circuit board design with SMA connector was made to measure its mixed-mode S-parameters measurements. The mixed-mode S-parameters can be obtained either from single-ended S-parameters by conversion, or from true mixed-mode S-parameters measurements. The integrate true-mode stimulus application was required for the true mixed-mode S-parameters measurements. The researchers designed three devices under test and calibration kits for SMA connector. These devices under test included (1) no trace, (2) with trace, and (3) with trace and vias devices. These devices represented the simplest possible power distribution networks, and he demonstrated applying mixed-mode S-parameters to these measurements. Since these devices did not include any components, so the measurement results from the conversion and the true measurements came out to be really close. Due to the limitation of the tool used, the measurements has been performance in the frequency range between 10MHz ~ 5GHz.

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CHAPTER 1

INTRODUCTION

Power distribution network (PDN) becomes important these days since microelectronic technology is scaling down to provide better and faster performance. The supply voltage continues to decrease and the operation frequency continues to increase which create the signal integrity and power integrity issues in integrated circuits, electronic packaging, and printed circuit boards. The objective of signal integrity is to make sure the timing and signal of high speed data transmission and the objective of power integrity is to meet the DC power requirement and reduce the power fluctuation caused by the current switch [1], [2]. For this research work, the student researcher tried to combine true mixed-mode S-parameters and the PDN measurements to determine and illustrate how the mixed-mode S-parameters can be supportive in electronic technology from measurement perspective. PDN included several components; DC source, capacitors, inductors, printed circuit boards, vias, and printed circuit plane [3]. Those elements share one common feature, low impedance. When the measurement instruments usually have 50 ohm source impedance, most of devices have less than 1 ohm. This would cause the entire signal reflected and distinguishing 0.1 ohm from 0.01 ohm becomes very difficult and challenging [4]. In courses offered at University of Idaho, the student researcher studied and learned the subjects of signal integrity and power integrity, the question comes in mind what was different between these two? Is the signal integrity and power integrity the same issues? Why the power integrity become more and more important? In general, the impedance of the signal integrity was targeting around 50 ohm, and the power integrity was targeting at milliohm range [5]. From the measurement perspective, there were some limitations that challenge the high-speed network measurement. At gigabit signaling

with transmission line created in printed circuit board that combined with coupling, noise must be taken into account [6].

CHAPTER 2

BACKGROUND AND LITERATURE REVIEW

2.1 Power Distribution Network

In the semiconductor industry, remarkable challenges like Technology Challenge, Power Challenge and Design productivity challenge are fighting with the continuation of Moore's Law [7]. For technology challenges, IC fabrication and advanced packaging system are significant. Power distribution network (PDN) is fundamental for power and signal challenge of the microprocessor, electronic packaging, interconnection, and printed circuit board (PCB). PDN is very important for any electronic device and very hard to generalization. The PDN with small portions changed will cause the failure of entire system. The purpose of design PDNs are to provide constant voltage, minimize ground bounce noise, and reduce EMI problems. The power distribution networks include the vias, the traces, the power and ground planes on the printed circuit board, the solder balls, the leads of the packages, the signal traces, the wirebonds, and all the passive components. The PDN interconnects are used to transport the power and carry the return signals with very low impedance required. How can you differentiate the PDN and signal trace? There is only one plane for each voltage in the power distributions networks. This plane can be as big as entire motherboard with thousands of components attached [8]. The electrical signal rise time becomes shorter and shorter, and this would involve fast current transient that effects the signal integrity and creates new problems related to the power integrity in PCB. The interconnections of PDN are acting like resistors in series with inductors and capacitors, and this situation can be defined as lumped circuit model. To design of PDN, two parameters that needed to be considered (1) knee frequency, and (2) target impedance. The knee frequency is also known as bandwidth (BW),

which can be determined as $0.35/T_r$ where T_r is rise time. The target impedance can be determined as $(V_{dd}*\Delta V)/(0.5*Imax)$ where V_{dd} is power supply, ΔV is maximum V_{dd} tolerance allowed in percentage, and I_{max} is maximum current consumed by the load [9]. Figure 1 shows the typical mother board.

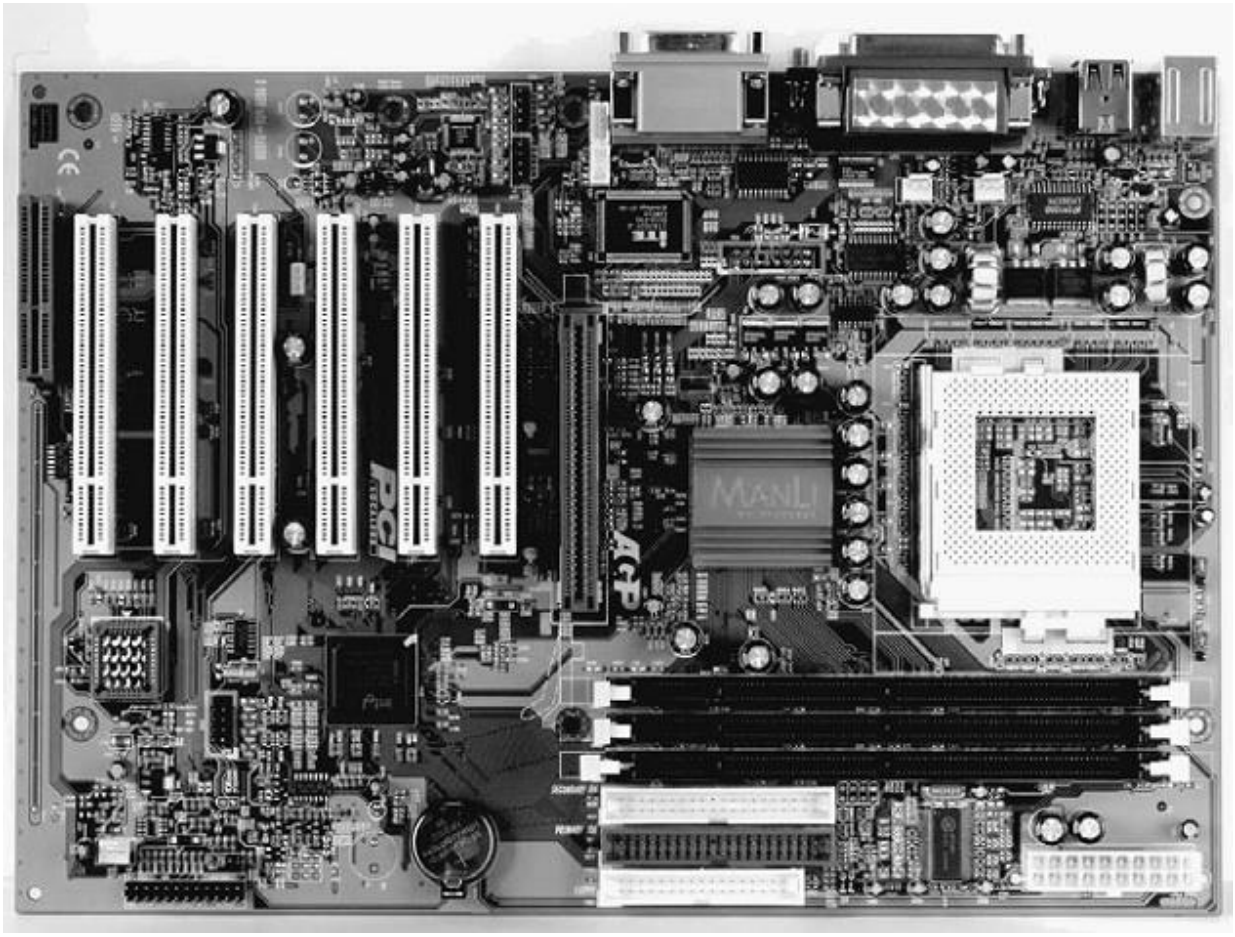


Figure 1 Mother board [8]

Switching noise might result in a serious timing skew or false triggering in high-speed digital system. A method called external coupled resistive termination would be helpful for suppressing this noise [10]. Analyzing the resonant field patterns reveals that the bulk noise is accumulated close to the plane edges because of the open-end boundary condition. Adding extra loading at the field bulk effectively reduces the quality factors and consequently minimizes the noise accumulation [10]. Figure 2 shows the equivalent circuit of external

coupled resistive termination. The edge is terminated with certain value of resistor. A metal post is placed between the power and the ground planes. The top end of the metal post does not contact with the power plane but should be as close as possible [10].

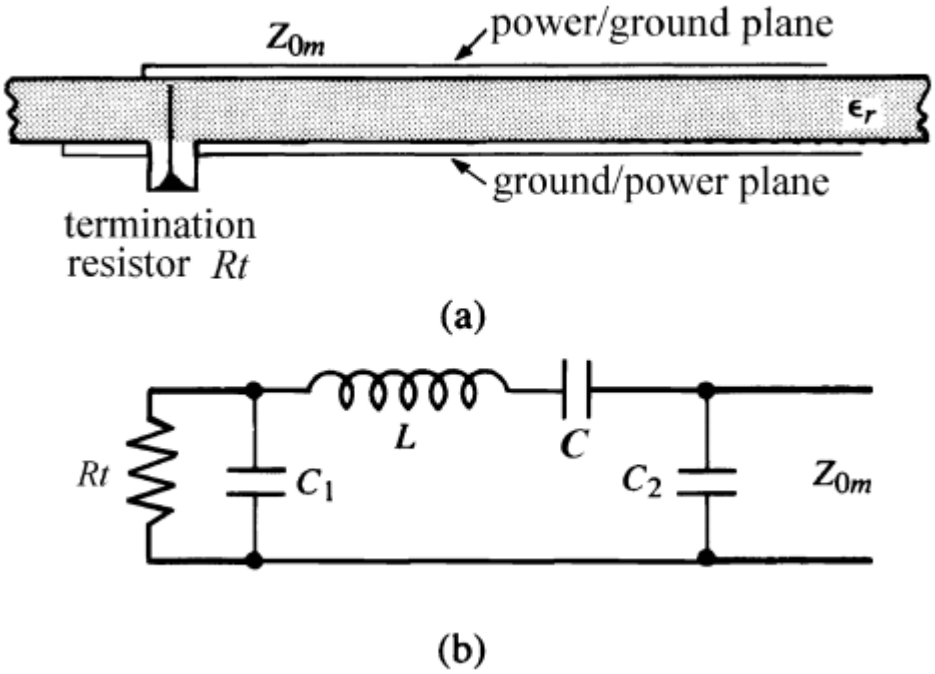


Figure 2 Equivalent circuit of power/ground plane [10]

There is another method called hybrid scattering matrix method. Applying the modal decomposition of the waves propagating inside the power-ground planes and the signal trace, the electromagnetic fields can be decomposed into the parallel plate mode and transmission line mode [11]. Figure 3 shows the typical structure of the signal trace route in PDN.

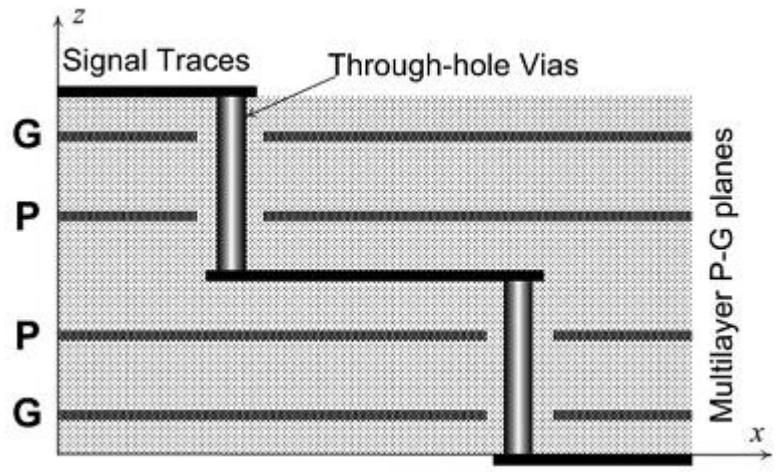


Figure 3 Signal trace route in PDN

As the supply voltage decreases, the power consumption and the frequency increase, the power distribution networks design plays an important role. In high-speed printed circuit boards, it is important to determine the proper values and locations of decoupling capacitors so that the power distribution networks would have very low impedance over certain range of frequencies [12]. PDN noise has also affected power integrity design of a high speed device. The PDN noise above gigahertz is expected to be an issue because the distributed and parasitic effects of the power distribution networks become dominant at higher frequency [13]. Proper impedance control of the power supply with appropriate choice of the amount, location, and values of capacitors is very significant. The interconnection between power and device is acting like inductance and resistance. With the fast current transient in power connections, the power supply could not stay at constant voltage in the entire power connection and voltage fluctuations would more likely to happen [14]. The noise in supply voltage results from the parasitic resistances and inductances in the power distribution network, both on and off the integrated circuit chip [15]. The parasitic resistances causing I-R drop are usually contributed by the metal lines on-chip and the bond wire or ball-grid-array contacts, whereas the parasitic inductances causing voltage ripple are mainly associated with

the vias, traces, pads, and other interconnects both on package and on the printed circuit board [15].

PDN designs are not only power planes but also voltage regulator modules, selecting capacitors, and interconnections, etc. It is very important to have proper power distribution networks design to maintain constant voltage [14]. Power and ground planes are needed to have low impedance over wide range frequencies. Parallel of power and ground planes in multilayer printed circuit boards exhibit multiple resonances which increases the impedance and also the radiation from the edge of the board. Resistive termination along with the board edges reduces the resonances peaks [16]. Power distribution networks for system-on-package are somehow challengeing. The power consumption and supply voltage for some microprocessor products in last decade are shown below in Figure 4. The power increased from 5 to 150 watt, and supply voltage decreased from 5 to 1.2 volt and the frequency increased from 16 MHz to 3 GHz and higher in those days [17].

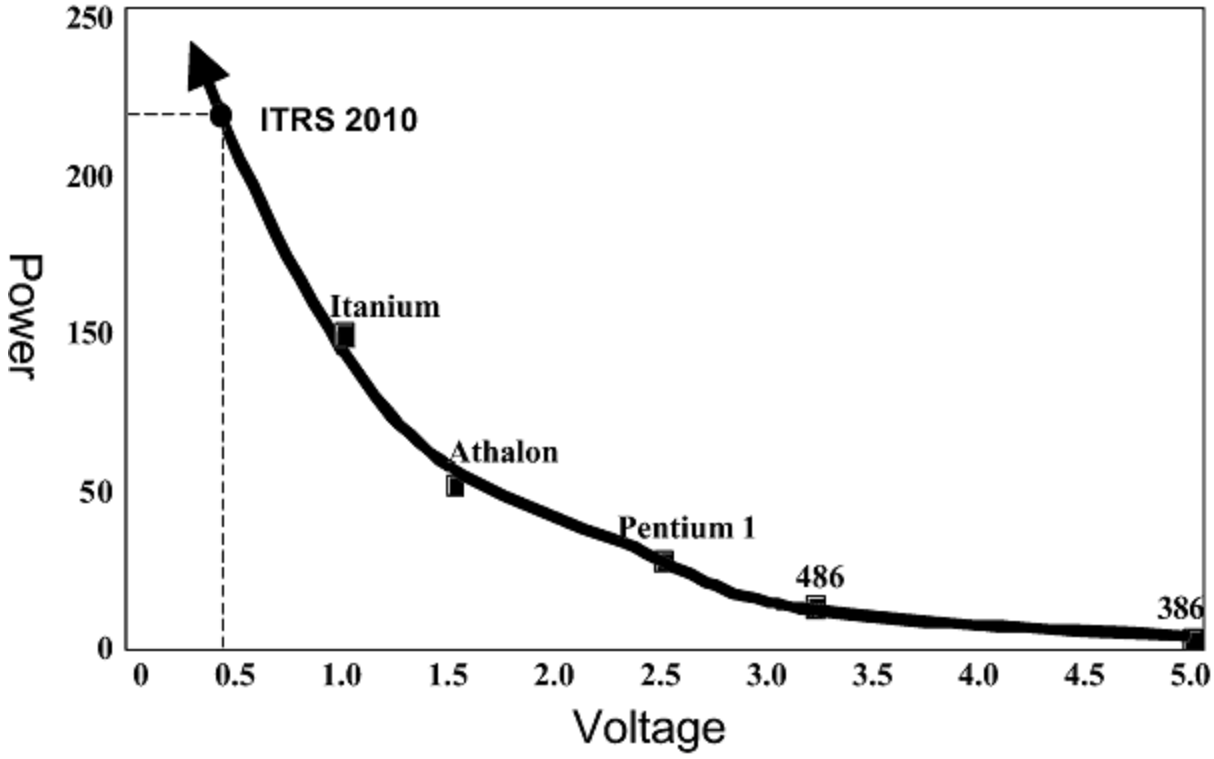


Figure 4 Power consumption verse supply voltage

The PDN included both chip level and package level. The Simultaneous Switching Noise (SSN) is known as a major problem of PDN since it causes performance degradation, produces problems of skew and timing jitter, electromagnetic interference (EMI), and noise. The electronic package is spared to two spheres: the top/bottom portion and the inner portion. The inner portion is the part of the package enclosed by the power-ground planes which is top and bottom layer. These two spheres contain multiport networks, and they are related at the farthest anti-pad domain of the plate-through vias [18]. With shrinking geometry size, the packaging size are getting smaller. The circuit boards with increasing frequencies, exhibit packaging issues and system-level performance issues that become more and more significant. Therefore, integrity of signal transmission becomes critical at high frequencies in IC packaging and PCBs. High package inductance, inappropriate routing, mismatched traces

and placement, inadequate safety for critical paths, and inappropriate return current paths are always the issues for electronic packaging [19].

Power Distribution Networks Impedance

To measure the impedance of an unknown device over a wide frequency range, vector network analyzers and LRC meters can be used. With only one port, any of these choices will be limited to impedance values of a few hundred milliohms or higher and inductances of a few hundred picohenry or higher. The reason for this limitation is the practical difficulty of creating connections from the measuring instrument to the unknown impedance. One millimeter of wire can represent an impedance of a milliohm or more resistance at low frequency and hundreds of picohenry inductance at high frequency. By applying calibration, some of extra impedance can be removed, but will face a difficult task in defining the geometry and connection points with such a high accuracy that the calibration could be effective at high frequency and low frequency values [20]. Figure 5 shows the one port impedance measurement. One port measurement of S-parameters can be described as:

$$S_{11} = \frac{Z_{in} - 50}{Z_{in} + 50}$$

$$Z_{11} = Z_{in} = 50\frac{1 + S_{11}}{1 - S_{11}}$$

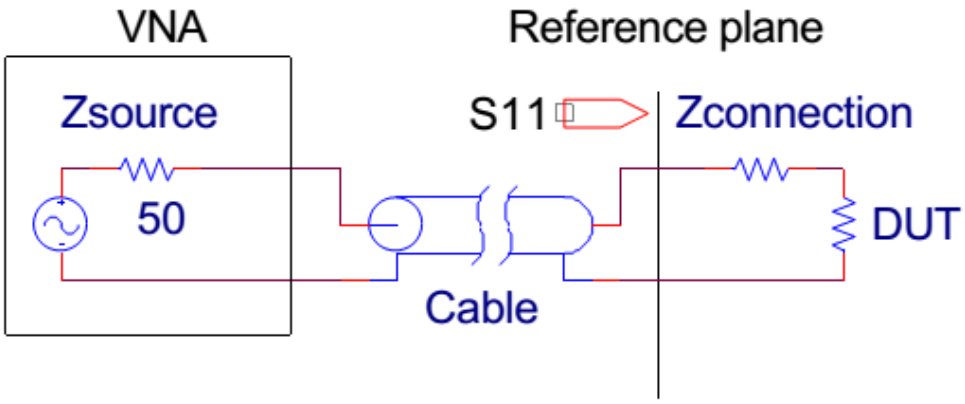


Figure 5 One port impedance measurement

Vector network analyzer provides two ports measurement which is similar to the four wire DC resistance measurement setup. Figure 6 shows that two port connections use port 1 to launch a known signal current into the unknown impedance, and port 2 is used to measure the voltage drop. The same extra connection impedance that appears directly in series to the unknown impedance in one port measurement is now transformed into the two loops of vector network analyzer ports, each having nominally 50 ohm impedance. The two port measurement will still introduce little error up to several GHz frequencies. Figure 7 illustrates two port measurements.

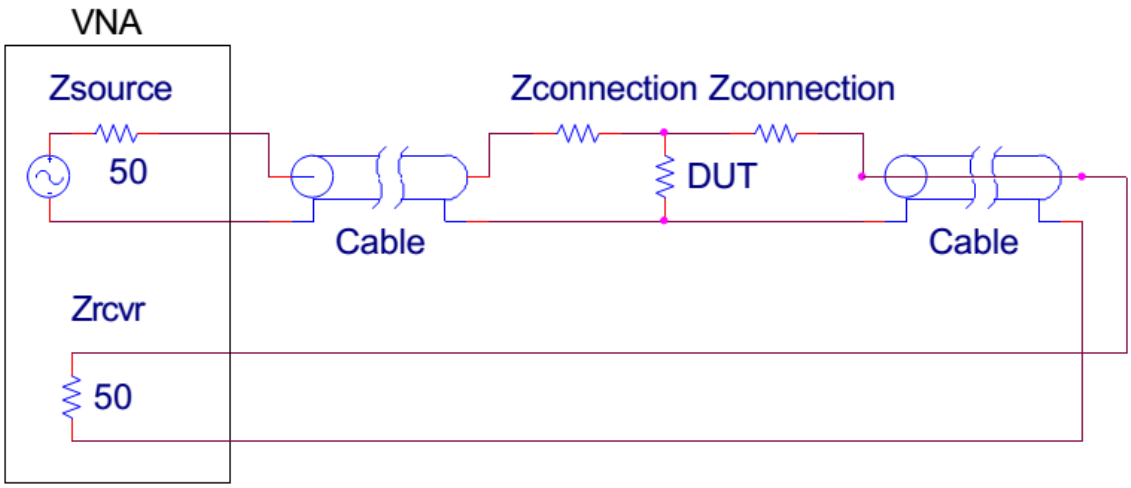


Figure 6 Two ports impedance measurement

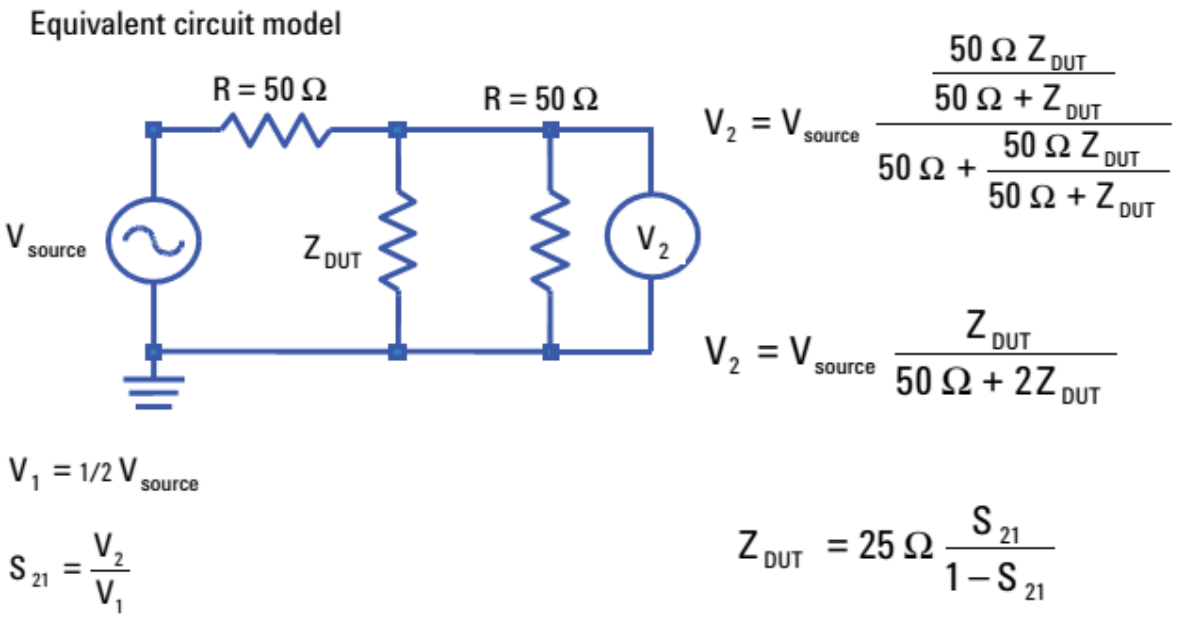


Figure 7 Two ports impedance measurement circuit diagram

Usually, measured power distribution networks components can be approximated with a very simple equivalent circuit in a given frequency range. Figure 8 shows the common equivalent circuits for power distribution networks.

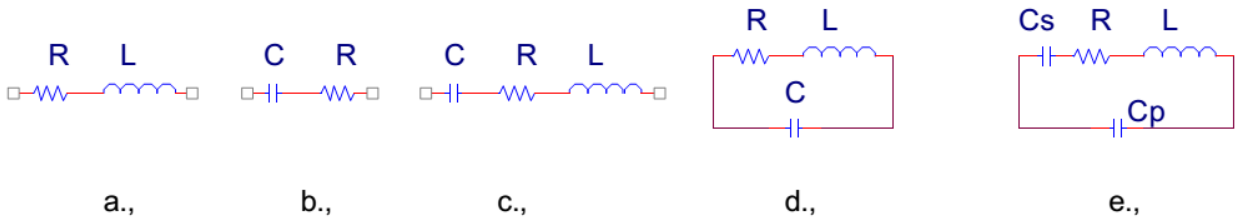


Figure 8 Common equivalent circuit for PDN

Series C-R-L equivalent circuit can be applied to bare plane pairs (from very low frequencies up to close to the first modal parallel resonance), and to many bypass capacitors. Parallel C-R-L equivalent circuits can be applied to shorted plane pairs, and to capacitors mounted on plane pairs. Under circumstances when a frequency independent R-L or C-R model is sufficient, the extraction is straightforward and accurate. When series or parallel C-R-L models are used, the components show non-negligible frequencies dependency and an iterative solution is

necessary to obtain the values for all equivalent circuit elements. There are other technique that can be used to obtain the on die power supply impedance of high power CMOS IC as function of frequency [21]. One technique uses the power supply current variation to stimulate the network and clock rate to obtain several measurements. Another approach measuring for impedance profiles and transient currents is presented in [22].

2.2 S- Parameters

S-parameters are also known as scattering parameters. S-parameters are used to describe as behavioral model which describing the general behavior of linear and passive interconnects. In the frequency domain, S-parameters can be used to describe the behavior of device under test. In time domain, S-parameters would no longer be useful, and time domain reflectometer (TDR) produces more effective results. At high frequencies, open and short terminations of the device are hard to make and very difficult to measure the currents and the voltages with these set up. However, what can be measured is the wave entering a port or being reflected by a port. The S-parameters describe the ports of a network or blocks circuit by measuring the incident and the reflected signals at each port. The S-parameters are measured as functions of frequency and these are measure of how much power or voltage are transferred via a port from the chip to the board. S-parameters are the complex ratio between the reflected wave and the incident wave and they are complex in nature since both the magnitude and the phase of the input signal are changed by the network. S-parameters mainly depend on four components:

i. Network
ii. Frequency
iii. Load Impedance (Output Impedance)

iv. Source impedance (Input impedance)

The S-parameters can be written as functions of voltage. Figure 9 showed two port networks.

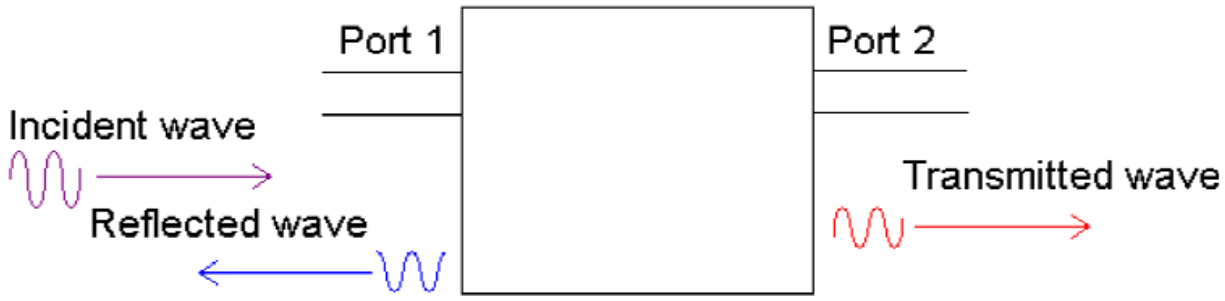


Figure 9 Two ports networks [23]

$$\begin{bmatrix} b_1 \\ b_2 \end{bmatrix} = \begin{bmatrix} S_{11} & S_{12} \\ S_{21} & S_{22} \end{bmatrix} \begin{bmatrix} a_1 \\ a_2 \end{bmatrix} \quad (1)$$

The matrix elements S_{11}, S_{12}, S_{21}, and S_{22} are referred as S-Parameters. The S_{11}, S_{22} are described as reflection coefficients, and S_{12}, S_{21} are the transmission coefficients, respectively. S-parameters are measured by giving a signal to the network, and the network can be anything such as passive components, transmission lines, or integrated circuit. The variables a_1 and a_2 are normalized incident voltages defined as follows:

$$a1 = \frac{V_1 + I_1 Z_0}{2\sqrt{Z_0}} = \frac{voltage\ wave\ incident\ at\ port\ 1}{\sqrt{Z_0}}$$

$$a2 = \frac{V_2 + I_2 Z_0}{2\sqrt{Z_0}} = \frac{voltage\ wave\ incident\ at\ port\ 2}{\sqrt{Z_0}}$$

The variables b_1 and b_2 are normalized reflected voltages defined as:

$$b1 = \frac{V_1 - I_1 Z_0}{2\sqrt{Z_0}} = \frac{voltage\ wave\ reflected\ at\ port\ 1}{\sqrt{Z_0}}$$

$$b2 = \frac{V_2 - I_2 Z_0}{2\sqrt{Z_0}} = \frac{voltage\ wave\ reflected\ at\ port\ 2}{\sqrt{Z_0}}$$

We know the fact that,

S_{11} represents the input reflection coefficient with the output port terminated by a matching load,

$$S_{11} = \frac{b1}{a1} \text{ with } a_2 = 0$$

S_{22} represents the output reflection coefficient with the input port terminated by a matching load

$$S_{22} = \frac{b2}{a2} \text{ with } a_1 = 0$$

S_{12} represents the reverse transmission gain with the input port terminated by a matching load

$$S_{12} = \frac{b1}{a2} \text{ with } a_1 = 0$$

S_{21} represents the forward transmission gain with output port terminated by a matching load

$$S_{21} = \frac{b2}{a1} \text{ with } a_2 = 0$$

Notice from [24], HP application note showed the equation below.

$$s_{11} = \frac{b_1}{a_1} = \frac{\frac{V_1}{I_1} - Z_0}{\frac{V_1}{I_1} + Z_0} = \frac{Z_1 - Z_0}{Z_1 + Z_0}$$

and $$Z_1 = Z_0 \frac{(1 + s_{11})}{(1 - s_{11})}$$,

where $Z_1=V_1/I_1$ is the input impedance at port 1.

The advantage of S-Parameters springs from the simple relationship between the variables a_1, a_2, b_1, and b_2, and various power waves as follows:

$|a_1|^2$ = Power incident on the input of the network.
= Power available from a source impedance Z_0.

$|a_2|^2$ = Power incident on the output of the network.
= Power reflected from the load.

$|b_1|^2$ = Power reflected from the input port of the network.
= Power available from a Z_0 source minus the power delivered to the input of the network.

$|b_2|^2$ = Power reflected from the output port of the network.
= Power incident on the load.
= Power that would be delivered to a Z_0 load.

If we take absolute value and square the S-Parameters, we can obtain the following,

$$|s_{11}|^2 = \frac{\text{Power reflected from the network input}}{\text{Power incident on the network input}}$$

$$|s_{22}|^2 = \frac{\text{Power reflected from the network output}}{\text{Power incident on the network output}}$$

$$|s_{21}|^2 = \frac{\text{Power delivered to a } Z_0 \text{ load}}{\text{Power available from } Z_0 \text{ source}}$$

$|s_{12}|^2$ = Reverse transducer power gain with Z_0 load and source.

The S-Parameters can have any number of ports. For n-port networks, S-Parameters contain n^2 of matrix. For example, if a network has 4 ports, then, its S-parameters would have 4x4 matrices. The number of row and columns is equal to the number of ports in S-parameters matrix. For an n-port network, S-parameters can be written as:

$$\begin{pmatrix} b_1 \\ b_2 \\ \vdots \\ b_n \end{pmatrix} = \begin{bmatrix} S_{11} & S_{12} & \cdots & S_{1n} \\ S_{21} & S_{22} & \cdots & S_{2n} \\ \vdots & \vdots & \ddots & \vdots \\ S_{n1} & S_{n2} & \cdots & S_{nn} \end{bmatrix} \begin{pmatrix} a_1 \\ a_2 \\ \vdots \\ a_n \end{pmatrix}$$

Or,

$$[b] = [S]\,[a]$$

Here, [b] is the reflected wave; [S] is the Scattering matrix and [a] is the incident wave.

2.3 Mixed mode S- Parameters

A two port single-ended can be described as 2x2 S-parameters matrix. To describe two-port differential network, a 4x4 S-parameters matrix is required. Figure 10 illustrates the differential two-port networks.

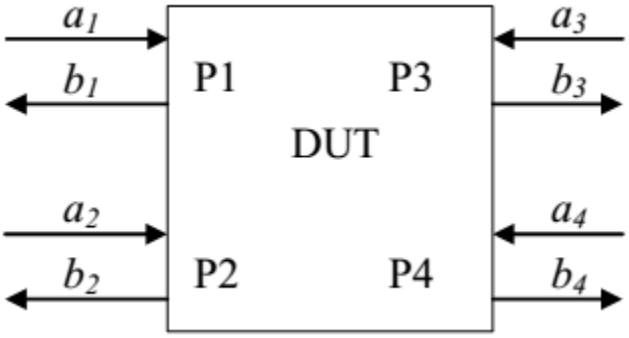


Figure 10 Differential two port networks [25]

Since the real world differential signal is composed of both differential and common mode signals, the single-ended four-port S-parameters matrix does not give enough insight information about the differential and common mode transmission. The mixed-mode S-parameters must be used. The differential two-port and mixed-mode S-parameters are described below,

$$\begin{bmatrix} b_{d1} \\ b_{d2} \\ b_{c1} \\ b_{c2} \end{bmatrix} = \begin{bmatrix} \begin{bmatrix} S_{dd11} & S_{dd12} \\ S_{dd21} & S_{dd22} \end{bmatrix} & \begin{bmatrix} S_{dc11} & S_{dc12} \\ S_{dc21} & S_{dc22} \end{bmatrix} \\ \begin{bmatrix} S_{cd11} & S_{cd12} \\ S_{cd21} & S_{cd22} \end{bmatrix} & \begin{bmatrix} S_{cc11} & S_{cc12} \\ S_{cc21} & S_{cc22} \end{bmatrix} \end{bmatrix} \begin{bmatrix} a_{d1} \\ a_{d2} \\ a_{c1} \\ a_{c2} \end{bmatrix}$$

Where a_{dn}, a_{cn}, b_{dn}, and b_{cn} are normalized differential-mode incident-power, common-mode incident-power, differential-mode reflected-power, and common-mode reflected-power at port n. The mixed-mode S-parameters can be described as four different explanations. It can be defined as following:

- S_{dd} sub-matrix: differential-mode S-parameters
- S_{dc} sub-matrix: mode conversion of common to differential mode waves
- S_{cd} sub-matrix: mode conversion of differential to common mode waves
- S_{cc} sub-matrix: common-mode S-parameters

Figure 11 describes the mixed-mode S-parameters,

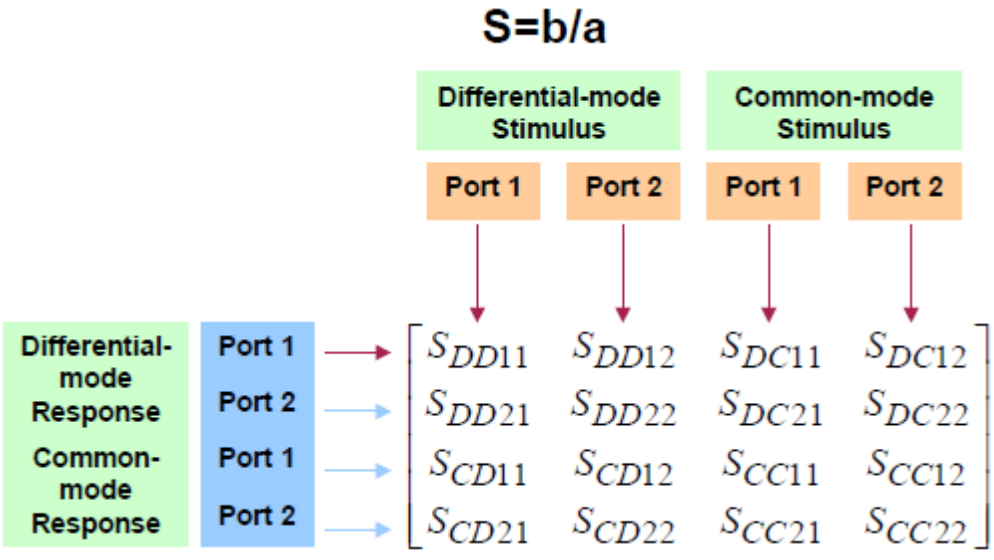


Figure 11 Mixed-mode S-parameter [25]

Single-ended S-parameters can be converted into mixed mode S parameters [26] [27]. In a single-ended ground-referenced device, the input voltage is the difference between the voltage on the node and the ground, and the current is the current flowing into the input node; the ground current is not considered in determining the input current [28]. The differential and the common modes can be expressed in single-ended S-parameters, where b is the voltage out of the port and a is the voltage into the port from equation (1)

$$b_{D1} = \frac{1}{\sqrt{2}}(b_1 - b_2) \qquad a_{D1} = \frac{1}{\sqrt{2}}(a_1 - a_2)$$
$$b_{D2} = \frac{1}{\sqrt{2}}(b_3 - b_4) \qquad a_{D2} = \frac{1}{\sqrt{2}}(a_3 - a_4)$$
$$b_{C1} = \frac{1}{\sqrt{2}}(b_1 + b_2) \qquad a_{C1} = \frac{1}{\sqrt{2}}(a_1 + a_2)$$
$$b_{C2} = \frac{1}{\sqrt{2}}(b_3 + b_4) \qquad a_{C2} = \frac{1}{\sqrt{2}}(a_3 + a_4)$$

Using the definitions of port voltage above, the differential-voltage out of port 1 is:

$$b_{D1} = S_{D1D1}a_{D1} + S_{D1D2}a_{D2} + S_{D1C1}a_{C1} + S_{D1C2}a_{C2}$$

If extending the same process to the full matrix, the result would be:

$$\begin{bmatrix} b_{D1} \\ b_{D2} \\ b_{C1} \\ b_{C2} \end{bmatrix} = \begin{bmatrix} S_{D1D1} & S_{D1D2} & S_{D1C1} & S_{D1C2} \\ S_{D2D1} & S_{D2D2} & S_{D2C1} & S_{D2C2} \\ S_{C1D1} & S_{C1D2} & S_{C1C1} & S_{C1C2} \\ S_{C2D1} & S_{C2D2} & S_{C2C1} & S_{C2C2} \end{bmatrix} \begin{bmatrix} a_{D1} \\ a_{D2} \\ a_{C1} \\ a_{C2} \end{bmatrix} = \begin{bmatrix} [S_{DD}] & [S_{DC}] \\ [S_{CD}] & [S_{CC}] \end{bmatrix} \begin{bmatrix} a_{D1} \\ a_{D2} \\ a_{C1} \\ a_{C2} \end{bmatrix}$$

The relationship between the single-ended and the mixed-mode S-parameters can be described as follows:

Differential to Differential

$$S_{D1D1} = \frac{1}{2}\left(S_{11} - S_{21} - S_{12} + S_{22}\right)$$
$$S_{D1D2} = \frac{1}{2}\left(S_{13} - S_{23} - S_{14} + S_{24}\right)$$
$$S_{D2D1} = \frac{1}{2}\left(S_{31} - S_{41} - S_{32} + S_{42}\right)$$
$$S_{D2D2} = \frac{1}{2}\left(S_{33} - S_{43} - S_{34} + S_{44}\right)$$

Common to Differential

$$S_{D1C1} = \frac{1}{2}\left(S_{11} - S_{21} + S_{12} - S_{22}\right)$$
$$S_{D1C2} = \frac{1}{2}\left(S_{13} - S_{23} + S_{14} - S_{24}\right)$$
$$S_{D2C1} = \frac{1}{2}\left(S_{31} - S_{41} + S_{32} - S_{42}\right)$$
$$S_{D2C2} = \frac{1}{2}\left(S_{33} - S_{43} + S_{34} - S_{44}\right)$$

Differential to common

$$S_{C1D1} = \frac{1}{2}\left(S_{11} + S_{21} - S_{12} - S_{22}\right)$$
$$S_{C1D2} = \frac{1}{2}\left(S_{13} + S_{23} - S_{14} - S_{24}\right)$$
$$S_{C2D1} = \frac{1}{2}\left(S_{31} + S_{41} - S_{32} - S_{42}\right)$$
$$S_{C2D2} = \frac{1}{2}\left(S_{33} + S_{43} - S_{34} - S_{44}\right)$$

Common to Common

$$S_{C1C1} = \frac{1}{2}\left(S_{11} + S_{21} + S_{12} + S_{22}\right)$$
$$S_{C1C2} = \frac{1}{2}\left(S_{13} + S_{23} + S_{14} + S_{24}\right)$$
$$S_{C2C1} = \frac{1}{2}\left(S_{31} + S_{41} + S_{32} + S_{42}\right)$$
$$S_{C2C2} = \frac{1}{2}\left(S_{33} + S_{43} + S_{34} + S_{44}\right)$$

There is other way to describe the single-ended and the mixed-mode conversion. The matrix representation of the equation is given as follow:

$$\begin{bmatrix} a_{d1} \\ a_{d2} \\ a_{c1} \\ a_{c2} \end{bmatrix} = \frac{1}{\sqrt{2}} \begin{bmatrix} 1 & -1 & 0 & 0 \\ 0 & 0 & 1 & -1 \\ 1 & 1 & 0 & 0 \\ 0 & 0 & 1 & 1 \end{bmatrix} \begin{bmatrix} a_1 \\ a_2 \\ a_3 \\ a_4 \end{bmatrix}$$

$$\begin{bmatrix} b_{d1} \\ b_{d2} \\ b_{c1} \\ b_{c2} \end{bmatrix} = \frac{1}{\sqrt{2}} \begin{bmatrix} 1 & -1 & 0 & 0 \\ 0 & 0 & 1 & -1 \\ 1 & 1 & 0 & 0 \\ 0 & 0 & 1 & 1 \end{bmatrix} \begin{bmatrix} b_1 \\ b_2 \\ b_3 \\ b_4 \end{bmatrix}$$

This can be rewritten as an equation,

$$a^{mm} = Ma^{std}$$

$$b^{mm} = Mb^{std}$$

The superscript “mm” represents mixed-mode and the superscript “std” represents the standard parameters. “M” can be written as follow:

$$M = \frac{1}{\sqrt{2}} \begin{bmatrix} 1 & -1 & 0 & 0 \\ 0 & 0 & 1 & -1 \\ 1 & 1 & 0 & 0 \\ 0 & 0 & 1 & 1 \end{bmatrix}$$

Apply the above equations, and the conversion from standard parameter to mixed-mode to the definition for single-ended S-parameters yields the following equation [27] [29],

$$S^{mm} = MS^{std}M^{-1}$$

Z parameters or impedance parameters are the complex ratio of voltage to current. In every case, one port of this parameter remains open, so this parameter is also known as open circuit impedance.

$$[V] = [Z][I]$$

Or,

$$\begin{bmatrix} V_1 \\ V_2 \end{bmatrix} = \begin{bmatrix} Z_{11} & Z_{12} \\ Z_{21} & Z_{22} \end{bmatrix} \begin{bmatrix} I_1 \\ I_2 \end{bmatrix}$$

For two ports Z parameters,

Z_{11} represents the input impedance where port 2 is open circuit,

$$Z_{11} = \frac{V_1}{I_1} \text{ with } I_2 = 0$$

Z_{12} represents the transfer impedance where port 1 is open circuit,

$$Z_{12} = \frac{V_1}{I_2} \text{ with } I_1 = 0$$

Z_{21} represents the transfer impedance where port 2 is open circuit,

$$Z_{21} = \frac{V_2}{I_1} \text{ with } I_2 = 0$$

Z_{12} represents the output impedance where port 1 is open circuit,

$$Z_{22} = \frac{V_2}{I_2} \text{ with } I_1 = 0$$

2.4 Past Work

PDN has been more important than past 20 years. There are a lot of researchers focusing on PDN analysis. What are the functions of PDN?[30] (1) Provided clean power to the active devices, (2) Served as the return path for signal, and (3) Ensure that radiation related to PDN does not violate legal limit. Beside those three functions, there were two major classes of PDN: core power distribution networks and input/output power distribution network [30]. PDN usually involved with capacitor selections and place location. The difficulty of PDN designs were not only providing clean power to the device, but also providing the signal return path. PDN design of high speed and high power systems were not simple. There were contradictory design philosophies, component selection and layout rules. Improper PDN design would increase the supply rail noise. Board level PDN design methods by their impedance profiles and worst case transient noise needed to be compared. Bypass capacitor location maters the most in PDN, where the target impedance does not match the power/ground impedance [31].

For the low impedance PDN characterization, semi-floating ground reference on the gain phase test port of the vector network analyzer could reduce the cable braid loop errors. The S-parameters test port of the vector network analyzer can do the measurement of 100Hz to 3GHz with one cable and probe connection [32].

PDN impedance can be changed, and long resistive traces have significant difference between actual and apparent impedance. The surface roughness would change DC resistance, and the overshoot caused by AC resistance could go beyond the DC resistance value [33]. Measuring the low impedance PDN requires several considerations such as instrument, cables, probes, connection of measurement components, and the biggest challenges were connection

discontinuity and cable braid loop error [34]. Measuring of micro-ohm impedance requires careful consideration of the selection of measurement method, configuration, and setup. Recent instrumentation advances make it possible to achieve a low-frequency noise floor of ten micro-ohms or less with conventional two-port VNA shunt-through connection. Using a hybrid field solver and two-port vector network analyzer measurement method, researchers have shown good correlation of impedance between simulations and measurements in the milliohm range [35]. We knew the selection of capacitors was equally important compared to other considerations. In signal integrity, we knew that if we measured un-terminated trace, at the end of trace resonances could be created. If we do not do anything about it, it could increase conducted and radiated noise. If we place regular low-ESR bypass capacitors at the edge, this does not help for resonance. A low-ESR capacitor is almost pure reactance which could not absorb the bouncing waves [36]. The PDN for multilayer PCB should distribute low noise and stable power for integrated circuit for entire board. PDN planning is a trade-off of cost and performance. The goals of PDN planning are: to provide higher confidence in performance and reliability of the device product, at the lowest cost of production, meet the performance target, and eliminate issues in early design. The PDN impedance for computer-based product must keep low and flat over a large frequency range for improved product performance. Loop inductance could be reduced by placing the capacitors vias close to each other [37]. The best way to avoid radiation problems is to ensure a resonance-free impedance profile. The PDN design could be divided by front end and back end which means design of the chips, packages, and PCB PDN would have several different teams to accomplish. The front end includes selecting the proper stack-up for the packages and boards, and doing pre-layout simulations. The back end includes post-layout simulation and hardware validation.

The PDN design is usually done in frequency domain. The noise is allowed typically up to 10%, but for some applications, it can drop to 1%. The power rail impedance must be less than the dynamic impedance of the load [38].

CHAPTER 3

MEASUREMENTS PROCEDURES AND EQUIPMENT

3.1 PNA Network Analyzer N5225A

For the PDN measurements, Idaho Microelectronics Laboratories (IML) are equipped with PNA N5225A network analyzer from Agilent or Keysight. The PNA has four ports with two internal signal source from 10MHz thru 50GHz. To operate the PNA necessitates a prime requirement of wearing wrist strap, for electrostatic discharge protection. Static electricity usually comes from our body, and it can damage circuit elements when discharged. To prevent damage to the instrument, we will always have to be grounded which means to wear wrist strap prior to coming to the station and touching the instruments. The PNA purchased possess standard 4-port configuration and temporary license for integrated true-mode stimulus application (iTMSA). The iTMSA provides true differential and true common stimulus and enables balanced measurements under real operating conditions. The iTMSA also has the ability to do forward-only sweep, reverse-only sweep, and frequency or power sweep with arbitrary phase for balanced measurements. The operating environment is also important to maintain better performance. The PNA is maintained in a controlled environment for both temperature and humidity. Temperature is kept between 20 degree and 26 Celsius, and when calibration has been done, the temperature must be maintained within 1 degree Celsius. The humidity should be kept between 0% to 95% at 40 degree Celsius maximum and non-condensing. The PNA needs to warm up 30 minutes prior to operation in order to have accurate measurements.

The PNA has measurement uncertainty; that includes the residual systematic errors and the random errors even after calibration.

The systematic errors are:

- Directivity
- Source match
- Load match
- Reflection and transmission frequency tracking
- Isolation (crosstalk)

The random errors are:

- Noise
- Drift
- Connector repeatability
- Test cable stability

All the measurements must include those error terms. This is unpredictable errors [39].

3.2 Calibrations

Good equipment and calibration standards are required to have accurate S-parameters measurements. There are several types of calibration techniques. The most common are short-open-load-reflect (SOLT) and thru-reflect-line (TRL). The question comes to mind, why do we need to do calibration? We should be able to connect adaptors, cables, and probes, and do simply measurements. But, the answer is "NO". Any measurements without calibration would be inaccurate, but even with good calibration that can still contain some errors which cannot be removed. Calibrations are usually applied to network analyzer, and remove the errors from instruments, cable, probe or SMA connector. After calibrations have done, there would be a

new reference point. Depending on its frequency range and the application, both calibrations have their own advantages and disadvantages.

SOLT calibration is easier to perform and it's most widely used in coaxial cable measurements. There are many coaxial calibration kits available to fit most of connector types [40]. There are some standards for both TRL and SOLT. For TRL THRU, it should be no loss and no characteristic impedance, $S_{21}=S_{12}=1$, and $S_{11}=S_{22}=0$ for zero length. For non-zero length, the characteristic impedance of THRU must be the same as the LINE, and attenuation of THRU does not need to be known. For TRL REFLECT, reflection coefficient magnitude is optimally 1, the reflection coefficient must be identical on both ports, and the phase of reflection coefficient must be within quarter length or 90 degree. For the TRL LINE, characteristic impedance of the LINE starts as the reference impedance of the measurements. The length of line should be quarter wavelength, and the ratio of usable bandwidth is 8:1 for a single THRU/LINE pair [41]. The researcher have used only SOLT calibration for two ports calibration and short-open-load (SOL) for one port calibration.

3.3 Probes, connectors, and calibration substrates

In this thesis, the researcher used probes and SMA connectors to perform S-parameters measurements. The probes first used were GS-500 Z-Probe for one port measurement, and later on SG-500 Z-Probe for two port measurements were purchased. There are many different vendors and types of probes for difference purposes and applications. The price can vary from several hundred to several thousand dollars. The probes can be described as infinity probes, air coplanar probes, Z probes, RFIC and functional test probes, board test and signal integrity probes, and special-purpose RF/microwave probes. We have air coplanar probes and Z probes in the cleanroom. The Z probes can be divided into four different types.

1. Z Probe
2. Dual Z Probe
3. Z Probe Power
4. Z Probe PCB

Those Z probes can be used from DC up to 67GHz, and the connector of probes from 1.85mm 2.4mm, and 2.92mm. The probes have GS, SG GSG, SGS, GSSG, and GSGSG configuration. GS represent the ground and signal for example: GSG is ground-signal-ground probe. The pitch of Z probe can be as small as 50 um and up to 2500 um. The probe I used was Z Probe PCB GS-500 and SG-500. Those probes were used for PCB, IC pins and ceramic substrate probing [42]. Figure 12 is air coplanar probe.

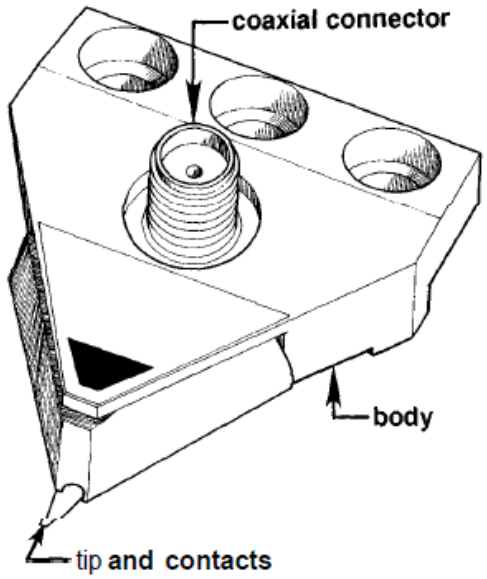
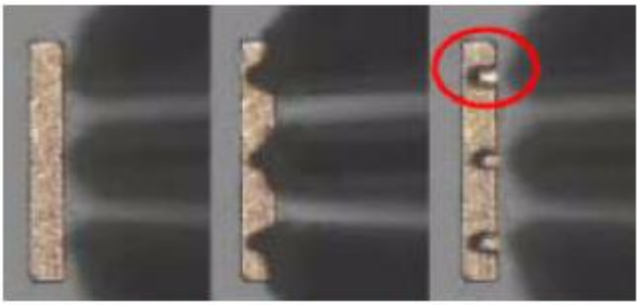


Figure 12 Air coplanar probe [42]

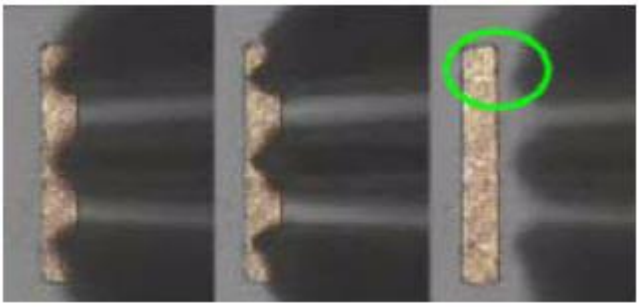
The question is how to operate the Z probe in order to have best accurate and secure measurement? The probe tips are very fragile, thus are subject to break, and so efforts are made to avoid overtravel is very important. The recommended overtravel for Z probe is 5 µm

on gold and 30 µm on aluminum pads [43]. Included in this document are some figures for worse and best overtravel cases. The other figures describe the top view, the side view, and the bottom view of the probe and the substrate [44].



Worst case: touch down before pad, overtravel = 100 µm

Figure 13 Worse case for probing



Best case: touch down on pad, low overtravel = 5 µm

Figure 14 Best case for probing

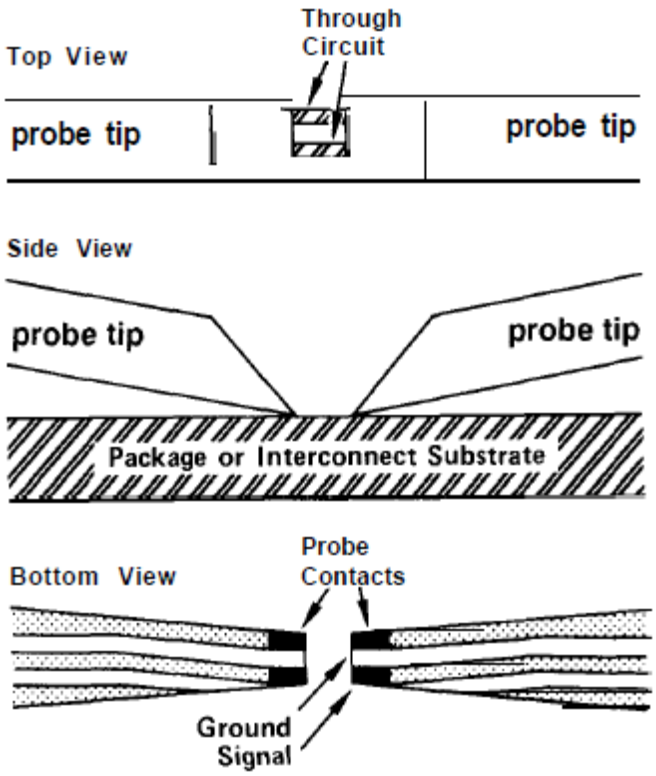


Figure 15 Top, side, and bottom view of probe [44]

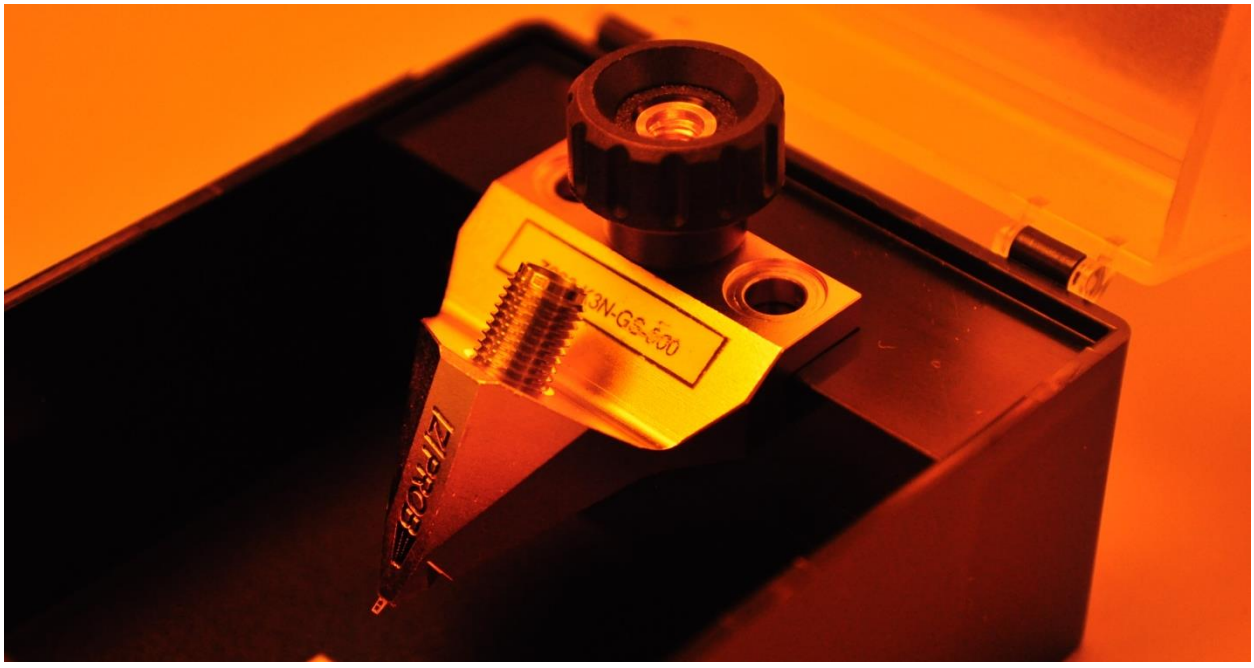


Figure 16 : Z-Probe PCB GS-500

The connectors are used during the measurements to connect probe, cable, and SMA, and have proper connectors also needed to be considered. There are also many different sizes of connectors, each connector size can operate in a different range of frequency. The smaller size would have the higher operating frequency. The connector for the designated in this work for the Z-probe is 2.4mm to 2.92 mm. The 2.4 mm is connected to the cable, and the 2.92 mm is connected to the probe. Figure 17 shows the SG-500 probe with connector.

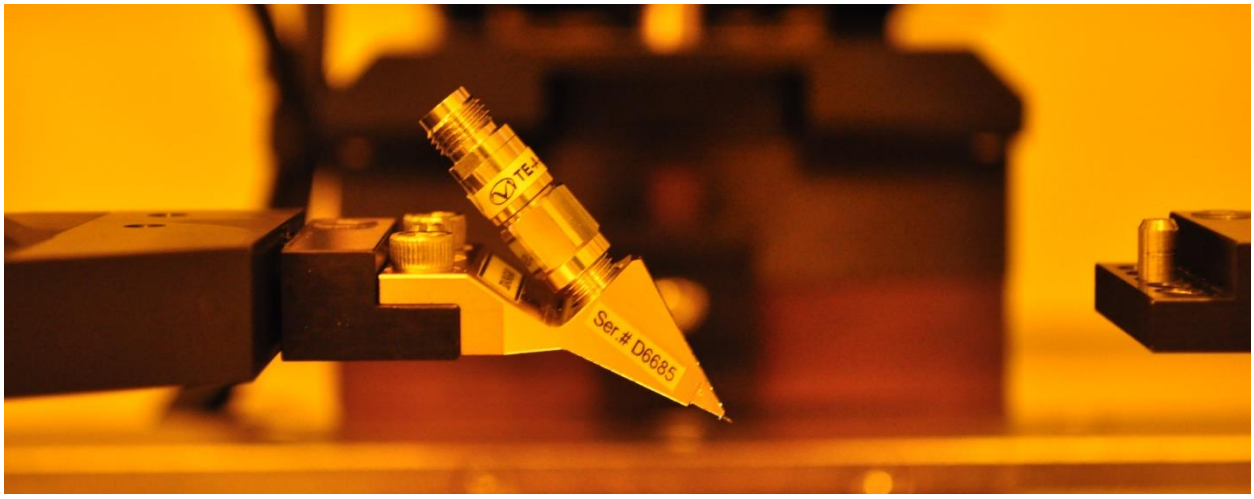


Figure 17 Z-Probe PCB SG-500 with connector

For the calibration substrate, purchasing from company is most reliable decision, but most of time, calibration substrates cost much more than an educational institution can afford. Due to the high roughness of the PCB manufacturing company, it is not reasonable to make your own calibration substrates for probes, so we had to purchase calibration substrates.. Calibration substrates for probes would have short, open, load, thru (through), and line. These substrates are made realizing the limitation range of the pitch. The calibration substrate used is called CSR-5, and is made especially for Z-probes. The CSR-5 has following characteristics illustrated in Table 1.

Table 1 CSR-5 Characteristics

Material	Alumina
Size	16 x 13.7mm
Thickness	635um
Dielectric Constant	ε = 10.2
Effective Permittivity	5.73
Effective Velocity	0.43
Phase Velocity	7.36 ps/m
THRU Impedance	nominally 50 Ω
DC accuracy (LOAD)	50 Ω +/- 0.15 Ω
Temperature	between –263°C and +150°C
Maximum Power	0.3W

The standards on divided into two groups: transmission and reflection. There are aliment standards which can be used for computer control probes that are given by (X, Y) coordinates. For two ports calibrations, the probe must be GS/SG configuration. Figure 18 shows the spacing of the probe and the calibration standard on the substrate [45]. Figure 19 showed the probe contact substrate. This was used to make sure the probe tips landed perfectly. If one tip landed first, and the other tip did not make any contact with DUT, it would cause the bad measurements and it might damage the probes if I tried to over travel the probes. Figure 20

showed the calibration substrates. The calibration substrates include short, open, load, thru, and line standard. With this calibration substrates, I could apply several different methods of calibration.

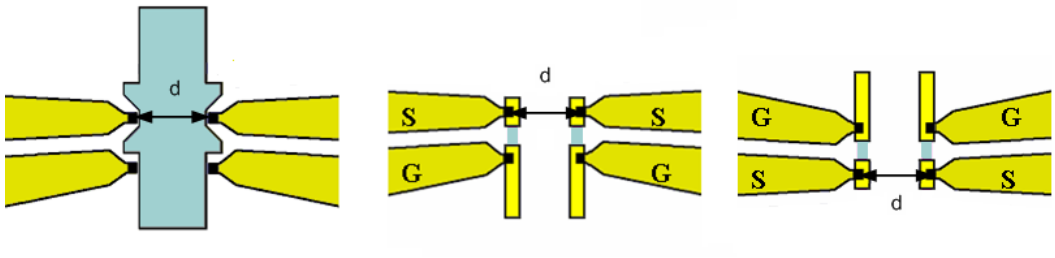


Figure 18 Probe spacing

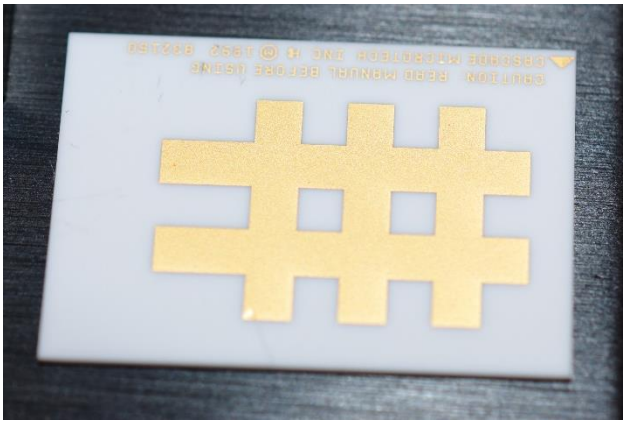


Figure 19 Contact substrate

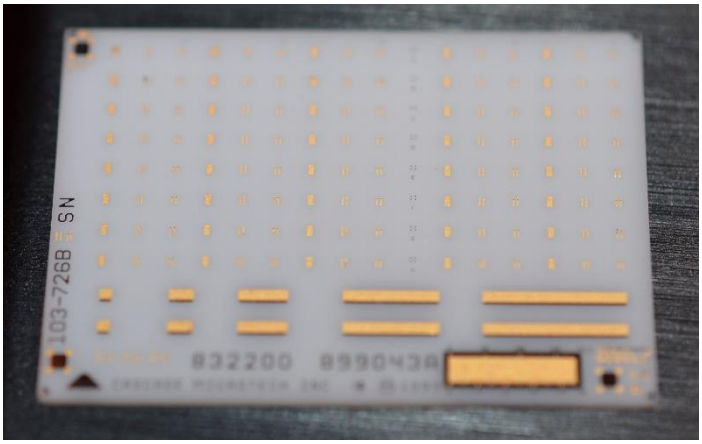


Figure 20 Calibration substrate

3.4 Measurement Procedures and Equipment

For this research work, N5225A PNA microwave network analyzer has been used, the PNA has four ports with two internal sources and operates in a frequency range extending from 10 MHz to 50 GHz. Prior to conducting any electrical measurements, the entire connectors and adaptors are cleaned with pure alcohol as shown in Figures 21 and 22 (cleaning connectors and cables). After cleaning, one would need to apply a gage kit calibration. There are two types of gage kits available in the laboratory facility. One gage kit is 2.92 mm/3.5 mm analog gage kit and the other gage kit is 1.85 mm/ 2.4 mm digital gage kit. Those gage kits calibration tools figure 23 are to test all the connectors and adaptors in order to have correct contact. The gage kits need to be calibrated with standard connector then apply 4 lb. wrench and set to zero, Figures 24 and 25 (analog and digital gage kits). Next, apply gage kit to adaptors and connectors. To make correct contact, turn the screw in one end and hold it tight in other end. This can avoid the connections get grind each other and damage the center pin. After the gage kit connects to the adaptors or the connectors, the proper wrench with certain force is used. Now from the gage kit, the value must be negative indicating a good connection. If the values turn to be positive, the adaptors or connectors would have been damaged. If one can ignore what happen and continue to use those adaptors, whatever connects with those damage adaptors would be damaged as well. Figure 26 show how to apply wrench and Figure 27 and 28 show the negative reading after the gage is applied.

Figure 21 Connector cleaning

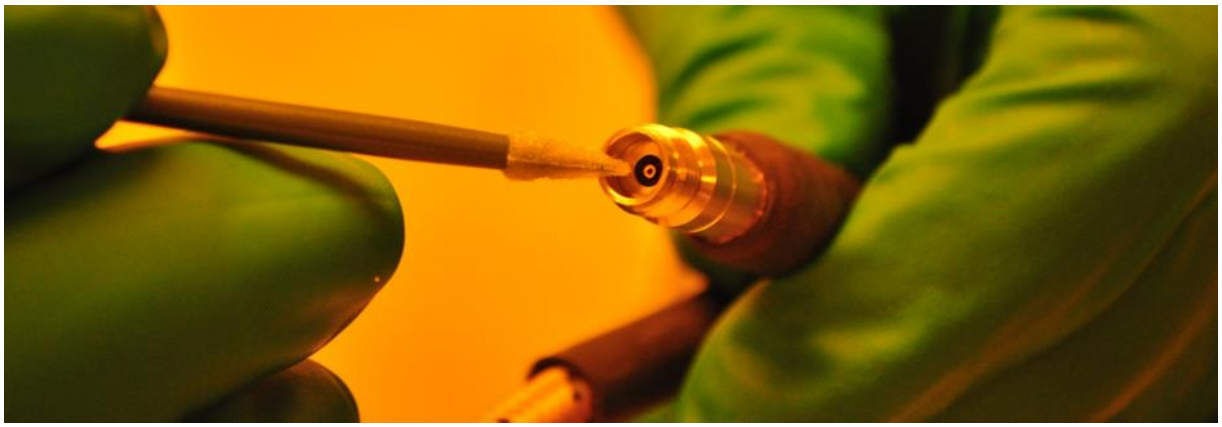


Figure 22 Cable cleaning

Figure 23 Gage Kit

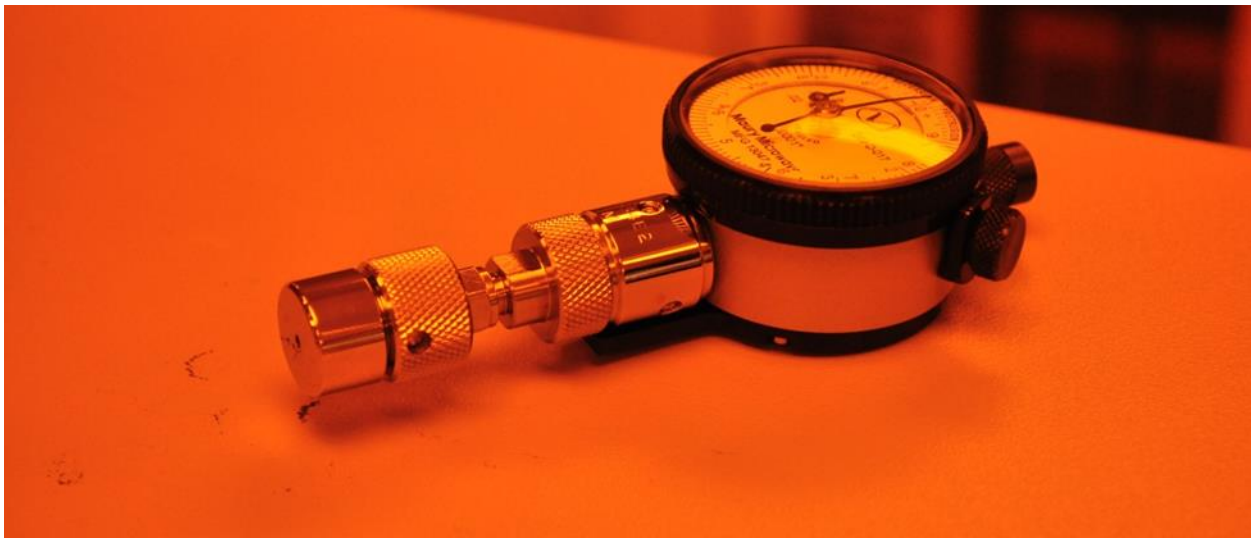


Figure 24 Analog gage kit (3.5/2.92mm)

Figure 25 Digital gage kit (2.4/1.85mm)

Take out probe from box; probes are purchased from a company named Cascade Microtech GS 500 and SG 500 Z-Probe. The GS 500 means ground-signal 500µm pitch at tip. Place Z-probe to the station, and connect with 2.4mm/2.92mm adaptor. The cable is 2.4 mm at connection with 50 GHz maximum operation frequency.

Equipment Infrastructure

- PNA N5225A
- Probe Station
- Vacuum Environment
- Safe Lights
- Microscope

Level substrate and Calibration

The CSR-5 has alignment short open load, and line standard. To perform calibration method for example SOL, SOLT, TRL etc., alignment standard provide accurate probe distance which give same amount of parasitic capacitance in each measurement. Figure 29 shows the two ports probing with level substrate.

Figure 26 Apply two wrench to tight connector

Figure 27 Digital gage kit calibrate cable (negative reading)

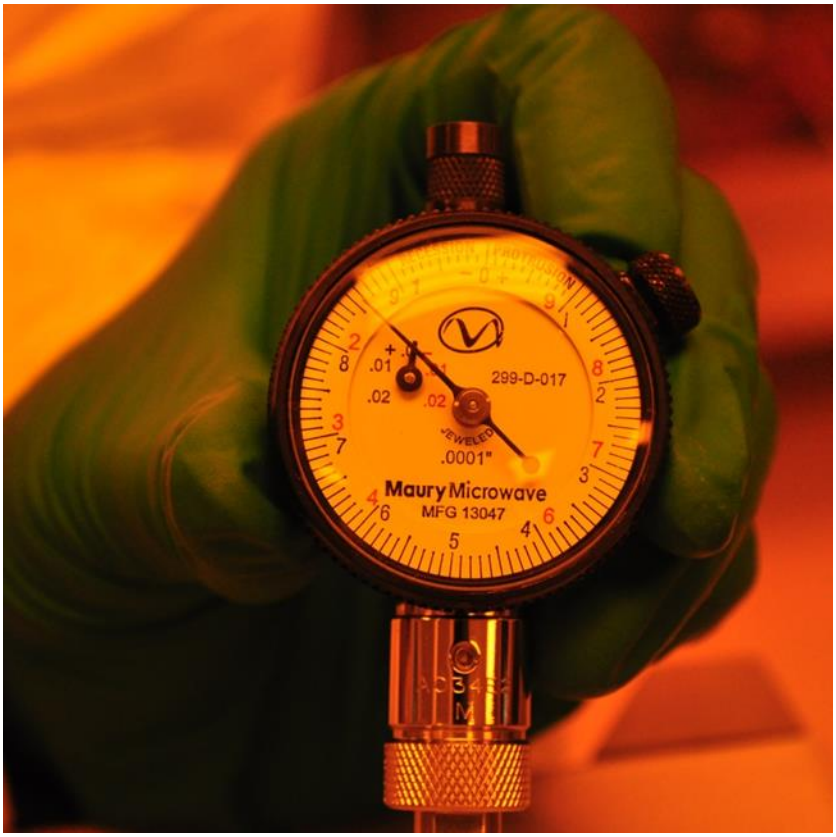


Figure 28 Analog gage kit calibrate connector (negative reading)

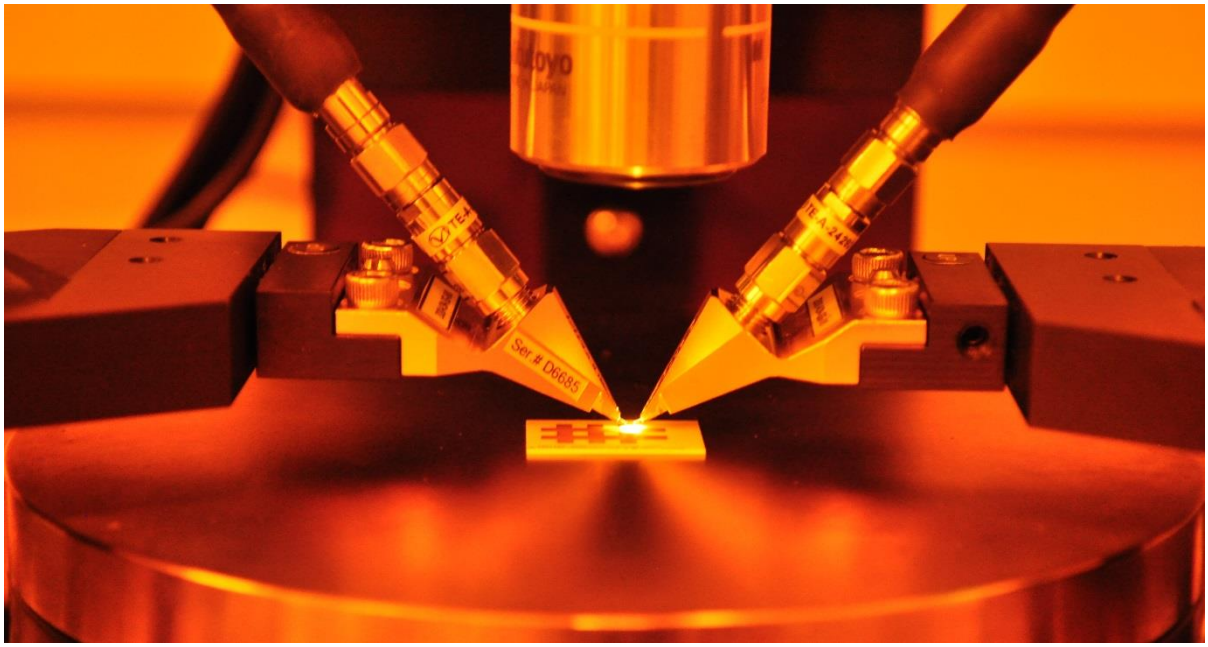


Figure 29 Two ports probing

3.5 Device Under Test (DUT)

During the course of this research, three different PCB boards were designed and created for testing. The first and the second PCB boards were made for Z-probe probing. The last board was made for SMA connector which is much reasonable and cheaper. Figure 30 was the first PCB that had a probing space of 10 mil. There were short, open, and load calibration standards on this PCB. Because of unpredictable calibration parameters, the measurements were done with inaccurate results, but it was really good experience to make this one. Since these measurements were not good enough, the calibration substrate CSR-5 was acquired. Figure 31 shows the second design of PCB. This PCB was designed for mixed-mode S-parameters measurements. You can see that there were huge conductors surrounding the device under test. This was the purpose of additional ground for probing. Due to the measurement limitations, the researcher had to design the third PCB by using the SMA

connector. Figure 32 shows the portion of PCB with three devices under test. This PCB designed with two layers and included PDN with no traces and no vias, PDN with trace, and PDN with traces and vias. To have those three different design was to start with very simple design, and moved to realistic models. Figure 33 shows the other side of PCB. Figure 34 shows the design of calibration. Since the researcher used the SOLT calibration, so he had to design and calculate the calibration parameters. Figure 35 shows the four port measurements with SMA connector.

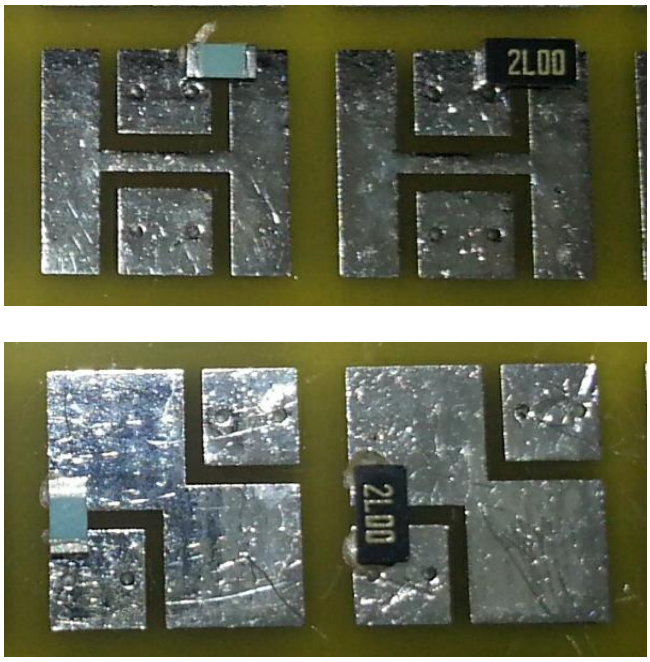


Figure 30 First PCB (different structure)

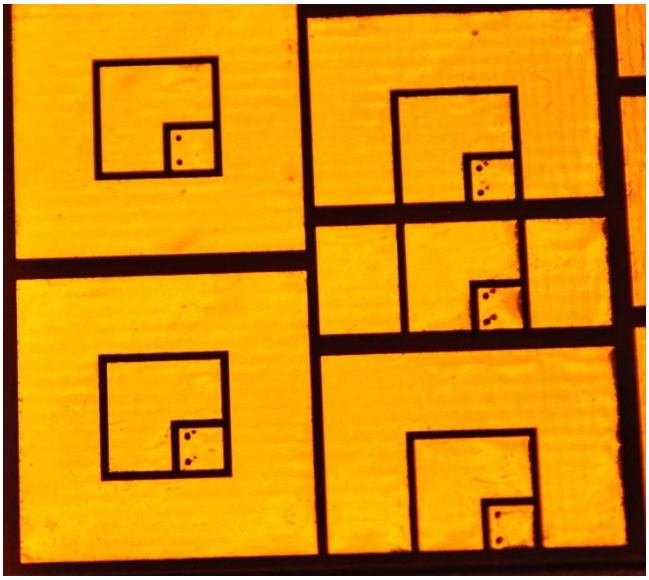


Figure 31 Second PCB

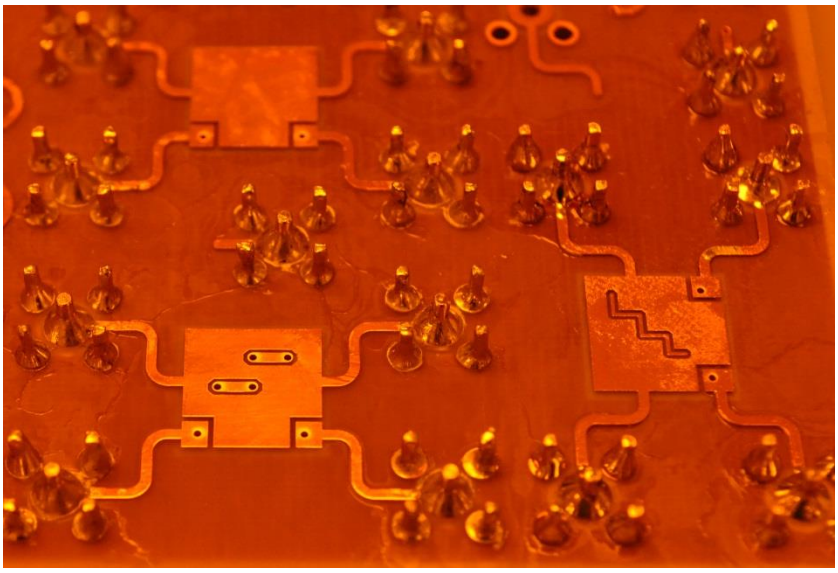


Figure 32 Third PCB design front view

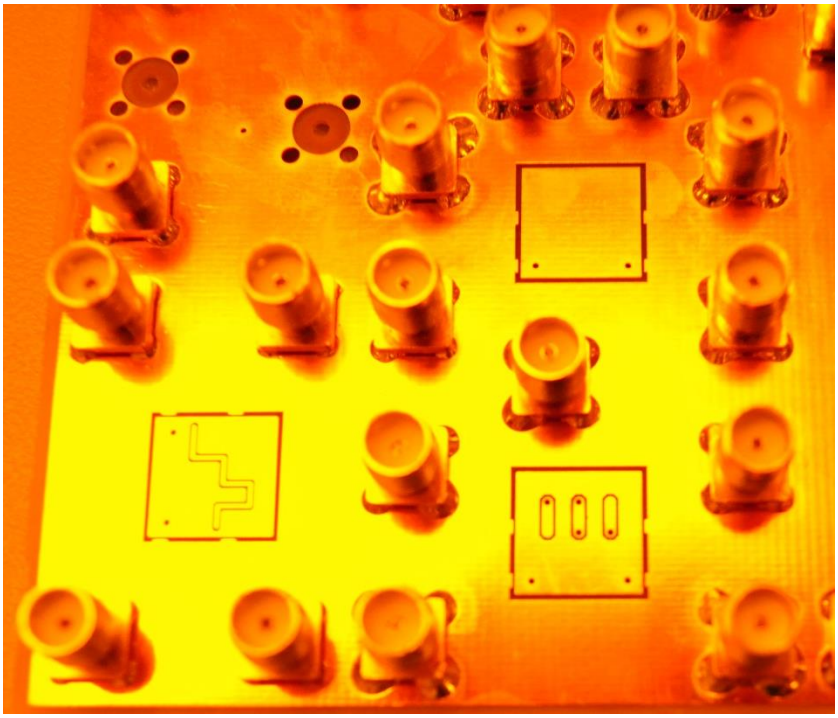


Figure 33 Third PCB design back view with SMA connector

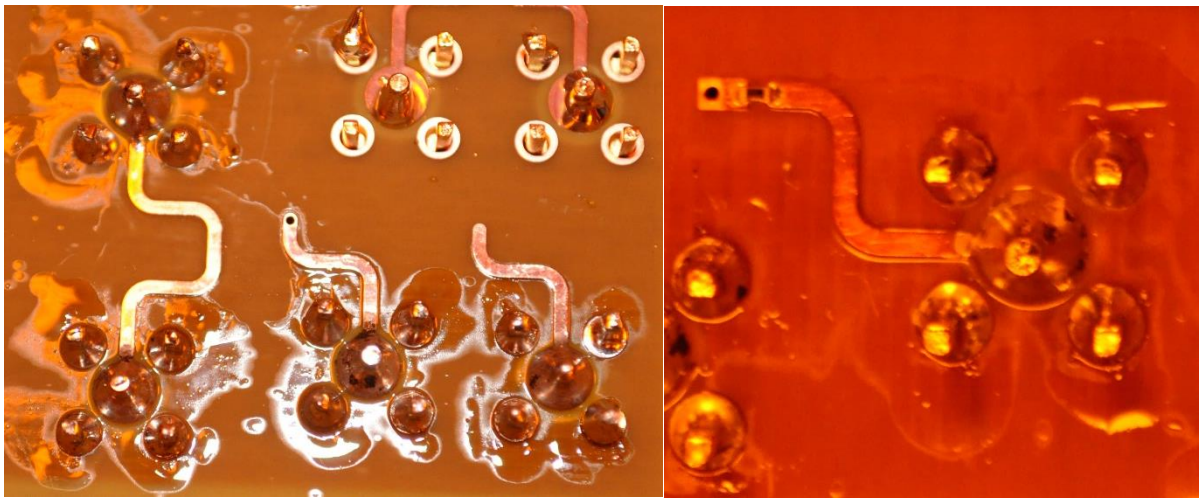


Figure 34 Third PCB calibration tools (Left: thru, short, open Right: 50 ohm load)

Figure 35 four ports measurement

CHAPTER 4

MEASUREMENTS RESULTS

4.1 SOLT Calibration

What is SOLT stands for? SOLT represents the word short-open-load-thru. The short calibration meaning two ports connected with short conductor and known estimated inductance values. The open calibration means two ports connected with open circuit and known estimated capacitance values. The load calibration means two ports connected with a load. The load ideally should be 50 ohms with 50 ohms source impedance and 50 ohms cable or transmission line. For low to middle range frequencies, chip resistor would work perfectly. For higher frequencies, we would need to consider other types of load to have accurate calibration. The chip resistor included inductance and capacitance and during high frequencies it would behave like inductor and capacitor. The thru calibration means two ports connected with zero length conductors. The question comes how one know and can judge that the calibration is correct? The easiest way to confirm is re-measure the calibration standards, for example: short, open, and load. From Smith-Chart, one would know that the open circuit should be located in the right hand side within the circle. The short circuit should be located in the left hand side within the circle. The reason one is at the left and the other one is located at the right is because both magnitudes are the same but they are 180 degree out of phase. For the perfect calibration, the plot in Smith-Chart would show only one dot, but it is impossible to happen. The researcher's efforts are aimed to obtain correct calibration data from setting the research goal to be the plot within the circle. If the plot goes beyond the circle, which mean the device become active, then the calibration would be considered incorrect. From the

Smith-Chart plot, short, open, and load measurements were confirmed to be proper. Figure 36, 37, and 38 show the check of calibration.

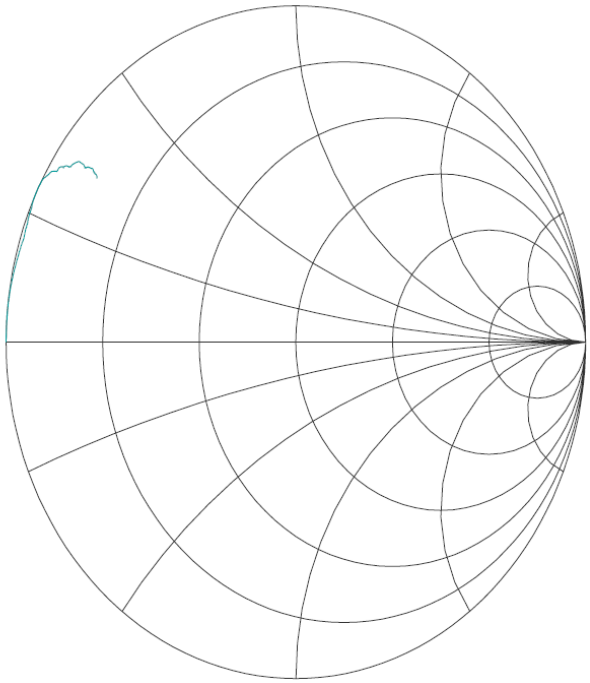


Figure 36 Measured short standard after calibration

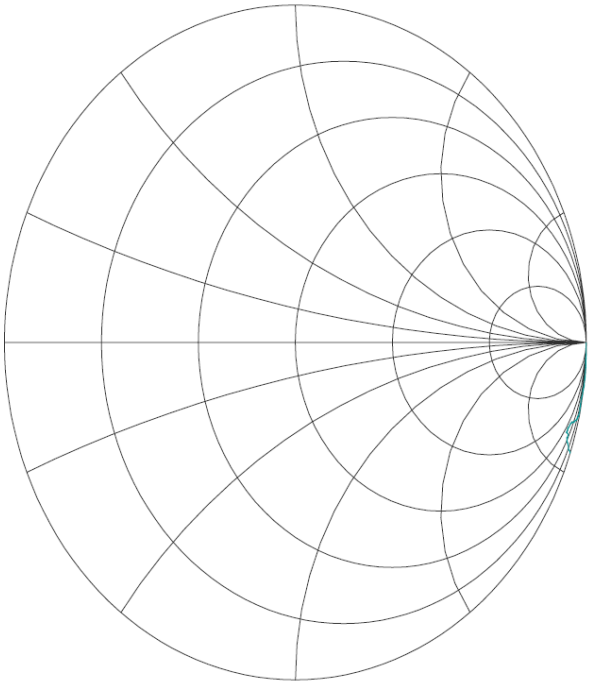


Figure 37 Measured open standard after calibration

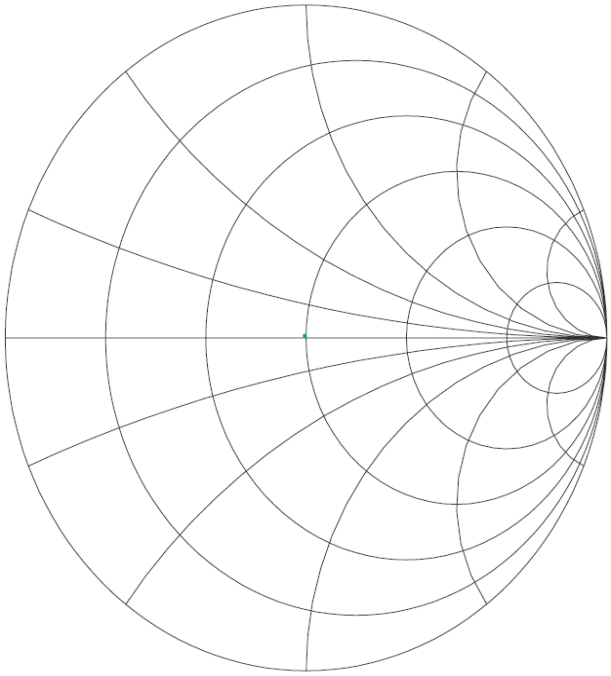


Figure 38 Measured load standard after calibration

4.2 Single-Ended S-Parameters Measurement Using Probe

The measurement result of board impedance with termination of 5.1 ohm resistor was showing in Figure 39. The researcher can clearly see from the figure that it was around 5.1 ohm which was corresponding to the terminal resistor. The red curve was plotted from the built-in function in Matlab "S2Z". I was trying to determine both built-in function and converted equation would have same agreement. In figure 40, there were three curves. Again, the red curve was plotted with built-in function, blue curve was plotted with equation, and green curve was plotted with simulations. This simulation was done at University of Idaho and the method is discussed from [46]. Apparently, the simulation was measured with perfectly 10 ohm, but we knew that was not correct, because during the measurement there could have some error from not only the device but also the machine, cable, connector, and probe. For Figure 41, the researcher tried to measure low impedance but due to the design of

PCB that he picked up some error. This error came from the chip resistor and the adhesive used.

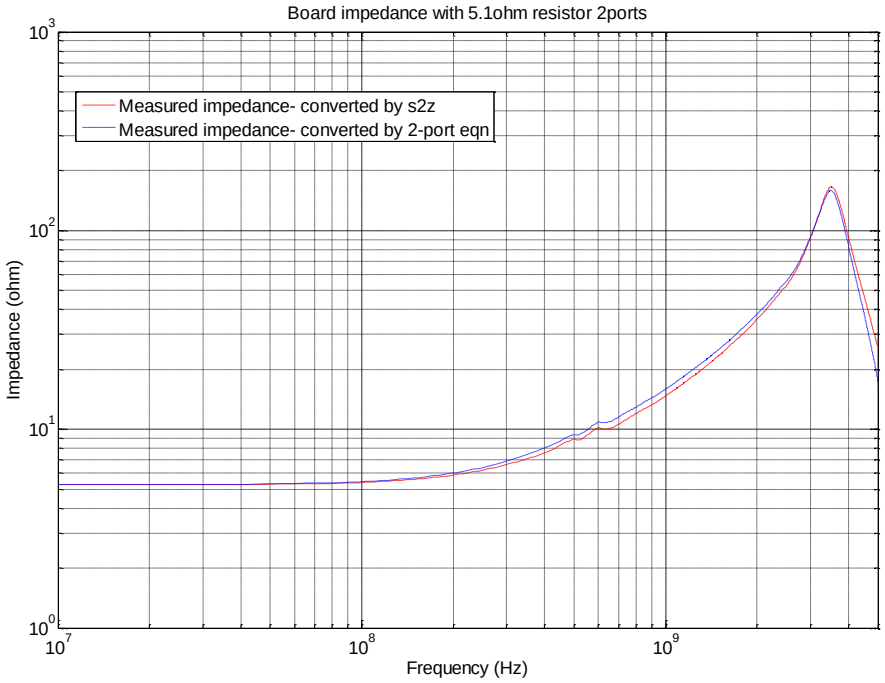


Figure 39 Board impedance with 5.1 ohms resistor

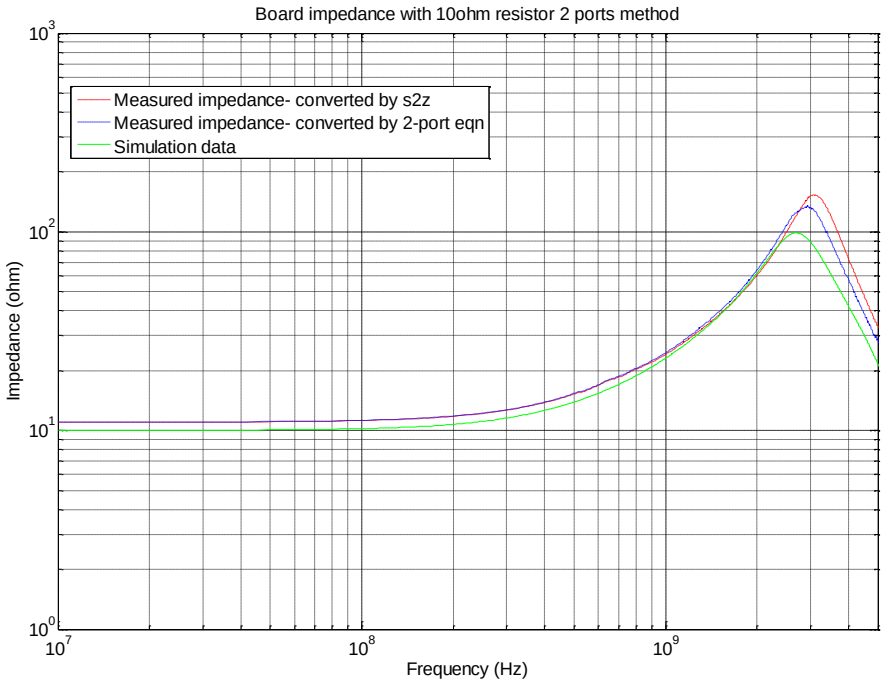


Figure 40 Board impedance with 10 ohms resistor

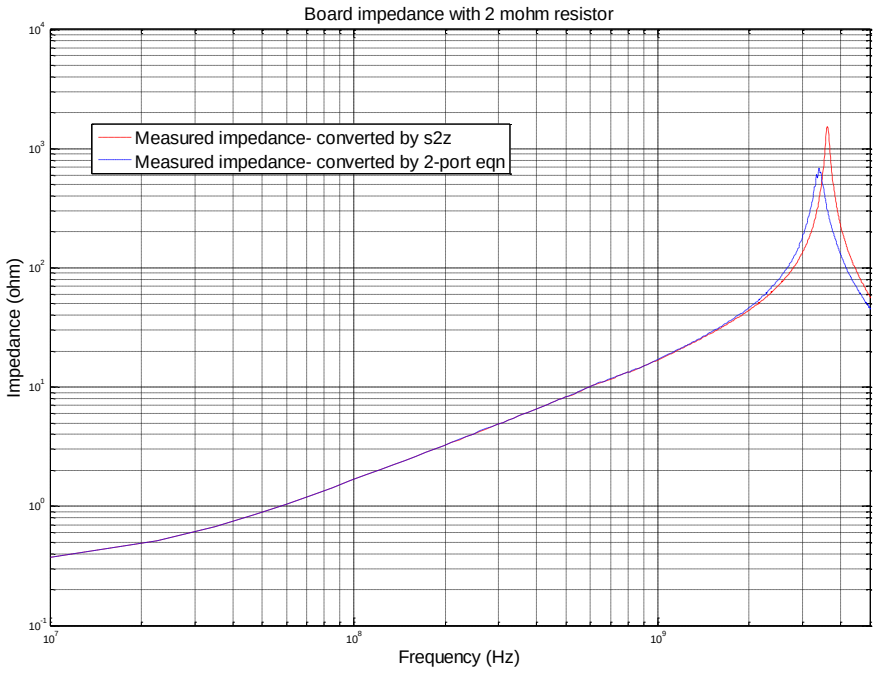


Figure 41 Board impedance with 2 m-ohms resistor

4.3 PDN Measurement Using SMA Connector with No Trace

From Figure 42 and Figure 43, the single-ended S-parameters measurements, the researcher could determine since the DUT was designed as symmetric, so the $Z_{14} = Z_{41}$, $Z_{23}=Z_{32}$, $Z_{11}=Z_{22}$, and $Z_{33}=Z_{44}$. The curves were not identical, but the results were very close. Figure 44 and Figure 45 showed the mixed-mode measurements. He tried to compare with the conversion and true measurements; it turned out to be really close. This is because he did not place any components on the PCB design which mean he measured only passive components such as parasitic capacitance.

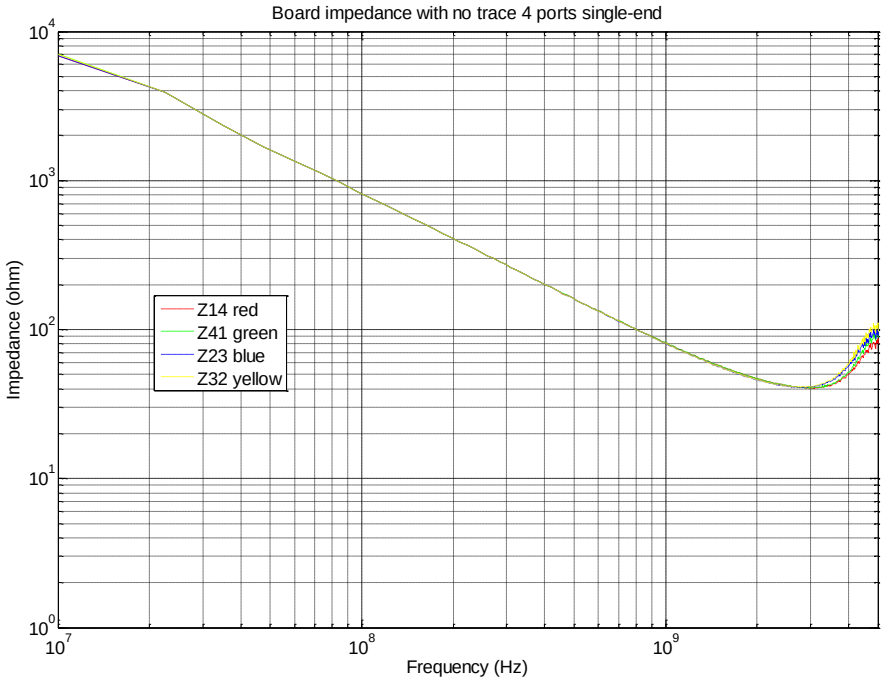


Figure 42 Single-ended measurement Z14, Z41, Z23, and Z32

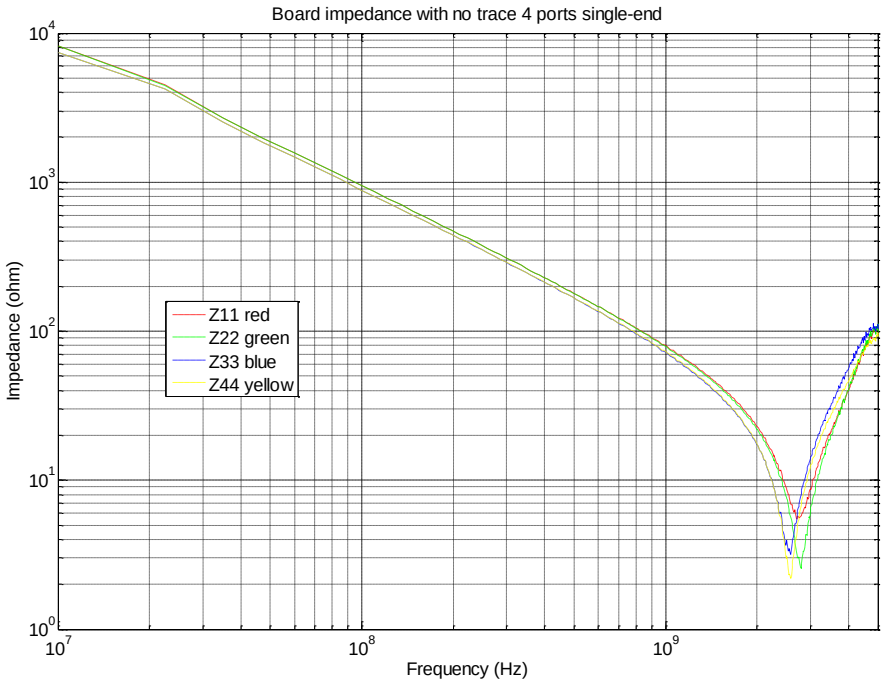


Figure 43 Single-ended measurements Z11, Z22, Z33, and Z44

Figure 44 Mixed-mode measurement Zcc11 no trace

Figure 45 Mixed-mode measurement Zcc22 no trace

4.4 PDN Measurement Using SMA Connector with Trace

Figure 46 and Figure 47 showed the mixed-mode measurements of the PCB with some traces. It is quite visible from the curves that both conversions and true mixed-mode measurements agree with each other.

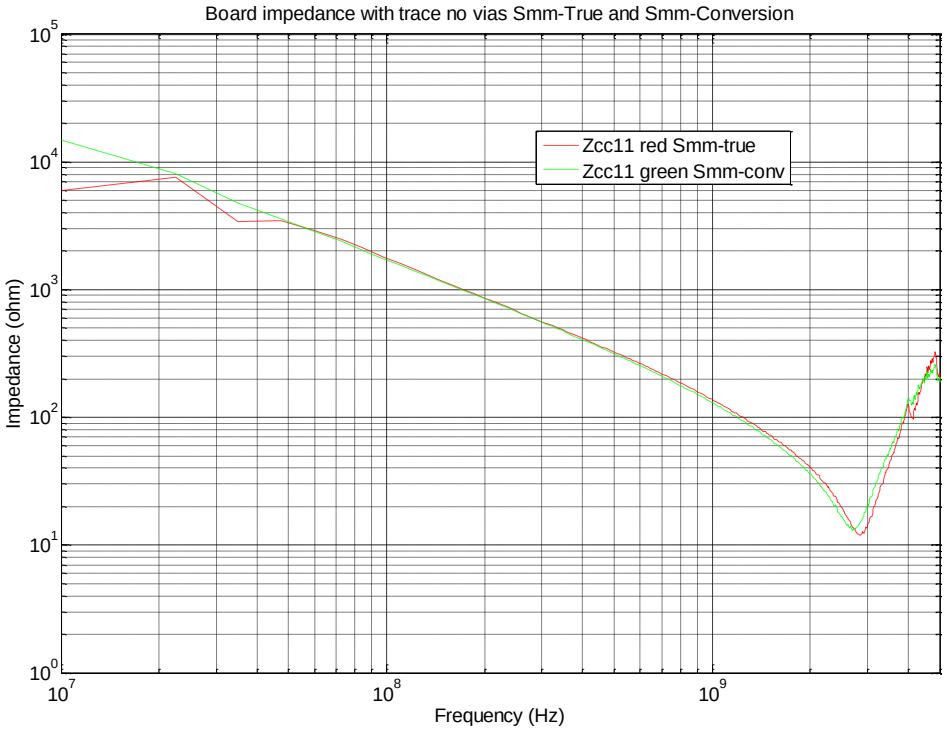


Figure 46 Mixed-mode measurement Zcc11 no vias

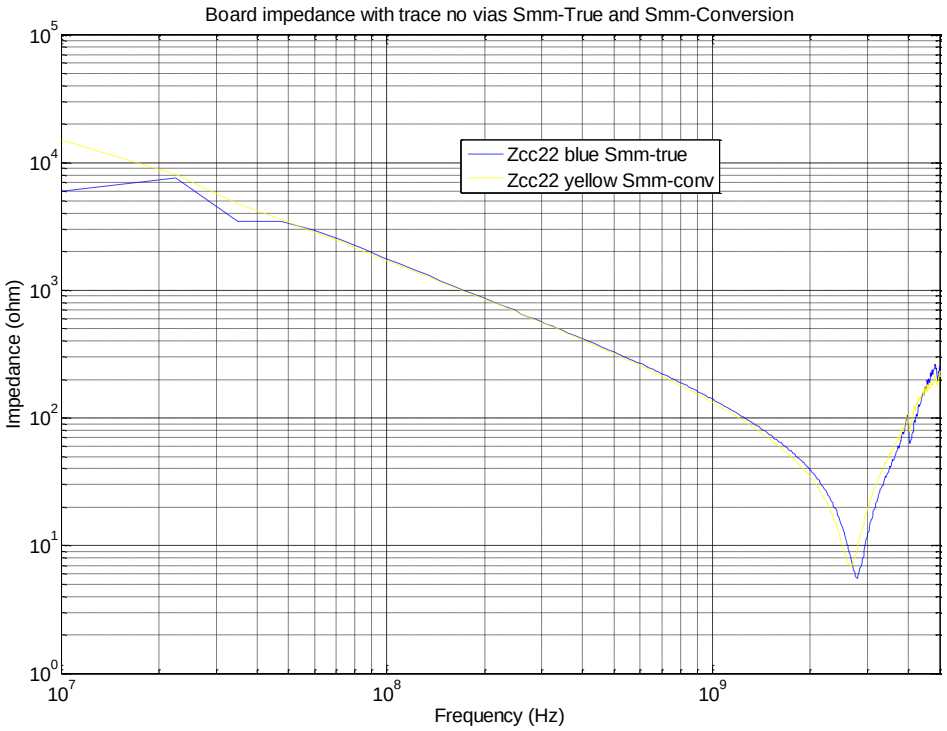


Figure 47 Mixed-mode measurement Zcc22 no vias

4.5 PDN Measurement Using SMA Connector with Vias

Figure 48 and Figure 49 showed the mixed-mode measurements with trace and vias. In Figure 48, the curves looked very agreeable, but not in Figure 49. This is because the loss and error for connectors and SMA.

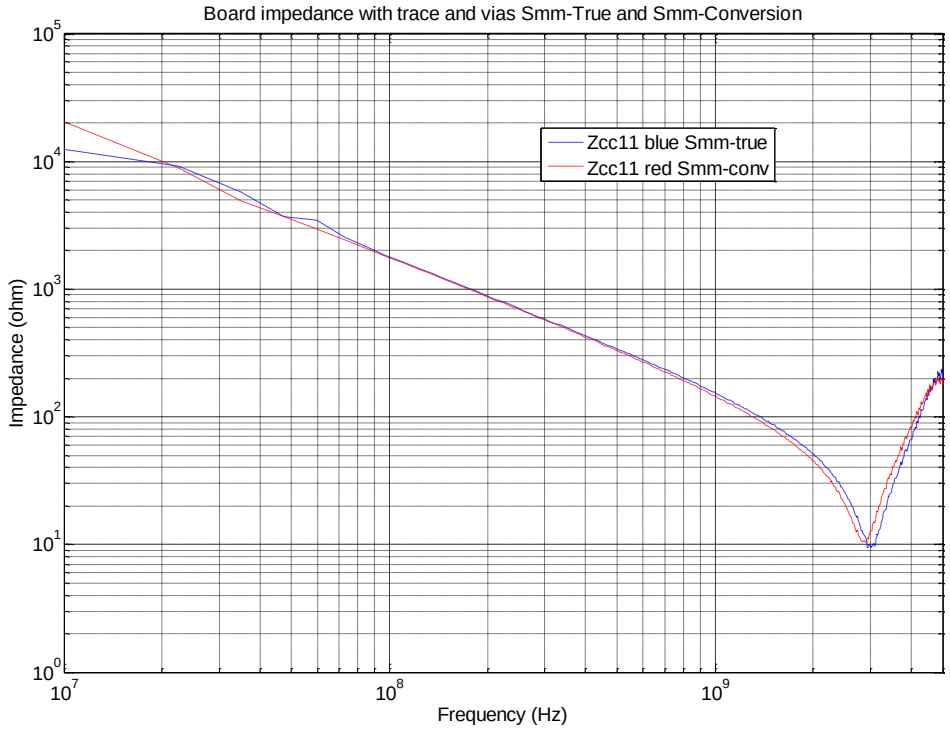


Figure 48 Mixed-mode measurement Zcc11 with vias

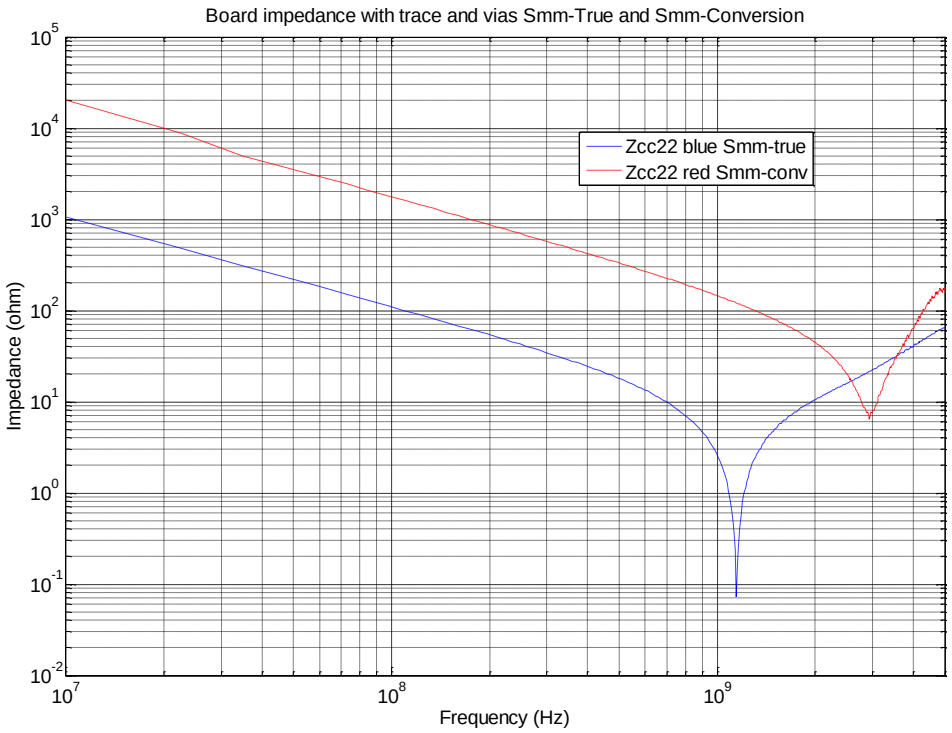


Figure 49 Mixed-mode measurement Zcc22 with vias

CONCLUSION

High speed, high densities, high performance and small devices play an important role in microelectronics and electronic packaging. Signal integrity and power integrity are the principal challenges for any electronic, microelectronic, and semiconductor companies. Especially faster timing and lower noise is the main contributor for signal and power integrity design. Power distribution network and mixed-mode S-parameters can be one of the solutions to analyze the issues of power and signal integrity. The system's increasing physical complexity (i.e., various supply rails, continuously increasing currents, decreasing supply voltages, discontinuous return paths, impedance mismatch, and higher chip leakage) makes the semiconductor devices design even more complicated. As the size of electronic packaging shrinks and the operation frequency increases, signal and power integrity becomes more and more challenging.

The student researcher outlined that in the real world differential signal is composed of both differential and common mode signals, the single-ended four-port S-parameters matrix does not give enough insight information about the differential and common mode transmission, therefore, the mixed-mode S-parameters must be used. This research experiment had designed two layer PCB which represent the power and ground planes. Due to no existence of any active and/or passive components therefore, the mixed-mode conversion and true mixed-mode measurements had similar results. In the future, I would have included some electronic components and include the simulation analysis. For this research, I prove that I have the ability to apply true mixed-mode S-parameters measurements and the results compared to mixed-mode from the conversion were mostly identical. Most of errors or noise came from

the connectors and SMA connectors I used. I was not able to determine that I have lossless and no phase shift connectors.

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